8 × 32 ANALOG CROSS POINT SWITCH

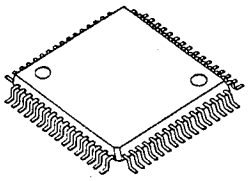
■ GENERAL DESCRIPTION

The **NJU7370** is a 8 × 32 Analog Cross Point Switch which consists of a 8 × 32 analog switch array, an address decoder and a latch circuit.

ON(short mode) or OFF(open mode) of 256 points in a 8 × 32 switch array are easily controlled by setting the address. The power supplies for the logic block and for the switch block are separated, therefore the supply voltage for the switches can be adjusted corresponding to the input signal level.

The small tolerance of the on-resistance of the switches causes to be suitable for a small input selector of audio appliances or other appliances.

■ PACKAGE OUTLINE



NJU7370F

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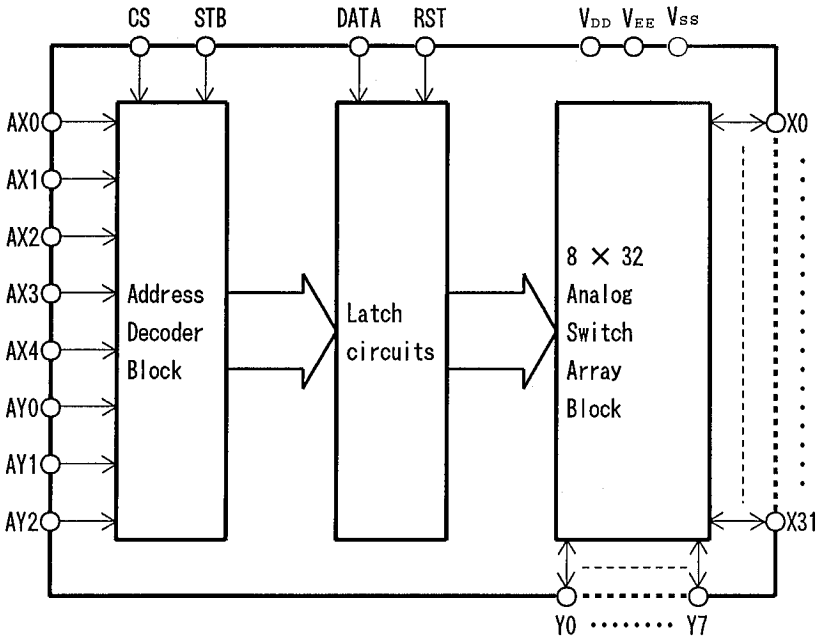
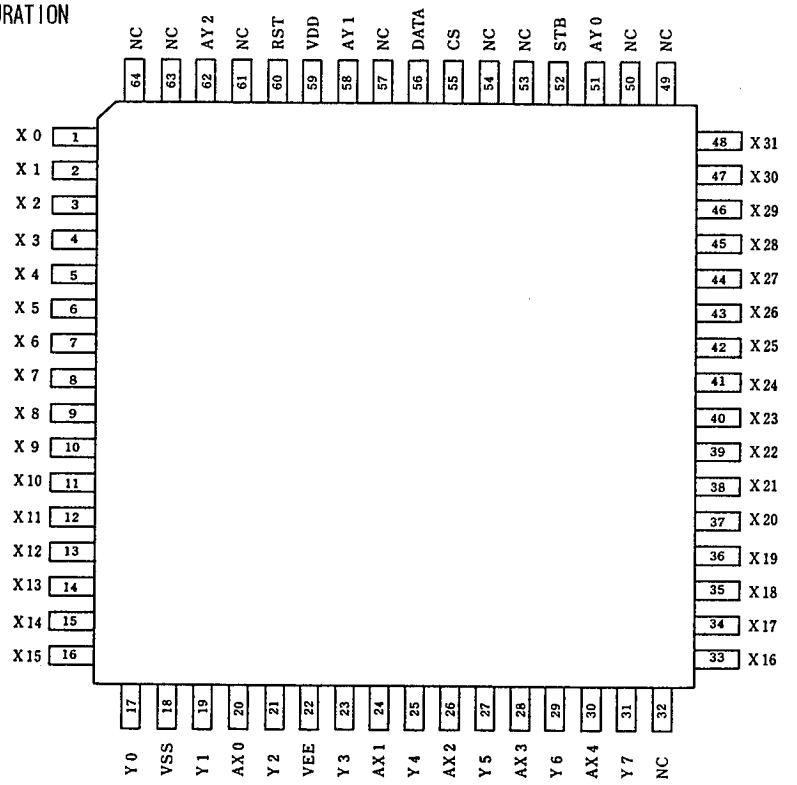
■ FEATURES

- 8 × 32 Analog Switches Array
- Low On-Resistance of switches 100Ω MAX (V_{EE}-V_{SS}=10V)
- Tolerance of On-Resistance 20Ω MAX
- Low Distortion (T.H.D) 0.01% TYP
- Address Decoder and Latch circuits on chip
- Wide Operating Voltage Range V_{DD}-V_{SS}=6V (Logic Block) V_{DD}-V_{EE}=11V (Switch Block)
- Low Operating Current 1μA MAX (V_{IN}=V_{DD} or V_{IN}=V_{SS})
- Package Outline — QFP64
- C-MOS Technology

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ TERMINAL DESCRIPTION

No.	SYMBOL	F U N C T I O N
59	V_{DD}	LOGIC/Switch Power Source (+)
18	V_{SS}	LOGIC Power Source (GND)
22	V_{EE}	Switch Power Source (-)
55	CS	Chip Select Signal Input
52	STB	Strobe Signal Input
56	DATA	Switch ON/OFF Signal Input
60	RST	Master Reset Signal Input
20,24	AX0～AX1	X0～X1 Address Signal Input
26,28,30	AX2～AX4	X2～X4 Address Signal Input
51,58,62	AY0～AY2	Y0～Y2 Address Signal Input
1～16 33～48	X0 ～X15 X16～X31	X0～X31 Analog Switches Array Input/Output
17,19,21 23,25 27,29,31	Y0～Y2 Y3～Y4 Y5～Y7	Y0～Y7 Analog Switches Array Input/Output

■ FUNCTIONAL DESCRIPTION

(1) Address Decoder Block

The address decoder block decodes AX0~AX4 of X side and AY0~AY2 of Y side to 32 lines of X side and 8 lines of Y side, then the decoded signals select a switch out of the 8 × 32 analog switches array. The address can be set when an input signal condition to CS terminal is High level.

Following table shows address decoding.

AX0	AX1	AX2	AX3	AX4	AY0	AY1	AY2	Connection
0	0	0	0	0	0	0	0	X0 - Y0
1	0	0	0	0	0	0	0	X1 - Y0
0	1	0	0	0	0	0	0	X2 - Y0
1	1	0	0	0	0	0	0	X3 - Y0
0	0	1	0	0	0	0	0	X4 - Y0
1	0	1	0	0	0	0	0	X5 - Y0
0	1	1	0	0	0	0	0	X6 - Y0
1	1	1	0	0	0	0	0	X7 - Y0
0	0	0	1	0	0	0	0	X8 - Y0
1	0	0	1	0	0	0	0	X9 - Y0
0	1	0	1	0	0	0	0	X10 - Y0
1	1	0	1	0	0	0	0	X11 - Y0
0	0	1	1	0	0	0	0	X12 - Y0
1	0	1	1	0	0	0	0	X13 - Y0
0	1	1	1	0	0	0	0	X14 - Y0
1	1	1	1	0	0	0	0	X15 - Y0
0	0	0	0	1	0	0	0	X16 - Y0
1	0	0	0	1	0	0	0	X17 - Y0
0	1	0	0	1	0	0	0	X18 - Y0
1	1	0	0	1	0	0	0	X19 - Y0
0	0	1	0	1	0	0	0	X20 - Y0
1	0	1	0	1	0	0	0	X21 - Y0
0	1	1	0	1	0	0	0	X22 - Y0
1	1	1	0	1	0	0	0	X23 - Y0
0	0	0	1	1	0	0	0	X24 - Y0
1	0	0	1	1	0	0	0	X25 - Y0
0	1	0	1	1	0	0	0	X26 - Y0
1	1	0	1	1	0	0	0	X27 - Y0
0	0	1	1	1	0	0	0	X28 - Y0
1	0	1	1	1	0	0	0	X29 - Y0
0	1	1	1	1	0	0	0	X30 - Y0
1	1	1	1	1	0	0	0	X31 - Y0
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	1 ↓ 1	0 ↓ 0	0 ↓ 0	X0 ↓ X31 - Y1 ↓ Y1
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 0	1 ↓ 1	0 ↓ 0	X0 ↓ X31 - Y2 ↓ Y2
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	1 ↓ 1	1 ↓ 1	0 ↓ 0	X0 ↓ X31 - Y3 ↓ Y3
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 0	0 ↓ 0	1 ↓ 1	X0 ↓ X31 - Y4 ↓ Y4
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	1 ↓ 1	0 ↓ 0	1 ↓ 1	X0 ↓ X31 - Y5 ↓ Y5
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 0	1 ↓ 1	1 ↓ 1	X0 ↓ X31 - Y6 ↓ Y6
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	1 ↓ 1	1 ↓ 1	1 ↓ 1	X0 ↓ X31 - Y7 ↓ Y7

(2) Latch Circuits

Analog data are loaded when each input signal condition to CS and STB terminals is High level, and their data are latched when an input signal to STB terminal falls from High to Low. The condition of a switch becomes ON when the latched data is High, and it becomes OFF when the latched data is Low. When the input signal condition to RST terminal is High, the latch circuits are reset and all switches become OFF.

(3) 8 × 32 Analog Switch Array Block

The analog switch array consisted of 8 × 32 switches are controlled by the output signals from latch circuits.

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}-V_{SS} V_{DD}-V_{EE} V_{SS}-V_{EE}	- 0.3 ~ +14.0 - 0.3 ~ +14.0 - 0.3 ~ +14.0	V
Analog Input Voltage	V_{INA}	V_{EE}-0.3 ~ V_{DD}+0.3	V
Digital Input Voltage	V_{IN}	V_{SS}-0.3 ~ V_{DD}+0.3	V
Input Current	I_{IN}	±15	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_{opr}	- 25 ~ + 75	℃
Storage Temperature Range	T_{stg}	- 40 ~ +125	℃

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■ ELECTRICAL CHARACTERISTICS

·DC CHARACTERISTICS (V_{DD}=10V, V_{SS}=V_{EE}=0V, Ta=25℃)

PARAMETER	SYMBOL	RATINGS	MIN	TYP	MAX	UNIT
Operating Voltage Range	V_{DD}-V_{SS} V_{DD}-V_{EE}		4.5 4.5	5.0 10.0	6.0 11.0	V
Analog Input Voltage	V_{INA}		V_{EE}		V_{DD}	V
Digital Input Voltage	V_{IN}		V_{SS}		V_{DD}	V
Operating Current	I_{DD1}	Digital Input Terminal, V_{IN}=V_{SS} or V_{DD}		1	100	μA
	I_{DD2}	Digital Input Terminal, V_{IN}=2.4V+V_{SS} V_{DD}=10V, V_{SS}=5V, V_{EE}=0V		0.4	1.5	mA
	I_{DD3}	Digital Input Terminal, V_{IN}=3.4V		5	15	mA
Switch OFF Leakage Current	I_{OFF}	$\|V_{Xi}-V_{Yj}\|$=V_{DD}-V_{EE}		±1	±500	nA
Low-Level Input Voltage	V_{IL}	V_{DD}=10V, V_{SS}=5V, V_{EE}=0V			0.8+V_{SS}	V
High-Level Input Voltage	V_{IH}	V_{DD}=10V, V_{SS}=5V, V_{EE}=0V	2.0+V_{SS}			V
Input Leakage Current	I_{LEAK}			0.1	10	μA

·SWITCH CHARACTERISTICS (V_{DD}=5V, V_{SS}=0V, V_{EE}=-5V, $\|V_{Xi}-V_{Yj}\|$=0.4V, Ta=25℃)

PARAMETER	SYMBOL	RATINGS	MIN	TYP	MAX	UNIT
ON-Resistance	R_{ON1}	V_{DD}-V_{EE}=10V		80	100	Ω
	R_{ON2}	V_{DD}-V_{EE}=5V		200	250	
Deviation of ON-Resistance	ΔR_{ON}	V_{DD}=10V, V_{SS}=V_{EE}=0V, V_{DC}=V_{DD}/2		10	20	Ω

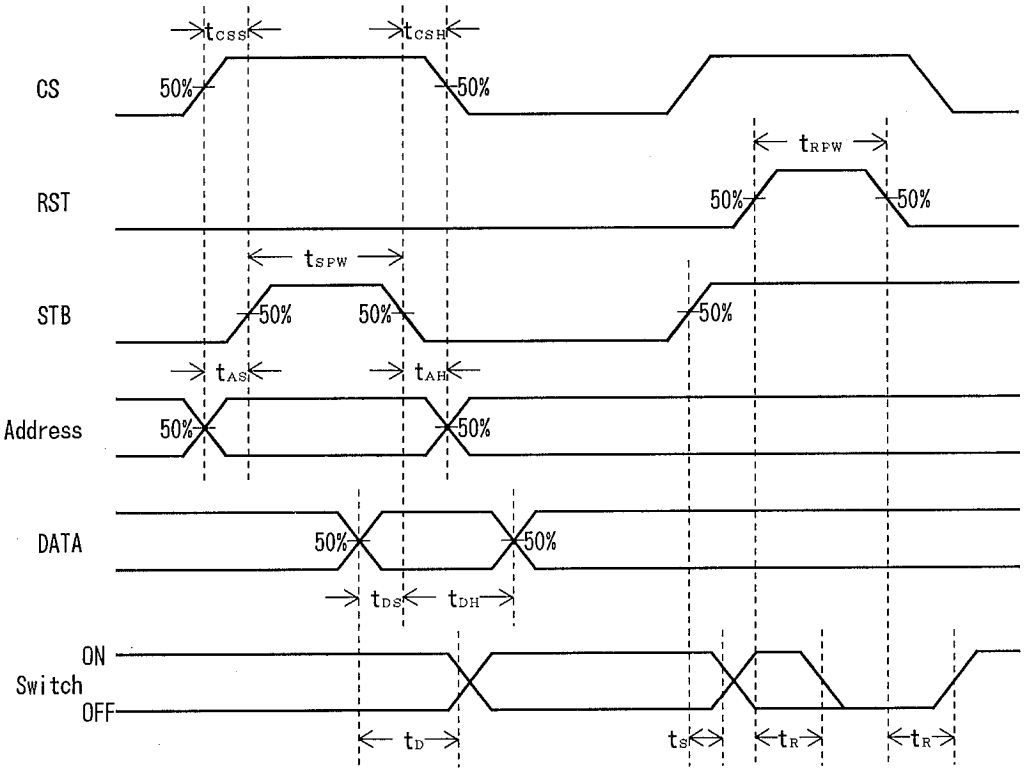
·SWITCHING CHARACTERISTICS (V_{DD}=5V, V_{SS}=0V, V_{EE}=-5V, Ta=25°C)

PARAMETER	SYMBOL	RATINGS	MIN	TYP	MAX	UNIT
Input Capacitance	Cs	X,Y Terminal f=1MHz,Switch OFF		15		pF
Maximum Transmitting Frequency (ON)	F_{MAX}	Switch ON;V_{INA}=2V_{pp} Sign wave;R_L=1kΩ		45		MHz
Total Harmonic Distortion Ratio	THD	Switch ON;V_{INA}=2V_{pp} Sign wave;f=1kHz,R_L=1kΩ		0.01		%
Feed Threw (OFF)	FDT	All Switch OFF;V_{INA}=2V_{pp} Sign wave;f=1kHz,R_L=1kΩ		-95		dB
Cross Talk	X_{talk1}	V_{INA}=2V_{pp} f=10MHz,R_L=75Ω		-45		dB
	X_{talk2}	f=10kHz,R_L=600Ω		-90		
	X_{talk3}	f=10kHz,R_L=1kΩ		-85		
	X_{talk4}	f=1kHz,R_L=10kΩ		-80		
Transmitting Time	tps	R_L=1kΩ;C_L=50pF			30	ns

·AC CHARACTERISTICS (V_{DD}=5V, V_{SS}=0V, V_{EE}=-5V, Ta=25°C)

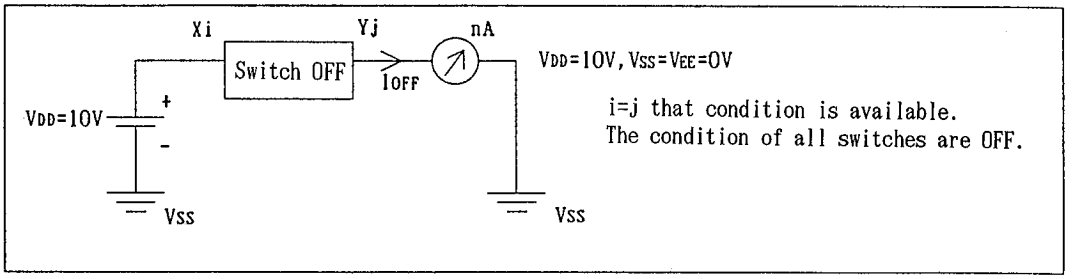
PARAMETER	SYMBOL	RATINGS	MIN	TYP	MAX	UNIT
Cross Talk on Control Input Signal	CX_{talk}	V_{IN}=3V,Square wave R_{IN}=1kΩ,R_L=10kΩ		30		mVpp
Input Capacitance	C_{DI}	f=1MHz,Control Terminals		10		pF
Switching Frequency	Fo				20	MHz
Data Setup Time	t_{DS}	R_L=1kΩ,C_L=50pF	0			ns
Data Hold Time	t_{DH}		60			ns
Address Setup Time	t_{AS}		0			ns
Address Hold Time	t_{AH}		60			ns
CS Setup Time	t_{CSS}		0			ns
CS Hold Time	t_{CSH}		60			ns
Strobe Pulse Width	t_{SPW}		30			ns
Reset Pulse Width	t_{RPW}		40			ns
Strobe Transmitting Time	t_S			80	150	ns
Data Transmitting Time	t_D			50	100	ns
Latch Reset Time	t_R			35	100	ns

■ Timing Diagram

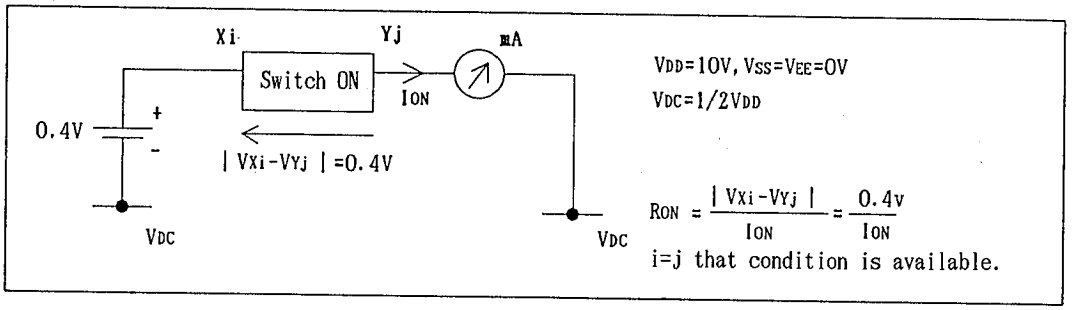


■ MEASUREMENT CIRCUITS

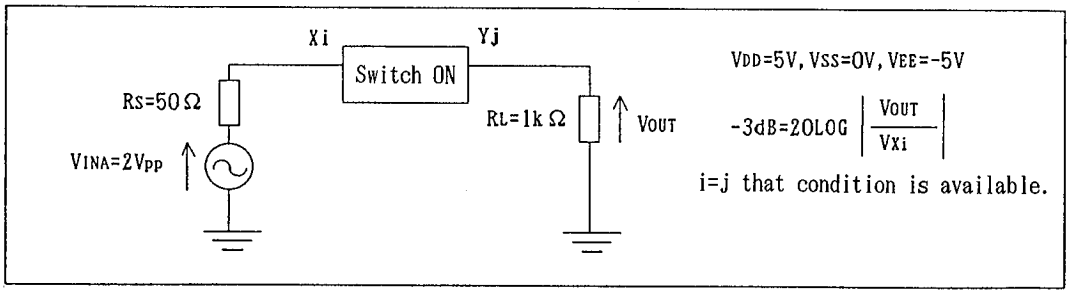
(1) OFF LEAKAGE(I_{OFF}) MEASUREMENT CIRCUIT



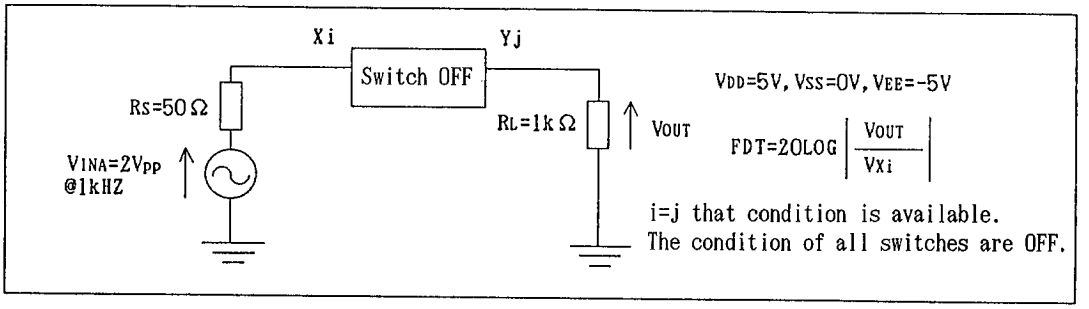
(2) $R_{ON}/\Delta R_{ON}$ MEASUREMENT CIRCUIT



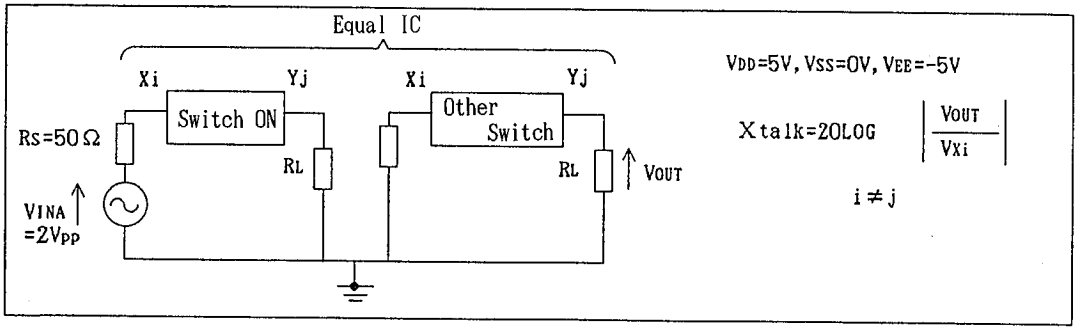
(3) MAXIMUM TRANSMITTING FREQUENCY(F_{MAX}) MEASUREMENT CIRCUIT



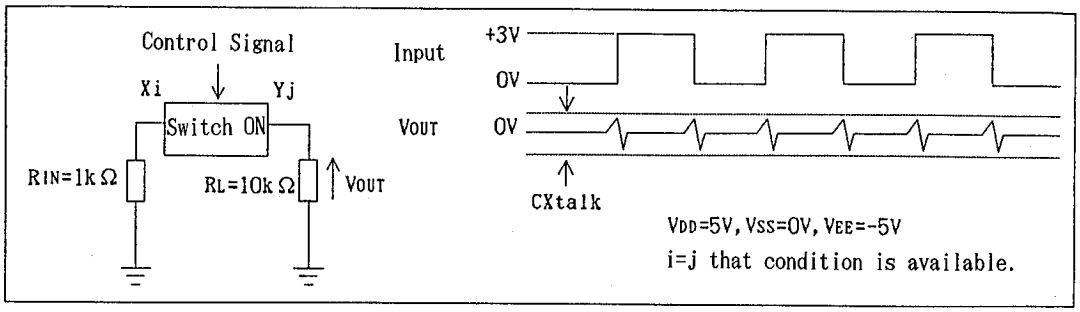
(4) FIELD THREW(FDT) MEASUREMENT CIRCUIT



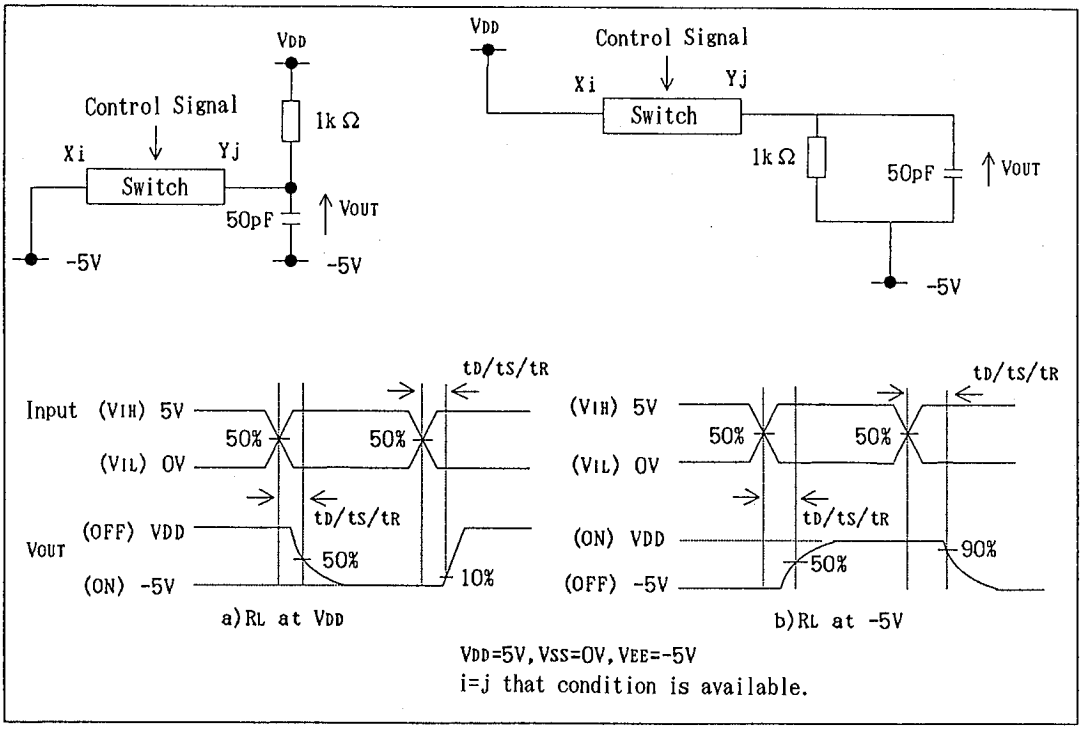
(5) CROSS TALK(X_{talk}) MEASUREMENT CIRCUIT



(6) CONTROL INPUT CROSS TALK(CX_{talk}) MEASUREMENT CIRCUIT



(7) CONTROL MEMORY TIMING MEASUREMENT CIRCUIT



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