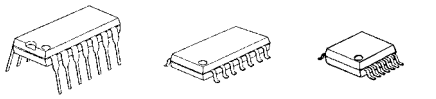
Headphone Amplifier with Electronic Volume

■ GENERAL DESCRIPTION

The **NJW1109** is a headphone amplifier with electronic volume. It includes widely gain adjustable volume, +20 to –80 dB, and mute function. These are controlled by I^2C bus. The **NJW1109** is suitable for headphone output on TV set.

■ PACKAGE OUTLINE

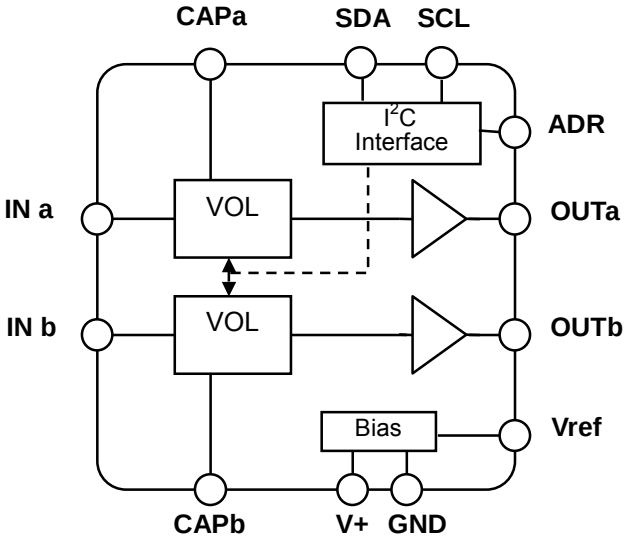


NJW1109D **NJW1109M** **NJW1109V**

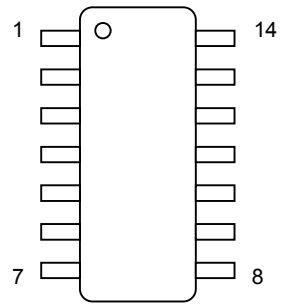
■ FEATURES

- Operating Voltage 7.5 to 10 V
- Electronic Volume +20dB to -80dB / 0.5dB step, Mute
- I^2C Bus Interface
- Bi-CMOS Technology
- Package Outline DIP14, DMP14, SSOP14

■ BLOCK DIAGRAM



■ PIN FUNCTION



No.	SYMBOL	FUNCTION	No.	SYMBOL	FUNCTION
1	V+	Power Supply	8	SCL	I^2C Bus Clock Input
2	OUTb	Bch Output	9	Vref	Reference voltage stabilized capacitor connect terminal
3	N.C.	No Connect	10	INa	Ach Input
4	CAPb	Balance control click noise absorbing capacitor connect terminal	11	CAPa	Volume control click noise absorbing capacitor connect terminal
5	INb	Bch Input	12	N.C.	No Connect
6	ADR	I^2C Bus Slave Address Select	13	OUTa	Ach Output
7	SDA	I^2C Bus Data Input	14	GND	Ground

■ **ABSOLUTE MAXIMUM RATING (Ta=25°C)**

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V^+	12	V
Power Dissipation	P_D	500 (DIP14) 500* (DMP14) 440* (SSOP14)	mW
Operating Temperature Range	Topr	-20 to +75	°C
Storage Temperature Range	Tstg	-40 to +125	°C

*(Note) EIA/JEDEC STANDARD Test board(76.2 x 114.3 x 1.6mm, 2layers, FR-4)mounting

■ **ELECTRICAL CHARACTERISTICS**

(V^+=9V, V_{IN}=-20dBV, f=1kHz, R_L=100Ω, VOL = 0dB , Ta=25°C)

●**POWER SUPPLY**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		7.5	9	10	V
Operating Current	I_{CC}	No Signal	-	5	8	mA
Reference Voltage	V_{REF}		4.0	4.5	5.0	V

●**AMPLIFIER**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Volume Maximum Gain	G_{VMAX}	VOL = +20dB setting	18	20	22	dB
Volume Minimum Gain	G_{VMIN}	VOL = -80dB setting		-80		
Voltage Gain Channel Balance	ΔGv	VOL = 0dB setting	-1.5	0	1.5	dB
Maximum Input Voltage	V_{IM}	VOL = -10dB setting THD=3%	8.9 (2.8)	9.5 (3.0)	-	dBV (Vrms)
Output Power	P_O	VOL = 10dB, THD=10%	70	100	-	mW
Total Harmonic Distortion	THD	VOL = 0dB setting	-	0.1	1	%
Channel Separation	CS	Rg=600Ω, Vin = 0dBV	70	80	-	dB
Mute Level	Mute	VOL = Mute, Vin = 0dBV	-	-100	-90	dB
Output Noise Voltage 1	V_{NO1}	Rg=0Ω, A-Weighted	-	-95 (18)	-85 (56)	dBV (μVrms)
Output Noise Voltage 2	V_{NO2}	VOL = Mute Rg=0Ω, A-Weighted	-	-105 (5.6)	-95 (18)	dBV (μVrms)
Power Supply Ripple Rejection	PSRR	Vripple=-20dBV, Rg=0Ω	-	70	-	dB

●**CONTROL**

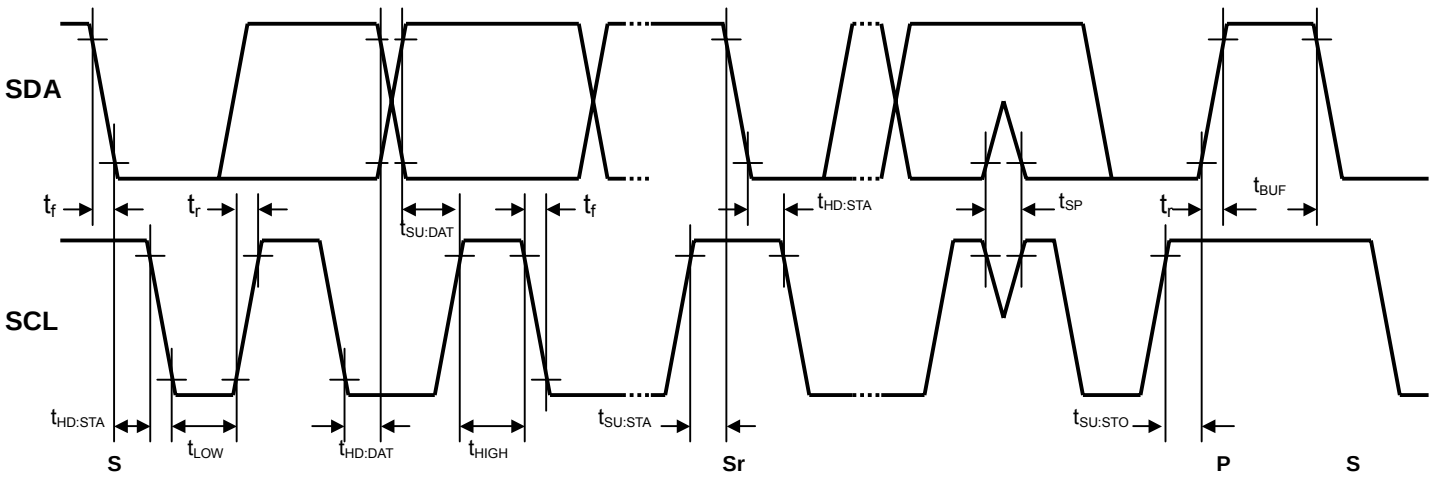
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
High Level Input Voltage	V_{ADRH}	High : Slave Address 84H	$V^+/2$	-	-	V
Low Level Input Voltage	V_{ADRL}	Low : Slave Address 80H	-	-	1.0	V

■ I²C BUS CHARACTERISTICS (SDA, SCL)

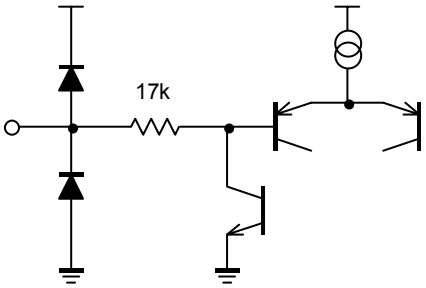
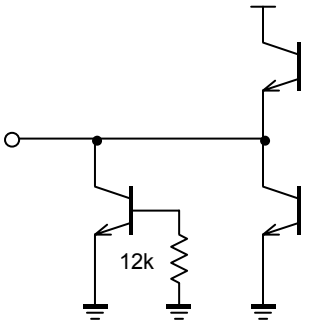
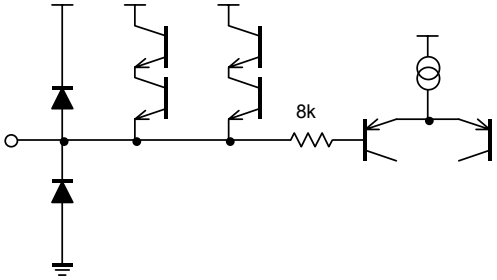
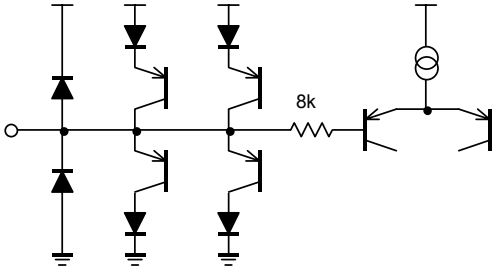
I²C BUS Load Conditions: Pull up resistance 4kΩ (Connected to +5V), Load capacitance 200pF (Connected to GND)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Low Level Input Voltage	V_{IL}	0.0	-	1.5	V
High Level Input Voltage	V_{IH}	2.5	-	5.0	V
Hysteresis of Schmitt trigger inputs	V_{hys}	0.25	-	-	V
LOW level output voltage (3mA at SDA pin)	V_{OL}	0	-	0.4	V
Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance from 10pF to 400pF	t_{of}	$20+0.1C_b$	-	250	ns
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0	-	50	ns
Input current each I/O pin with an input voltage between $0.1V_{DD}$ and $0.9V_{DDmax}$	I_i	-10	-	10	μA
Capacitance for each I/O pin	C_i	-	-	10	pF
SCL clock frequency	f_{SCL}	-	-	400	kHz
Hold time (repeated) START condition.	$t_{HD:STA}$	0.6	-	-	μs
LOW period of the SCL clock	t_{LOW}	1.3	-	-	μs
HIGH period of the SCL clock	t_{HIGH}	0.6	-	-	μs
Set-up time for a repeated START condition	$t_{SU:STA}$	0.6	-	-	μs
Data hold time	$t_{HD:DAT}$	0	-	0.9	μs
Data set-up time	$t_{SU:DAT}$	100	-	-	ns
Rise time of both SDA and SCL signals	t_r	-	-	300	ns
Fall time of both SDA and SCL signals	t_f	-	-	300	ns
Set-up time for STOP condition	$t_{SU:STO}$	0.6	-	-	μs
Bus free time between a STOP and START condition	t_{BUF}	1.3	-	-	μs
Capacitive load for each bus line	C_b	-	-	400	pF
Noise margin at the LOW level	V_{nL}	0.5	-	-	V
Noise margin at the HIGH level	V_{nH}	1	-	-	V

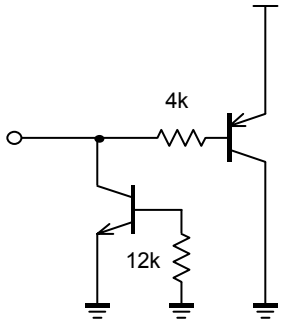
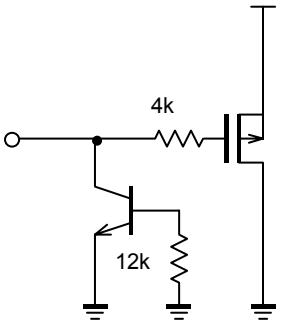
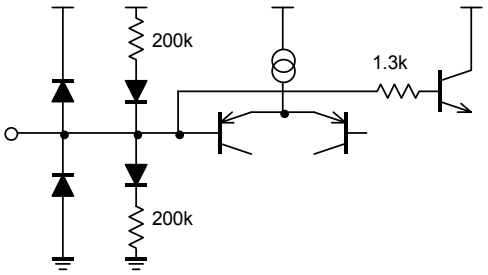
C_b ; total capacitance of one bus line in pF.



■TERMINAL DESCRIPTION

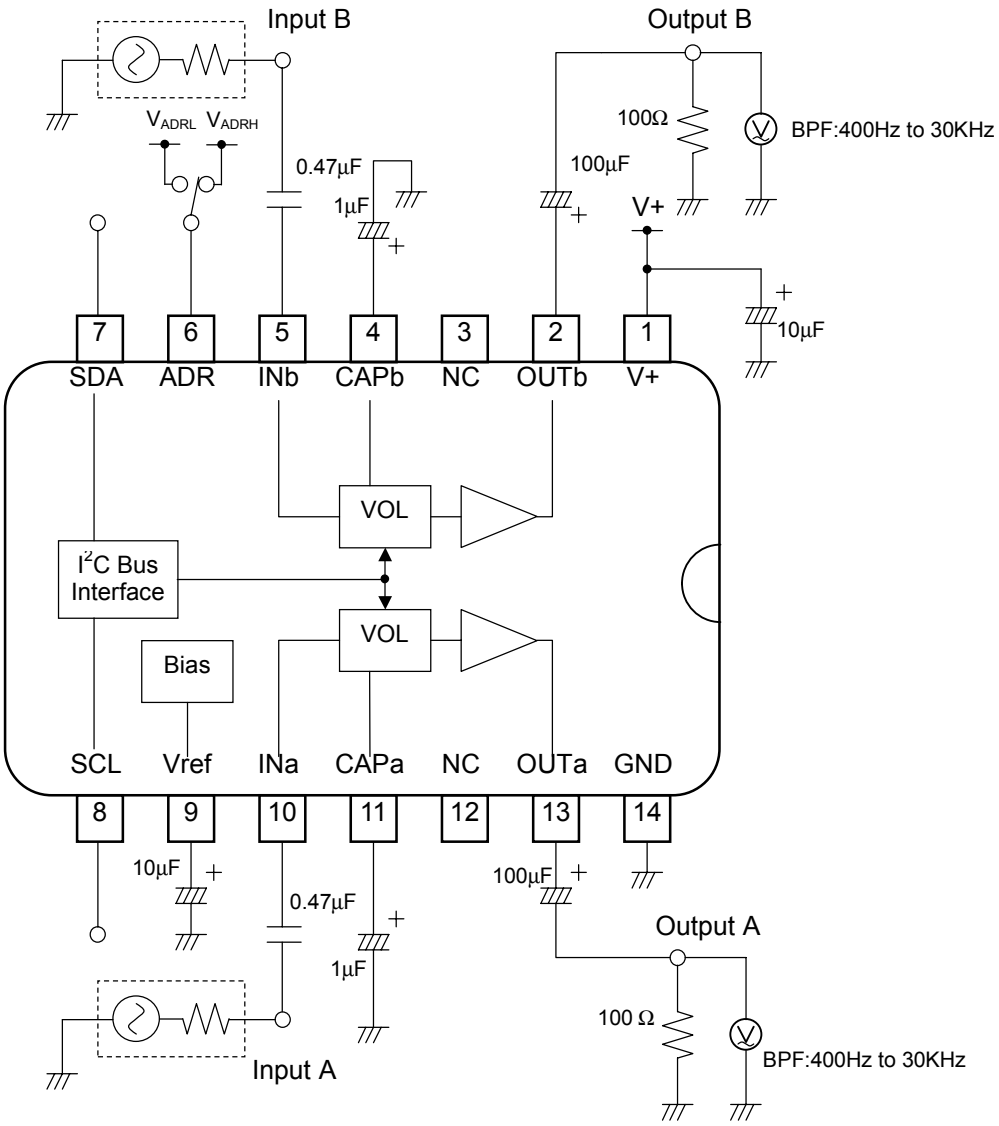
No.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLTAGE
5 10	INb INa	Bch Input Ach Input		V+/2
2 13	OUTb OUTa	Bch Output Ach Output		V+/2
4	CAPb	Balance control click noise absorbing capacitor connect terminal		3.8V
11	CAPa	Volume control click noise absorbing capacitor connect terminal		3.1V

■TERMINAL DESCRIPTION

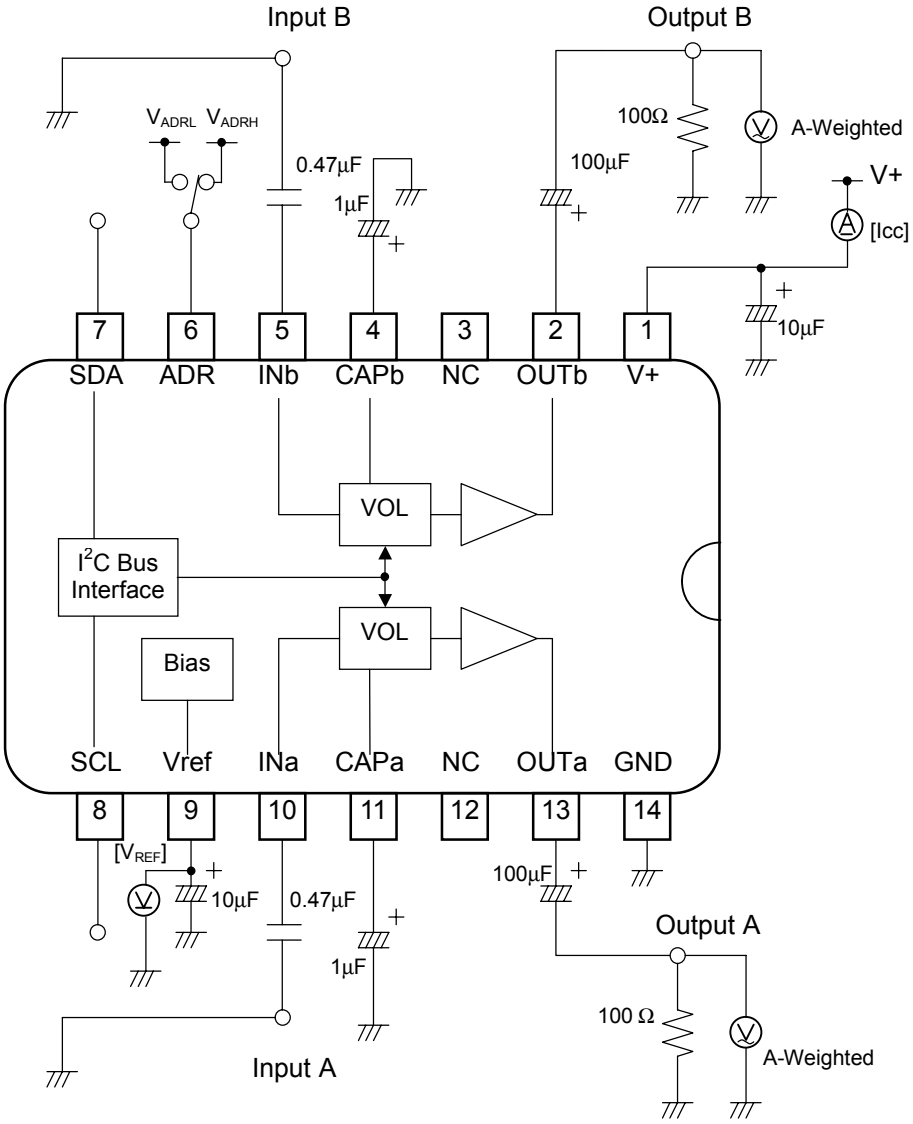
No.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLTAGE
6	ADR	I^2C Bus Slave Address Select		-
7 8	SDA SCL	I^2C Bus Data Input I^2C Bus Clock Input		-
9	Vref	Reference voltage stabilized capacitor connect terminal		V+/2
1	V+	Power Supply	-	-
14	GND	Ground	-	-

■ **TEST CIRCUIT**

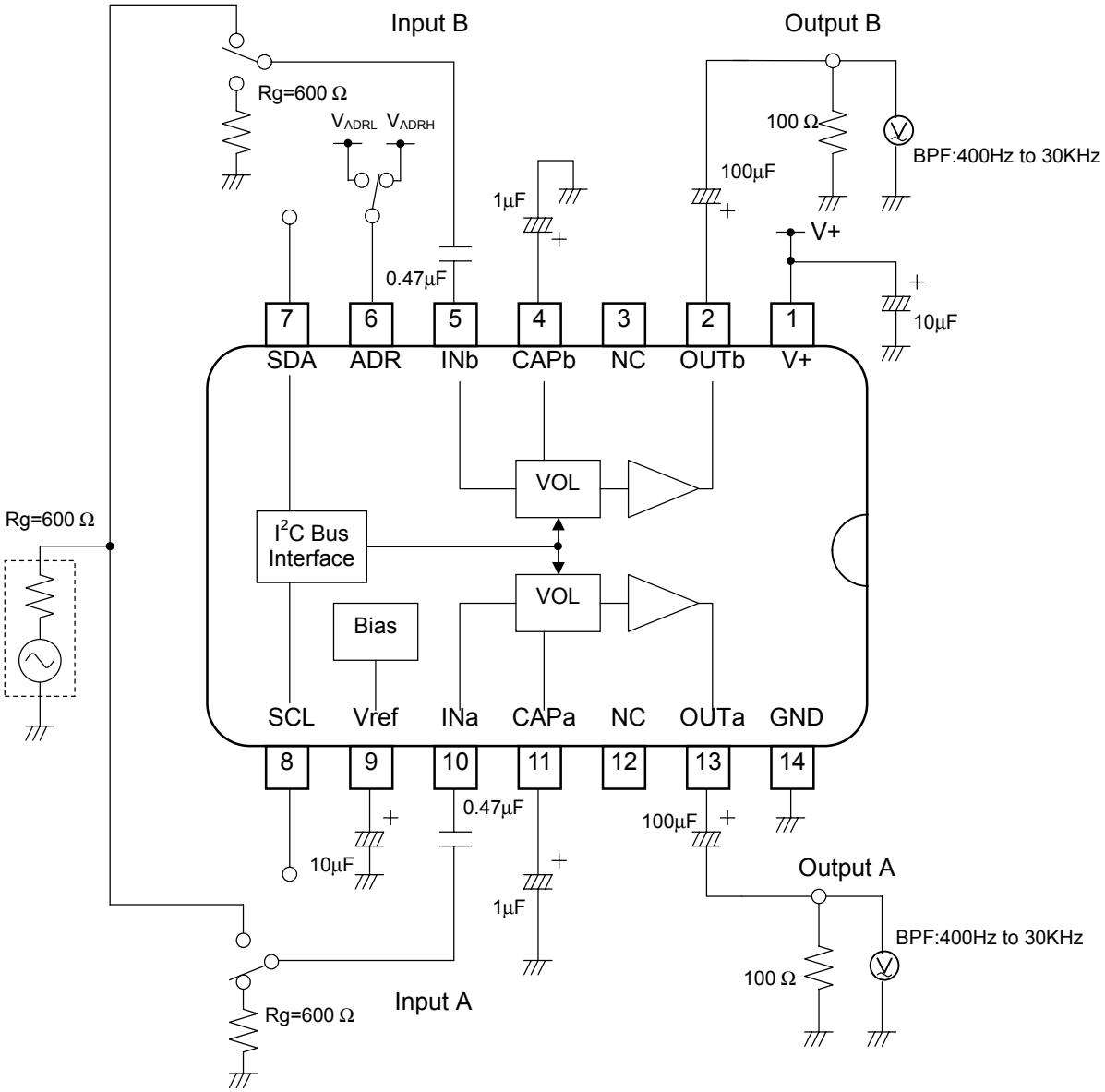
TEST CIRCUIT 1 (G_{VMAX}, G_{VMIN}, ΔG_V, V_{IM}, P_O, THD, Mute)



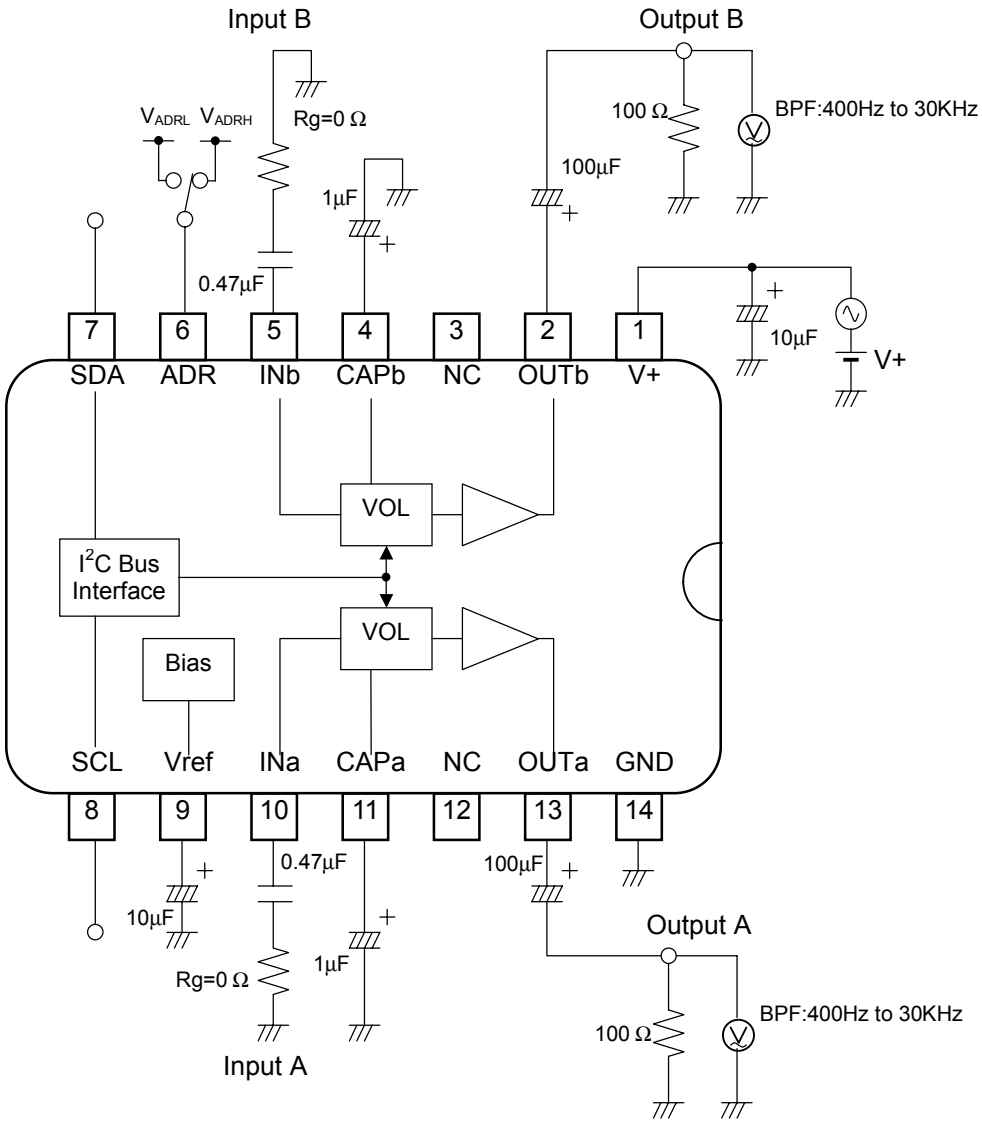
TEST CIRCUIT 2 (I_{CC}, V_{REF}, V_{NO1},V_{NO2})



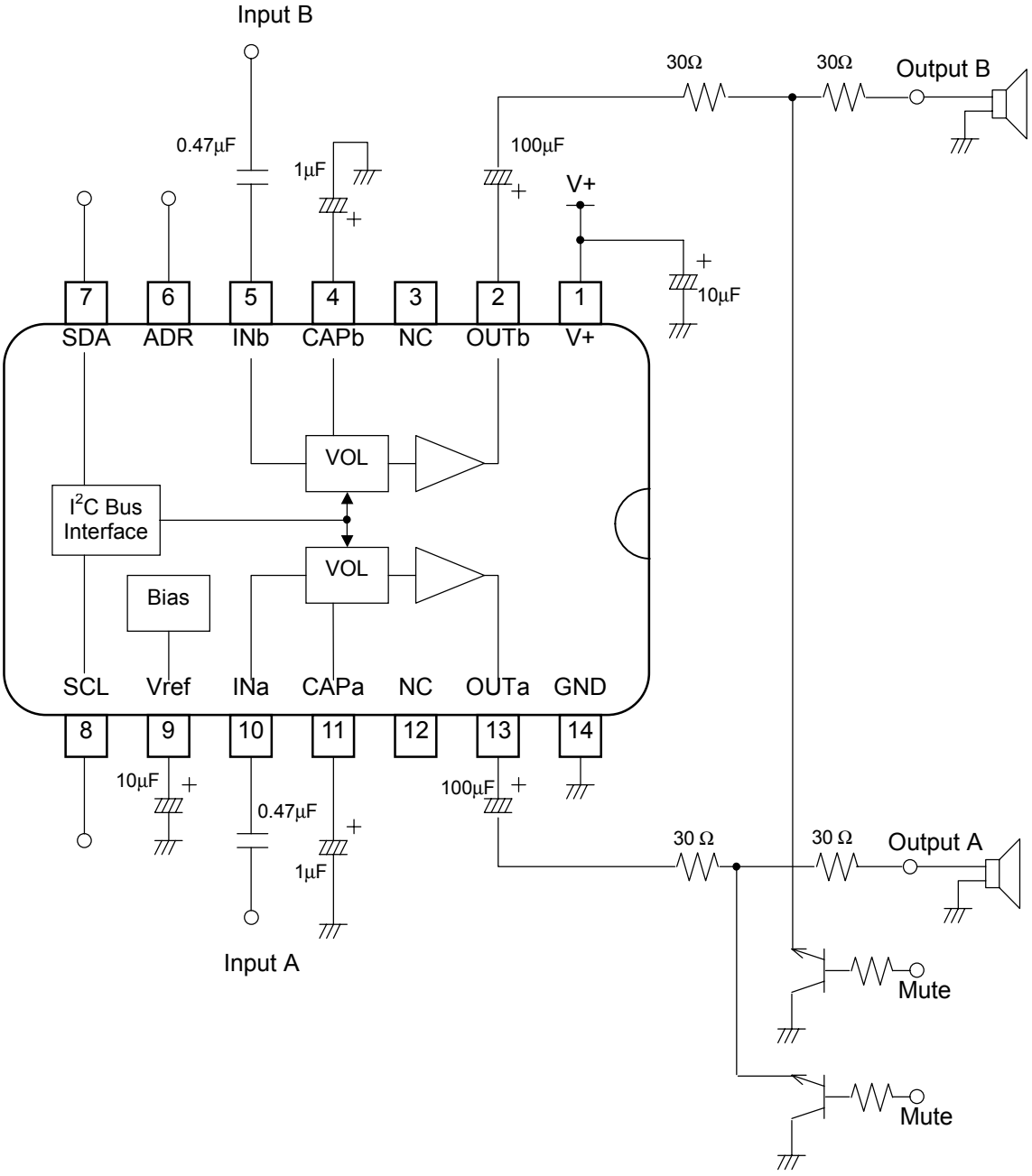
TEST CIRCUIT 3 (CS)



TEST CIRCUIT 4 (PSRR)



■ **APPLICATION CIRCUIT**



■ DEFINITION OF I²C REGISTER

● I²C BUS FORMAT

	MSB		LSB	MSB		LSB	MSB		LSB
S	Slave Address		A	Select Address		A	Data		A	P
1bit	8bit		1bit	8bit		1bit	8bit		1bit	1bit

S: Starting Term
A: Acknowledge Bit
P: Ending Term

● SLAVE ADDRESS

MSB							LSB	
1	0	0	0	0	0	0	0	80H (ADR = Low)
1	0	0	0	0	1	0	0	84H (ADR = High)

● SELECT ADDRESS

The auto-increment function cycles the select address as follows.
00H→01H→00H

Select Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	VOL							
01H	CHS	BAL					Don't Care	

■CONTROL REGISTER DEFAULT VALUE

Control register default value is all "0".

Select Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	0	0	0	0	0	0	0	0
01H	0	0	0	0	0	0	0	0

■CONTROL COMMAND TABLE

a) Master Volume

Select Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	VOL							

•VOL : Master Volume
Attenuation level : +20 to –80dB(0.5dB/step), MUTE

b) Balance

Select Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
01H	CHS	BAL					Don't Care	

•CHS : Balance channel select
"0" : Ach "Bch is attenuated" "1" : Bch "Ach is attenuated"

•BAL : Ach and Bch Ach and Bch Balance
Balance Level : 0 to –30dB (1dB/Step) , MUTE

■**CONTROL COMMAND TABLE**

a) Master Volume (Select Address: 00H) Volume level : +20 to –80dB(0.5dB/step), MUTE

		VOL							
Gain(dB)	**HEX**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
20	FF	1	1	1	1	1	1	1	1
19.5	FE	1	1	1	1	1	1	1	0
19	FD	1	1	1	1	1	1	0	1
18.5	FC	1	1	1	1	1	1	0	0
18	FB	1	1	1	1	1	0	1	1
17.5	FA	1	1	1	1	1	0	1	0
17	F9	1	1	1	1	1	0	0	1
16.5	F8	1	1	1	1	1	0	0	0
16	F7	1	1	1	1	0	1	1	1
15.5	F6	1	1	1	1	0	1	1	0
15	F5	1	1	1	1	0	1	0	1
14.5	F4	1	1	1	1	0	1	0	0
14	F3	1	1	1	1	0	0	1	1
13.5	F2	1	1	1	1	0	0	1	0
13	F1	1	1	1	1	0	0	0	1
12.5	F0	1	1	1	1	0	0	0	0
12	EF	1	1	1	0	1	1	1	1
11.5	EE	1	1	1	0	1	1	1	0
11	ED	1	1	1	0	1	1	0	1
10.5	EC	1	1	1	0	1	1	0	0
10	EB	1	1	1	0	1	0	1	1
9.5	EA	1	1	1	0	1	0	1	0
9	E9	1	1	1	0	1	0	0	1
8.5	E8	1	1	1	0	1	0	0	0
8	E7	1	1	1	0	0	1	1	1
7.5	E6	1	1	1	0	0	1	1	0
7	E5	1	1	1	0	0	1	0	1
6.5	E4	1	1	1	0	0	1	0	0
6	E3	1	1	1	0	0	0	1	1
5.5	E2	1	1	1	0	0	0	1	0
5	E1	1	1	1	0	0	0	0	1
4.5	E0	1	1	1	0	0	0	0	0
4	DF	1	1	0	1	1	1	1	1
3.5	DE	1	1	0	1	1	1	1	0
3	DD	1	1	0	1	1	1	0	1
…	…	…	…	…	…	…	…	…	…
-79.5	38	0	0	1	1	1	0	0	0
-80	37	0	0	1	1	0	1	1	1
…	…	…	…	…	…	…	…	…	…
Mute	00	0	0	0	0	0	0	0	0

b) Balance (Select Address: 01H) Balance level : 0 to –30dB(1dB/step), MUTE

Channel Setting (CHS)	D7
Attenuated Bch Gain	0
Attenuated Ach Gain	1

Gain(dB)	BAL				
	D6	D5	D4	D3	D2
0	0	0	0	0	0
-1	0	0	0	0	1
-2	0	0	0	1	0
-3	0	0	0	1	1
-4	0	0	1	0	0
-5	0	0	1	0	1
-6	0	0	1	1	0
-7	0	0	1	1	1
-8	0	1	0	0	0
-9	0	1	0	0	1
-10	0	1	0	1	0
-11	0	1	0	1	1
-12	0	1	1	0	0
-13	0	1	1	0	1
-14	0	1	1	1	0
-15	0	1	1	1	1
-16	1	0	0	0	0
-17	1	0	0	0	1
-18	1	0	0	1	0
-19	1	0	0	1	1
-20	1	0	1	0	0
-21	1	0	1	0	1
-22	1	0	1	1	0
-23	1	0	1	1	1
-24	1	1	0	0	0
-25	1	1	0	0	1
-26	1	1	0	1	0
-27	1	1	0	1	1
-28	1	1	1	0	0
-29	1	1	1	0	1
-30	1	1	1	1	0
MUTE	1	1	1	1	1

[CAUTION]
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