National Semiconductor

PRELIMINARY
October 1990

NM24C09
8192-Bit Serial EEPROM with Synchronous Serial Bus and Write Protect

General Description

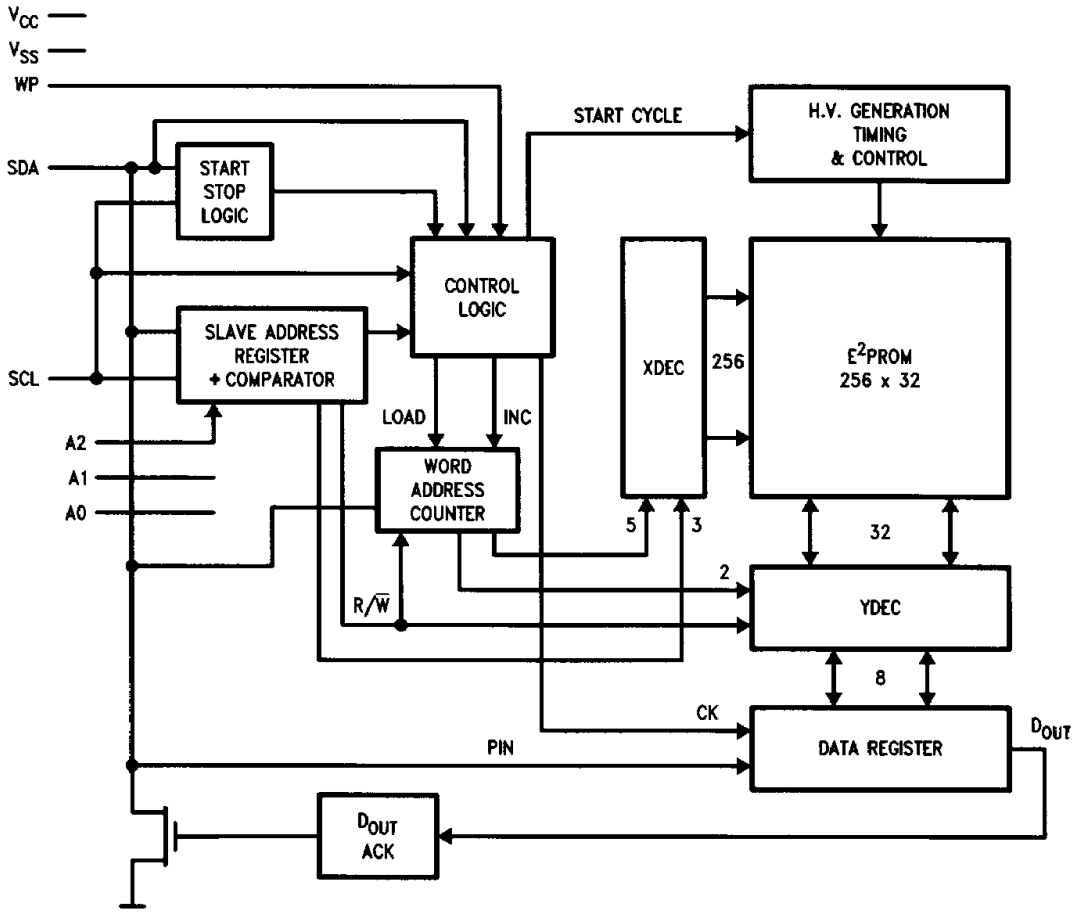
The NM24C09 is a CMOS 8192-bit serial E²PROM, internally organized as four 256 x 8 pages. The NM24C09 features a serial interface and software protocol allowing operation on a two wire bus. Programming of the upper half of the memory can be disabled by connecting the WP pin to V_{CC}.

National E²PROMs are designed and tested for applications requiring endurance of 100,000 data changes per bit. Data retention is specified to be greater than 40 years.

Features

- Low Power CMOS
  - — 2 mA active current typical
  - — 60 μA standby current typical
- Internally organized as four pages
  - — Each 256 x 8
- Hardwire write protect for upper block
- 2 wire serial interface
- Provides bidirectional data transfer protocol
- Sixteen byte page write mode
  - — Minimizes total write time per byte
- Self timed write cycle
  - — Typical write cycle time of 5 ms
- Data retention greater than 40 years
- 8 pin mini-DIP or 14 pin SO package

Functional Diagram



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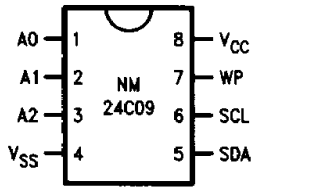
RRD-B20M110/Printed in U. S. A.

Connection Diagrams

Dual-In-Line Package (N)



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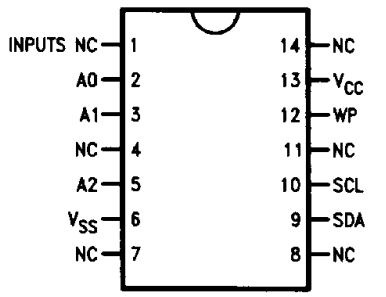
Top View

See NS Package Number N08E

Pin Names

A0, A1, A2	Address Inputs
V_{SS}	Ground
SDA	Data
SCL	Clock
V_{CC}	+5V
WP	Write Protect
NC	No Connection

SO Package (M)



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Top View

See NS Package Number M14B

Ordering Information

Commercial Temperature Range (0°C to +70°C)

Order Number
NM24C09N
NM24C09M

Extended Temperature Range (−40°C to +85°C)

Order Number
NM24C09EN
NM24C09EM

Military Temperature Range (−55°C to +125°C)

Order Number
NM24C09MN
NM24C09MM

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM24C09	0°C to +70°C
NM24C09E	−40°C to +85°C
NM24C09M (Mil. Temp.)	−55°C to +125°C
Positive Power Supply	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ. (Note 1)	Max	
I_{CC}	Power Supply Current	f_{SCL} = 100 kHz		2.0	3.0	mA
I_{SB} (Note 2)	Standby Current	V_{IN} = GND or V_{CC}		60	100	μA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	10	μA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	10	μA
V_{IL}	Input Low Voltage		−0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Capacitance T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Conditions	Max	Units
$C_{I/O}$ (Note 3)	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN} (Note 3)	Input Capacitance (A_0, A_1, A_2, SCL)	V_{IN} = 0V	6	pF

A.C. Conditions of Test

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	V_{CC} x 0.5
Output Load	1 TTL Gate and C_L = 100 pF

Note 1: Typical values are for T_A = 25°C and nominal supply voltage.

Note 2: SDA and SCL require pull up resistor.

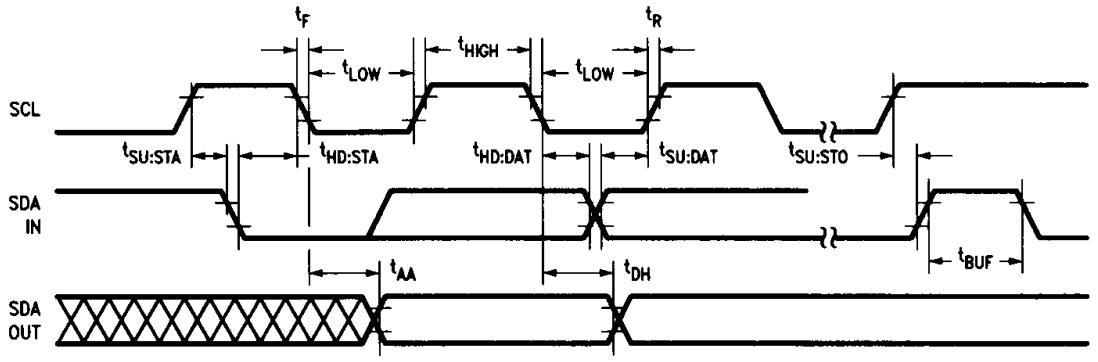
Note 3: This parameter is peridically sampled and not 100% tested.

Read and Write Cycle Limits

Symbol	Parameter	Min	Max	Units
f_{SCL}	SCL Clock Frequency	0	100	kHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	μs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		μs
$t_{HD:STA}$	Start Condition Hold Time	4.0		μs
t_{LOW}	Clock Low Period	4.7		μs
t_{HIGH}	Clock High Period	4.0		μs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		μs
$t_{HD:DAT}$	Data in Hold Time	0		μs
$t_{SU:DAT}$	Data in Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	μs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		μs
t_{DH}	Data Out Hold Time	300		ns
t_{WR} (Note 4)	Write Cycle Time		10	ms

Note 4: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end ot the internal erase/program cycle. During the write cycle, the NM24C09 bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Bus Timing



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Pin Descriptions

SERIAL CLOCK (SCL)

The SCL input is used to clock all data into and out of the device.

SERIAL DATA (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

ADDRESS (A_0, A_1)

The A_0, A_1 inputs are unused by the NM24C09 however, they must be tied to V_{SS} to insure proper device operation.

A2 CHIP ADDRESS INPUT

The level on this input is compared with the corresponding bit in the slave address. The chip is selected if the compare is true. Up to 2 NM24C09 can be connected to the bus. This input must be connected to either V_{SS} or V_{CC}.

WP WRITE PROTECTION

If tied high (logical 1) PROGRAM operations onto the upper memory page (addresses 1FF–3FF) will not be executed. READ operations are possible.

If tied low (logical 0) normal memory operation is enabled (READ/WRITE the entire memory 000–3FF).

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming. When write is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

Device Operation

The NM24C09 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operation. Therefore, the NM24C09 will be considered a slave in all applications.

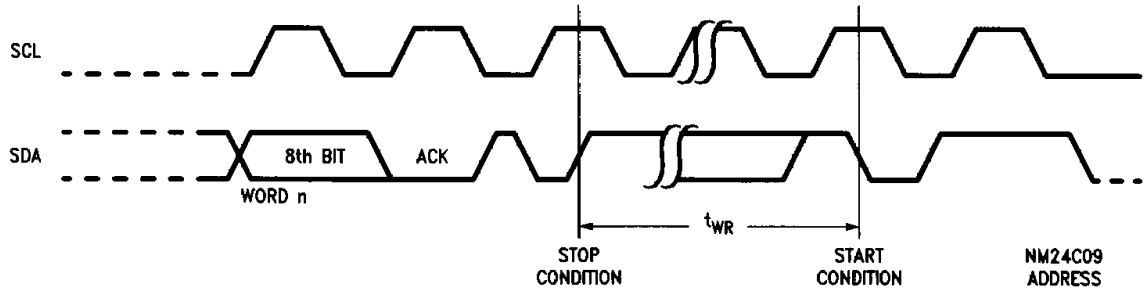
CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to *Figures 1* and *2*.

START CONDITION

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24C09 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Write Cycle Timing



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Write Cycle Limits

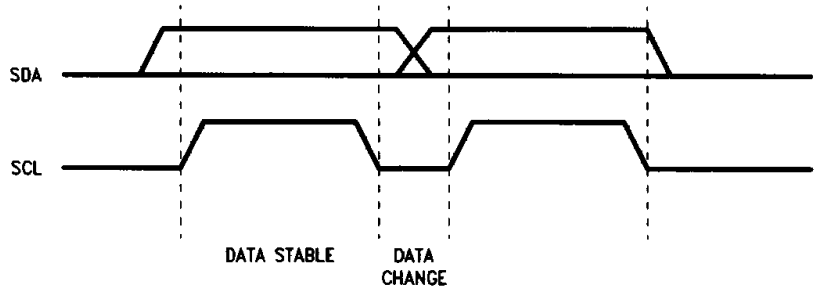

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FIGURE 1. Data Validity

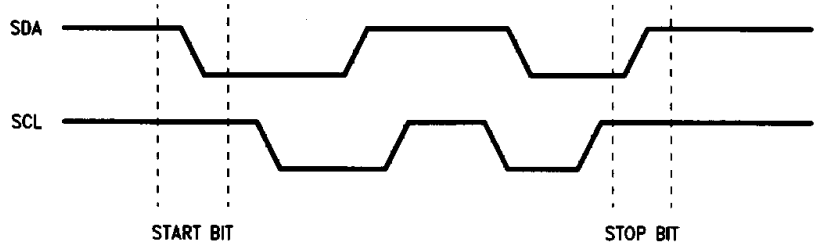

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FIGURE 2. Definition of Start and Stop

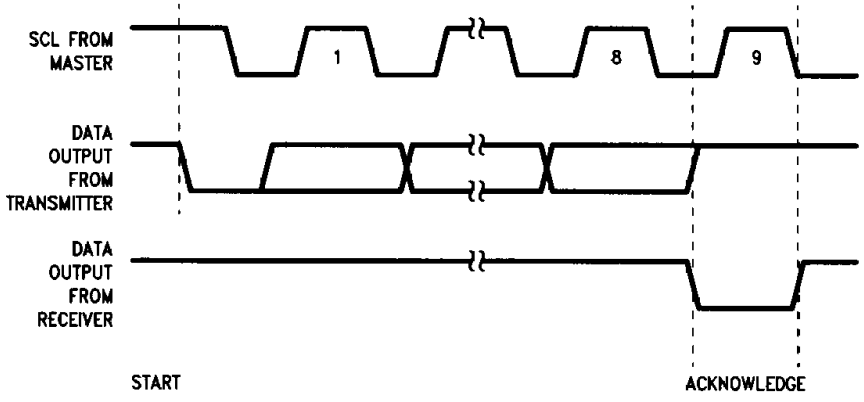

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FIGURE 3. Acknowledge Response from Receiver

STOP CONDITION

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24C09 to place the device in the standby power mode.

ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to *Figure 3*.

The NM24C09 will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the NM24C09 will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the NM24C09 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the NM24C09 will continue to transmit data. If an acknowledge is not detected, the NM24C09 will terminate further data transmissions and await the stop condition to return to the standby power mode.

Device Addressing

Following a start condition the bus master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see *Figure 4*). For the NM24C09 this is fixed as 1010[B].

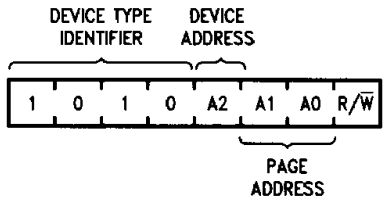

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FIGURE 4. Slave Address

The fifth bit is chip address bit A2. The next 2 bits of the slave address field are the page select bits. They are used by the master device to select which of the four 256 word pages of memory are to be accessed. These bits are, in effect, the 2 most significant bits of the word address. It should be noted, the protocol limits the size of memory to eight pages of 256 words; therefore, the protocol can support only 2 NM24C09 per system.

The last bit of the slave address defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected.

Following the start condition, the NM24C09 monitors the SDA bus comparing the slave address being transmitted with its slave address. Upon a compare the NM24C09 outputs an acknowledge on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the NM24C09 will execute a read or write operation.

Write Operations

BYTE WRITE

For a write operation, the NM24C09 requires a second address field. This address field is the word address, comprised of eight bits, providing access to any one of the 256 words in the selected page of memory. Upon receipt of the word address the NM24C09 responds with an acknowledge, and awaits the next eight bits of data, again responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM24C09 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the NM24C09 inputs are disabled, and the device will not respond to any requests from the master. Refer to *Figure 5* for the address, acknowledge and data transfer sequence.

PAGE WRITE

The NM24C09 is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first data word is tranferred, the master can transmit up to fifteen more words. After the receipt of each word, the NM24C09 will respond with an acknowledge.

After the receipt of each word, the four low order address bits are internally incremented by one. The high order seven bits of the word and slave address remain constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to *Figure 6* for the address, acknowledge and data transfer sequence.

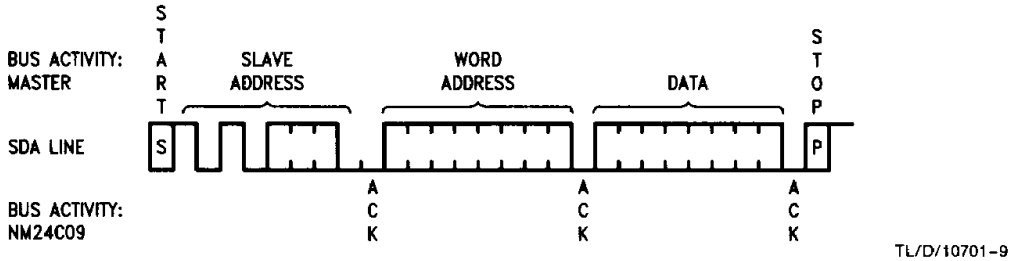

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FIGURE 5. Byte Write

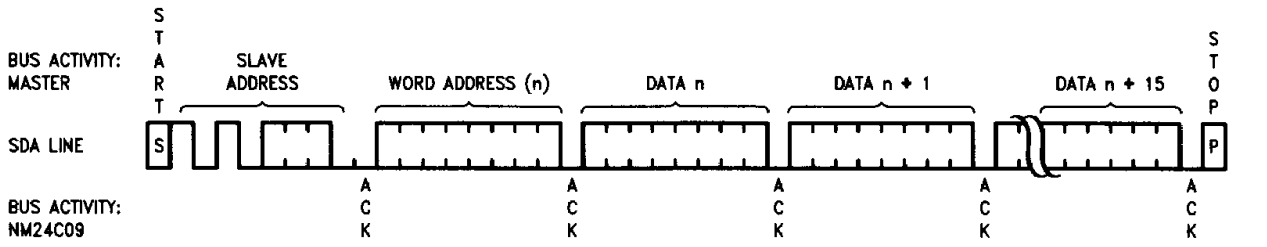

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FIGURE 6. Page Write

Write Operations (Continued)

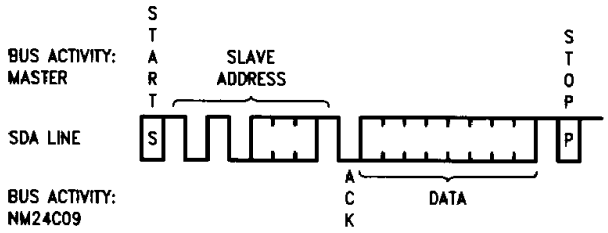

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FIGURE 7. Current Address Read

WRITE PROTECTION

Programming of the upper half of the memory will not take place if the WP pin of the NM24C09 is connected to V_{CC} (+5V). The NM24C09 will accept slave and word addresses but if the memory accessed is write protected by the WP pin, the NM24C09 will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the stop condition is asserted.

ACKNOWLEDGE POLLING

The disabling of the inputs can be used to take advantage of the FAST write cycle time. Once the stop condition is issued to indicate the end of the host's write operation the NM24C09 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM24C09 is still busy with the write operation no ACK will be returned. If the NM24C09 has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation.

Read Operations

Read operations are initiated in the same manner as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

CURRENT ADDRESS READ

Internally the NM24C09 contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the NM24C09 issues an acknowledge and transmits the eight bit word. The master will not acknowledge the transfer but does generate a stop condition and the NM24C09 discontinues tranmission. Refer to *Figure 7* for the sequence of address, acknowledge and data transfer.

RANDOM READ

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, and the slave address followed by the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the NM24C09 and then by the eight bit word. The master will not acknowledge the transfer but does generate the stop condition and the NM24C09 discontinues transmission. Refer to *Figure 8* for the address, acknowledge and data transfer sequence.

SEQUENTIAL READ

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted as with the other read modes, however, the master now resonds with an acknowledge, indicating it requires additional data. The NM24C09 continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge and generating a stop condition.

The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. If more than 1024 words are read, the counter "rolls over" and the NM24C09 continues to output data for each acknowledge received. Refer to *Figure 9* for the address, acknowledge and data transfer sequence.

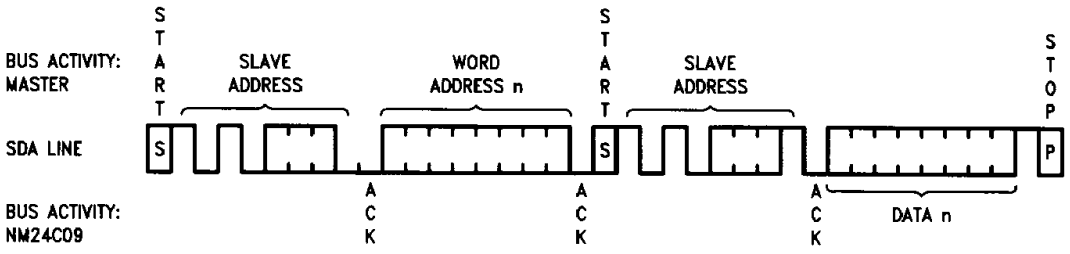

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FIGURE 8. Random Read

Read Operations (Continued)

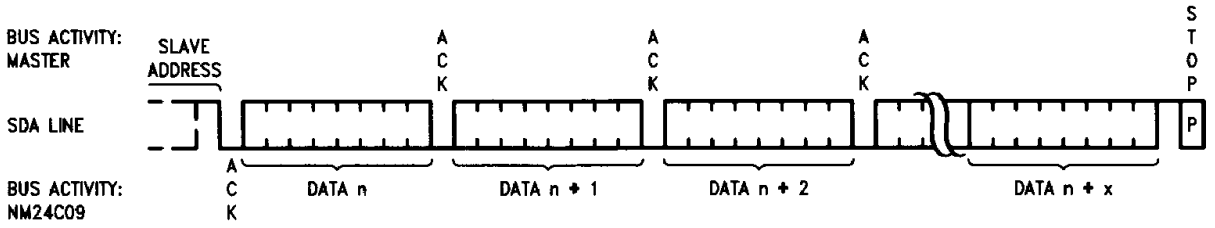

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FIGURE 9. Sequential Read

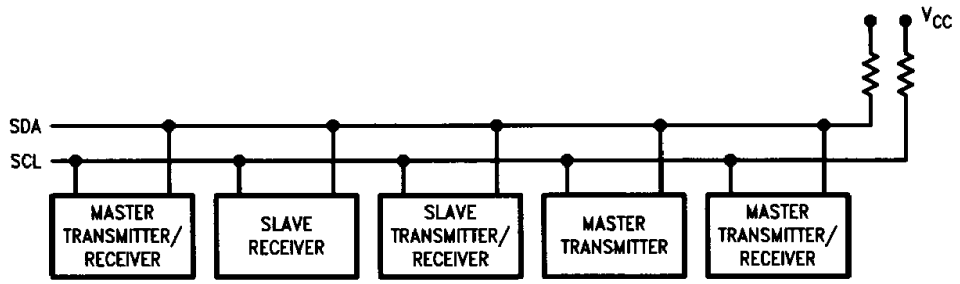

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FIGURE 10. Typical System Configuration

Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

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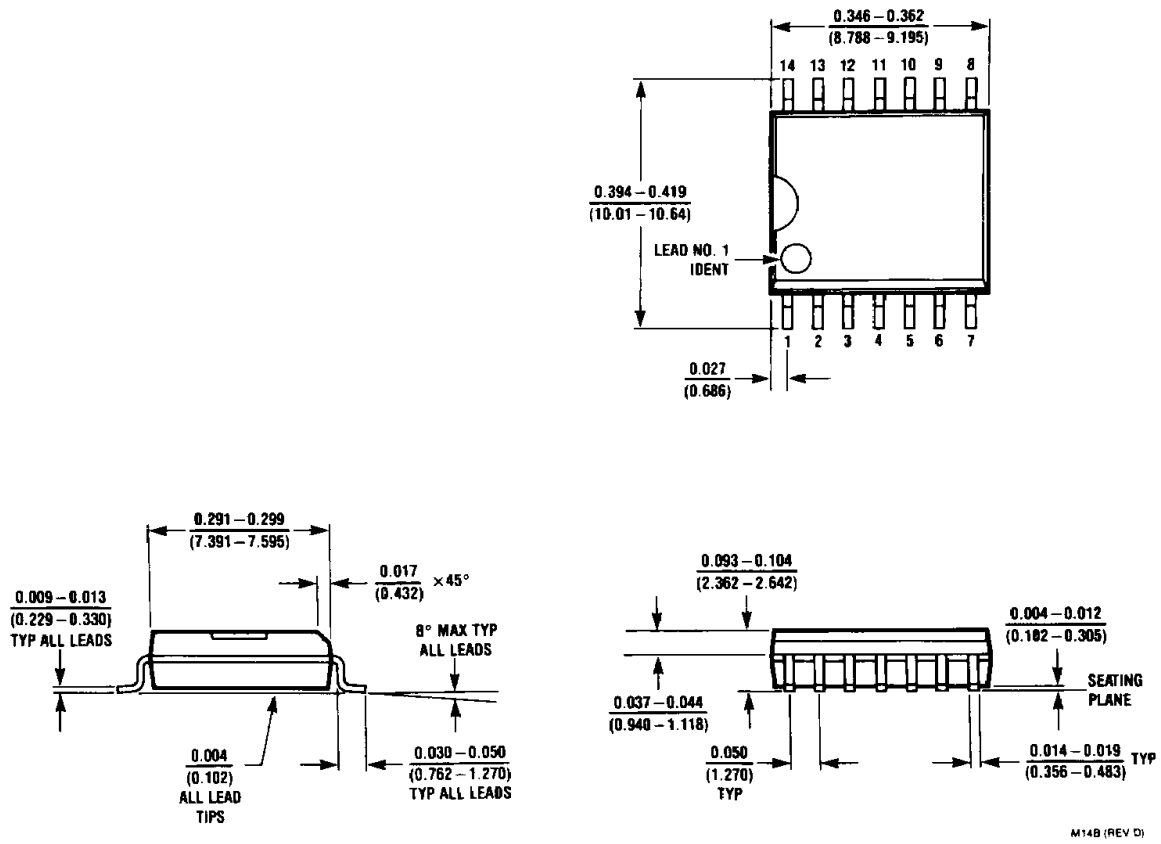
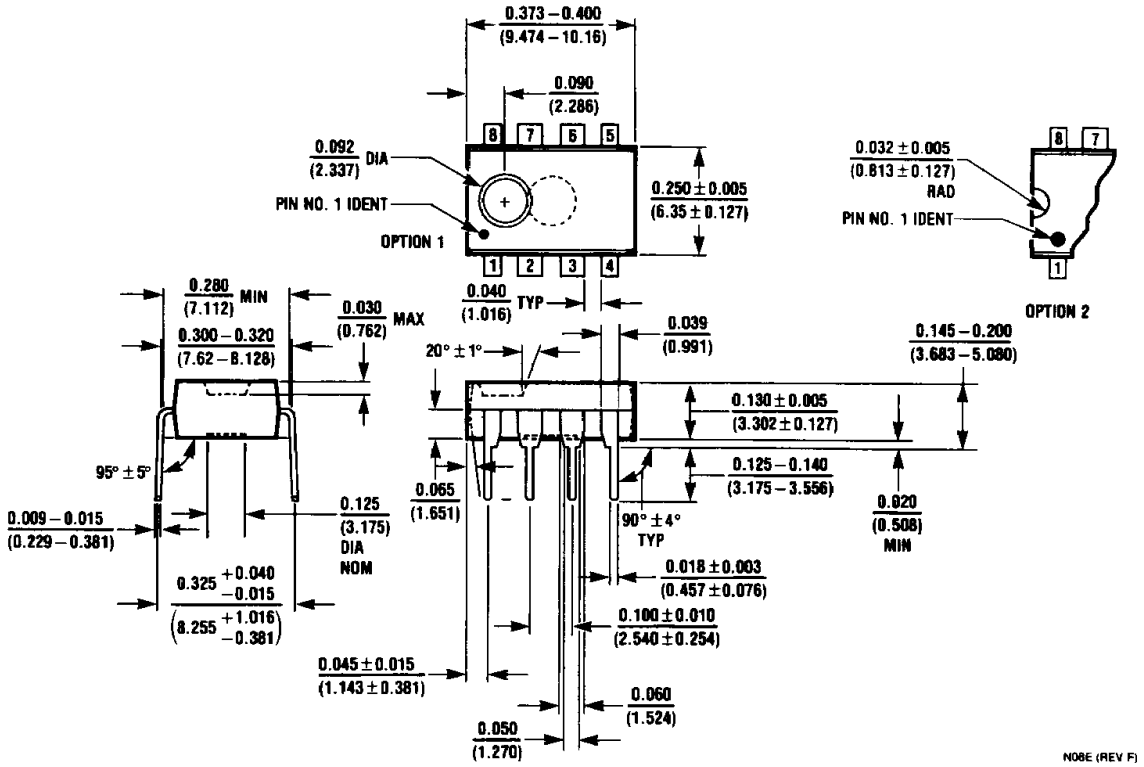
Physical Dimensions inches (millimeters)



SO Package (M)
Order Number NM24C09EM, NM24C09M or NM24C09MM
NS Package Number M14B

Physical Dimensions inches (millimeters) (Continued)



Dual-In-Line Package (N)
Order Number NM24C09EN, NM24C09MN or NM24C09N
NS Package Number N08E

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National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: (408) 721-5000
TWX: (910) 339-9240

National Semiconductor GmbH
Industriestrasse 10
D-8080 Furstenfeldbruck
West Germany
Tel: (0-81-41) 103-0
Telex: 527-649
Fax: (08141) 103554

National Semiconductor Japan Ltd.
Sanseido Bldg. 5F
4-15 Nishi Shinjuku
Shinjuku-Ku,
Tokyo 160, Japan
Tel: 3-299-7001
FAX: 3-299-7000

National Semiconductor Hong Kong Ltd.
Suite 513, 5th Floor
Chinachem Golden Plaza,
77 Mody Road, Tsimshatsui East,
Kowloon, Hong Kong
Tel: 3-7231290
Telex: 52996 NSSEA HX
Fax: 3-3112536

National Semicondutores Do Brasil Ltda.
Av. Brig. Faria Lima, 1383
6.0 Andor-Conj. 62
01451 Sao Paulo, SP, Brasil
Tel: (55/11) 212-5066
Fax: (55/11) 211-1181 NSBR BR

National Semiconductor (Australia) PTY, Ltd.
1st Floor, 441 St. Kilda Rd.
Melbourne, 3004
Victory, Australia
Tel: (03) 267-5000
Fax: 61-3-2677458