National Semiconductor

NSC810A RAM-I/O-Timer

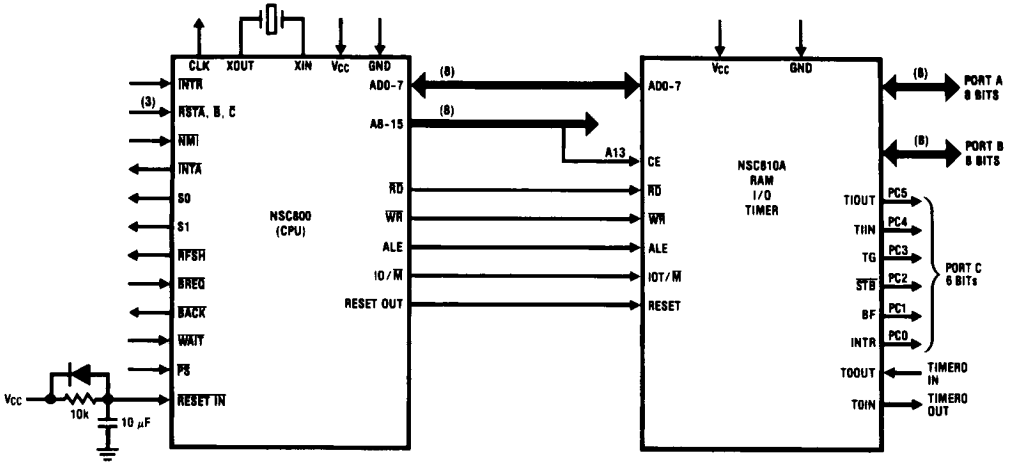
General Description

The NSC810A, the luxury model of our NSC800™ peripheral line, sports triple ported I/O, dual 16-bit timers and a 1024-bit static storage area. The three ports can be combined for a total of 22 general purpose I/O lines. In addition, port A has several strobed mode operations. Note the single instruction I/O bit operations for quick and efficient data handling from the ports. The timers feature 6 modes of operation and prescalers for those complicated timing tasks. The NSC810A comes in two models: the Dual-In-Line (DIP) and the surface mount chip carrier (LCC). It also comes in three exciting temperature ranges (Commercial, Industrial, and Military) and two reliability flows (extended burn-in and military class B in accordance with Method 5004 of MIL-STD-883). This is brought to you through the microCMOS silicon gate technology of National Semiconductor.

Features

- Three programmable I/O ports
- Dual 16-bit programmable counter/timers
- 2.4V–6.0V power supply
- Very low power consumption
- Fully static operation
- Single-instruction I/O bit operations
- Timer operation—DC to 5 MHz
- Bus compatible with NSC800™ family
- Speed: compatible with NSC800
  - NSC810A-4 → NSC800-4 @ 4.0 MHz
  - NSC810A-3 → NSC800 @ 2.5 MHz
  - NSC810A-1 → NSC800-1 @ 1.0 MHz

NSC810A Connection Diagram



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1.0 Absolute Maximum Ratings

(Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	−65°C to +150°C
Voltage at Any Pin with Respect to Ground	−0.3V to V_{CC} + 0.3V
V_{CC}	7V
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

2.0 Operating Conditions

V_{CC} = 5V ± 10%

NSC810A-1 → 0°C to +70°C
−40°C to +85°C

NSC810A-3 → 0°C to +70°C
−40°C to +85°C
−55°C to +125°C

NSC810A-4 → 0°C to +70°C
−40°C to +85°C
−55°C to +125°C

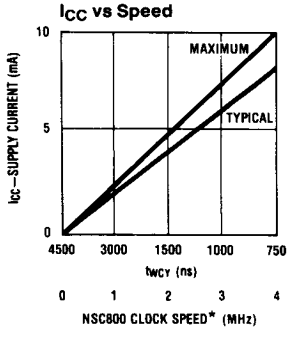
3.0 DC Electrical Characteristics

V_{CC} = 5V ±10%, GND = 0V, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Logical 1 Input Voltage		0.8 V_{CC}		V_{CC}	V
V_{IL}	Logical 0 Input Voltage		0		0.2 V_{CC}	V
V_{OH}	Logical 1 Output Voltage	I_{OH} = −1.0 mA I_{OUT} = −10 μA	2.4 V_{CC}−0.5			V V
V_{OL}	Logical 0 Output Voltage	I_{OL} = 2 mA I_{OUT} = 10 μA	0 0		0.4 0.1	V V
I_{IL}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$	−10.0		10.0	μA
I_{OL}	Output Leakage Current	$0 \le V_{IN} \le V_{CC}$	−10.0		10.0	μA
I_{CC}	Active Supply Current	I_{OUT} = 0, Timer = Mode 1, T0IN = T1IN = 2.5 Mhz, t_{WCY} = 750 ns, T_A = 25°C		8	10	mA
I_Q	Quiescent Current	No Input Switching, T_A = 25°C, RESET = 0, IO/$\overline{M}$ = 1, $\overline{RD}$ = 1, $\overline{WR}$ = 1, ALE = 1, V_{IN} = V_{CC}, t_{IN} = 0 Hz, t_{OUT} = 0		10	100	μA
C_{IN}	Input Capacitance			4	7	pF
C_{OUT}	Output Capacitance			6	10	pF
V_{CC}	Power Supply Voltage	(Note 2)	2.4	5	6	V
V_{DRV}	Data Retention Voltage		1.8			V

Note 1: Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.

Note 2: Operation at lower power supply voltages will reduce the maximum operating speed. Operation at voltages other than 5V ±10% is guaranteed by design, not tested.



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*When NSC810A is used with NSC800

4.0 AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$, GND = 0V

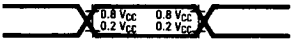
Symbol	Parameter	Conditions	NSC810A-1		NSC810A-3		NSC810-4		Units
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Access Time from ALE	C_L = 150 pF		1000		400		300	ns
t_{AH}	AD0-7, CE, IOT/$\overline{M}$ Hold Time		100		60		30		ns
t_{ALE}	ALE Strobe Width (High)		200		125		100		ns
t_{ARW}	ALE to $\overline{RD}$ or $\overline{WR}$ Strobe		150		120		75		ns
t_{AS}	AD0-7, CE, IOT/$\overline{M}$ Set-Up Time		100		45		25		ns
t_{DH}	Data Hold Time		150		90		40		ns
t_{DO}	Port Data Output Valid			350		310		300	ns
t_{DS}	Data Set-Up Time		100		80		50		ns
t_{PE}	Peripheral Bus Enable			320		200		200	ns
t_{PH}	Peripheral Data Hold Time		150		125		100		ns
t_{PS}	Peripheral Data Set-Up Time		100		75		50		ns
t_{PZ}	Peripheral Bus Disable (TRI-STATE®)			150		150		150	ns
t_{RB}	$\overline{RD}$ to BF Invalid			300		300		300	ns
t_{RD}	Read Strobe Width		400		320		185		ns
t_{RDD}	Data Bus Disable		0	100	0	100	0	75	ns
t_{RI}	$\overline{RD}$ to $\overline{INTR}$ Output			320		320		300	ns
t_{RWA}	$\overline{RD}$ or $\overline{WR}$ to Next ALE		125		100		75		ns
t_{SB}	$\overline{STB}$ to BF Valid			300		300		300	ns
t_{SH}	Peripheral Data Hold with Respect to $\overline{STB}$		150		125		100		ns
t_{SI}	$\overline{STB}$ to $\overline{INTR}$ Output			300		300		300	ns
t_{SS}	Peripheral Data Set-Up with Respect to $\overline{STB}$		100		75		50		ns
t_{SW}	$\overline{STB}$ Width		400		320		220		ns
t_{WB}	$\overline{WR}$ to BF Output			340		340		300	ns
t_{WI}	$\overline{WR}$ to $\overline{INTR}$ Output			320		320		300	ns
t_{WR}	$\overline{WR}$ Strobe Width		400		320		220		ns
t_{WCY}	Width of Machine Cycle		3000		1200		750		ns

Note: Test conditions: t_{WCY} = 3000 ns for NSC810A-1, 1200 ns for NSC810A-3, 750 ns for NSC810A-4

5.0 Timer AC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_C	Clock Frequency		DC		2.5	MHz
F_{CP}	Clock Frequency	Prescale Selected	DC		5.0	MHz
t_{CW}	Clock Pulse Width		150			ns
t_{CWP}	Clock Pulse Width	Prescale Selected	75			ns
t_{GS}	Gate Set-Up Time	With Respect to Negative Clock Edge	100			ns
t_{GH}	Gate Hold Time	With Respect to Negative Clock Edge	250			ns
t_{CO}	Clock to Output Delay	C_L = 100 pF			350	ns

AC TESTING INPUT/OUTPUT WAVEFORM



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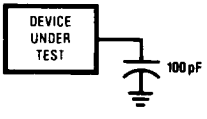
AC TESTING LOAD CIRCUIT



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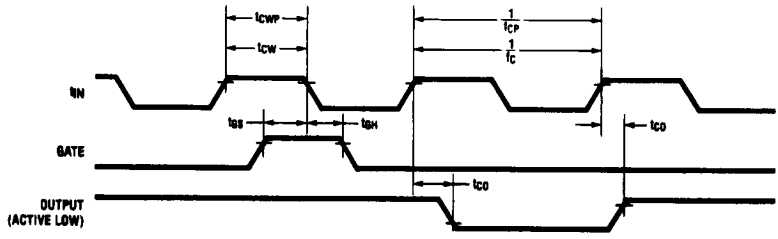
6.0 Timing Waveforms

Timer Waveforms



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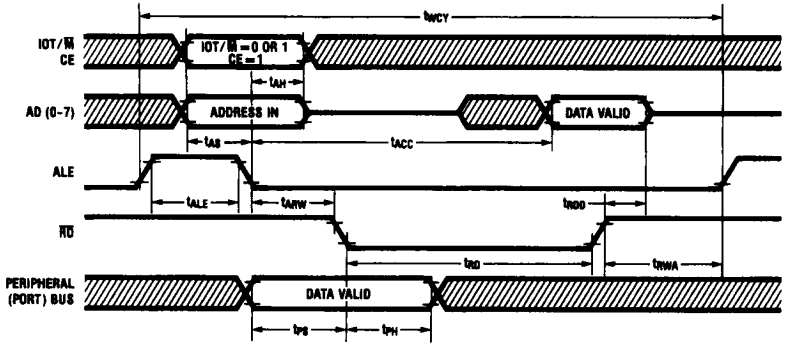
Read Cycle (Read from RAM, Port or Timer)



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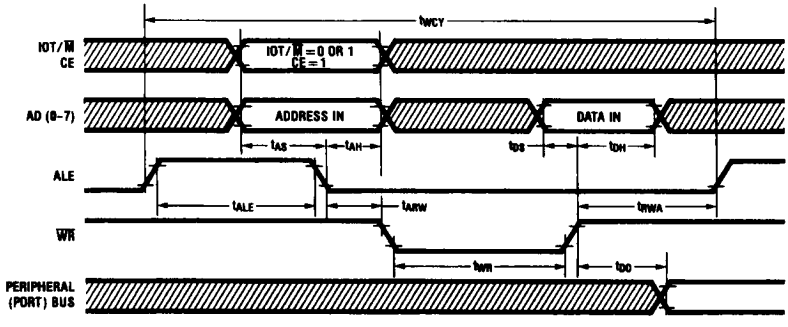
Note: Diagonal lines indicate interval of invalid data.

Write Cycle (Write to RAM, Port or Timer)



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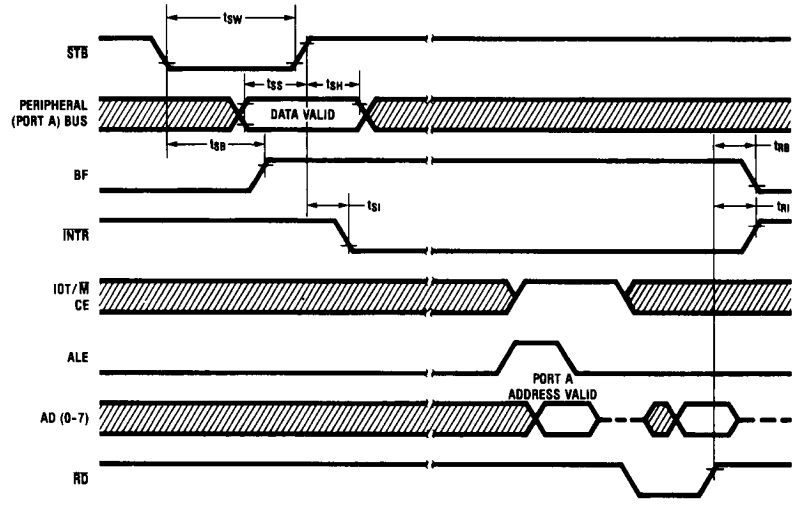
Note: Diagonal lines indicate interval of invalid data.

6.0 Timing Waveforms (Continued)

Strobed Mode Input



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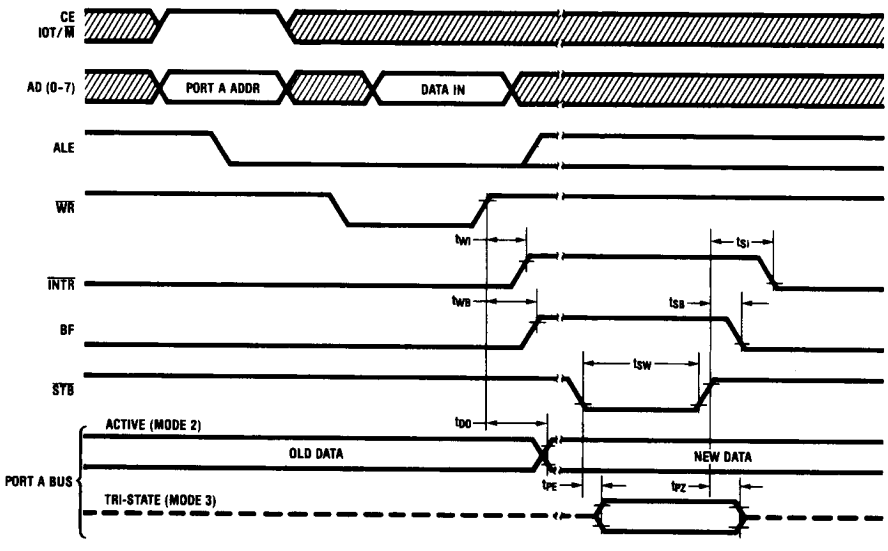
Note: Diagonal lines indicate interval of invalid data.

Strobed Mode Output



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Note: Diagonal lines indicate interval of invalid data.

7.0 Pin Descriptions

The function and mnemonic for the NSC810A signals are described below:

7.1 INPUT SIGNALS

Reset (RESET): RESET is an active-high input that resets all registers to 0 (low). The RAM contents remain unaltered.

Input/Output Timer or RAM Select (IOT/$\overline{M}$): IOT/$\overline{M}$ is an I/O memory select input line. A logic 1 (high) input selects the I/O-timer portion of the chip; a logic 0 (low) input selects the RAM portion of the chip. IOT/$\overline{M}$ is latched at the falling edge of ALE.

Chip Enable (CE): CE is an active-high input that allows access to the NSC810A. CE is latched at the falling edge of ALE.

Read ($\overline{RD}$): The $\overline{RD}$ is an active-low input that enables a read operation of the RAM or I/O-timer location.

Write ($\overline{WR}$): The $\overline{WR}$ is an active-low input that enables a write operation to RAM or I/O-timer locations.

Address Latch Enable (ALE): The falling edge of the ALE input latches AD0–AD7, CE and IOT/$\overline{M}$ inputs to form the address for RAM, I/O or timer.

Timer 0 Input (T0IN): T0IN is the clock input for timer 0.

7.2 OUTPUT SIGNALS

Timer 0 Output (T0OUT): T0OUT is the programmable output of timer 0. After reset, T0OUT is set high.

7.3 POWER SUPPLY SIGNALS

Positive DC Voltage (V_{CC}): V_{CC} is the 5V supply pin.

Ground (GND): Ground reference pin.

7.4 INPUT/OUTPUT SIGNALS

Address/Data Bus (AD0–AD7): The multiplexed bidirectional address/data bus; AD0–AD7 pins, are in the high impedance state when the NSC810A is not selected. AD0–AD7 will latch address inputs at the falling edge of ALE. The address will designate a location in RAM, I/O or timer. $\overline{WR}$ input enables 8-bit data to be written into the addressed location. $\overline{RD}$ input enables 8-bit data to be read from the addressed location. The $\overline{RD}$ or $\overline{WR}$ inputs occur while ALE is low.

Port A, 0–7 (PA0–PA7): Port A is an 8-bit basic mode input/output port, also capable of strobed mode I/O utilizing three control signals from port C. Strobed mode of operation on port A has three different modes; strobed input, strobed output with active peripheral bus, strobed output with TRI-STATE peripheral bus.

Port B, 0–7 (PB0–PB7): Port B is an 8-bit basic mode input/output port.

Port C, 0–5 (PC0–PC5): Port C is a 6-bit basic mode I/O port. Each pin has a programmable second function, as follows:

PC0/$\overline{INTR}$: $\overline{INTR}$ is an active-low, strobed mode interrupt request to the Central Processor Unit (CPU).

PC1/BF: BF is an active-high, strobed mode, buffer full output to peripheral devices.

PC2/$\overline{STB}$: $\overline{STB}$ is an active-low, strobed mode input from peripheral devices.

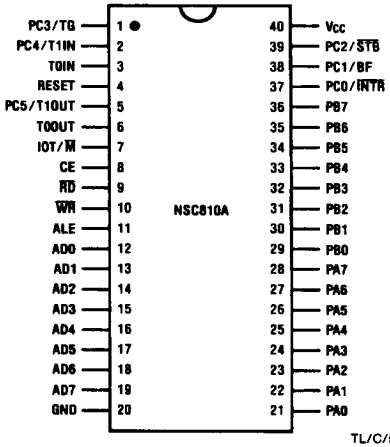
PC3/TG: TG is the timer gating signal.

PC4/T1IN: T1IN is the clock input for timer 1.

PC5/T1OUT: T1OUT is the programmable output of timer 1.

8.0 Connection Diagrams

Dual-In-Line Package



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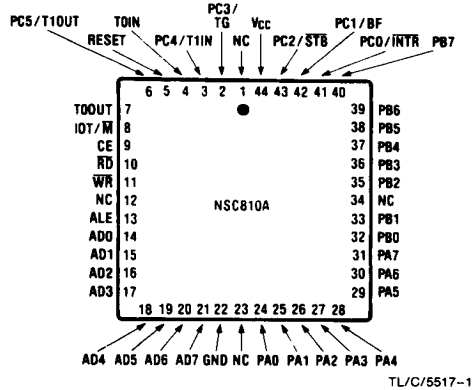
Top View

Order Number NSC810AD or NSC810AN
See NS Package Number D40C or N40A

Chip Carrier



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Top View

NC = no connect

Order Number NSC810AE or NSC810AV
See NS Package Number E44B or V44A

9.0 Functional Description

Figure 1 is a detailed block diagram of the NSC810A. The functional description that follows describes the RAM, I/O and TIMER sections.

9.1 RANDOM ACCESS MEMORY (RAM)

The memory portion of the RAM-I/O-timer is accessed by a 7-bit address input to pins AD0 through AD6. The IOT/$\overline{M}$ input must be low (RAM select) and the CE input must be high at the falling edge of ALE to address the RAM. Address bit AD7 is a "don't care" for RAM addressing. Timing for RAM read and write operations is shown in the timing diagrams. The RAM is 128 x 8.

9.2 DETAILED BLOCK DIAGRAM

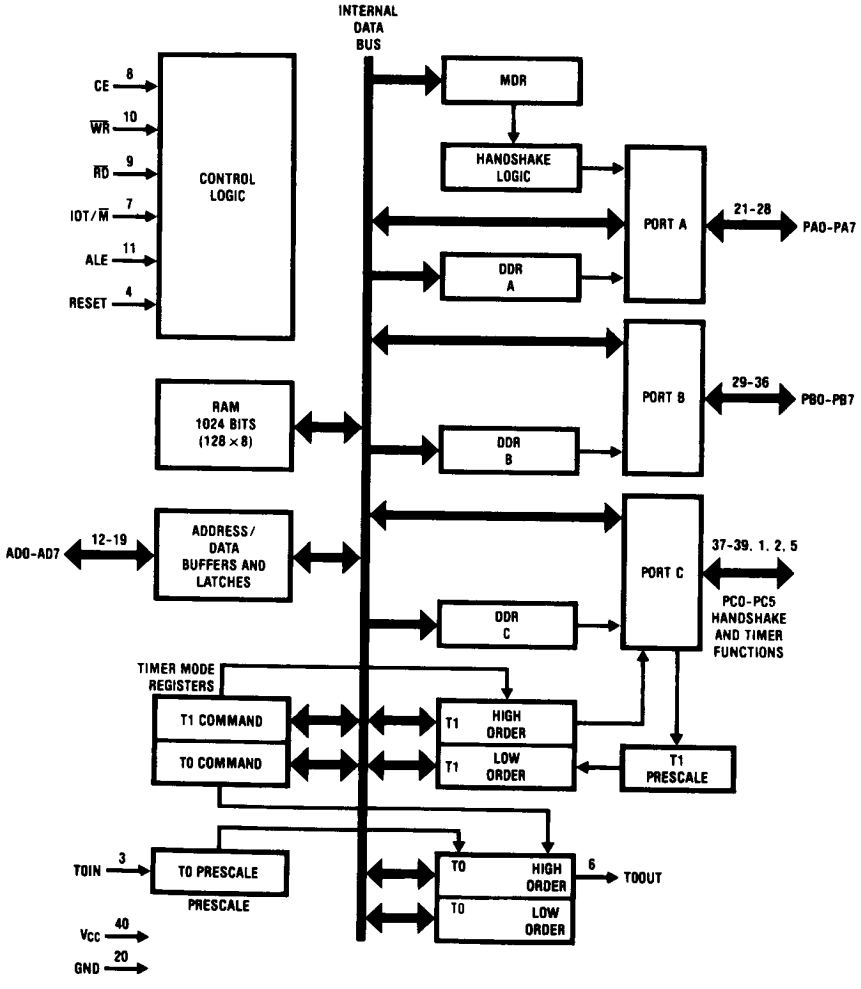

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FIGURE 1

9.0 Functional Description (Continued)

9.3 I/O PORTS

The three I/O ports, labeled A, B, and C, can be programmed to be almost any combination of Input and Output bits. Ports A and B are configured as 8 bits wide, while port C is 6 bits. There are four different modes of operation for the ports. Three of the modes are for timed transfer of data between the peripheral and the NSC810A, this is called strobed I/O. The fourth mode is for direct transfer without handshaking with the peripheral.

The NSC810A can be programmed to operate in four different modes. One of these modes (Basic I/O) allows direct transfer of I/O data without any handshaking between the NSC810A and the peripheral. The other three modes (Strobed I/O) provide for timed transfers of I/O data with handshaking between the NSC810A and the peripheral.

The determination of the mode, data direction and data is done by five registers which are, handily, under program control. The Mode Definition Register (MDR), oddly enough, determines which mode the device will operate in, while the Data Direction Register (DDR) establishes the direction of the data transfer. The Data register contains the data that is being sent or has been received. The other two registers (bit-set, bit-clear) allow the individual bits in the data register to be set or cleared without affecting the other bits. Each port has its own set of these registers, except the MDR which affects ports A and C only.

In the strobed I/O modes, port C bits 0, 1 and 2 function as INTR (for the processor), BF, and STB respectively.

9.3.1 Registers

As can be seen in Table I, all the registers affecting I/O transfer are grouped at the lower address locations, this allows quicker handling and more maneuverability in tight data transfers. Also note in Table I that the NSC810A uses 23 I/O addresses out of a block of 26. The upper three bits of the address are determined by the chip enable address.

- **Mode Definition Register (MDR)**

As noted above this register defines the operating mode for ports A and C (port B is always in the basic I/O mode). The upper 3 bits of port C will also be in the basic I/O mode even when the lower 3 bits are being used for handshaking.

The four modes are as follows:

Mode 0—Basic I/O (Input or Output)

Mode 1—Strobed Mode Input

Mode 2—Strobed Mode Output (Active Peripheral Bus)

Mode 3—Strobed Mode Output (TRI-STATE Peripheral Bus)

The address assignment of the MDR is xxx00111 as shown in Table I. Table II specifies the data that must be loaded into the MDR to select the mode.

- **Data Direction Registers (DDR)**

Each port has a DDR that determines whether an individual port bit will be an input or an output. This can be considered the traffic light for the transfer of data between the CPU and the peripheral. Each port bit has a corresponding bit in this register. If the DDR bit is set (1) the port bit is an output; if it is cleared (0) the port bit is an input. The DDR bits cannot be written to individually. The register as a whole must be set to be consistent with all desired port bit directions.

TABLE I. I/O and Timer Address Designations

8-Bit Address Field Bits								Designation I/O Port, Timer, etc.	R (Read) W (Write)
7	6	5	4	3	2	1	0		
x	x	x	0	0	0	0	0	Port A (Data)	R/W
x	x	x	0	0	0	0	1	Port B (Data)	R/W
x	x	x	0	0	0	1	0	Port C (Data)	R/W
x	x	x	0	0	0	1	1	Not Used	**
x	x	x	0	0	1	0	0	DDR - Port A	W
x	x	x	0	0	1	0	1	DDR - Port B	W
x	x	x	0	0	1	1	0	DDR - Port C	W
x	x	x	0	0	1	1	1	Mode Definition Reg.	W
x	x	x	0	1	0	0	0	Port A - Bit-Clear	W
x	x	x	0	1	0	0	1	Port B - Bit-Clear	W
x	x	x	0	1	0	1	0	Port C - Bit-Clear	W
x	x	x	0	1	0	1	1	Not Used	**
x	x	x	0	1	1	0	0	Port A - Bit-Set	W
x	x	x	0	1	1	0	1	Port B - Bit-Set	W
x	x	x	0	1	1	1	0	Port C - Bit-Set	W
x	x	x	0	1	1	1	1	Not Used	**
x	x	x	1	0	0	0	0	Timer 0 (LB)	*
x	x	x	1	0	0	0	1	Timer 0 (HB)	*
x	x	x	1	0	0	1	0	Timer 1 (LB)	*
x	x	x	1	0	0	1	1	Timer 1 (HB)	*
x	x	x	1	0	1	0	0	STOP Timer 0	W
x	x	x	1	0	1	0	1	START Timer 0	W
x	x	x	1	0	1	1	0	STOP Timer 1	W
x	x	x	1	0	1	1	1	START Timer 1	W
x	x	x	1	1	0	0	0	Timer 0 Mode	R/W
x	x	x	1	1	0	0	1	Timer 1 Mode	R/W
x	x	x	1	1	0	1	0	Not Used	**
x	x	x	1	1	0	1	1	Not Used	**
x	x	x	1	1	1	0	0	Not Used	**
x	x	x	1	1	1	0	1	Not Used	**
x	x	x	1	1	1	1	0	Not Used	**
x	x	x	1	1	1	1	1	Not Used	**

x = don't care

LB = low-order byte

HB = high-order byte

* A write accesses the modulus register, a read the read buffer.

** A read from an unused location reads invalid data, a write does not affect any operation of NSC810A.

TABLE II. Mode Definition Register Bit Assignments

Mode	Bit							
	7	6	5	4	3	2	1	0
0	x	x	x	x	x	x	x	0
1	x	x	x	x	x	x	0	1
2	x	x	x	x	x	0	1	1
3	x	x	x	x	x	1	1	1

9.0 Functional Description (Continued)

Any write or read to the port bits contradicting the direction established by the DDR will not affect the port bits output or input. However, a write to a port bit, defined as an input, will modify the output latch and a read to a port bit, defined as an output, will read this output latch. See *Figure 2*.

• Data Registers

These registers contain the actual data being transferred between the CPU and the peripheral. In Basic I/O, data presented by the peripheral (read cycle) will be latched on the falling edge of $\overline{RD}$. Data presented by the CPU (write cycle) will be valid after the rising edge of $\overline{WR}$ (see AC characteristics for exact timing).

During Strobed I/O, data presented by the peripheral must be valid on the rising edge of $\overline{STB}$. Data received by the peripheral will be valid on the rising edge of $\overline{STB}$. Data latched by the port on the rising edge of $\overline{STB}$ will be preserved until the next CPU read or $\overline{STB}$ signal.

• Bit Set-Clear Registers

The I/O features of the RAM-I/O-timer allow modification of a single bit or several bits of a port with the Bit-Set and Bit-Clear commands. The address selected indicates whether a Bit-Set or Clear will take place. The incoming data on the address/data bus is latched at the trailing edge of the $\overline{WR}$ strobe and is treated as a mask. All bits containing 1s will cause the indicated operation to be performed on the corresponding port bit. All bits of the mask with 0s cause the corresponding port bits to remain unchanged. Three sample operations are shown in Table III using port B as an example.

TABLE III. Bit-Set and Clear Examples

Operation Port B	Set B7	Clear B2 and B0	Set B4, B3 and B1
Address	xxx01101	xxx01001	xxx01101
Data	10000000	00000101	00011010
Port Pins			
Prior State	00001111	10001111	10001010
Next State	10001111	10001010	10011010

9.3.2 Modes

Two data transfer modes are implemented: Basic I/O and Strobed I/O. Strobed I/O can be further subdivided into three categories: Strobed Input, Strobed Output (active peripheral bus) and Strobed Output (TRI-STATE peripheral bus). The following descriptions detail the functions of these categories.

• Basic I/O

Basic I/O mode uses the $\overline{RD}$ and $\overline{WR}$ CPU bus signals to latch data at the peripheral bus. This mode is the permanent mode of operation for ports B and C. Port A is in this mode if the MDR is set to mode 0. Read and write byte operations and bit operations can be done in Basic I/O. Timing for these modes is shown in the AC Characteristics Table and described with the data register definitions.

When the NSC810A is reset, all registers are cleared to zero. This results in the basic mode of operation being selected, all port bits are made inputs and the output latch for each port bit is cleared to zero. The NSC810A, at this point, can read data from any peripheral port without further setup. If outputs are desired, the CPU merely has to program the appropriate DDR and then send data to the data ports.

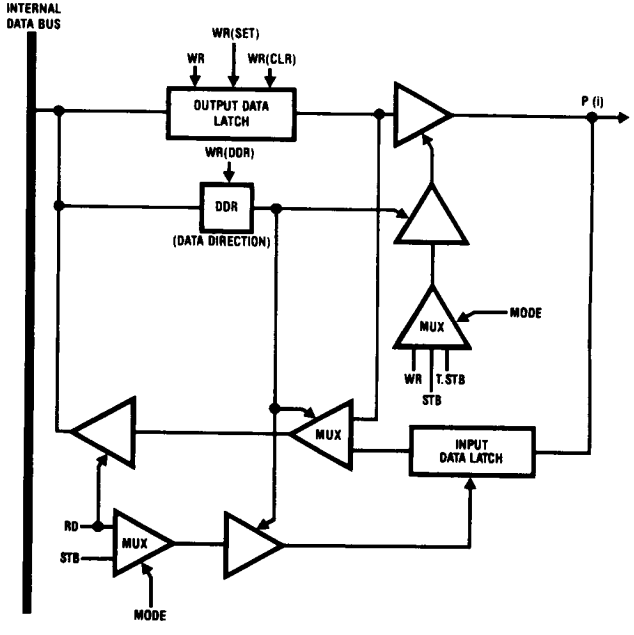

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FIGURE 2

9.0 Functional Description (Continued)

• Strobed I/O

Strobed I/O Mode uses the $\overline{STB}$, BF and $\overline{INTR}$ signals to latch the data and indicate that new data is available for transfer. Port A is used for the transfer of data when in any of the Strobed modes. Port B can still be used for Basic I/O and the lower 3-bits of port C are now the three handshake signals for Strobed I/O. Timing for this mode is shown in the AC Characteristic Tables.

Initializing the NSC810A for Strobed I/O Mode is done by loading the data shown in Table IV into the specified register. The registers should be loaded in the order (left to right) that they appear in Table IV.

TABLE IV. Mode Definition Register Configurations

Mode	MDR	DDR Port A	DDR Port C	Port C Output Latch
Basic I/O	xxxxxxx0	Port bit directions are determined by the bits of each port's DDR		
Strobed Input	xxxxxx01	00000000	xxx011	xxx1xx
Strobed Output (Active)	xxxxx011	11111111	xxx011	xxx1xx
Strobed Output (TRI-STATE)	xxxxx111	11111111	xxx011	xxx1xx

• Strobed Input (Mode 1)

During strobed input operations, an external device can load data into port A with the $\overline{STB}$ signal. Data is input to the PA0–7 input latches on the leading (negative) edge of $\overline{STB}$, causing BF to go high (true). On the trailing (positive) edge of $\overline{STB}$ the data is latched and the interrupt signal, $\overline{INTR}$, becomes valid indicating to the CPU that new data is available. $\overline{INTR}$ becomes valid only if the interrupt is enabled, that is the output data latch for PC2 is set to 1.

When the CPU reads port A, address x'00, the trailing edge of the $\overline{RD}$ strobe causes BF and $\overline{INTR}$ to become inactive, indicating that the strobed input cycle has been completed.

• Strobed Output—Active (Mode 2)

During strobed output operations, an external device can read data from port A using the $\overline{STB}$ signal. Data is initially loaded into port A by the CPU writing to I/O address x'00. On the trailing edge of $\overline{WR}$, $\overline{INTR}$ is set inactive and BF becomes valid indicating new data is available for the external device. When the external device is ready to accept the data in port A it pulses the $\overline{STB}$ signal. The rising edge of $\overline{STB}$ resets BF and activates the $\overline{INTR}$ signal. $\overline{INTR}$ becomes valid only if the interrupt is enabled, that is the output latch for PC2 is set to 1. $\overline{INTR}$ in this mode indicates a condition that requires CPU intervention (the output of the next byte of data).

• Strobed Output—TRI-STATE (Mode 3)

The Strobed Output TRI-STATE Mode and the Strobed Output active (peripheral) bus mode function in a similar manner with one exception. The exception is that the data signals on PA0–7 assume the high impedance state at all times except when accessed by the $\overline{STB}$ signal. Strobed Mode 3 is identical to Strobed Mode 2, except as indicated above.

Example Mode 1 (Strobed Input):

Action Taken	$\overline{INTR}$	BF	Results of Action
INITIALIZATION			
Reset NSC810A	H	L	Basic input mode all ports.
Load 01'H into MDR	H	L	Strobed input mode entered; no byte loads to port C after this step; bit-set and clear commands to $\overline{INTR}$ and BF no longer work.
Load 00'H into DDR A	H	L	Sets data direction register for port A to input; data from port A peripheral bus is available to the CPU if the $\overline{STB}$ signal is used, other handshake signals aren't initialized, yet.
Load 03'H into DDR C	H	L	Sets data direction register of port C; buffer full signal works after this step and it is unaffected by the bit-set and clear registers.
Load 04'H into Port C Bit-Set Register	H	L	Sets output latch (PC2) to enable $\overline{INTR}$; $\overline{INTR}$ will latch active whenever $\overline{STB}$ goes low; $\overline{INTR}$ can be disabled by a bit-clear to PC2.*
OPERATION			
$\overline{STB}$ pulses low	L	H	Data on peripheral bus is latched into port A; $\overline{INTR}$ is cleared by a CPU read of port A or a bit-clear of $\overline{STB}$.
CPU reads Port A	H	L	CPU gets data from port A; $\overline{INTR}$ is cleared; peripheral is signalled to send next byte via an inactive BF signal. Repeat last two steps until EOT at which time CPU sends bit-clear to the output latch (PC2).

* Port C can be read by the CPU at anytime, allowing polled operation instead of interrupt driven operation.

9.0 Functional Description (Continued)

Example Mode 2 (Strobed Output—active peripheral bus):

Action Taken	$\overline{INTR}$	BF	Results of Action
INITIALIZE			
Reset NSC810A	H	L	basic input mode all ports.
Load 03'H into MDR	H	L	strobed output mode entered; no byte loads to port C after this step; bit-set and clear commands to $\overline{INTR}$ and BF no longer work.
Load FF'H into DDR A	H	L	Sets data direction register for port A to output; data from port A is available to the peripheral if the $\overline{STB}$ signal is used other handshake signals aren't initialized, yet.
Load 03'H into DDR C	H	L	Sets data direction register of port C; buffer full signal works after this step and it is unaffected by the bit-set and clear registers
Load 04'H into Port C Bit-Set Register	L	L	Sets output latch (PC2) to enable $\overline{INTR}$; active $\overline{INTR}$ indicates that CPU should send data; $\overline{INTR}$ becomes inactive whenever the CPU loads port A; $\overline{INTR}$ can be disabled by a bit-clear to $\overline{STB}$.*
OPERATION			
CPU writes to Port A	H	H	Data on CPU bus is latched into port A; $\overline{INTR}$ is set by the CPU write to port A; active
$\overline{STB}$ pulses low	L	L	BF indicates to peripheral that data is valid; Peripheral gets data from port A; $\overline{INTR}$ is reset active; The active $\overline{INTR}$ signals the CPU to send the next byte. Repeat last two steps until EOT at which time CPU sends bit-clear to the output latch (PC2).

*Port C can be read by the CPU at any time, allowing polled operation instead of interrupt driven operation.

In addition to its timing function, $\overline{STB}$ enables port A outputs to active logic levels. This Mode 3 operation allows other data sources, in addition to the NSC810A, to access the peripheral bus.

• Handshaking Signals

In the Strobed mode of operation, the lower 3-bits of port C transmit/receive the handshake signals (PC0 = $\overline{INTR}$, PC1 = BF, PC2 = $\overline{STB}$).

$\overline{INTR}$ (Strobe Mode Interrupt) is an active-low interrupt from the NSC810A to the CPU. In strobed input mode, the CPU reads the valid data at port A to clear the interrupt. In strobed output mode, the CPU clears the interrupt by writing data to port A.

The $\overline{INTR}$ output can be enabled or disabled, thus giving it the ability to control strobed data transfer. It is enabled or disabled, respectively, by setting or clearing bit 2 of the port C output data latch ($\overline{STB}$).

PC2 is always an input during strobed mode of operation, its output data latch is not needed. Therefore, during strobed mode of operation it is internally gated with the interrupt signal to generate the $\overline{INTR}$ output. Reset clears this bit to zero, so it must be set to one to enable the $\overline{INTR}$ pin for strobed operation.

Once the strobed mode of operation is programmed, the only way to change the output data latch of PC2 is by using the Bit-Set and Clear registers. The port C byte write command will not alter the output data latch of PC2 during the strobed mode of operation.

$\overline{STB}$ (Strobe) is an active low input from the peripheral device, signalling a data transfer. The NSC810A latches data on the rising edge of $\overline{STB}$ if the port bit is an input and the peripheral should latch data on the rising edge of $\overline{STB}$ if the port bit is an output.

BF (Buffer Full) is a high active output from the NSC810A. For input port bits, it indicates that new data has been received from the peripheral. For output port bits, it indicates that new data is available for the peripheral.

Note: In either input or output mode the BF may be cleared by rewriting the MDR.

9.4 TIMERS

The NSC810A has two timers. These are independently programmable, 16-bit binary down-counters. Full count is reached at n + 1, where n is the count loaded into the modulus registers. Timer outputs provide six distinct modes of operation and allow the CPU to check the present count at anytime. Each timer has an independent clock input and output. Start and stop words from the CPU can individually start and stop the timers in any of the modes. A common gate signal can start and stop both timers in three of the six modes. Timer 0 has three possible input clock prescalers ÷1, ÷2 and ÷64. Timer 1 has two possible input clock prescalers ÷1 and ÷2.

Primary components of one timer are shown in *Figure 3.* The timer mode register is a read/write register providing

9.0 Functional Description (Continued)

the primary characterization of the timer output. The start/stop logic and prescaler block divides the clock input by the prescale factor, passing the output (INTCLK) to the binary down-counter. This block also gates the clock input signal (TIN) with the timer gate signal (TG). The timer block loads the modulus from the modulus register and uses (INTCLK) to count to zero. It loads the current count into the read buffer block where the CPU can access it at anytime. This timer block also indicates to the output control logic when the modulus is loaded (or reloaded) and when the count reaches 0. The output control logic block drives the output pins according to the timer mode register and the timer block. The output of the timer block (*Figure 3*) (terminal count) is related to the input TIN by:

$$\text{terminal count} = \frac{\text{TIN}}{\text{p}[2(\text{m} + 1)]}$$

where:

TIN = the input frequency

p = the programmed prescale

m = the modulus

This relationship can be seen directly (TOUT) in Mode 5 (square wave) as it is not masked by the subsequent output logic.

9.4.1 Registers

There are five control registers for each timer. These are shown in the second group of Table I. They determine all timer functions and outputs.

• Modulus Registers and Read Buffer

There are two modulus registers per timer (low byte, high byte). These are write only registers, and the two 8-bit values loaded by the CPU are combined into a 16-bit modulus for the timer's down counter.

When the CPU reads from the modulus register addresses, it actually accesses the read buffers. These contain the low and high byte of the decremented modulus. This count is constantly updated by the timer block on the falling edge of INTCLK and can be read without stopping the timers (see single/double precision).

• Timer Mode Register

The timer mode register determines the operating configuration and the active input and output signal levels. Each timer has its own timer mode register, allowing independent operation.

The timer mode register (TMR) may be written or read at any time; however, to assure accurate timing it is important to modify the mode only when the timer is stopped (see Timer Programming). The timer mode is selected from one of six modes by TMR bits 0, 1, and 2 (see Table V). Bits 3 and 4 select the prescale value if the prescaler is to be used. Bits 5, 6 and 7 select the modulus width (8- or 16-bits), gate input polarity, and timer output polarity (active-high or low), respectively. The bit functions of the TMR are illustrated in *Figure 4*.

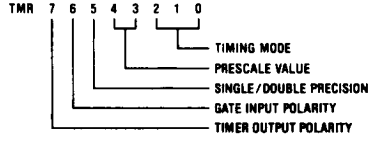

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FIGURE 4. Timer Mode Register

TABLE V. Mode Selection

Bit 2	1	0	–	Timer Function
0	0	0	–	Timer Stopped and Reset
0	0	1	–	Event Counter
0	1	0	–	Event Timer (Stopwatch)
0	1	1	–	Event Timer (Resetting)
1	0	0	–	One Shot
1	0	1	–	Square Wave
1	1	0	–	Pulse Generator
1	1	1	–	Timer Stopped and Reset

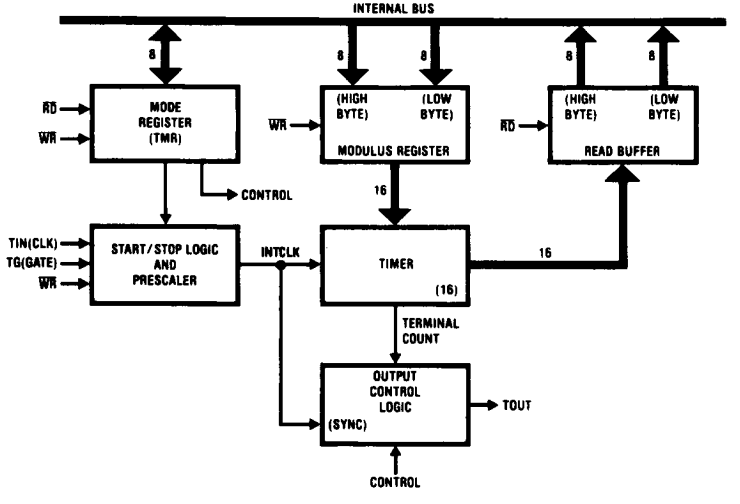

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FIGURE 3. Timer Internal Block Diagram (One of Two Timers)

9.0 Functional Description (Continued)

— Timer Prescaler

There is a prescale function associated with each timer. It serves as an additional divisor to lengthen the counts for each timer circuit. The value of the divisor is fixed and selectable in each TMR, as shown below.

	Bits		
TMR0	**4**	**3**	**Prescale**
	0	0	÷1
	0	1	÷2
	1	1	÷64

The ÷64 is not available on timer 1; TMR1 bit 4 is a "don't care."

	Bits		
TMR1	**4**	**3**	**Prescale**
	x	0	÷1
	x	1	÷2

The timer prescale divides the input clock (TIN) and provides the output (INTCLK) to the drive the timer block (*Figure 3*).

— Single/Double Precision

Bit 5 of the TMR determines whether a single or double byte can be accurately read from the read buffer. This option does not affect the use of the modulus registers by the timer block (i.e., the modulus used is always a double byte regardless of the precision mode selected).

The read buffer keeps track of the count and is constantly being updated by the timer block. In order to allow the CPU to read the read buffer, the NSC810A must discontinue updates to this buffer during the read. The precision bit determines whether one or two bytes in the read buffer will be frozen during the read process. In double precision mode, the NSC810A freezes high and low bytes in the read buffer for two consecutive read cycles. In the single precision mode, the NSC810A freezes the read buffer for only one read cycle. Read accesses should be done as follows.

When the TMR bit 5 is:

0— (double byte) read or write the low byte first, then the high byte to maintain proper read/write communications.

1— (single byte) In this mode either the high or low byte of the count can be read at any given instant but not both bytes consecutively. Always write the low byte first, then the high byte to load the modulus.

The following example illustrates this point. If the read buffer had a value of 0200 when the low byte was read and the down-counter decremented to 01FF before the high byte was read, then in the double precision mode the CPU would have read 00 and 02, respectively. In the single precision mode the CPU would have read 00 and 01.

NOTE: In the double precision mode, the high byte should be read immediately after the low byte. Do not access any other registers or unused address locations between the reads.

— Gate Input Polarity

In modes 2, 3 and 4, the TG input is the common hardware control for starting and stopping the timers.

The polarity of the gate input may be selected by the contents of bit 6 of the TMR. If bit 6 equals 0, the gate signal will be active-high or positive edge for mode 4; if bit 6 equals 1, the gate polarity will be active-low or negative edge for mode 4. Modes 2 and 3 are level sensitive. Mode 4 is edge sensitive.

— Timer Output Polarity

Like the gating function, the polarity of the output signal is programmable via bit 7 of the TMR. A zero will cause an active-low output; a one will generate an active-high output.

The output for T1 is multiplexed with port C, bit 5. (Similarly T1IN is multiplexed with port C, bit 4.) When any timer mode other than 0 or 7 is specified for T1, or when mode 2, mode 3, or mode 4 is specified for T0, the three port C pins, bit 3, bit 4, and bit 5, become TG, T1IN and T1OUT, respectively.

• Start and Stop Registers

This is the software start and stop for the timers. There is one start and one stop register for each timer. Writing any data to the start register of a timer starts that timer or transfers start and stop control to TG (in the gated modes 2, 3 and 4). Writing any data to the stop register stops the timer and removes start and stop control from TG (in the gated modes 2, 3 and 4). Restarting the timers causes the modulus to be reloaded for all gated timer modes (2, 3 and 4).

During software restarts of the timers (write to the STOP register and then to the START register) the modulus will be reloaded only if the internal clock signal (INTCLK) is in the high level or makes at least one transition to the high level between the time that the STOP and START registers are written. If INTCLK doesn't meet one of these criteria then the modulus will not be reloaded and the timer will continue to count down from where it was stopped.*

Since it is difficult, if not impossible, to know the level of INTCLK in non-gated modes the recommended practice for restart operation is to reload the modulus after stopping the timer using the 4 step programming procedure in the Timer Programming section of this datasheet. In gated modes INTCLK always stops high.

***NOTE:** INTCLK is coupled via the prescaler to TIN and reacts to the TIN clock input regardless of whether the timer is started or stopped.

— Start/Stop Timing

Figure 5 shows the relationships between the $\overline{WR}$ signal (start register), TIN and INTCLK for both the non-gated and gated modes. The TG signal is only sampled during the positive half of the TIN cycle. This means that when the gated modes are used the internal clock (INTCLK) is never stopped in the low state. Hence, when TG goes active high INTCLK is restarted on the next high-to-low transition of TIN. When TG goes inactive low INTCLK will stop as soon as TIN is high.

9.4.2 Timer Pins

TIN, TOUT, and TG

Timer 0 has dedicated pins for its clock, T0IN, and its output, T0OUT. Timer 1 must borrow its input and output pins from port C. This is accomplished by writing to the TMR for timer 1. If mode 1, 2, 3, 4, 5 or 6 is specified in TMR1, the pins from port C (PC3, PC4 and PC5) are automatically made available to the timer(s) for gating (TG), T1IN and T1OUT, respectively. These pins are also taken from port C any time timer 0 is in mode 2, 3, 4, so that it has a TG pin. In order to change pins PC3, PC4 and PC5 back to their original configuration as Basic I/O, the timer mode registers must be reset by selecting mode 0 or 7.

TG (PC3), the timer gate, is used for hardware control to start/stop (or trigger) the timers. The timer gate may be used individually by either timer or simultaneously by both timers.

For modes 2 and 3, the timer starts on the gate-active transition assuming the start address was previously written. If

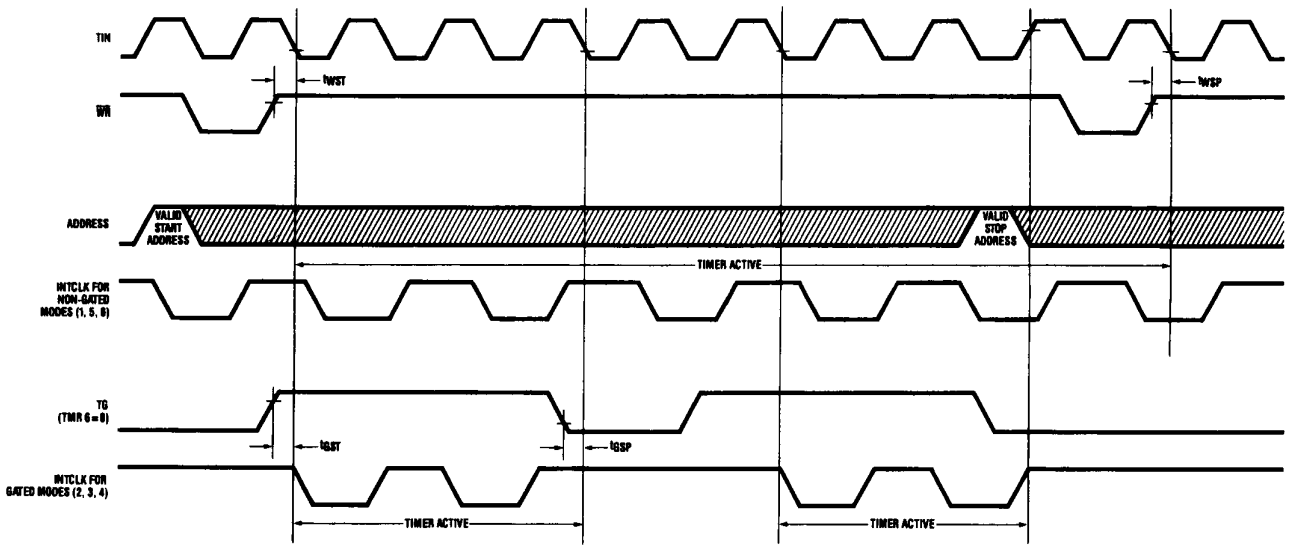

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FIGURE 5. Start/Stop Timing

Note: Diagonal lines indicate interval of invalid data.
For mode 4 (one shot), only start-timing applies.
t_{WST}—$\overline{WR}$ set-up for starting timer 150 ns.
t_{WSP}—$\overline{WR}$ set-up for stopping timer 150 ns.
t_{GST}—TG (gate) set-up for starting timer 100 ns.
t_{GSP}—TG (gate) set-up for stopping timer 100 ns.

9.0 Functional Description (Continued)

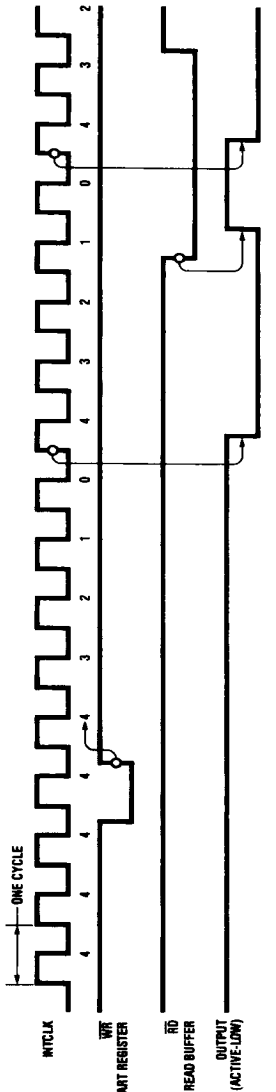


FIGURE 6a. Event Counter Mode (Mode 1)

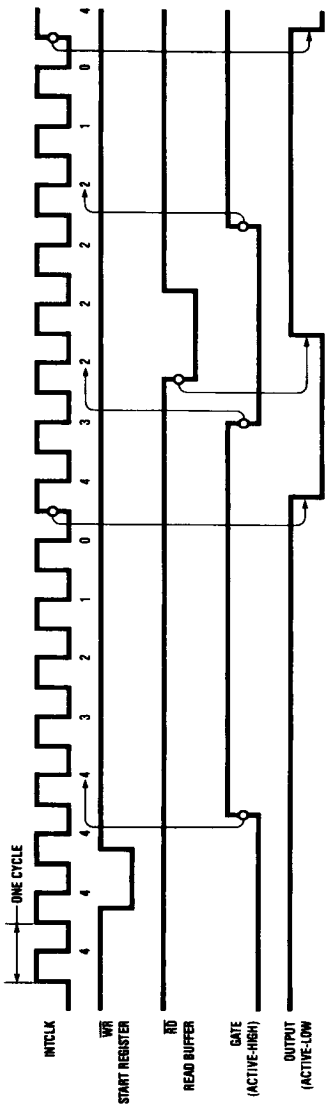


FIGURE 6b. Accumulative Timer (Mode 2)

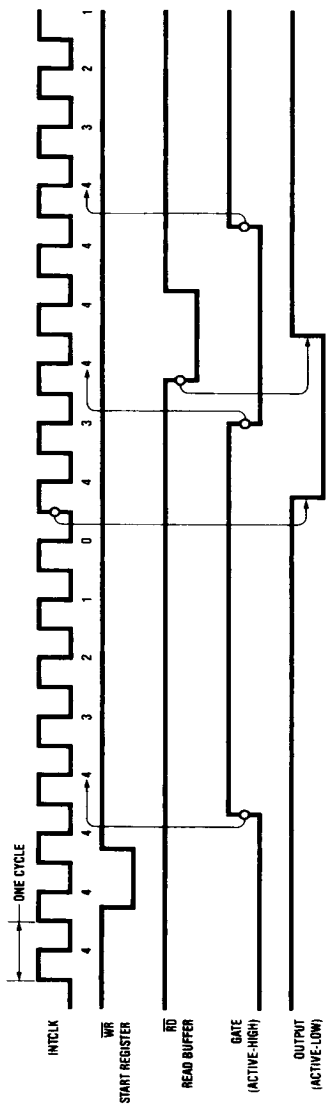


FIGURE 6c. Restartable Timing

9.0 Functional Description (Continued)

TABLE VI. Timer Programming Selection Example

Mode Register Bit (TMR) 7	6	5	4	3	2	1	0	Timer Output Polarity Active L/H	Timer Gate Polarity Active L/H	Mode Description Single/Double Precision S/D	Prescale Value	Timing Mode	Port C DDR 543210
TIMER 0													
x	x	x	x	x	0	0	0	x	x	x	x	0	x x x x x x
0	x	0	0	0	0	0	1	L	x	D	÷1	1	x x x x x x
1	x	0	1	1	1	1	0	H	x	D	÷64	6	x x x x x x
1	0	0	0	1	1	0	0	H	H	D	÷2	4	1 0 0 x x x
0	1	1	0	0	0	1	0	L	L	S	÷1	2	1 0 0 x x x
TIMER 1													
x	x	x	x	x	1	1	1	x	x	x	x	7	x x x x x x
0	x	0	x	0	0	0	1	L	x	D	÷1	1	1 0 0 x x x
1	0	1	x	1	1	0	1	H	H	S	÷2	5	1 0 0 x x x
0	1	0	x	0	0	1	1	L	L	D	÷1	3	1 0 0 x x x

the timer gate makes an active transition prior to a write to the start register's address, the trailing edge of the $\overline{WR}$ strobe starts the timer. However, for mode 4 the timer always waits for an active gate edge following a write to the start address before it begins counting.

The DDR for port C must be programmed with the correct I/O direction for TG, T1IN and T1OUT of timer 1. See Table VI for programming examples.

9.4.3 Timer Modes

The low-order three bits (bits 0, 1, 2) of the timer mode registers (TMR) define the mode of operation for the timers. Each TMR may be written to, or read from, at any time. However, to ensure accurate timing, it is important to modify the mode of the timer only when the timer is stopped. Inputs of 000 or 111 define a NOP (no operation) mode. In either of these modes (0 or 7) the timer is stopped, INTCLK is high, and the output is inactive. Inputs of 001 through 110 will select one of six distinct timer functions.

In the explanations that follow, assume that the modulus register for the timer was loaded with the appropriate value (0004) by writing to the low and high bytes of each timer modulus register. Assume also, that the prescale is ÷1.

- **Event Counter (mode 1 TMR bits = 001)**

In this non-gated mode the count is decremented for each clock period (INTCLK) input to the timer block (see *Figure 6a*). When the count reaches zero, the output goes valid and remains valid, until the read buffer is read by the CPU or the timer stop register is written.

At the terminal count (0) the modulus is reloaded into the timer block and the count continues even when the output is valid. This mode can be used to cause periodic interrupts to the CPU.

- **Accumulative Timer (mode 2, TMR bits = 010)**

In this gated mode, the counter will decrement only when the gate input is active (see *Figure 6b*). If the gate becomes inactive, the counter will hold at its present value and continue to decrement when the gate again becomes active. When the count decrements to zero, the output becomes valid and remains valid until the count is read by the CPU or the timer is stopped.

At the terminal count the timer is reloaded and the count continues as long as the gate is active.

This mode can be used to time processor independent events and to interrupt the CPU when they occur. The prescale and modulus need to be longer than the expected event duration and the gate should go inactive at the event, to preserve the read buffer count for the CPU.

- **Restartable Timer (mode 3, TMR bits = 011)**

In this gated mode, the counter will decrement only when the gate input is active. If the gate becomes inactive, the counter will reload the modulus and hold this value until the gate again becomes active (see *Figure 6c*). If the timer is read when the gate is inactive, you will always read the value the timer has counted down to, not the value the timer has been reloaded with.

At terminal count the output becomes valid and the timer is reloaded. The timer will continue to run as normal, the only difference is the output is valid. The output remains valid until the count is read by the CPU or the timer stop register is written.

NOTE: The gate inactive time must be longer than the high time of the internal clock (INTCLK) on the chip. Therefore, with ÷64 prescale selected the gate inactive time must be 33 input clocks or greater.

9.0 Functional Description (Continued)

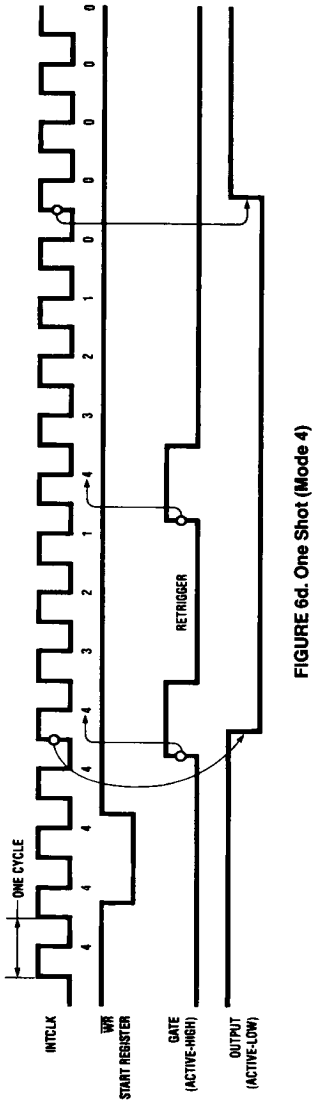


FIGURE 6d. One Shot (Mode 4)

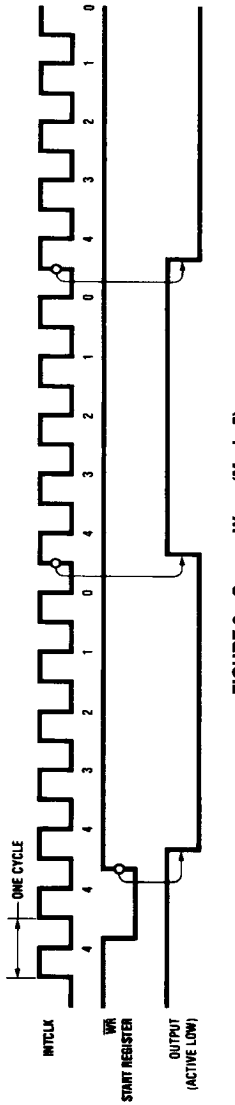


FIGURE 6e. Square Wave (Mode 5)

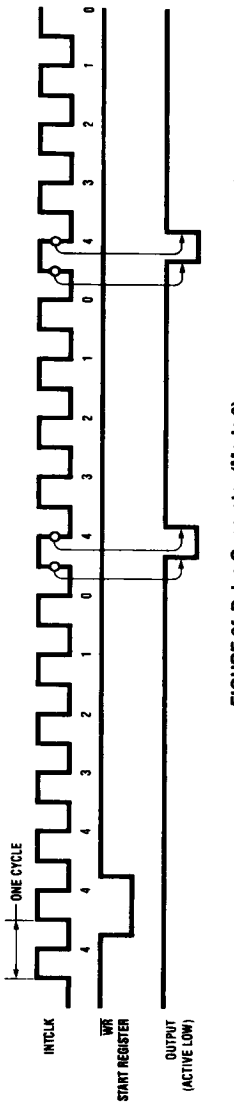


FIGURE 6f. Pulse Generator (Mode 6)

9.0 Functional Description (Continued)

• One Shot Mode (mode 4, TMR bits = 100)

In this gated mode, the timer holds the modulus count until the active gate edge (see *Figure 6d*). The output immediately becomes valid and remains valid as the counter decrements. The gating signal may go inactive without affecting the count. If TG (the gate) becomes inactive and returns active prior to the terminal count, the modulus will be reloaded, retriggering the one shot period. When the timer reaches the terminal count, the output becomes inactive (see NOTE). The gate, in this mode, is edge sensitive; the active edge is defined by the TMR.

NOTE: The one shot cannot be retriggered during its last internal count (INTCLK) regardless of prescaler selected. Therefore, using the divide by 1 prescaler, it cannot be retriggered during the last clock (TIN), using the divide by 2 prescaler during the last two clocks (TIN) and using the divide by 64 prescaler during the last 64 clocks (TIN).

• Square Wave Mode (mode 5, TMR bits = 101)

In this non-gated mode, the output will go active as soon as the timer is started. The counter decrements for each clock period (INTCLK) and complements its output when zero is reached (see *Figure 6e*). The modulus is then reloaded and counting continues. Assuming a regular clock input, the output will then be a square wave with a period equal to twice the prescale value times the value loaded into the modulus +1 (see equation Timer section intro.). Therefore, varying the modulus will vary the period of the square wave.

• Pulse Generator (mode 6, TMR bits = 110)

In this non-gated mode, the counter decrements for each period of INTCLK (see *Figure 6f*). When the terminal count is reached the output becomes valid for ½ of the TIN clock width for a prescale of ÷1, for one full TIN clock width for a prescale of ÷2 and for 32 TIN clock widths for a prescale of ÷64. The modulus is then reloaded and the sequence is repeated. Varying the prescale and modulus varies the frequency of the pulse.

9.4.4 Timer Programming

The following is the proper sequence to program the timer and should always be used:

1. Write timer mode register selecting mode 0 or 7. This stops the timer, resets the prescaler, and sets internal clock high.
2. Write timer mode register again, this time loading it for your requirements.
3. Write the modulus values, low byte first, high byte second.
4. Start the timers.

The timer read buffer is only updated when the internal timer clock (INTCLK) makes a negative-going transition. Therefore, enough input clock cycles (TIN) must occur to cause a transition of INTCLK given the programmed pre-scaler. After the first transition, the new modulus will be loaded into the read buffer and it can then be read by the CPU.

To guarantee the integrity of the data during a read operation, updates to the timer read buffer are blocked out. If an update is blocked out due to a read, the read buffer will not be updated until the next active transition of INTCLK. Thus, it would appear as if a count was skipped between reads. For example, if the output latches were FF when a block out (read) occurred, the next update could occur at FD, thereby giving an appearance that the count FE was skipped. In actuality the correct number of clocks has occurred for the read buffer to hold FD.

Writing the modulus value when the timer is running does not update the timer immediately. The new value written will get into the timer when the timer reaches its terminal count and reloads its value. If the timer is stopped and a modulus is written the new modulus value will get into the timer when the internal clock is high during the modulus write or on the next low to high internal clock transition. The next time the timer reaches its terminal count it will load the new modulus into the timer. One way to guarantee the new modulus will get into the timer is to follow steps 1 through 4. Although this procedure guarantees that the data will get into the timer you will not be able to read it back until you get a negative-going transition on the internal clock.

Rewriting modulus does not reset the prescaler. The only way to reset the prescaler is to write the mode register and have the internal clock signal be high for some period between the write of the mode register and the start of the timer. Once again, steps 1 through 4 will reset the prescaler.

10.0 NSC810A/883 MIL-STD-883 Class B Screening

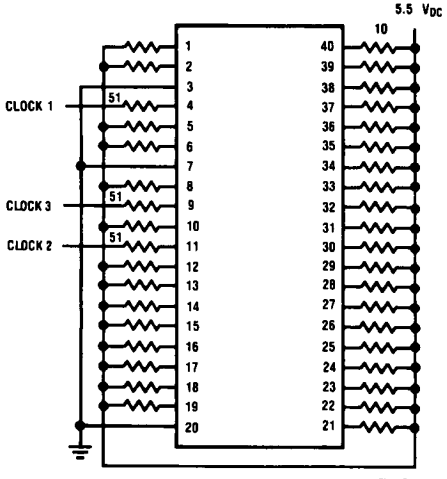
National Semiconductor offers the NSC810AD and NSC810AE with full class B screening per MIL-STD-883 for Military/Aerospace programs requiring high reliability. In addition, this screening is available for all of the key NSC800 peripheral devices.

Electrical testing is performed in accordance with RETS810AX, which tests or guarantees all of the electrical performance characteristics of the NSC810A data sheet. A copy of the current revision of RETS810AX is available upon request. The following table is the MIL-STD-883 flow as of the date of publication.

Test	MIL-STD-883 Method/Condition	Requirement
Internal Visual	2010 B	100%
Stabilization Bake	1008 C 24 Hrs. @ +150°C	100%
Temperature Cycling	1010 C 10 Cycles −65°C/ +150°C	100%
Constant Acceleration	2001 E 30,000 G's, Y1 Axis	100%
Fine Leak	1014 A or B	100%
Gross Leak	1014 C	100%
Burn-In	1015 160 Hrs. @ +125°C (using burn-in circuits shown below)	100%
Final Electrical	+25°C DC per RETS810AX	100%
PDA	5% Max	
	+125°C AC and DC per RETS810AX	100%
	−55°C AC and DC per RETS810AX	100%
	+25°C AC per RETS810AX	100%
QA Acceptance	5005	Sample per
Quality Conformance	5056	Method 5005
External Visual	2009	100%

11.0 Burn-In Circuit

5242HR
NSC810AD/883B (Dual-In-Line)



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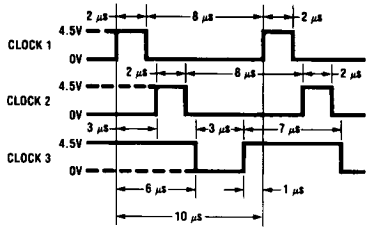
12.0 Timing Diagram

Input Clocks



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Note 1: All resistors ±5%, ¼ watt unless otherwise designated, 125°C operating life circuit.

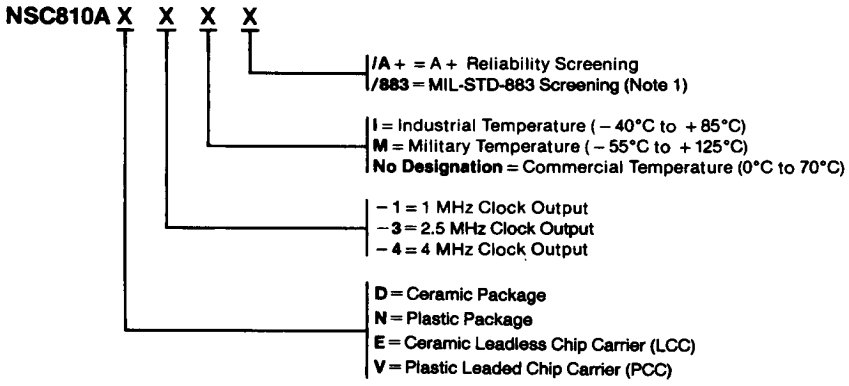
Note 2: E package burn-in circuit 5244HR is functionally identical to the D package.

Note 3: All resistors 2.7 kΩ unless marked otherwise.

Note 4: All clocks 0V to 4.5V.

Note 5: Device to be cooled down under power after burn-in.

13.0 Ordering Information



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Note 1: Do not specify a temperature option; all parts are screened to military temperature.

14.0 Reliability Information

Gate Count	4000
Transistor Count	14,000