ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089

NTE21256
262,144–Bit Dynamic Random Access Memory (DRAM)

Description:

The NTE21256 is a 262,144 word by 1–bit dynamic Random Access Memory. This 5V–only component is fabricated with N–channel silicon gate technology.

Nine multiplexed address inputs permit the NTE21256 to be packaged in an industry standard 16–Lead DIP package. Features of this device include single power supply with ±10% tolerance, on–chip address, date registers which eliminate the need for interface registers, and fully TTL compatible inputs and outputs, including clocks.

In addition to the usual read, write, and read–modify–write cycles, the NTE21256 is capable of early and late write cycles, $\overline{RAS}$–only refresh, and hidden refresh. Common I/O capability is given by using early write operation.

The NTE21256 also features page mode which allows high–speed random access of bits in the same row.

Features:

- 262,144 x 1–Bit Organization
- Single +5V Supply, ±10% Tolerance
- Low Power Dissipation:
  - –385mW active (Max)
  - –28mW standby (Max)
- Access Time: 150ns
- Cycle Time: 260ns
- All Inputs and Outputs TTL Compatible
- On–Chip Substrate Bias Generator
- Three–State Data Output
- Read, Write, Read–Modify–Write, $\overline{RAS}$–Only–Refresh, Hidden Refresh
- Common I/O Capability using “Early Write” Operation
- Page Mode Read and Write, Read–Write
- 256 Refresh Cycles with 4ms Refresh Period

Absolute Maximum Ratings: (Note 1)

Operating Temperature Range, T_{opr} . . . . . 0° to +70°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C
Voltage on any pin relative to V_{SS} . . . . . –1 to +7V
Power Dissipation, P_D 1W
Data Out Current (Short Circuit) 50mA

Note 1. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Functional Description:

Device Initialization

Since the NTE21256 is a dynamic RAM with a single +5V supply, no power sequencing is required. For power–up, an initial pause of 200µs is necessary for the internal bias generator to establish the proper substrate bias voltage. To initialize the nodes of the dynamic circuitry, a minimum of 8 active cycles of the Row Address Strobe ($\overline{RAS}$) has to be performed. This is also necessary after an extended inactive state of greater than 4ms.

Addressing (A0–A8)

For selecting one of the 262,144 memory cells, a total of 18 address bits are required. First 8 Row Address bits are set up on pins A0 through A8 and latched into the row address latches by the Row Address Strobe ($\overline{RAS}$). Then the 9 column address bits are set up on pins A0 through A8 and latched into the column address latches by the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on the falling edges of $\overline{RAS}$ and $\overline{CAS}$. It should be noted that $\overline{RAS}$ is similar to a Chip Enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

Write Enable ($\overline{WE}$)

The read or write mode is selected with the $\overline{WE}$ input. A logic high (V_{IH}) on $\overline{WE}$ dictates read mode; logic low (V_{IL}) dictates write mode. The data input is disabled when read mode is selected. When $\overline{WE}$ goes low prior to $\overline{CAS}$, data output (DO) will remain in the high–impedance state for the entire cycle permitting common I/O operation.

Data Input (DI)

Data is written during a write or read–modify–write cycle. The falling edge of $\overline{CAS}$ or $\overline{WE}$ strobes data into the on–chip data latch. In an early write cycle, $\overline{WE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal.

Data Output (DO)

The output is three–state TTL compatible with a fan–out of two standard TTL loads. Data Out has the same polarity as Data In. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle or read–write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (Min) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (Max). In an early write cycle, the output is always in the high impedance state. In a delayed write or read–modify–write cycle, the output will follow the sequence for the read cycle. With $\overline{CAS}$ going high the output returns to the high impedance state within t_{OFF}.

Hidden Refresh

$\overline{RAS}$–only refresh cycle may take place while maintaining valid output data. This feature is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} of a previous memory read cycle.

Refresh Cycle

A refresh operation must be performed at least every 4ms to retain data. Since the output buffer is in the high impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$–only refresh sequence avoids any signal during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$, causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

Page Mode

Page–mode operation allows effectively faster memory access by maintaining the row address and strobing random column addresses onto the chip. Thus, the time necessary to setup and strobe sequential row addresses for the same page is no longer required. The maximum number of columns that can be addressed in sequence is determined by t_{RAS}, the maximum $\overline{RAS}$ low pulse width.

DC Characteristics: (T_A = 0° to +70°C, V_{SS} = 0V, V_{CC} = +5V ±10% unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input High Voltage (All Inputs)	V_{IH}	Notes 2, Note3	2.4	–	V_{CC} +1	V
Input Low Voltage (All Inputs)	V_{IL}	Notes 2, Note3	–1.0	–	0.8	V
Output High Voltage	V_{OH}	Note 4	2.4	–	–	V
Output Low Voltage	V_{OL}	Note 5	–	–	0.4	V
Average V_{CC} Supply Current	I_{CC1}	t_{RC} = 260ns, Note 6	–	–	70	mA
Standby V_{CC} Supply Current	I_{CC2}	Note 7	–	–	5	mA
Average V_{CC} Supply Current during $\overline{RAS}$–only refresh cycles	I_{CC3}	Note 6	–	–	65	mA
Average V_{CC} supply Current during Page Mode	I_{CC4}	Note 6	–	–	55	mA
Input Leakage Current (Any Input)	$I_{I\ (L)}$		–	–	10	µA
Output Leakage Current	$I_{O\ (L)}$	$\overline{CAS}$ at Logic 1, 0 ≤ V out ≤ 5.5	–	–	10	µA
Supply Voltage	V_{CC}	Note 2	4.5	–	5.5	V
	V_{SS}		0	–	0	V

Note 2. All voltages referenced to V_{SS}.

Note 3. Overshooting and undershooting on input levels of +6.5V or –2V for a period 0f 30ns Max. will influence function and reliability of the device.

Note 4. I_{OH} = 4mA and 100pf load.

Note 5. I_{OL} = 4mA and 100pf load.

Note 6. I_{CC} depends on frequency of operation. Maximum current is measured at the fastest cycle rate.

Note 7. $\overline{RAS}$ and $\overline{CAS}$ are both at V_{IH}.

Capacitance: (Note 6)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Capacitance (A0–A8, DI)	C_{I1}		–	–	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{I2}		–	–	7	pF
Output Capacitance (DO, $\overline{CAS}$ = V_{IH} to disable output)	C_O		–	–	7	pF

Note 6. Effective capacitance calculated from the equation:

$$C = \frac{I \bullet \Delta t}{\Delta V}$$ with ΔV = 3V or measured with Boonton meter.

AC Test Conditions:

Input Pulse Levels . . . . . 0 to 3.0V
Input Rise and Fall Times . . . . . 5ns between 0.8 and 2.4V
Input Timing Reference Levels . . . . . 0.8 to 2.4V
Output Timing Reference Levels . . . . . 0.4 to 2.4V
Output Load . . . . . equivelent to 2 standard TTL loads and 100pf

AC Characteristics: (T_A = 0° to +70°C, V_{CC} = 5V ±10%, Note 9, Note 10, Note 11 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Random Read or Write Cycle Time	t_{RC}	Note 12	260	–	–	ns
Read–Modify–Write Cycle Time	t_{RWC}	Note 12	310	–	–	ns
Access Time from $\overline{RAS}$	t_{RAC}	Notes 13, Note 14	–	–	150	ns
Access Time from $\overline{CAS}$	t_{CAC}	Notes 13, Note 15	–	–	75	ns
$\overline{RAS}$ Pulse Width	t_{RAS}		150	–	10^4	ns
$\overline{CAS}$ Pulse Width	t_{CAS}		75	–	–	ns
Refresh Period	t_{REF}		–	–	4	ms
$\overline{RAS}$ Precharge Time	t_{RP}		100	–	–	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}		0	–	–	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	Note 16	30	–	75	ns
$\overline{RAS}$ Hold Time	t_{RSH}		75	–	–	ns
$\overline{CAS}$ Hold Time	t_{CSH}		150	–	–	ns
Row Address Setup Time	t_{ASR}		0	–	–	ns
Row Address Hold Time	t_{RAH}		20	–	–	ns
Column Address Setup Time	t_{ASC}		0	–	–	ns
Column Address Hold Time	t_{CAH}		30	–	–	ns
Column Address Hold Time referenced to $\overline{RAS}$	t_{AR}	Note 17	105	–	–	ns
Transition Time (Rise and Fall)	t_T	Note 9	3	–	50	ns
Read Command Setup Time	t_{RCS}		0	–	–	ns
Read Command Hold Time referenced to $\overline{CAS}$	t_{RCH}	Note 18	0	–	–	ns
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	Note 18	10	–	–	ns
Output Buffer Turn–Off Delay	t_{OFF}	Note 19	0	–	40	ns

Note 9. V_{IH} and V_{IL} are reference levels to measure timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

Note 10. An initial pause of 200µs is required after power–up followed by a minimum of eight initialization cycles prior to normal operation.

Note 11. The time parameters specified here are valid for a transition time of t_T = 5ns for the input signals

Note 12. The specification for t_{RC} (Min), t_{RWC} (Min), and page–mode cycle time (t_{PC}) are only used to indicate cycle time at which proper operation over full temperature range (0°C ≤ T_A ≤ +70°C) is assured.

Note 13. Measured with a load equivalent to two TTL loads and 100pf.

Note 14. Assumes that $t_{RCD} \le t_{RCD}$ (Max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

Note 15. Assumes that $t_{RCD} \le t_{RCD}$ (Max).

Note 16. Operation within the t_{RCD} (Max) limit ensures that t_{RAC} (Max) can be met. t_{RCD} (Max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max) limit, then access time is controlled exclusively by t_{CAC}.

Note 17. $t_{RCD} + t_{CAH} \ge t_{AR}$ Min, $t_{RCD} + t_{DH} \ge t_{DHR}$ Min, $t_{RCD} + t_{WCH} \ge t_{WCR}$ Min.

Note 18. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

Note 19. t_{OFF} (Max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

AC Characteristics (Cont'd): (T_A = 0° to +70°C, V_{CC} = 5V ±10%, Note 9, Note 10, Note 11 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Write Command Setup Time	t_{WCS}	Note 20	0	–	–	ns
Write Command Hold Time	t_{WCH}		45	–	–	ns
Write Command Hold Time referenced to $\overline{RAS}$	t_{WCR}	Note 17	120	–	–	ns
Write Command Pulse Width	t_{WP}		45	–	–	ns
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}		45	–	–	ns
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}		45	–	–	ns
Data in Setup Time	t_{DS}	Note 21	0	–	–	ns
Data in Hold Time	t_{DH}	Note 21	45	–	–	ns
Data in Hold Time referenced to $\overline{RAS}$	t_{DHR}	Note 17	120	–	–	ns
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	Note 20	75	–	–	ns
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	Note 20	150	–	–	ns
RMW Cycle $\overline{RAS}$ Pulse Width	t_{RRW}		200	–	–	ns
RMW Cycle $\overline{CAS}$ Pulse Width	t_{CRW}		125	–	–	ns
Page Mode Cycle Time	t_{PC}	Note 12	145	–	–	ns
Page Mode Read–Write Cycle Time	t_{PRWC}		190	–	–	ns
Page Mode $\overline{CAS}$ Precharge Time	t_{CP}		60	–	–	ns

Note 9. V_{IH} and V_{IL} are reference levels to measure timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

Note 10. An initial pause of 200µs is required after power–up followed by a minimum of eight initialization cycles prior to normal operation.

Note 11. The time parameters specified here are valid for a transition time of t_T = 5ns for the input signals

Note 12. The specification for t_{RC} (Min), t_{RWC} (Min), and page–mode cycle time (t_{PC}) are only used to indicate cycle time at which proper operation over full temperature range ($0°C \le T_A \le +70°C$) is assured.

Note 17. $t_{RCD} + t_{CAH} \ge t_{AR}$ Min, $t_{RCD} + t_{DH} \ge t_{DHR}$ Min, $t_{RCD} + t_{WCH} \ge t_{WCR}$ Min.

Note 20. t_{WCS}, t_{CWD}, and t_{RWC} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \ge t_{WCS}$ (Min), the cycle is an early write cycle and the Data Out will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \ge t_{CWD}$ (Min) and $t_{RWD} \ge t_{RWD}$ (Min) the cycle is a read–write cycle and the Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the Data Out (at access time) is indeterminate.

Note 21. t_{DS} and t_{DH} are referenced to the leading edge of $\overline{CAS}$ in early write cycles, and to the leading edge of $\overline{WE}$ in delayed write of read–modify–write cycles.

Pin Connection Diagram