



ELECTRONICS, INC.
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NTE56042 thru NTE56044 TRIAC, 16A, Sensitive Gate

Description:

The NTE56042 through NTE56044 are glass passivated, sensitive gate TRIACs in an isolated full-pack type package designed for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

Absolute Maximum Ratings:

Repetitive Peak Off-State Voltage, V_{DRM}	
NTE56042 (Note 1)	500V
NTE56043 (Note 1)	600V
NTE56044	800V
RMS On-State Current (Full Sine Wave, $T_{HS} \leq 38^{\circ}C$), $I_T(RMS)$	16A
Non-Repetitive Peak On-State Current, I_{TSM}	
(Full Sine Wave, $T_J = +125^{\circ}C$ prior to Surge, with Reapplied V_{DRMmax})	
$t = 20ms$	140A
$t = 16.7ms$	150A
I^2t for Fusing ($t = 10ms$), I^2t	98A ² sec
Repetitive Rate-of-Rise of On-State Current after Triggering, dl_T/dt	
($I_{TM} = 20A$, $I_G = 0.2A$, $dl_G/dt = 0.2A/\mu s$)	
$MT_2 (+)$, $G (+)$	50A/ μs
$MT_2 (+)$, $G (-)$	50A/ μs
$MT_2 (-)$, $G (-)$	50A/ μs
$MT_2 (-)$, $G (+)$	10A/ μs
Peak Gate Current, I_{GM}	2A
Peak Gate Voltage, V_{GM}	5V
Peak Gate Power, P_{GM}	5W
Average Gate Power (Over Any 20ms Period), $P_{G(AV)}$	500mW
Operating Junction Temperature, T_J	+125°C
Storage Temperature Range, T_{stg}	-40° to +150°C
Thermal Resistance, Junction-to-Heatsink (Full or Half Cycle), R_{thJHS}	
With Heatsink Compound	4.0K/W
Without Heatsink Compound	5.5K/W
Typical Thermal Resistance, Junction-to-Ambient, R_{thJA}	55K/W

Note 1. Although not recommended, off-state voltages up to 800V may be applied without damage, but the TRIAC may switch to the on-state. The rate-of-rise of current should not exceed 15A/ μs .

Electrical Characteristics: ($T_J = +25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static Characteristics						
Gate Trigger Current MT ₂ (+), G (+)	I _{GT}	V _D = 12V, I _T = 0.1A	–	2.5	10	mA
MT ₂ (+), G (–)			–	4.0	10	mA
MT ₂ (–), G (–)			–	5.0	10	mA
MT ₂ (–), G (+)			–	11	25	mA
Latching Current MT ₂ (+), G (+)	I _L	V _D = 12V, I _T = 0.1A	–	3.2	30	mA
MT ₂ (+), G (–)			–	16	40	mA
MT ₂ (–), G (–)			–	4.0	30	mA
MT ₂ (–), G (+)			–	5.5	40	mA
Holding Current	I _H	V _D = 12V, I _T = 0.1A	–	4.0	30	mA
On–State Voltage	V _T	I _T = 20A	–	1.2	1.6	V
Gate Trigger Voltage	V _{GT}	V _D = 12V, I _T = 0.1A	–	0.7	1.5	V
		V _D = 400V, I _T = 0.1A, T _J = +125°C	0.25	0.4	–	V
Off–State Leakage Current	I _D	V _D = V _{DRMmax} , T _J = +125°C	–	0.1	0.5	mA
Dynamic Characteristics						
Critical Rate–of–Rise of Off–State Voltage	dV _D /dt	V _{DM} = 67% V _{DRMmax} , T _J = +125°C, Exponential Waveform, Gate Open	–	50	–	V/μs
Gate Controlled Turn–On Time	t _{gt}	I _{TM} = 20A, V _D = V _{DRMmax} , I _G = 0.1A, dI _G /dt = 5A/μs	–	2	–	μs
Isolation Characteristics (T _{HS} = +25°C unless otherwise specified)						
RMS Isolation Voltage from All 3 Pins to External Heatsink	V _{ISOL}	R.H. ≤ 65%, Clean and Dustfree	–	–	1500	V
Capacitance from T2 to External Heatsink	C _{ISOL}	f = 1MHz	–	12	–	pF

