

# NTHD2102P

## Power MOSFET

-8.0 V, -4.6 A Dual P-Channel ChipFET™

### Features

- Offers an Ultra Low  $R_{DS(on)}$  Solution in the ChipFET Package
- Miniature ChipFET Package 40% Smaller Footprint than TSOP-6 making it an Ideal Device for Applications where Board Space is at a Premium
- Low Profile (<1.1 mm) Allows it to Fit Easily into Extremely Thin Environments such as Portable Electronics
- Designed to Provide Low  $R_{DS(on)}$  at Gate Voltage as Low as 1.8 V, the Operating Voltage used in many Logic ICs in Portable Electronics
- Simplifies Circuit Design since Additional Boost Circuits for Gate Voltages are not Required
- Operated at Standard Logic Level Gate Drive, Facilitating Future Migration to Lower Levels using the same Basic Topology
- Pb-Free Package is Available

### Applications

- Optimized for Battery and Load Management Applications in Portable Equipment such as MP3 Players, Cell Phones, Digital Cameras, Personal Digital Assistant and other Portable Applications
- Charge Control in Battery Chargers
- Buck and Boost Converters

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	-8.0	V
Gate-to-Source Voltage – Continuous	$V_{GS}$	$\pm 8.0$	V
Drain Current – Continuous – 5 seconds	$I_D$	-3.4	A
	$I_D$	-4.6	A
Total Power Dissipation Continuous @ $T_A = 25^\circ\text{C}$ (5 sec) @ $T_A = 25^\circ\text{C}$ Continuous @ $85^\circ\text{C}$ (5 sec) @ $85^\circ\text{C}$	$P_D$	1.1	W
		2.1	
		0.6	
		1.1	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
Continuous Source Current (Diode Conduction)	$I_S$	-1.1	A
Thermal Resistance (Note 1) Junction-to-Ambient, 5 sec Junction-to-Ambient, Continuous	$R_{\theta JA}$ $R_{\theta JA}$	60	$^\circ\text{C}/\text{W}$
		113	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	$T_L$	260	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

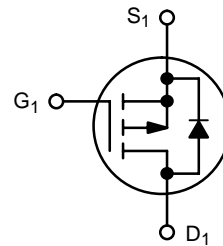
1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.27 in sq [1 oz] including traces).



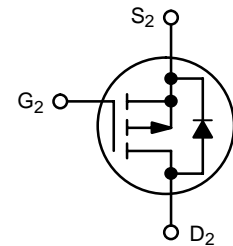
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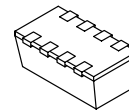
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
-8.0 V	50 m $\Omega$ @ -4.5 V	-4.6 A
	68 m $\Omega$ @ -2.5 V	
	100 m $\Omega$ @ -1.8 V	



P-Channel MOSFET

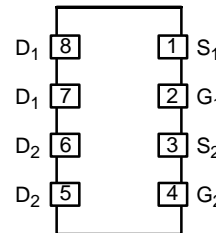


P-Channel MOSFET

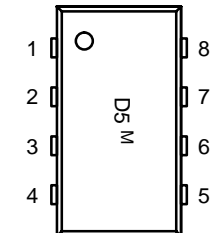


ChipFET  
CASE 1206A  
STYLE 2

### PIN CONNECTIONS



### MARKING DIAGRAM



D5 = Specific Device Code  
M = Month Code

### ORDERING INFORMATION

Device	Package	Shipping†
NTHD2102PT1	ChipFET	3000/Tape & Reel
NTHD2102PT1G	ChipFET (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTHD2102P

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 2) Temperature Coefficient (Positive)	$V_{(Br)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-8.0	-	-	V
Gate-Body Leakage Current Zero	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8.0\text{ V}$		-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -6.4\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = -6.4\text{ V}, V_{GS} = 0\text{ V},$ $T_J = 85^\circ\text{C}$		-	-1.0 -5.0	$\mu\text{A}$

### ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-0.45	-	-1.5	V
Static Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -3.4\text{ A}$ $V_{GS} = -2.5\text{ V}, I_D = -2.7\text{ A}$ $V_{GS} = -1.8\text{ V}, I_D = -1.0\text{ A}$	-	50 68 100	58 85 160	$\text{m}\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS} = -5.0\text{ V}, I_D = -3.4\text{ A}$	-	8.0	-	S
Diode Forward Voltage	$V_{SD}$	$I_S = -1.1\text{ A}, V_{GS} = 0\text{ V}$	-	-0.8	-1.2	V

### DYNAMIC CHARACTERISTICS

Input Capacitance	$C_{iss}$	$V_{DS} = -6.4\text{ V}$ $V_{GS} = 0\text{ V}$ $f = 1.0\text{ MHz}$	-	715	-	$\text{pF}$
Output Capacitance	$C_{oss}$		-	160	-	
Transfer Capacitance	$C_{rss}$		-	120	-	

### SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -6.4\text{ V}$ $V_{GS} = -4.5\text{ V}$ $I_D = -3.2\text{ A}$ $R_G = 2.0\ \Omega$		8.0	-	ns
Rise Time	$t_r$			20	-	
Turn-Off Delay Time	$t_{d(off)}$			20	-	
Fall Time	$t_f$			15	-	
Gate Charge	$Q_g$	$V_{GS} = -2.5\text{ V}$		8.0	16	nC
	$Q_{gs}$	$I_D = -3.2\text{ A}$		2.2	-	
	$Q_{gd}$	$V_{DS} = -6.4\text{ V}$		4.0	-	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = -0.9\text{ A}, di/dt = 100$		15	30	nA

2. Pulse Test: Pulse Width = 250  $\mu\text{s}$ , Duty Cycle = 2%.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL ELECTRICAL CHARACTERISTICS

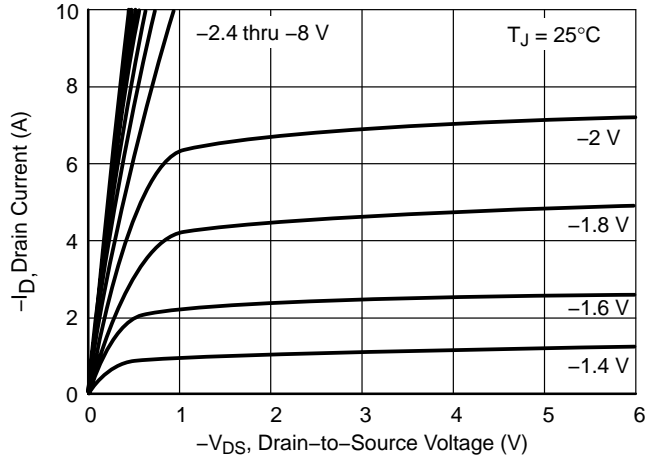


Figure 1. On-Region Characteristics

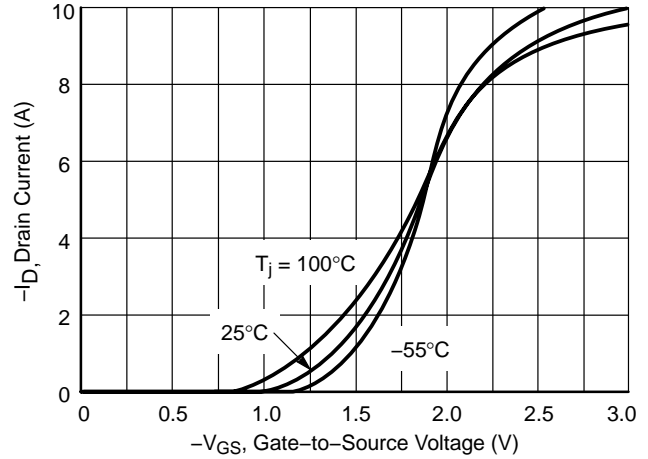


Figure 2. Transfer Characteristics

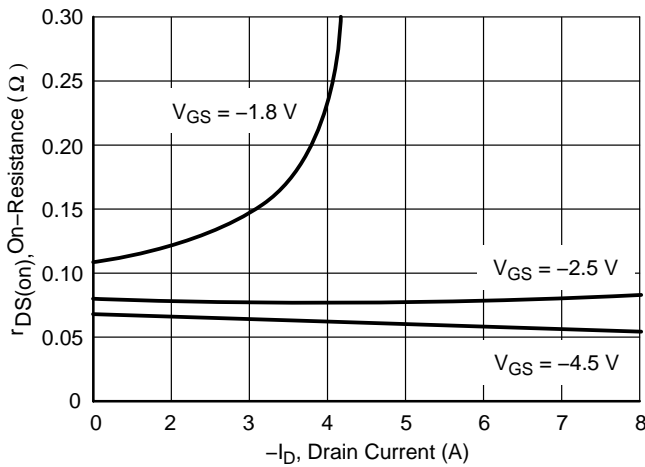


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

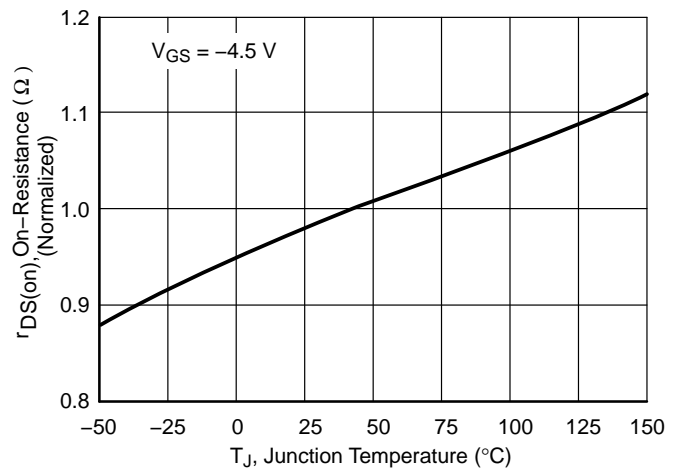


Figure 4. On-Resistance Variation vs. Temperature

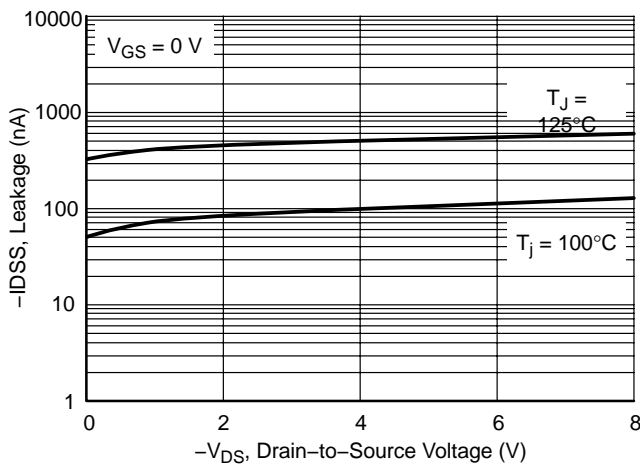


Figure 5. Drain-to-Source Leakage Current vs. Voltage

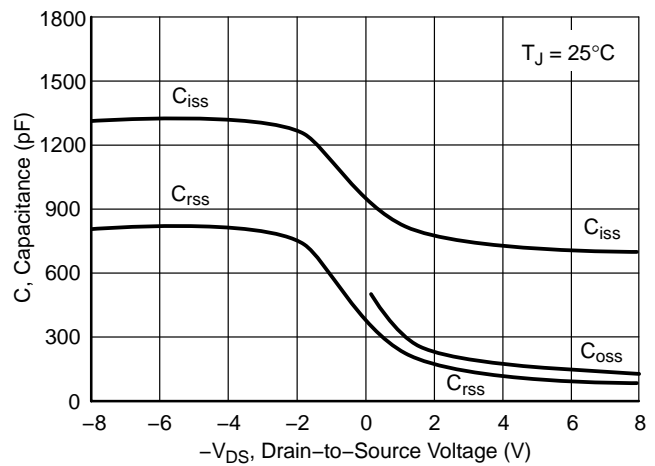


Figure 6. Capacitance Variation

TYPICAL ELECTRICAL CHARACTERISTICS

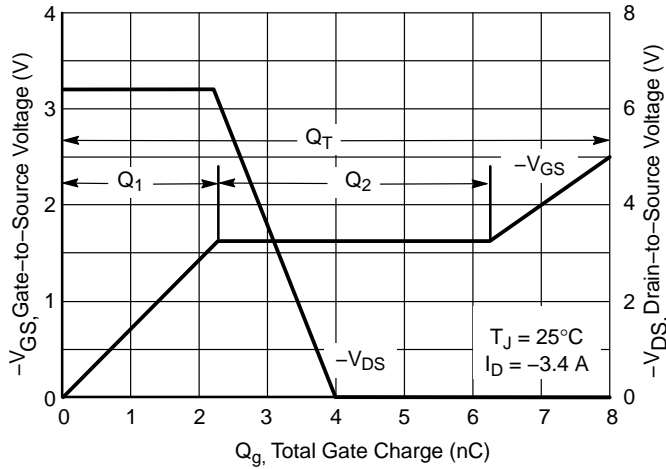


Figure 7. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

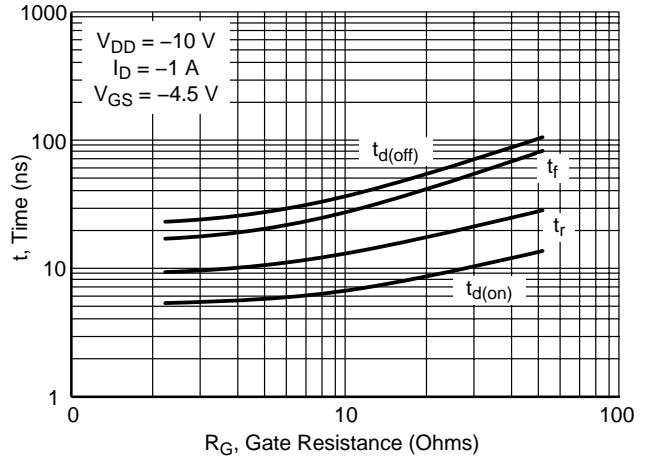


Figure 8. Resistive Switching Time Variation vs. Gate Resistance

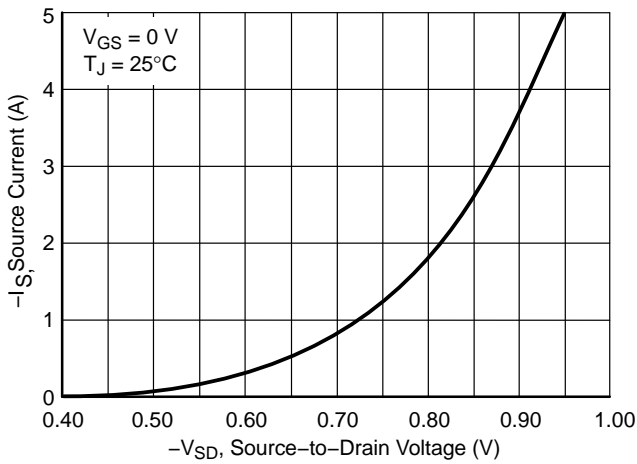


Figure 9. Diode Forward Voltage vs. Current

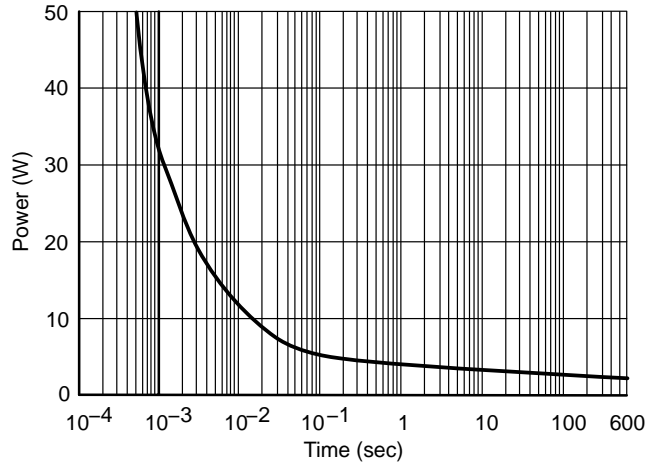


Figure 10. Single Pulse Power

TYPICAL ELECTRICAL CHARACTERISTICS

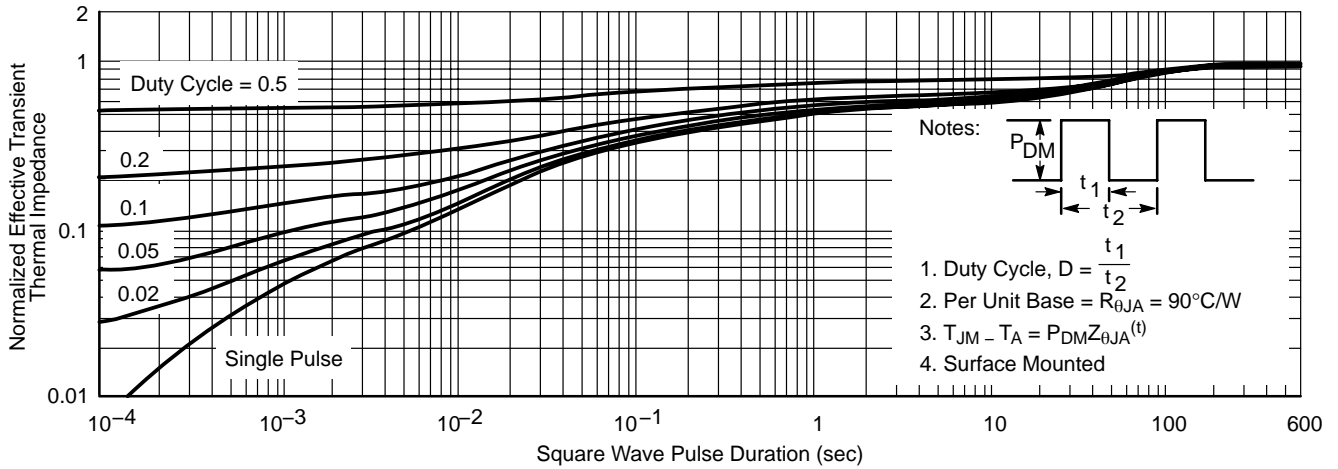


Figure 11. Normalized Thermal Transient Impedance, Junction-to-Ambient

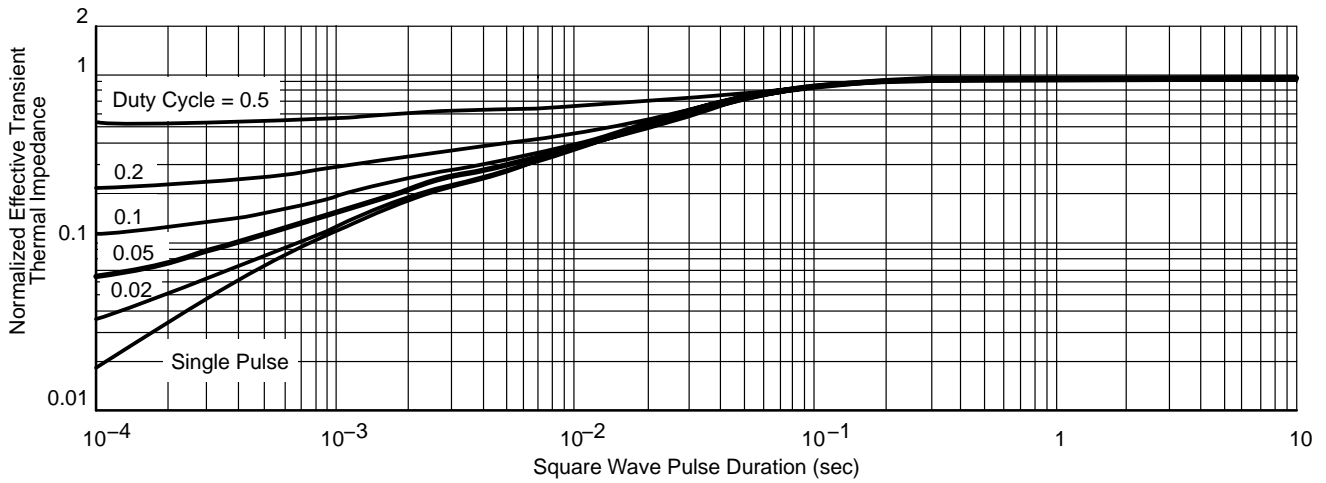
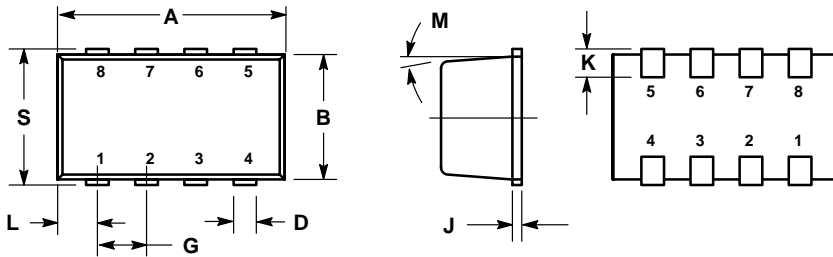


Figure 12. Normalized Thermal Transient Impedance, Junction-to-Foot

# NTHD2102P

## PACKAGE DIMENSIONS

### ChipFET CASE 1206A-03 ISSUE E

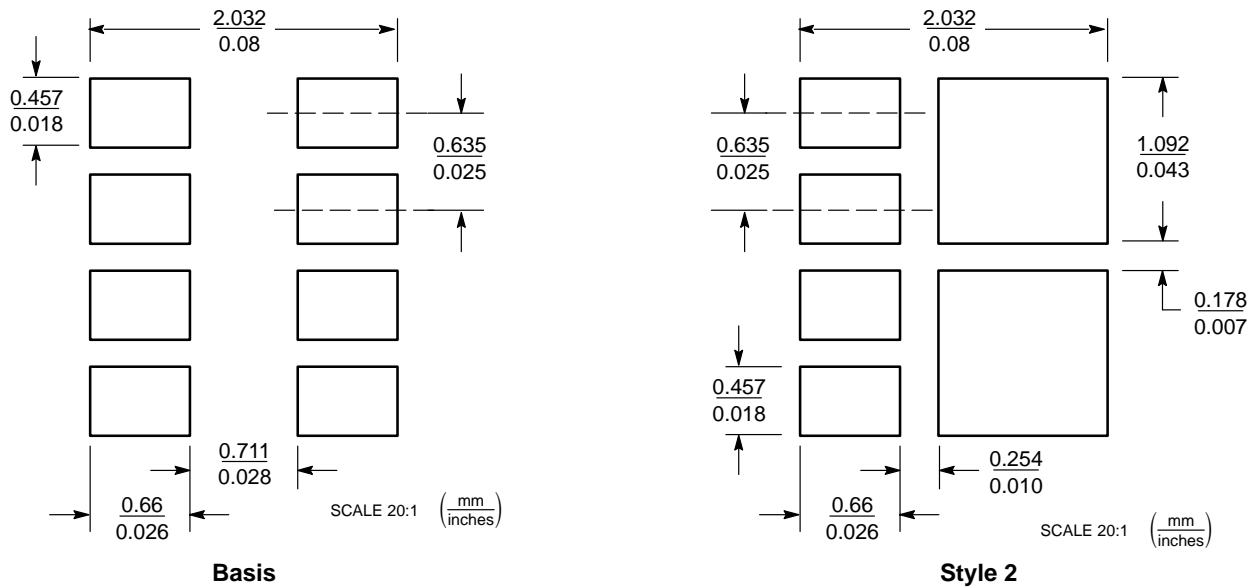


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
  4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
  5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
  6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.
  7. 1206A-01 AND 1206A-02 OBSOLETE. NEW STANDARD IS 1206A-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.95	3.10	0.116	0.122
B	1.55	1.70	0.061	0.067
C	1.00	1.10	0.039	0.043
D	0.25	0.35	0.010	0.014
G	0.65 BSC		0.025 BSC	
J	0.10	0.20	0.004	0.008
K	0.28	0.42	0.011	0.017
L	0.55 BSC		0.022 BSC	
M	5° NOM		5° NOM	
S	1.80	2.00	0.072	0.080

- STYLE 2:  
PIN 1. SOURCE 1  
2. GATE 1  
3. SOURCE 2  
4. GATE 2  
5. DRAIN 2  
6. DRAIN 2  
7. DRAIN 1  
8. DRAIN 1

## SOLDERING FOOTPRINTS\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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