

# NTP30N06L, NTB30N06L

## Power MOSFET 30 Amps, 60 Volts, Logic Level N-Channel TO-220 and D<sup>2</sup>PAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

### Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

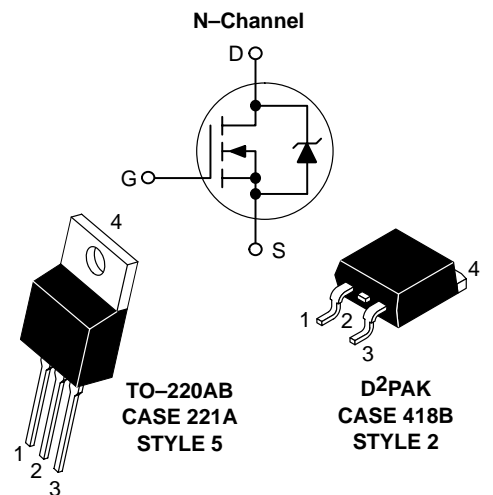
Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V <sub>DSS</sub>	60	Vdc
Drain-to-Gate Voltage (R <sub>GS</sub> = 10 MΩ)	V <sub>DGR</sub>	60	Vdc
Gate-to-Source Voltage	V <sub>GS</sub>		Vdc
– Continuous	V <sub>GS</sub>	±15	
– Non-Repetitive (t <sub>p</sub> ≤ 10 ms)	V <sub>GS</sub>	±20	
Drain Current	I <sub>D</sub>		Adc
– Continuous @ T <sub>A</sub> = 25°C	I <sub>D</sub>	30	
– Continuous @ T <sub>A</sub> = 100°C	I <sub>D</sub>	15	
– Single Pulse (t <sub>p</sub> ≤ 10 μs)	I <sub>DM</sub>	90	Apk
Total Power Dissipation @ T <sub>A</sub> = 25°C	P <sub>D</sub>	88.2	W
Derate above 25°C		0.59	W/°C
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	–55 to +175	°C
Single Pulse Drain-to-Source Avalanche Energy – Starting T <sub>J</sub> = 25°C (V <sub>DD</sub> = 50 Vdc, V <sub>GS</sub> = 5.0 Vdc, L = 0.3 mH I <sub>L(pk)</sub> = 26 A, V <sub>DS</sub> = 60 Vdc)	E <sub>AS</sub>	101	mJ
Thermal Resistance – Junction-to-Case	R <sub>θJC</sub>	1.7	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T <sub>L</sub>	260	°C



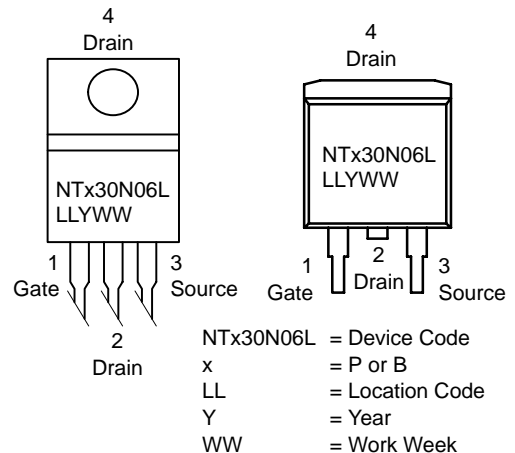
ON Semiconductor™

<http://onsemi.com>

**30 AMPERES**  
**60 VOLTS**  
**RDS(on) = 46 mΩ**



### MARKING DIAGRAMS & PIN ASSIGNMENTS



### ORDERING INFORMATION

Device	Package	Shipping
NTP30N06L	TO-220AB	50 Units/Rail
NTB30N06L	D <sup>2</sup> PAK	50 Units/Rail
NTB30N06LT4	D <sup>2</sup> PAK	800/Tape & Reel

# NTP30N06L, NTB30N06L

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Drain-to-Source Breakdown Voltage (Note 1.) (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 μAdc) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	60 –	71.8 69	– –	Vdc mV/°C
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 0 Vdc) (V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 150°C)	I <sub>DSS</sub>	– –	– –	1.0 10	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = ±15 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	–	–	±100	nAdc

## ON CHARACTERISTICS (Note 1.)

Gate Threshold Voltage (Note 1.) (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μAdc) Threshold Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	1.0 –	1.7 4.8	2.0 –	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 1.) (V <sub>GS</sub> = 5.0 Vdc, I <sub>D</sub> = 15 Adc)	R <sub>DS(on)</sub>	–	38	46	mΩ
Static Drain-to-Source On-Voltage (Note 1.) (V <sub>GS</sub> = 5.0 Vdc, I <sub>D</sub> = 30 Adc) (V <sub>GS</sub> = 5.0 Vdc, I <sub>D</sub> = 15 Adc, T <sub>J</sub> = 150°C)	V <sub>DS(on)</sub>	– –	1.3 1.06	1.7 –	Vdc
Forward Transconductance (Note 1.) (V <sub>DS</sub> = 7.0 Vdc, I <sub>D</sub> = 15 Adc)	g <sub>FS</sub>	–	21	–	mhos

## DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 25 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>iss</sub>	–	810	1150	pF
Output Capacitance		C <sub>oss</sub>	–	260	370	
Transfer Capacitance		C <sub>rss</sub>	–	80	115	

## SWITCHING CHARACTERISTICS (Note 2.)

Turn-On Delay Time	(V <sub>DD</sub> = 30 Vdc, I <sub>D</sub> = 30 Adc, V <sub>GS</sub> = 5.0 Vdc, R <sub>G</sub> = 9.1 Ω) (Note 1.)	t <sub>d(on)</sub>	–	10	20	ns
Rise Time		t <sub>r</sub>	–	200	400	
Turn-Off Delay Time		t <sub>d(off)</sub>	–	15.6	30	
Fall Time		t <sub>f</sub>	–	62	120	
Gate Charge	(V <sub>DS</sub> = 48 Vdc, I <sub>D</sub> = 30 Adc, V <sub>GS</sub> = 5.0 Vdc) (Note 1.)	Q <sub>T</sub>	–	16	32	nC
		Q <sub>1</sub>	–	3.9	–	
		Q <sub>2</sub>	–	10	–	

## SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I <sub>S</sub> = 30 Adc, V <sub>GS</sub> = 0 Vdc) (Note 1.) (I <sub>S</sub> = 30 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 150°C)	V <sub>SD</sub>	– –	1.01 1.03	1.2 –	Vdc
Reverse Recovery Time	(I <sub>S</sub> = 30 Adc, V <sub>GS</sub> = 0 Vdc, di <sub>S</sub> /dt = 100 A/μs) (Note 1.)	t <sub>rr</sub>	–	50	–	ns
		t <sub>a</sub>	–	32	–	
		t <sub>b</sub>	–	17	–	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	–	0.082	–	μC

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperatures.

# NTP30N06L, NTB30N06L

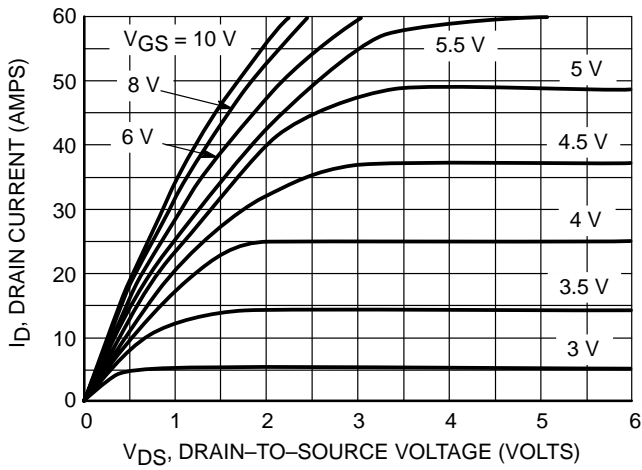


Figure 1. On-Region Characteristics

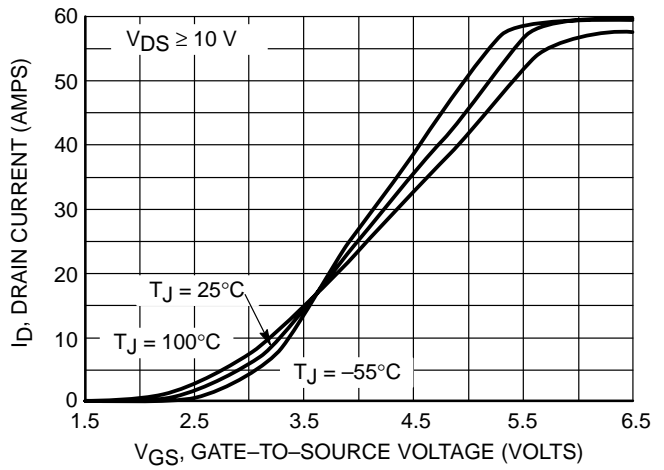


Figure 2. Transfer Characteristics

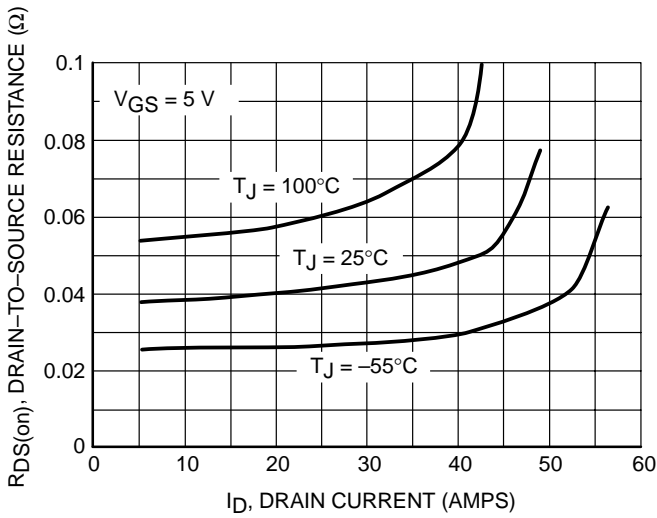


Figure 3. On-Resistance versus Gate-to-Source Voltage

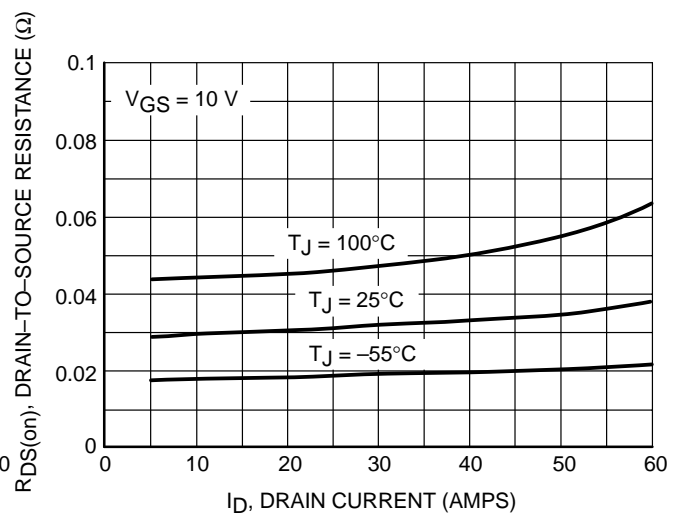


Figure 4. On-Resistance versus Drain Current and Gate Voltage

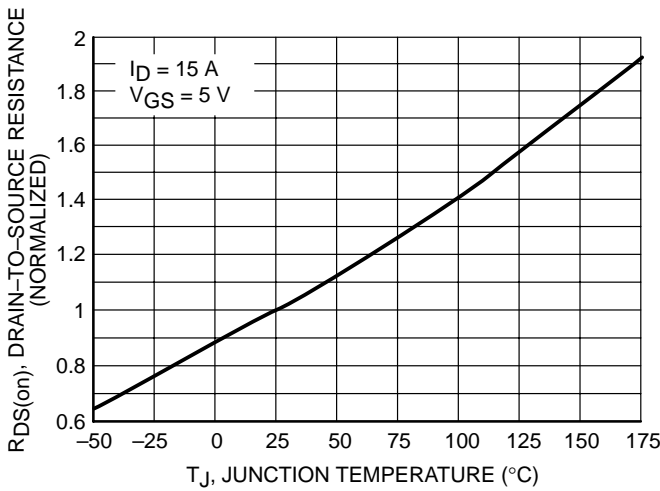


Figure 5. On-Resistance Variation with Temperature

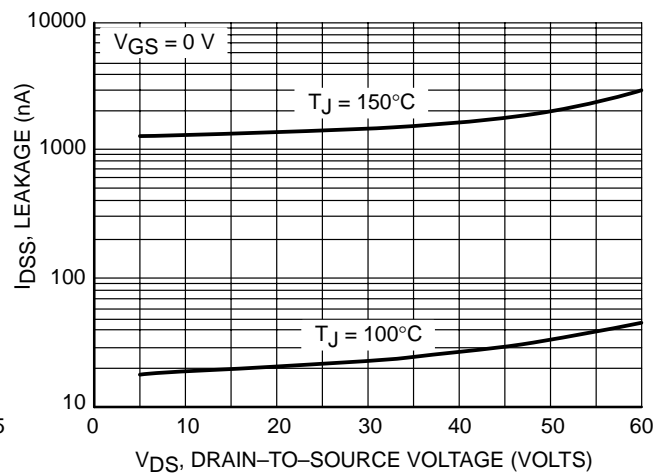


Figure 6. Drain-to-Source Leakage Current versus Voltage

# NTP30N06L, NTB30N06L

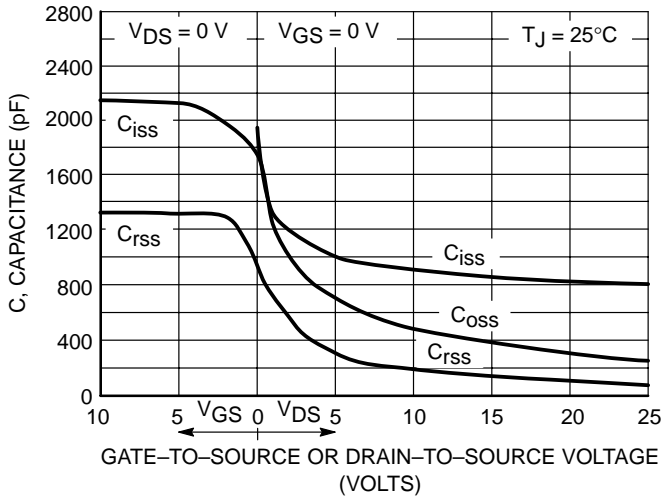


Figure 7. Capacitance Variation

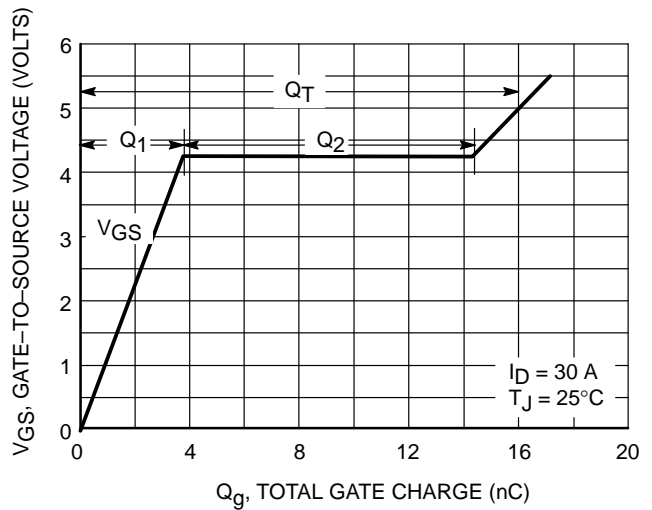


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

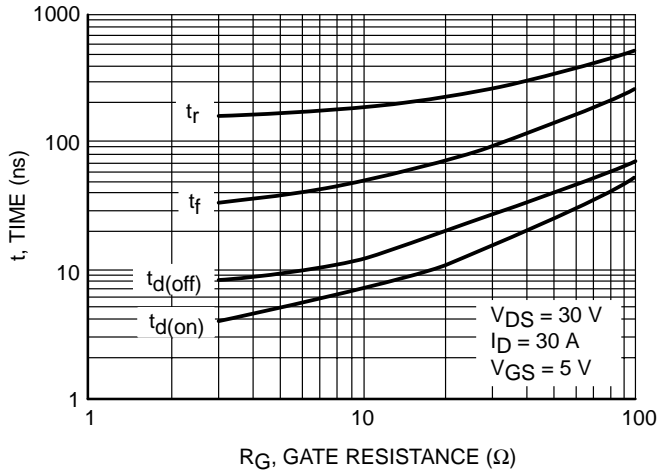


Figure 9. Resistive Switching Time Variation versus Gate Resistance

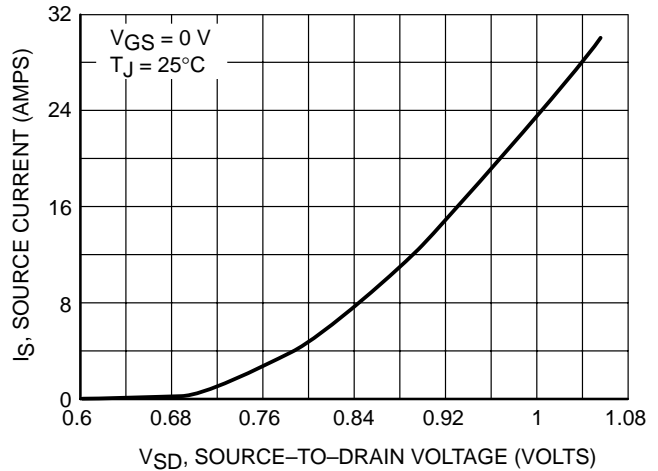


Figure 10. Diode Forward Voltage versus Current

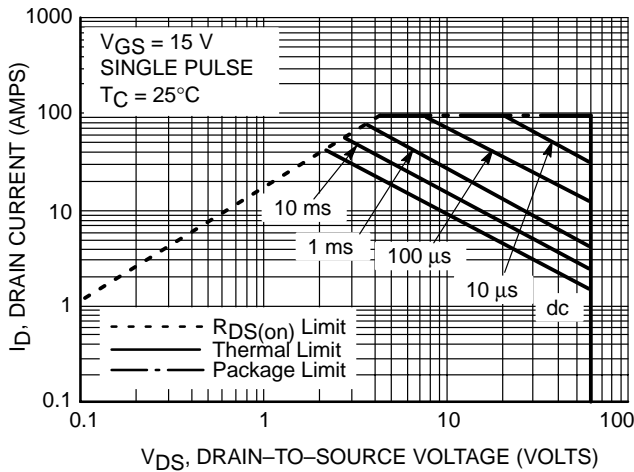


Figure 11. Maximum Rated Forward Biased Safe Operating Area

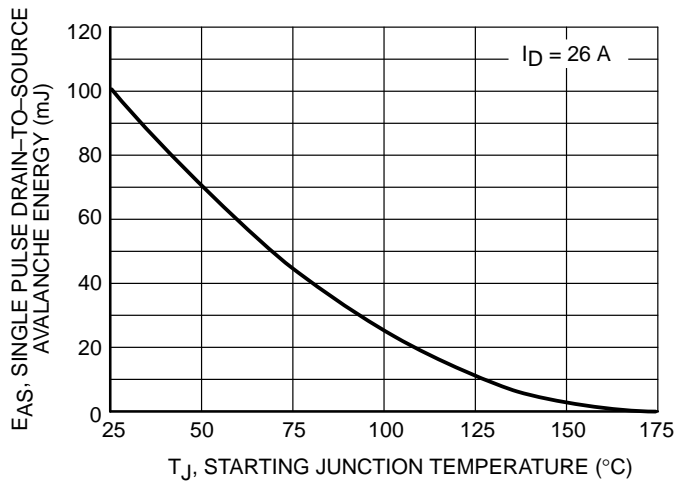


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

# NTP30N06L, NTB30N06L

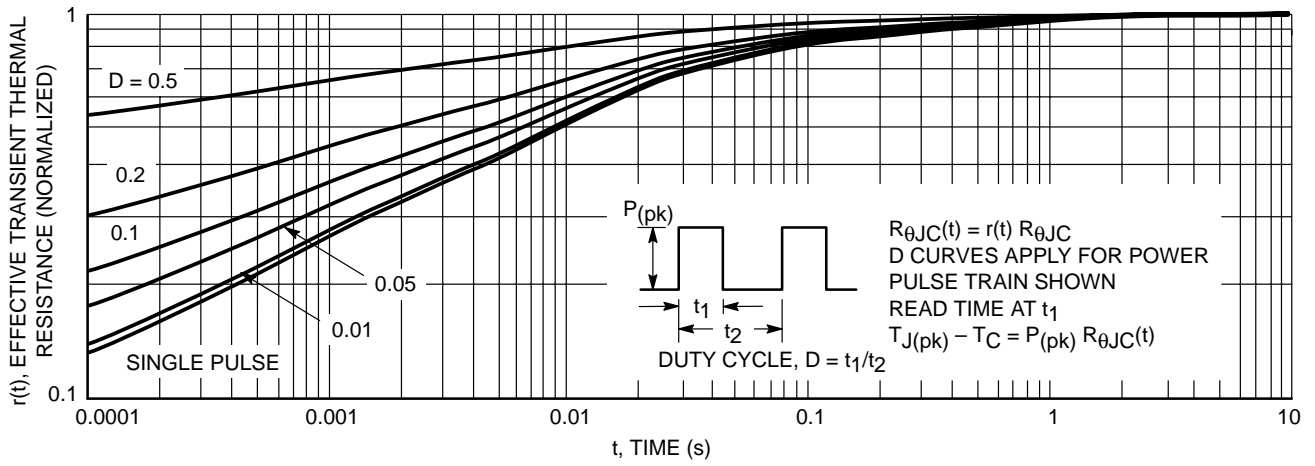


Figure 13. Thermal Response

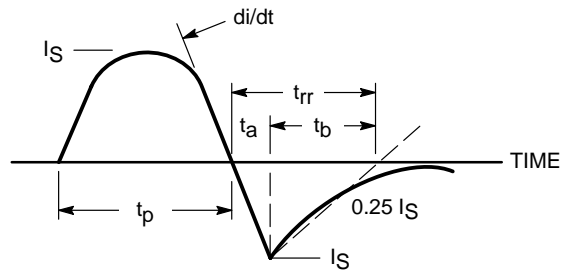
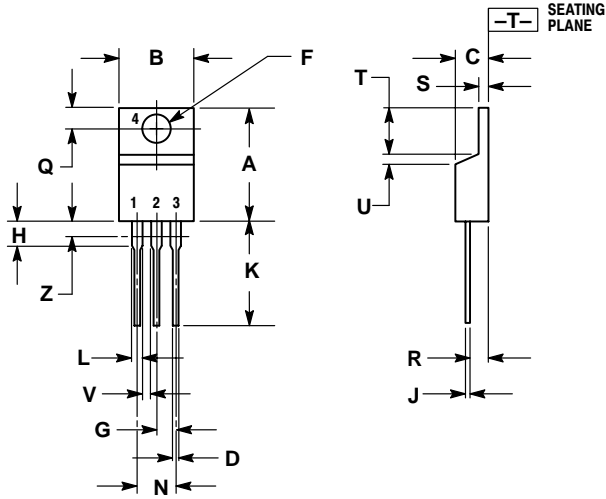


Figure 14. Diode Reverse Recovery Waveform

# NTP30N06L, NTB30N06L

## PACKAGE DIMENSIONS

TO-220 THREE-LEAD  
TO-220AB  
CASE 221A-09  
ISSUE AA



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

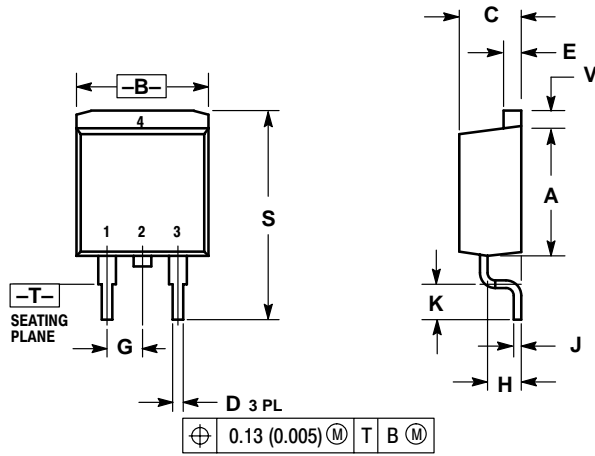
STYLE 5:

- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

# NTP30N06L, NTB30N06L

## PACKAGE DIMENSIONS

**D<sup>2</sup>PAK**  
CASE 418B-03  
ISSUE D




- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

- STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

# NTP30N06L, NTB30N06L

**ON Semiconductor** and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

## PUBLICATION ORDERING INFORMATION

### Literature Fulfillment:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** ONlit@hibbertco.com

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada

**JAPAN:** ON Semiconductor, Japan Customer Focus Center  
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031  
**Phone:** 81-3-5740-2700  
**Email:** r14525@onsemi.com

**ON Semiconductor Website:** <http://onsemi.com>

For additional information, please contact your local Sales Representative.