NTTS2P03R2

Power MOSFET
-2.48 Amps, -30 Volts

P−Channel Enhancement Mode
Single Micro8™ Package

Features

- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Miniature Micro8 Surface Mount Package
- Diode Exhibits High Speed, Soft Recovery
- Micro8 Mounting Information Provided

Applications

- Power Management in Portable and Battery−Powered Products, i.e.: Cellular and Cordless Telephones and PCMCIA Cards

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	−30	V
Gate−to−Source Voltage − Continuous	V_{GS}	±20	V
Thermal Resistance −			
Junction−to−Ambient (Note 1.)	$R_{\theta JA}$	160	°C/W
Total Power Dissipation @ T_A = 25°C	P_D	0.78	W
Continuous Drain Current @ T_A = 25°C	I_D	−2.48	A
Continuous Drain Current @ T_A = 70°C	I_D	−1.98	A
Thermal Resistance −			
Junction−to−Ambient (Note 2.)	$R_{\theta JA}$	70	°C/W
Total Power Dissipation @ T_A = 25°C	P_D	1.78	W
Continuous Drain Current @ T_A = 25°C	I_D	−3.75	A
Continuous Drain Current @ T_A = 70°C	I_D	−3.0	A
Thermal Resistance −			
Junction−to−Ambient (Note 3.)	$R_{\theta JA}$	210	°C/W
Total Power Dissipation @ T_A = 25°C	P_D	0.60	W
Continuous Drain Current @ T_A = 25°C	I_D	−2.10	A
Continuous Drain Current @ T_A = 70°C	I_D	−1.67	A
Pulsed Drain Current (Note 5.)	I_{DM}	−17	A
Thermal Resistance −			
Junction−to−Ambient (Note 4.)	$R_{\theta JA}$	100	°C/W
Total Power Dissipation @ T_A = 25°C	P_D	1.25	W
Continuous Drain Current @ T_A = 25°C	I_D	−3.02	A
Continuous Drain Current @ T_A = 70°C	I_D	−2.42	A
Pulsed Drain Current (Note 5.)	I_{DM}	−24	A
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

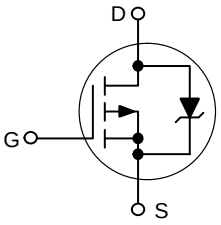
1. Minimum FR−4 or G−10 PCB, Time ≤ 10 Seconds.
2. Mounted onto a 2″ square FR−4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), Time ≤ 10 Seconds.
3. Minimum FR−4 or G−10 PCB, Steady State.
4. Mounted onto a 2″ square FR−4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), Steady State.
5. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

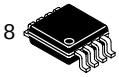
ON Semiconductor®

http://onsemi.com

−2.48 AMPERES
−30 VOLTS
85 mΩ @ V_{GS} = −10 V

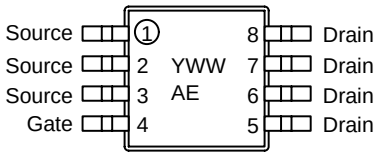
Single P−Channel





Micro8
CASE 846A
STYLE 1

MARKING DIAGRAM & PIN ASSIGNMENT



(Top View)

Y = Year
WW = Work Week
AE = Device Code

ORDERING INFORMATION

Device	Package	Shipping†
NTTS2P03R2	Micro8	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

© Semiconductor Components Industries, LLC, 2003

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted) (continued)

Rating	Symbol	Value	Unit
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = −30 Vdc, V_{GS} = −10 Vdc, Peak I_L = −3.0 Apk, L = 65 mH, R_G = 25 Ω)	E_{AS}	292.5	mJ
Maximum Lead Temperature for Soldering Purposes for 10 seconds	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted) (Note 6.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = −250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	−30 −	− −30	− −	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{GS} = 0 Vdc, V_{DS} = −30 Vdc, T_J = 25°C) (V_{GS} = 0 Vdc, V_{DS} = −30 Vdc, T_J = 125°C)		I_{DSS}	 − −	 − −	 −1.0 −25	μAdc
Gate−Body Leakage Current (V_{GS} = −20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	−	−	−100	nAdc
Gate−Body Leakage Current (V_{GS} = +20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	−	−	100	nAdc
ON CHARACTERISTICS						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = −250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	−1.0 −	−1.7 3.6	−3.0 −	Vdc
Static Drain−to−Source On−State Resistance (V_{GS} = −10 Vdc, I_D = −2.48 Adc) (V_{GS} = −4.5 Vdc, I_D = −1.24 Adc)		$R_{DS(on)}$	 − −	 0.063 0.100	 0.085 0.135	Ω
Forward Transconductance (V_{DS} = −15 Vdc, I_D = −1.24 Adc)		g_{FS}	−	3.1	−	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = −24 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	−	500	−	pF
Output Capacitance		C_{oss}	−	160	−	
Reverse Transfer Capacitance		C_{rss}	−	65	−	
SWITCHING CHARACTERISTICS (Notes 7. & 8.)						
Turn−On Delay Time	(V_{DD} = −24 Vdc, I_D = −2.48 Adc, V_{GS} = −10 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	−	10	−	ns
Rise Time		t_r	−	20	−	
Turn−Off Delay Time		$t_{d(off)}$	−	40	−	
Fall Time		t_f	−	35	−	
Turn−On Delay Time	(V_{DD} = −24 Vdc, I_D = −1.24 Adc, V_{GS} = −4.5 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	−	16	−	ns
Rise Time		t_r	−	40	−	
Turn−Off Delay Time		$t_{d(off)}$	−	30	−	
Fall Time		t_f	−	30	−	
Total Gate Charge	(V_{DS} = −24 Vdc, V_{GS} = −4.5 Vdc, I_D = −2.48 Adc)	Q_{tot}	−	15	22	nC
Gate−Source Charge		Q_{gs}	−	3.2	−	
Gate−Drain Charge		Q_{gd}	−	4.0	−	
BODY−DRAIN DIODE RATINGS (Note 7.)						
Diode Forward On−Voltage	(I_S = −2.48 Adc, V_{GS} = 0 Vdc) (I_S = −2.48 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	− −	−0.92 −0.72	−1.3 −	Vdc
Reverse Recovery Time	(I_S = −1.45 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	−	38	−	ns
		t_a	−	20	−	
		t_b	−	18	−	
Reverse Recovery Stored Charge		Q_{RR}	−	0.04	−	μC

6. Handling precautions to protect against electrostatic discharge is mandatory.
7. Indicates Pulse Test: Pulse Width = 300 μsec max, Duty Cycle = 2%.
8. Switching characteristics are independent of operating junction temperature.

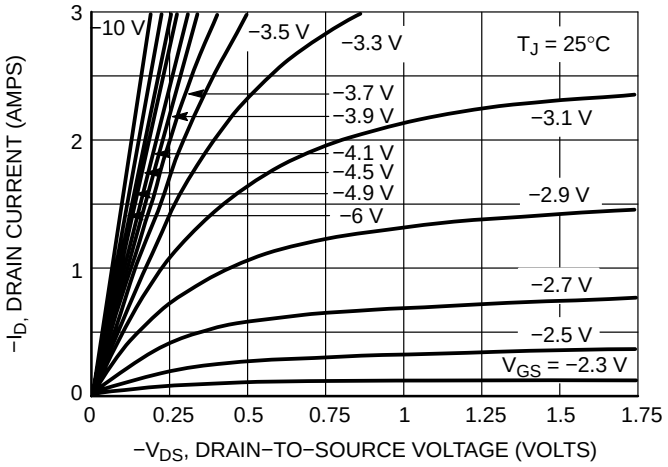


Figure 1. On−Region Characteristics

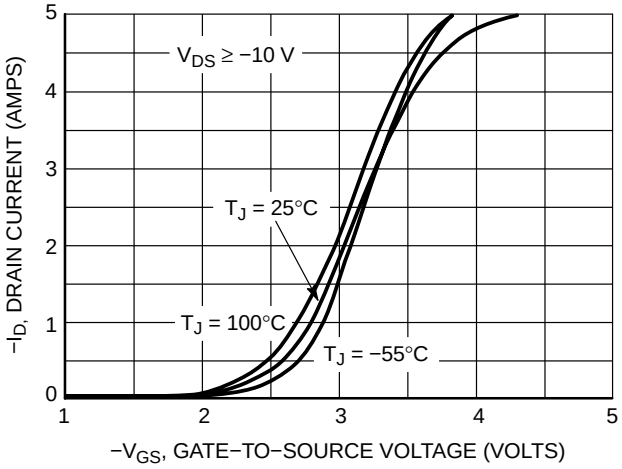


Figure 2. Transfer Characteristics

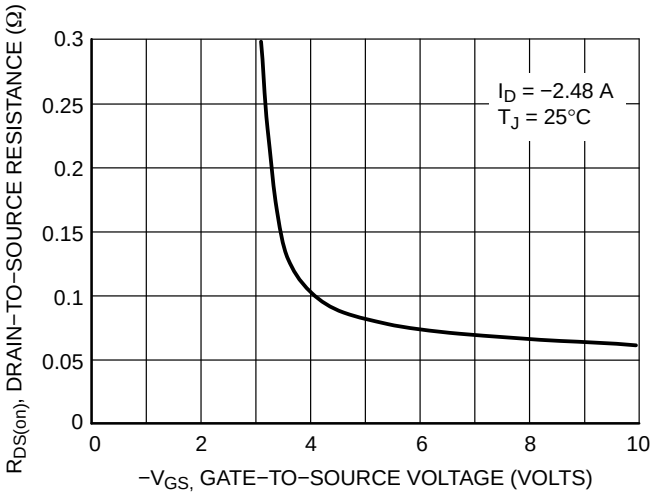


Figure 3. On−Resistance versus Gate−to−Source Voltage

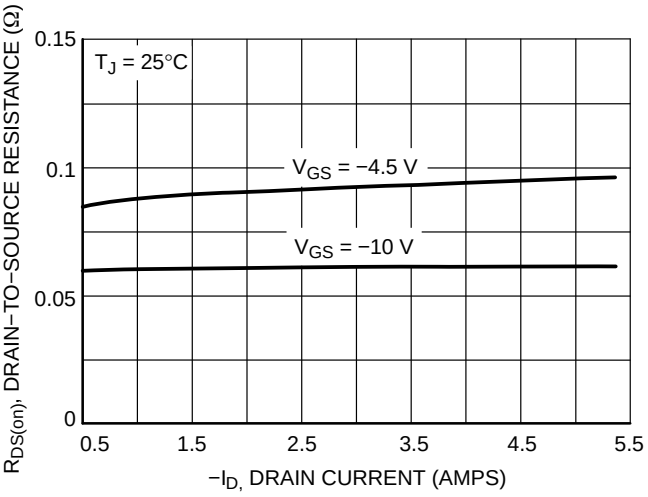


Figure 4. On−Resistance versus Drain Current and Gate Voltage

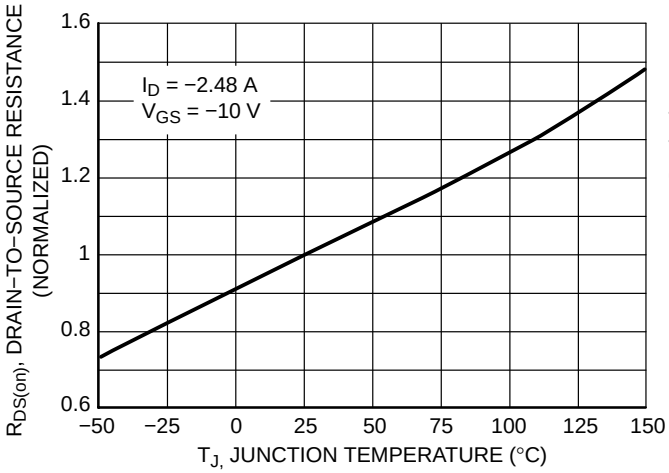


Figure 5. On−Resistance Variation with Temperature

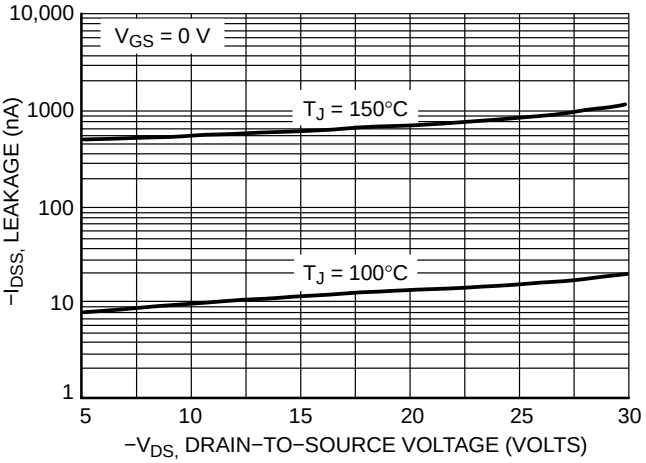


Figure 6. Drain−to−Source Leakage Current versus Voltage

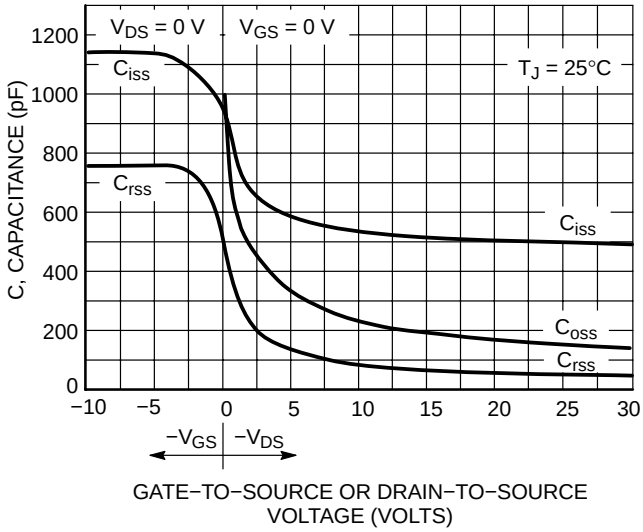


Figure 7. Capacitance Variation

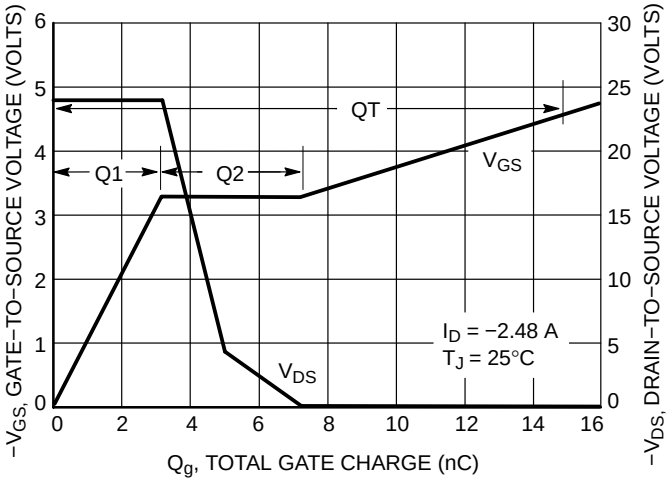


Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

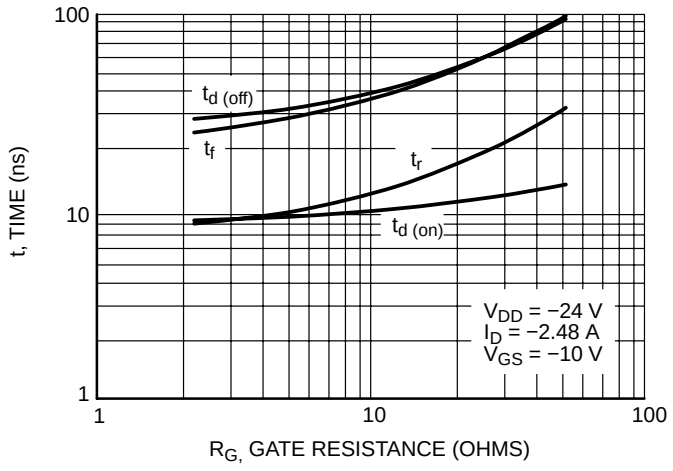


Figure 9. Resistive Switching Time Variation versus Gate Resistance

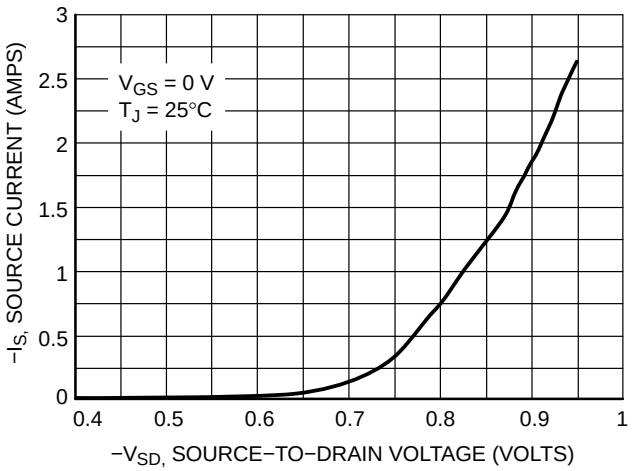


Figure 10. Diode Forward Voltage versus Current

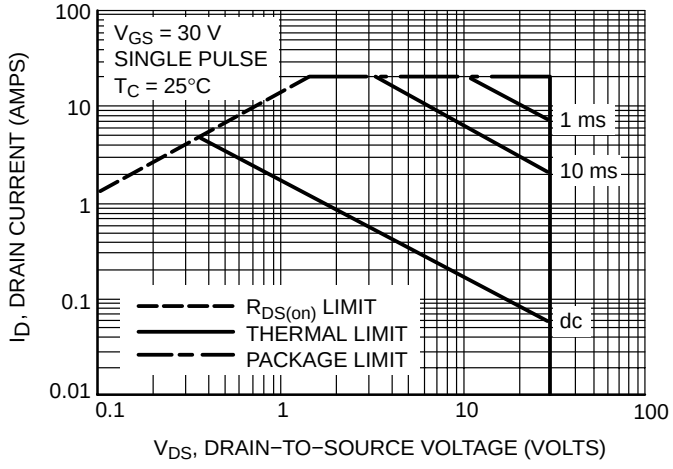


Figure 11. Maximum Rated Forward Biased Safe Operating Area

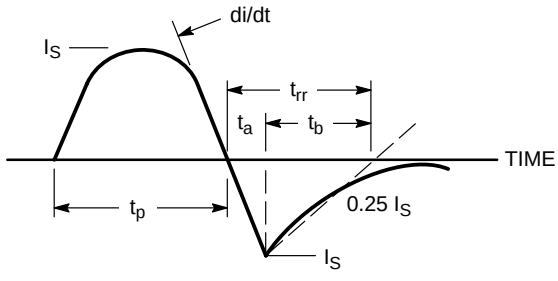


Figure 12. Diode Reverse Recovery Waveform

TYPICAL ELECTRICAL CHARACTERISTICS

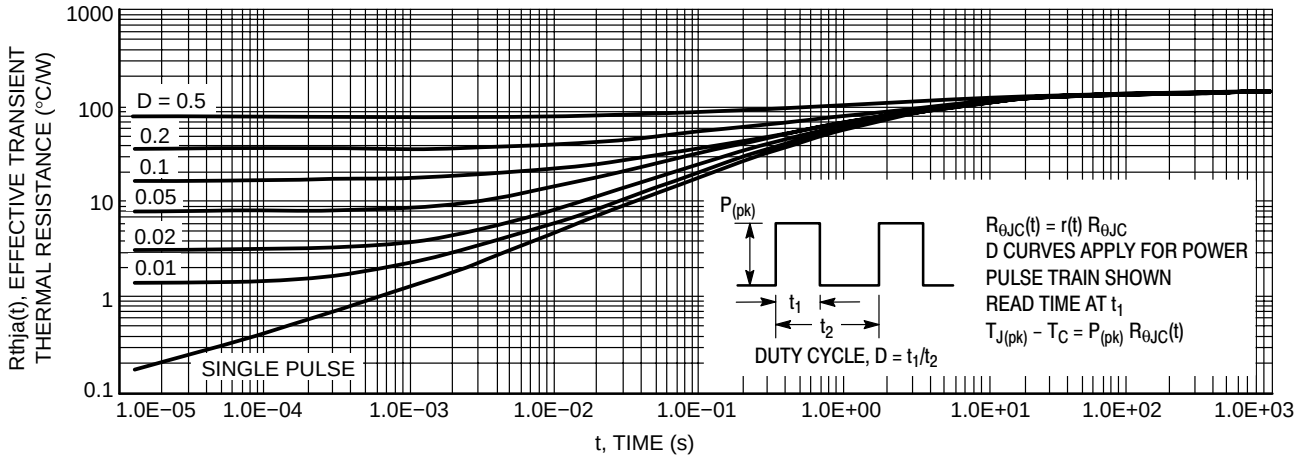
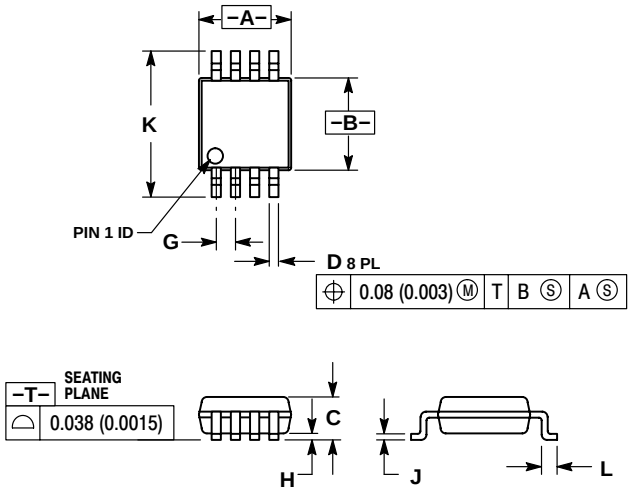


Figure 13. Thermal Response

PACKAGE DIMENSIONS

Micro8
CASE 846A−02
ISSUE F

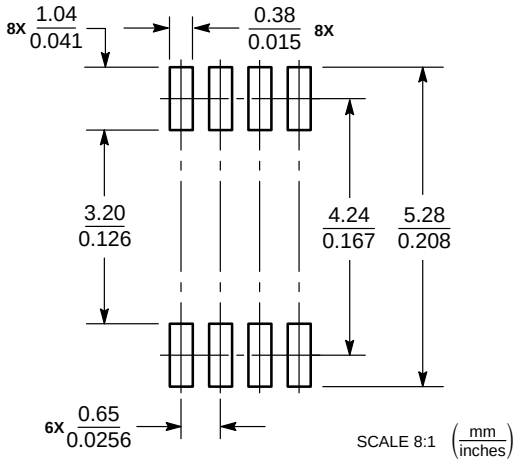


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A−01 OBSOLETE, NEW STANDARD 846A−02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	---	1.10	---	0.043
D	0.25	0.40	0.010	0.016
G	0.65 BSC		0.026 BSC	
H	0.05	0.15	0.002	0.006
J	0.13	0.23	0.005	0.009
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Micro8 is a trademark of International Rectifier.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2−9−1 Kamimeguro, Meguro−ku, Tokyo, Japan 153−0051
Phone: 81−3−5773−3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.