

# **STP80NF12**

## **General features**

Туре	V <sub>DSS</sub> (@Tjmax)	R <sub>DS(on)</sub>	I <sub>D</sub>
STP80NF12	120V	<0.018Ω	80A <sup>(1)</sup>

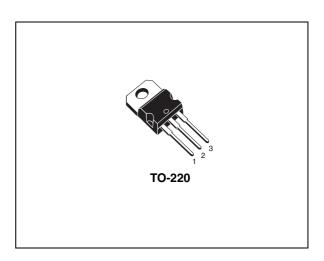
- Exceptional dv/dt capability
- 100% avalanche tested
- Application oriented characterization

## Description

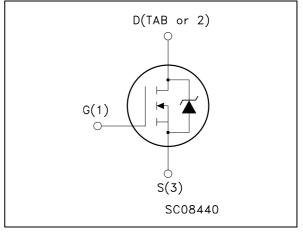
This MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced highefficiency, high-frequency isolated DC-DC converters for Telecom and Computer applications. It is also intended for any applications with low gate drive requirements.

## Applications

Switching application



## Internal schematic diagram



### **Order codes**

Part number	Marking	Package	Packaging
STP80NF12	P80NF12	TO-220	Tube

January	2007
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# 1 Electrical ratings

Table 1.	Absolute	maximum	ratings
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Symbol	Parameter	Valu	Unit	
Symbol	Farameter	STB_P_W80NF12	STP80NF12FP	Omt
V <sub>DS</sub>	Drain-source voltage (V <sub>GS</sub> = 0)	120		V
V <sub>DGR</sub>	Drain-gate voltage (R <sub>GS</sub> = 20KΩ)	120		V
V <sub>GS</sub>	Gate-source voltage	± 22	2	V
I <sub>D</sub> <sup>(1)</sup>	Drain current (continuous) at $T_C = 25^{\circ}C$	80 11 <sup>(2)</sup>		А
Ι <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> =100°C	60	60 <sup>(2)</sup>	А
I <sub>DM</sub> <sup>(3)</sup>	Drain current (pulsed)	320	320 <sup>(2)</sup>	А
P <sub>TOT</sub>	Total dissipation at $T_{C} = 25^{\circ}C$	300	45	W
	Derating factor	2.0	0.3	W/°C
dv/dt <sup>(4)</sup>	Peak diode recovery voltage slope	10		V/ns
V <sub>ISO</sub>	Insulation withstand voltage (DC)	2500		V
T <sub>J</sub> T <sub>stg</sub>	Operating junction temperature Storage temperature	-55 to 175		°C

1. Limited by Package

2. Limited only by maximum temperature allowed

3. Pulse width limited by safe operating area

4. Starting  $T_J = 25 \text{ }^{o}\text{C}$ ,  $I_D = 40\text{A}$ ,  $V_{DD} = 45\text{V}$ 

Symbol	Parameter	TO-247	D <sup>2</sup> PAK TO-220	TO-220FP	Unit
R <sub>thJC</sub>	Thermal resistance junction-case Max	0.5	0.5	3.33	°C/W
R <sub>thJA</sub>	Thermal resistance junction-ambient Max	50	62.5	62.5	°C/W
Τ <sub>Ι</sub>	Maximum lead temperature for soldering purpose	300	300	300	°C

# 2 Electrical characteristics

(T<sub>CASE</sub>=25°C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	$I_{D} = 250 \mu A, V_{GS} = 0$	120			V
I <sub>DSS</sub>	Zero gate voltage drain current ( $V_{GS} = 0$ )	V <sub>DS</sub> = Max rating, V <sub>DS</sub> = Max rating @125°C			1 10	μΑ μΑ
I <sub>GSS</sub>	Gate body leakage current (V <sub>DS</sub> = 0)	$V_{GS} = \pm 20V$			±100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2			V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 40A		0.013	0.018	Ω

#### Table 3. On/off states

### Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
g <sub>fs</sub> <sup>(1)</sup>	Forward transconductance	V <sub>DS</sub> =15V, I <sub>D</sub> = 40A		80		S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input capacitance Output capacitance Reverse transfer capacitance	V <sub>DS</sub> =25V, f=1 MHz, V <sub>GS</sub> =0		4300 600 230		pF pF pF
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 80V, I_{D} = 80A$ $V_{GS} = 10V$		140 23 51	189	nC nC nC

1. Pulsed: pulse duration=300 $\mu$ s, duty cycle 1.5%

### Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t <sub>d(on)</sub> t <sub>r</sub> t <sub>d(off)</sub> t <sub>f</sub>	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD}$ = 50 V, $I_D$ = 40A, R <sub>G</sub> =4.7 $\Omega$ , V <sub>GS</sub> =10V Figure 13 on page 8		40 145 134 115		ns ns ns ns



Symbol	Parameter	Test conditions	Min.	Тур.	Max	Unit
I <sub>SD</sub>	Source-drain current				80	A
I <sub>SDM</sub> <sup>(1)</sup>	Source-drain current (pulsed)				320	А
$V_{SD}^{(2)}$	Forward on voltage	I <sub>SD</sub> =80A, V <sub>GS</sub> =0			1.3	V
t <sub>rr</sub> Q <sub>rr</sub> I <sub>RRM</sub>	Reverse recovery time Reverse recovery charge Reverse recovery current	I <sub>SD</sub> =80A, di/dt = 100A/μs, V <sub>DD</sub> =35V, Τ <sub>J</sub> = 150°C		155 0.85 11		ns μC Α

 Table 6.
 Source drain diode

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration=300 $\mu s,$  duty cycle 1.5%



GC94470

10<sup>-1</sup> t<sub>P</sub>(s)

GC97390

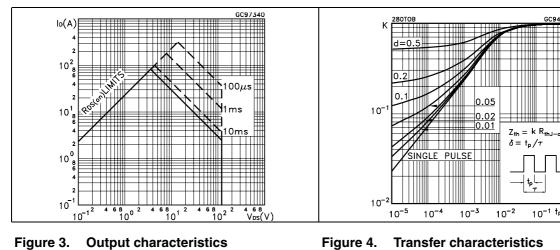
lo(A)

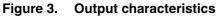
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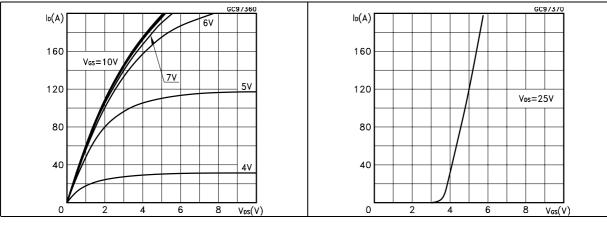
#### **Electrical characteristics (curves)** 2.1

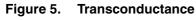
#### Figure 1. Safe operating area

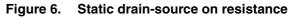
Figure 2. Thermal impedance



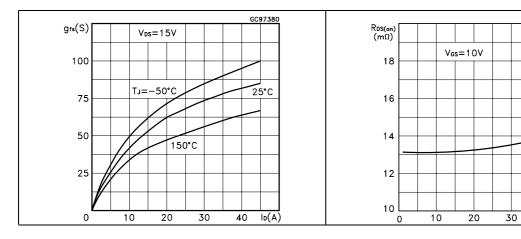




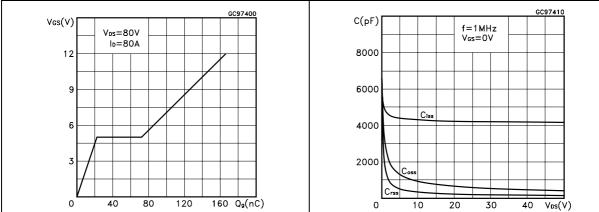




**Transfer characteristics** 







#### Gate charge vs. gate-source voltage Figure 8. Figure 7. **Capacitance variations**

Figure 9. Normalized gate threshold voltage vs. temperature

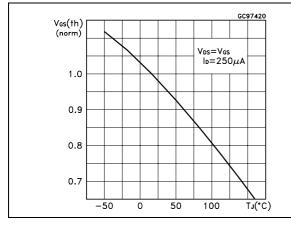


Figure 11. Source-drain diode forward characteristics

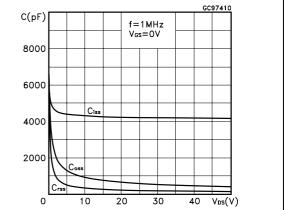


Figure 10. Normalized on resistance vs. temperature

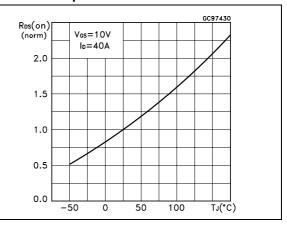
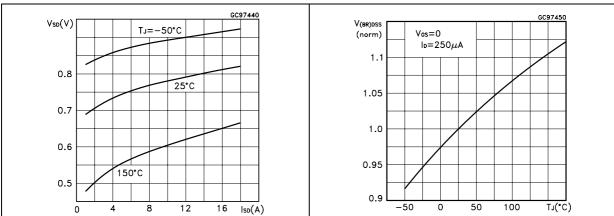


Figure 12. Normalized B<sub>VDSS</sub> vs. temperature



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# 3 Test circuit

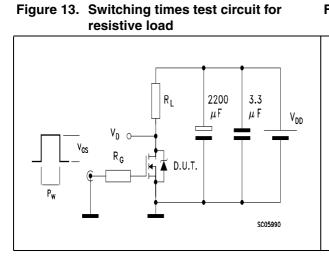
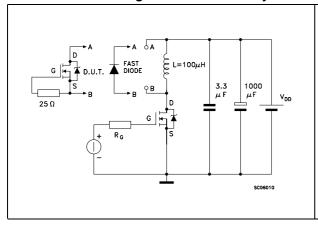
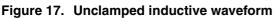


Figure 15. Test circuit for inductive load switching and diode recovery times





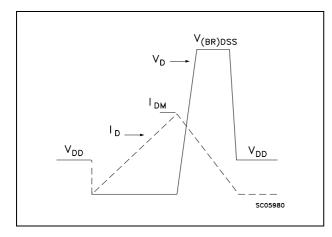


Figure 14. Gate charge test circuit

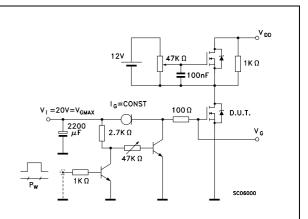
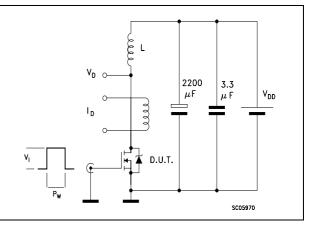


Figure 16. Unclamped Inductive load test circuit



# 4 Package mechanical data

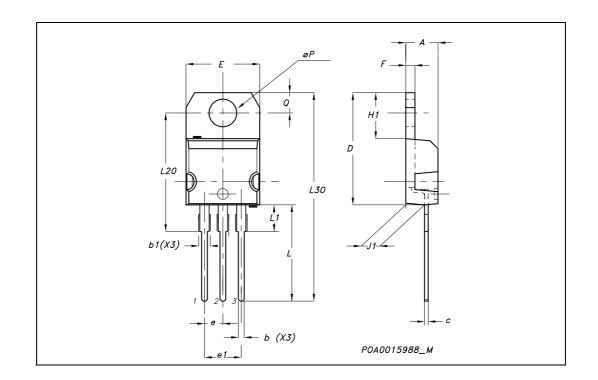
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DIM.	mm.			inch		
	MIN.	ТҮР	MAX.	MIN.	TYP.	MAX.
А	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
С	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
Е	10		10.40	0.393		0.409
е	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øР	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116

### **TO-220 MECHANICAL DATA**



# 5 Revision history

Table 7.	Revision	history
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Date	Revision	Changes
21-Jun-2004	2	Preliminary version
24-Jul-2006	3	The document has been reformatted, SOA updated
31-Jan-2007	4	Typo mistake on Table 1.



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