National Semiconductor

October 1994

PC87410 PCI-IDE Interface Controller

General Description

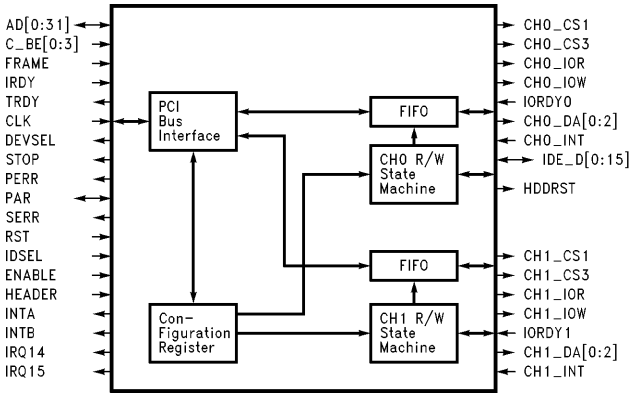
The PCI-IDE Interface Controller is designed to interface the IDE drive directly onto the PCI bus. It provides write posting and read pre-fetches, allowing the CPU to run concurrently with IDE cycles. It connects IDE drIves ''gluelessly'' into the PCI bus and supports faster ATA devices using modes 1, 2 and 3 through PIO accesses. It supports dual IDE channels for up to four drives, and works seamlessly with the National Semiconductor's SuperI/O™ family of products.

A full suite of software drives included with device are fully tested with DOS 5.0–6.x, Windows 3.x–4.x, Windows NT, OS/2 2.x, Novell Netware 3.1x–4.x, and SCO UNIX 3.x.

Key Features

- Fully compatible with PCI specifications rev 2.0 (April, 1993)
- Programmable Base Address registers
- Interfaces with the 32 bits PCI local bus to IDE drives
- Support IDE PIO timing mode 0, 1, 2 of ANSI ATA specifications
- Support Mode 3 (11 MB/s) timing proposal on enhanced IDE (IDE-2 or ATA-2) specifications
- Two IDE-2 channel supported (each channel supports 2 devices)
- Supports primary IDE or secondary IDE address
- 16-Byte FIFO provide 4-level Posted Write and Read ahead buffers per channel for concurrent system operation
- Programmable command and recovery timing for reads and writes per channel
- Independent timings for command registers and data registers
- Slew rate controlled output directly interface with IDE devices
- Supports either IRQ14/15 or INTA#/B#
- Hardware and Software chip enable/disable capability
- 100 pin PQFP package, NO other glue logic needed and 12 mA transceivers are built in

Block Diagram



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TRI-STATE® is a registered trademark of National Semiconductor Corporation.
SuperI/O™ is a trademark of National Semiconductor Corporation

RRD-B30M75/Printed in U. S. A.

Absolute Maximum Ratings 5V ±10%

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.5V to +7.0V
Input Voltage (V_I)	−0.5V to V_{DD} +0.5V
Output Voltage (V_O)	−0.5V to V_{DD} +0.5V
Storage Temperature (T_{STG})	−65°C to +165°C
Lead Temperature (T_L) (Soldering, 10 seconds)	+260°C

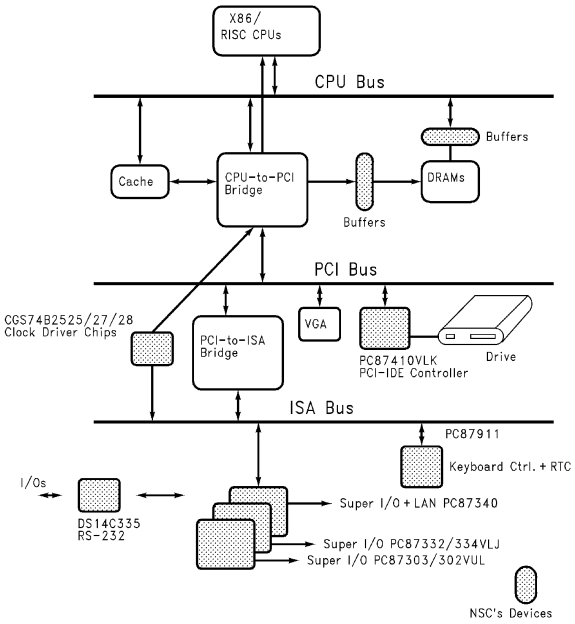
Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage	4.5	5.0	5.5	V
Operating Temperature (T_A)	0		+70	°C

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage					
	CMOS				$0.3V_{DD}$	V
	TTL				0.8	V
V_{IH}	Input High Voltage					
	CMOS		$0.7\ V_{DD}$			V
	TTL		2.0			V
I_{IH}	Input High Current	$V_{IN} = V_{DD}$	−10		10	μA
	Input with Pull-Down	$V_{IN} = V_{DD}$	10		200	μA
I_{IL}	Input Low Current	$V_{IN} = V_{SS}$	−10		10	μA
	Input with Pull-Down	$V_{IN} = V_{SS}$	−200		−10	μA
V_{OH}	Type B8	$I_{OH} = 8$ mA	2.4			V
	Type B12	$I_{OH} = 12$ mA	2.4			V
V_{OL}	Type B8	$I_{OL} = 8$ mA			0.4	V
	Type B12	$I_{OL} = 12$ mA			0.4	V
I_{OZ}	Output TRI-STATE Leakage Current	$V_{OH} = V_{SS}$ or V_{DD}	−10		10	μA
I_{DD}	V_{DD} Average Supply Current	No Load			10	mA

PCI__Based System



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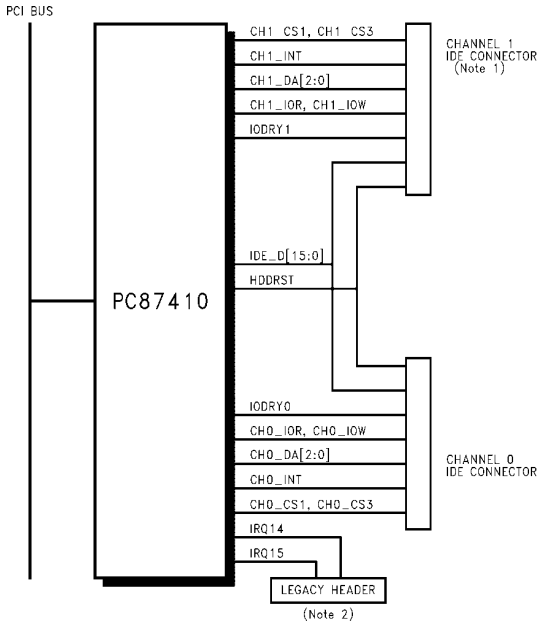
Basic Configuration

The following diagram shows how the PCI-IDE Interface Controller is used in a system.



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Note 1. Second IDE connector is optional

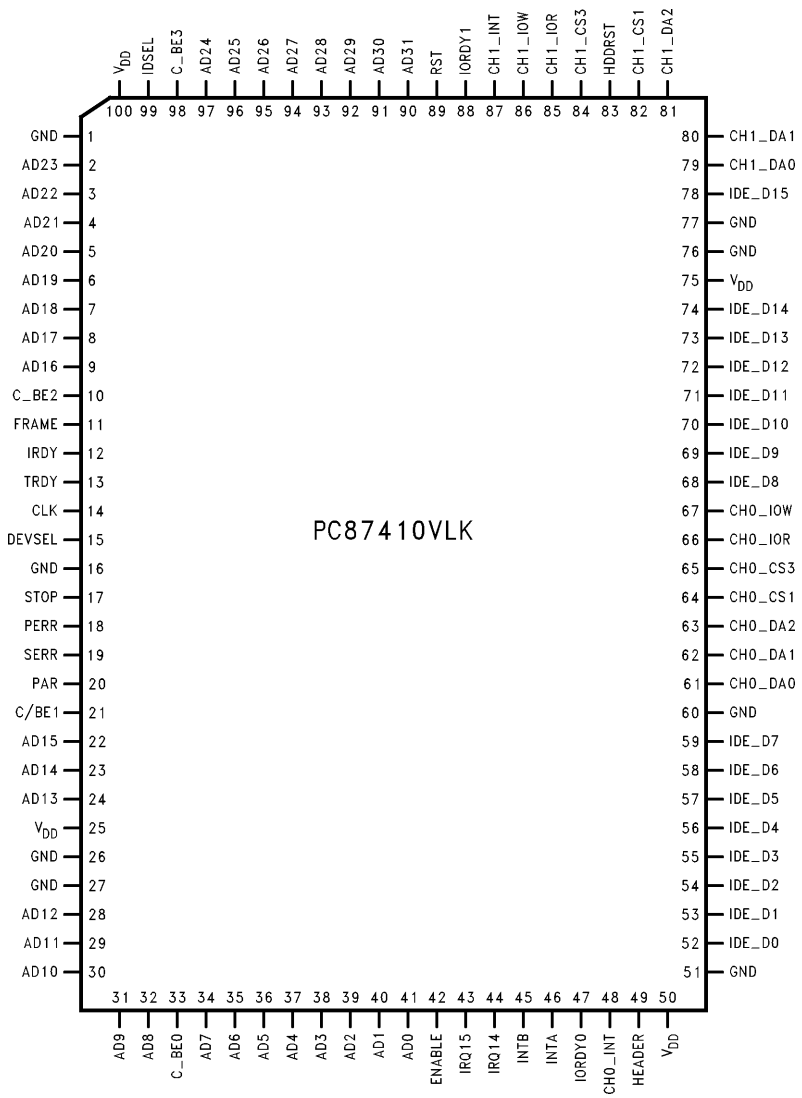
Note 2. Legacy header is needed under the following conditions:

a. The device is on a PCI adapter card.

b. IDE compatibility is required.

Connection Diagram

Plastic Quad Flatpak, EIAJ



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Order Number PC87410VLK
See NS Package Number VLK100A

Pin Description

PCI Interface

Name	Type	I_{OL}	Description
AD[31:0]	I/O	8 mA	**MULTIPLEXED ADDRESS AND DATA.** The direction of these pins are defined below: **Phase** Address Phase input Data Phase Read output Write input
C/BE [3:0]	I		**COMMAND/BYTE ENABLE** are multiplexed Bus command and Byte enables.
PAR	I/O	8 mA	**PARITY** is even parity across AD[31:0] and C/BE[3:0]. PAR is an input during writes and an output during reads.
FRAME#	I		**CYCLE FRAME** is driven by the initiator to indicate the beginning and duration of an access.
TRDY#	O/TRI-STATE®	12 mA	**TARGET READY** indicates that the current data phase of the transaction is ready to be completed.
IRDY#	I		**INITIATOR READY** indicates that the initiator is ready to complete the current data phase of the transaction.
STOP#	O/TRI-STATE	8 mA	**STOP** indicates that the current target is requesting the initiator to stop the current transaction.
DEVSEL#	O/TRI-STATE	8 mA	**DEVICE SELECT,** when actively drive, indicates the driving device has decoded its adderss as the target of the current access.
IDSEL	I		**INITIALIZATION DEVICE SELECT** is used as a chip select during configuration read and write transactions.
PERR#	O/TRI-STATE	8 mA	**PARITY ERROR** is used for reporting data parity errors during all PCI transactions except a Special Cycle. PERR# is an output during writes and an input during reads.
SERR#	O/TRI-STATE	8 mA	**SYSTEM ERROR** is used for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be castrophic. When reporting address parity errors, SERR# is an output. When reporting data parity errors for the Special Cycle command, SERR# is an output during writes and an input during needs.
INTA#, B#	O/TRI-STATE	8 mA, Slew Rate Control	**INTERRUPT.** Interrupt request A and B
CLK	I		**CLOCK.** Up to 33 MHz PCI Clock
RST#	I		**RESET.** PCI Reset

Power and Ground

Name	Type	Description
GND	I	**V_{SS} or GROUND**
V_{CC}	I	**V_{DD} or +5V.** Power to PCI buffers, core and IDE buffers.

Note: All signals are TTL except CH0__INT (Pin 48) and CH1__INT (Pin 87) are CMOS.

Pin Description (Continued)

IDE Interface

Name	Type	I_{OL}	Description
IDE__D[15:0]	I/O	12 mA, Slew Rate Control	**DRIVE DATA BUS.** This is an 8- or 16-bit bi-direction data between the PCI-IDE chip and the drive. The lower 8 bits are used for 8-bit transfers (e.g. command registers, ECC bytes).
CH0__DA[2:0]	O	12 mA, Slew Rate Control	**CHANNEL 0 ADDRESS LINES.** This is the 3-bit binary coded address asserted by the host to access a register or data port in the drive.
CH1__DA [2:0]	O	12 mA, Slew Rate Control	**CHANNEL 1 ADDRESS LINES.** This is the 3-bit binary coded address asserted by the host to access a register or data port in the drive.
IORDY0	I		**CHANNEL 0 I/O CHANNEL READY.** This signal is negated to extend the disk transfer cycle of any register access (read or write) when the drive is not ready to respond to a data transfer request.
IORDY1	I		**CHANNEL 1 I/O CHANNEL READY.** This signal is negated to extend the disk transfer cycle of any register access (read or write) when the drive is not ready to respond to a data transfer request.
CH0__IOR#	O	12 mA, Slew Rate Control	**CHANNEL 0 I/O READ.** This is the read strobe signal. The falling edge of CH0__IOR# enables data from a register or the data port of the drive onto the PCI bus.
CH0__IOW#	O	12 mA, Slew Rate Control	**Channel 0 I/O Read.** This is the write strobe signal. The rising edge of CH0__IOW# clocks data from the PCI-IDE chip into the register or the data port of the drive.
CH1__IOR#	O	12 mA, Slew Rate Control	**CHANNEL 1 I/O READ.** This is the read strobe signal. The falling edge of the CH1__IOR# enables data from a register or the data port of the drive onto the PCI bus.
CH1__IOW#	O	12 mA, Slew Rate Control	**CHANNEL 1 I/O WRITE.** This is the write strobe signal. The rising edge of CH1__IOW# clocks data from the PCI-IDE chip into the register or the data port of the drive.
HDDRST#	O	12 mA, Slew Rate Control	**DRIVE RESET.** This signal from the PCI-IDE chip is triggered by RST# or under software control which generates IDE reset for a min time of 62 μs.
CH0__CS1#, CH0__CS3#	O	12 mA, Slew Rate Control	**CHANNEL 0 CHIP SELECT 1 AND 3.** CH0__CS1# is the chip select signal to select the Command Block Register. CH0__CS3# is the chip select signal to select the Control Block Register.
CH1__CS1#, CH1__CS3#	O	12 mA, Slew Rate Control	**CHANNEL 1 CHIP SELECT 1 AND 3.** CH1__CS1# is the chip select signal to select the Command Block Registers. CH1__CS3# is the chip select to select the Control Block Registers.
CH0__INT CH1__INT	I		**CHANNEL INTERRUPTS.** These signals are used to interrupt the host system. CH0__INT is asserted only when the drive(s) on channel 0 has a pending interrupt, and the host has cleared nIEN in the Device Control Register. CH1__INT is asserted only when the drive(s) on channel 1 has a pending interrupt, and the host has cleared nIEN in the Device Control Register.
ENABLE	I		**CHIP ENABLE PIN.** Logic low will disable this chip. If this pin is tied to Logic High or not connected then the chip is enabled.
HEADER	I		**HEADER PIN.** See page 13.
IRQ14	O/TRI-STATE	8 mA, Slew Rate Control	The output of this pin is equivalent to ISA IRQ14 if HEADER is ''not connected'' or Logic High. However, this pin will go to TRI-STATE if HEADER is tied to Logic low.
IRQ15	O/TRI-STATE	8 mA, Slew Rate Control	The output of this pin is equivalent to ISA IRQ15 if HEADER is ''Not connected'' or Logic High. However, this pin will go to TRI-STATE if HEADER is tied to Logic low.

Configuration Registers The configuration register map is shown in Table I.

TABLE I

Reg. # (in HEX)	R/W	Description
00	R	**VENDOR ID** (100Bh)
02–3	R	**DEVICE ID** (D001h)
04–5	R/W	**COMMAND REGISTER.** The command register provides coarse control over a device's ability to generate and respond to PCI cycles. bit 0—controls the response to the I/O space accesses specified in the Base Address Register. Default value is determined by the ENABLE pin. 1: Chip enable 0: Chip enable bit 6— allows the controller to detect parity errors on the PCI bus and report these errors to the system. 1: enable parity checking 0: disable parity checking (default) bit 8—allows the controller to detect system errors on the PCI bus and report these errors to the system. 1: enable system error checking 0: disable system error checking (default)
06	R/W	**STATUS REGISTER.** This register is used to record status information for PCI bus related events. ''Reads'' from this register behaves normally. However, ''write'' to this register is slightly different respect to the ordinary register. This register can be reset but not set. In order to reset this register, a logical High need to write to the corresponding bit. For details, please check P.156 of the PCI specification 2.0 (April 30, 1993). bit 9–10: These bit encode the timing of DEVSEL#. (read only) 00: fast 01: medium, Default bit 14: 1 means system error bit 15: This bit will be set by a device whenever that device detects a data parity error. This bit is disabled when parity error handling is disabled. A logical one means detection of parity error. Please check P. 157 of the PCI specification 2.0 (April 30, 1993).
Reg. # (in HEX)	**R/W**	**Description**
08	R	**REV. ID** (00h)
09	R	**PROGRAMMING INTERFACE,** default is 00h
0A	R	**SUB-CLASS CODE,** default is 01h (means IDE controller)
0B	R	**BASIC CLASS CODE,** default is 01h (means mass storage)
0C–0D		Not Used
0E	R	**HEADER TYPE,** default is 00h
10–13	R/W	**BASE ADDRESS REGISTERS 0.** For Primary IDE Data Control Ports (Default: 000001F0h–000001F7h) bit0: fixed to 1 bit1: fixed to 0 bit2: fixed to 0
14–17	R/W	**BASE ADDRESS REGISTERS 1.** For Primary IDE Control Status Ports (Default: 000003F6h) Note: only ''3F6'' byte is accessible bit0: fixed to 1 bit1: fixed to 0
18–1B	R/W	**BASE ADDRESS REGISTER 2.** For Secondary IDE Data Control Ports. (Default: 00000170h–0000177h) bit0: fixed to 1 bit1: fixed to 0 bit2: fixed to 0
1C–1F	R/W	**BASE ADDRESS REGISTER 3.** For Secondary IDE Control Status Ports. (Default: 00000376h) Note: only ''376'' byte is accessible bit0: fixed to 1 bit1: fixed to 0

Configuration Registers The configuration register map is shown in Table I. (Continued)

TABLE I (Continued)

Reg. # (in HEX)	R/W	Description
20–27		Not used.
3C	R/W	**INTERRUPT LINE,** default is 0Eh
3D	R	**INTERRUPT PIN** Default is 00h if HEADER pin is HIGH Default is 01h if HEADER pin is LOW
3E–3F		Not used
40		**IDE CHANNEL 0 TIMING CONTROL REGISTER.** This register is the cycle control register for 1F0h port. Default is set at B5H. **(Note 1)** bit 7, 6: address/chip select setup time 0 0 — 1 PCI clk 0 1 — 2 PCI clk 1 0 — 3 PCI clk (default) 1 1 — 4 PCI clk bit 5 4 3: address/chip select/write data hold time 0 0 0 — 1 PCI clk 0 0 1 — 2 PCI clk 0 1 0 — 3 PCI clk 0 1 1 — 4 PCI clk 1 0 0 — 5 PCI clk 1 0 1 — 6 PCI clk 1 1 0 — 8 PCI clk (default) 1 1 1 — 12 PCI clk bit 2 1 0: Command active time 0 0 0 — 2 PCI clk (**Note 3**) 0 0 1 — 3 PCI clk 0 1 0 — 4 PCI clk 0 1 1 — 5 PCI clk 1 0 0 — 6 PCI clk 1 0 1 — 8 PCI clk (default) 1 1 0 — 12 PCI clk 1 1 1 — 16 PCI clk
41	W/O	**IDE CHANNEL 0 READ—AHEAD COUNTER, LOW BYTE.** It provides values for loading bit0–bit7 of read—ahead counter. bit0: bit0 of the read—ahead counter bit1: bit1 of the read—ahead counter bit2: bit2 of the read—ahead counter bit3: bit3 of the read—ahead counter bit4: bit4 of the read—ahead counter bit5: bit5 of the read—ahead counter bit6: bit6 of the read—ahead counter bit7: bit7 of the read—ahead counter
42	Bit 7 is R/W, others are W/O	**IDE CHANNEL 9 READ__AHEAD COUNTER, HIGH BYTE.** It provides values for loading bit8–bit9 read__ahead counter. bit0: bit8 of the read—ahead counter bit1: bit9 of the read—ahead counter bit7: read—ahead function control 1: enable 0: disable (default)

Configuration Registers The configuration register map is shown in Table I. (Continued)

TABLE I (Continued)

Reg. # (in HEX)	R/W	Description
43		**IDE CHANNEL 0 FUNCTION REGISTER.** bit3: channel 0 I/O decode enable bit 1: enable (default) 0: disable bit2: IORDY0 function control 1: enable 0: disable (default) bit1: CH0__INT status (read only) 1: interrupt pending 0: no interrupt pending bit0: CH0__INT request to be masked or not 1: be masked 0: not be masked (default)
44		**IDE CHANNEL 1 TIMING CONTROL REGISTER.** This register is the cycle control register for 170h port. Default is set at B5h. **(Note 1)** bit 7, 6: address/chip select setup time 0 0 1 PCI clk 0 1 2 PCI clk 1 0 3 PCI clk (default) 1 1 4 PCI clk bit 5 4 3: address/chip select/write data hold time 0 0 0 1 PCI clk 0 0 1 2 PCI clk 0 1 0 3 PCI clk 0 1 1 4 PCI clk 1 0 0 5 PCI clk 1 0 1 6 PCI clk 1 1 0 8 PCI clk (default) 1 1 1 12 PCI clk bit 2 1 0: Command active time 0 0 0 2 PCI clk 0 0 1 3 PCI clk 0 1 0 4 PCI clk 0 1 1 5 PCI clk 1 0 0 6 PCI clk 1 0 1 8 PCI clk (default) 1 1 0 12 PCI clk 1 1 1 16 PCI clk
45	W/O	**IDE CHANNEL 1 READ—AHEAD COUNTER, LOW BYTE.** It provides values for loading bit0−bit7 of read__ahead counter. bit0: bit0 of the read__ahead counter bit1: bit1 of the read__ahead counter bit2: bit2 of the read__ahead counter bit3: bit3 of the read__ahead counter bit4: bit4 of the read__ahead counter bit5: bit5 of the read__ahead counter bit6: bit6 of the read__ahead counter bit7: bit7 of the read__ahead counter

Configuration Registers The configuration register map is shown in Table I. (Continued)

TABLE I (Continued)

Reg. # (in HEX)	R/W	Description
46	Bit 7 is R/W, others are W/O	**IDE CHANNEL 1 READ__AHEAD COUNTER, HIGH BYTE.** It provides values for loading bit8−bit9 of read__ahead counter bit0: bit8 of the read—ahead counter bit1: bit9 of the read—ahead counter bit7: read—ahead function control 1: enable 0: disable (default)
47		**IDE CHANNEL 1 FUNCTION REGISTER.** bit3: channel 1 I/O decode enable bit 1: enable (default) 0: disable bit2: IORDY1 function control 1: enable 0: disable (default) bit1: CH1—INT status (read only) 1: interrupt pending 0: no interrupt pending bit0: CH1—INT request to be masked or not 1: be masked 0: not be masked (default)
48		**PCI CONTROL REGISTER.** bit3: host posted write cycle timing select 1: min. 1 wait state (default) 0: min. 0 wait state (**Note 2**) bit2: active HDDRST# output active control 1: activate HDDRST#(default) 0: No action bit1: DEVSEL# timing select 1: medium (default) 0: fast bit0: Header for IDE support on PCI is present or not 1: present 0: absent, Default Values is determined by the ''Header Pin''.
49−4F		Not used.

Note 1: Total cycle time is calculated by adding setup time, hold time, and active time plus 1 clk.

Note 2: When 0 wait state is used then DEVSEL# timing select bit should be set to 0 (fast).

Note 3: If register 40 is 00, then IORDY0 should be disabled.
If register 44 is 00, then IORDY1 should be disabled.

Relation Table for INTA#, INTB#, IRQ14/15 with HEADER and channel I/O base registers

Condition	Outcome
When chip is disabled (HEADER is ''don't care'') and the setting of channel 0/1 I/O base register setting is ''don't care''	IRQ14: off IRQ15: off INTA#: off INTB#: off[16]
HEADER is absent (**Note 1**), chip is enabled and the setting of channel 0/1 I/O base register setting is ''don't care''	IRQ14: off IRQ15: off INTA#: inversion of CH0__INT, if CH0__INT is not masked by the bit0 of register 43h. Otherwise, it is at TRI-STATE. INTB#: inversion of CH1__INT, if CH1__INT is not masked by the bit0 of register 47h. Otherwise, it is at TRI-STATE.
HEADER is present, chip is enabled Channel 0 I/O is set at ''primary IDE port''	IRQ14: same value of CH0__INT, if CH0__INT is not masked by the bit0 of register 43h. Otherwise, it is at TRI-STATE.
HEADER is present, chip is enabled Channel 0 I/O is set at ''other I/O port''	INTA#: inversion of CH0__INT, if CH0__INT is not masked by the bit0 of register 43h. Otherwise, it is at TRI-STATE. IRQ14: off
HEADER is present, chip is enabled Channel 1 I/O is set at ''secondary IDE port''	IRQ15: same value of CH1__INT, if CH1__INT is not masked by the bit0 of register 47h. Otherwise, it is at TRI-STATE.
HEADER is present, chip is enabled Channel 1 I/O is set at ''other I/O port''	INTA#: inversion of CH1__INT, if CH1__INT is not masked by the bit0 of register 47h. Otherwise, it is at TRI-STATE. IRQ15: TRI-STATE
HEADER is present, chip is enabled Channel 0 is not primary port and Channel 1 is not secondary port	IRQ14: TRI-STATE IRQ15: TRI-STATE INTA#: Inversion of ORed value of CH0__INT and CH1__INT, if none of the CH0__INT and CH1__INT is masked by the bit0 of their respective registers. Otherwise, it is at TRI-STATE.

Note: INTB# is always at TRI-STATE when HEADER is present.

Note 1: HEADER absent means Logic Low.

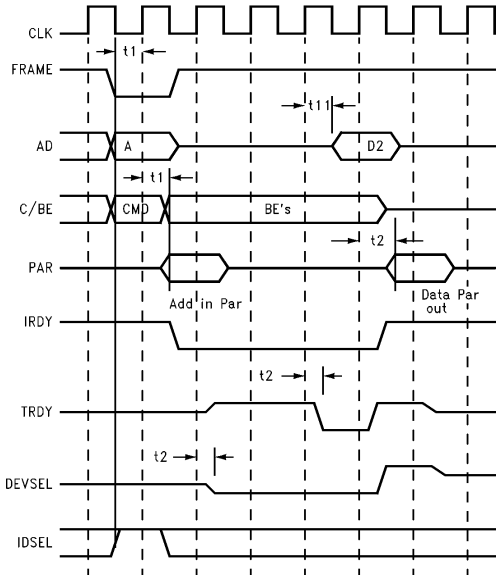
Timing Specification

Symbol	Parameter	Conditions	Min	Max	Units
t0	CLK period		30		ns
t1	PCI signals input setup time (Note)		7		ns
t2	PCI signals CLK to output valid		6	12	ns
t3	CLK to CHx__DA[2:0], CHx__CS1, 3#, CHx__IOR#, CHx__IOW#, IDE__D[15:0] valid		6	15	ns
t4	IORDYx setup time to CLK rising		6		ns
t5	IORDYx hold time from CLK rising		0		ns
t6	CHx__DA[2:0], CHx__CS1, 3# setup time to CHx__IOR#, CHx__IOW# falling		1	4	CLK
t7	CHx__IOR#, CHx__IOW# active pulse width		2	16	CLK
t8	CHx__DA[2:0], CHx__CS1, 3# hold time from CHx__IOR#, Chx__IOW# rising		1	12	CLK
t9	IDE__D[15:0] read data setup time to CLK rising		10		ns
t10	IDE__D[15:0] read data hold time from CLK rising		0		ns
t11	CLK to AD[31:0] read data valid delay		0	14	ns
t12	CHx__DA[2:0], CHx__CS1, 3# setup time to CHx__IOR#, CHx__IOW# falling (Non Data Cycle)		4	4	CLK
t13	CHx__DA[2:0], CHx__CS1, 3# hold time from CHx__IOR#, CHx__IOW# rising (Non Data Cycle)		5	6	CLK
t14	CHx__IOR#, CHx__IOW#, active pulse width (Non Data Cycle)		15	16	CLK

Note: If fast decode is enabled, the address setup time (t1 min) is 12 ns.

Timing Diagrams

Configuration Register Read Cycle



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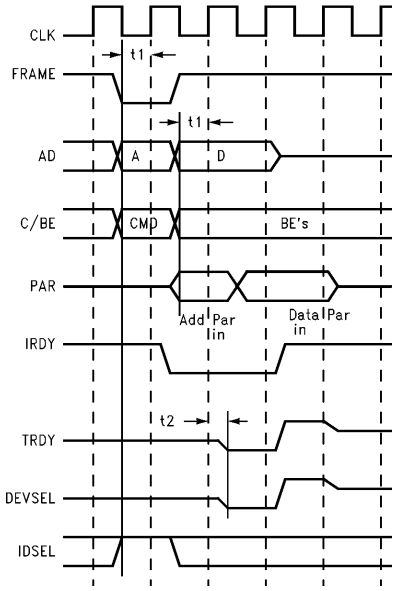
Configuration Register Write Cycle



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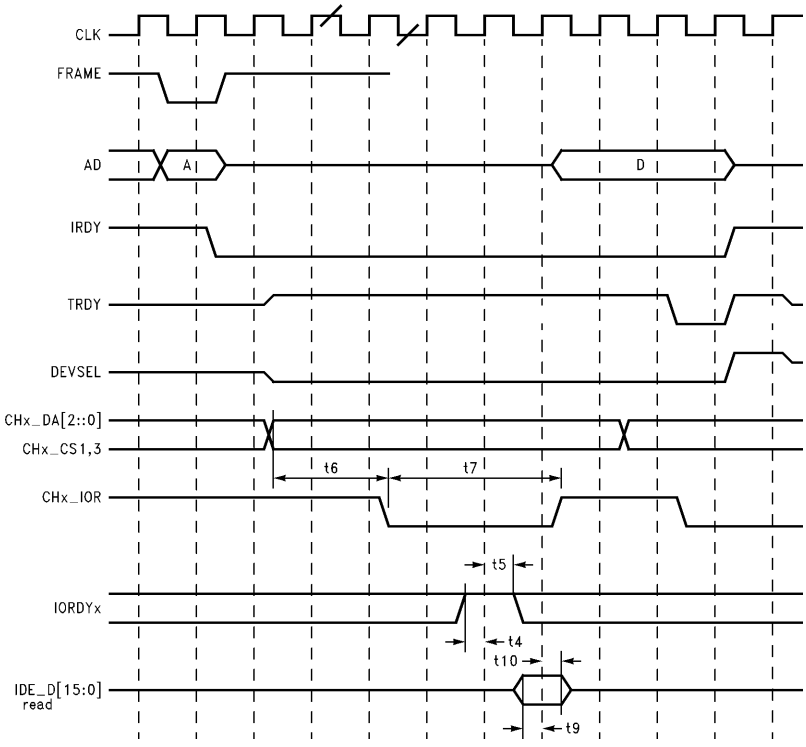
Read Ahead Cycles (Read Buffer Miss)



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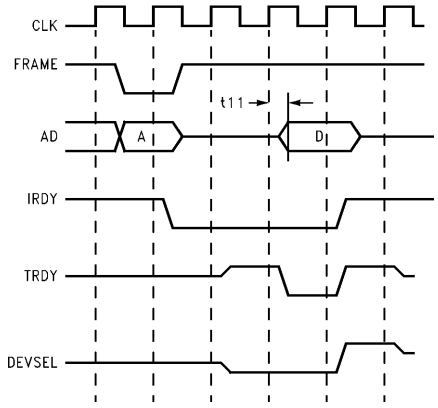
Timing Diagrams (Continued)

Read Ahead Cycles (read buffer hit)



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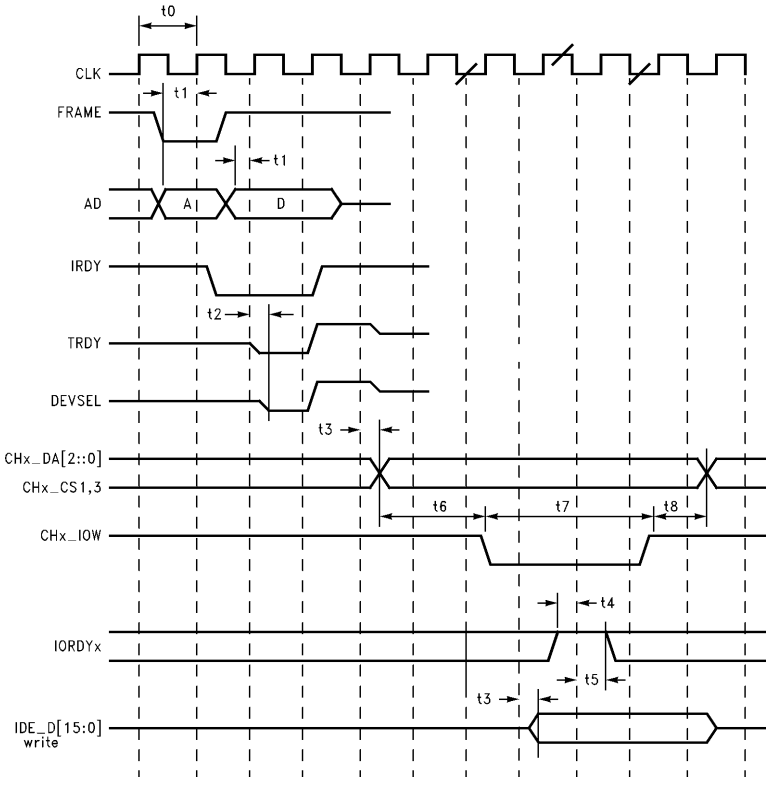
PCI Posted Write Cycles (medium decode)



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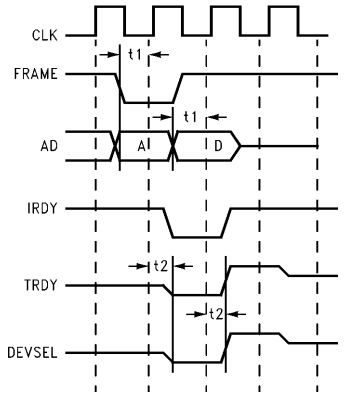
Timing Diagrams (Continued)

PCI Posted Write Cycles (fast decode)



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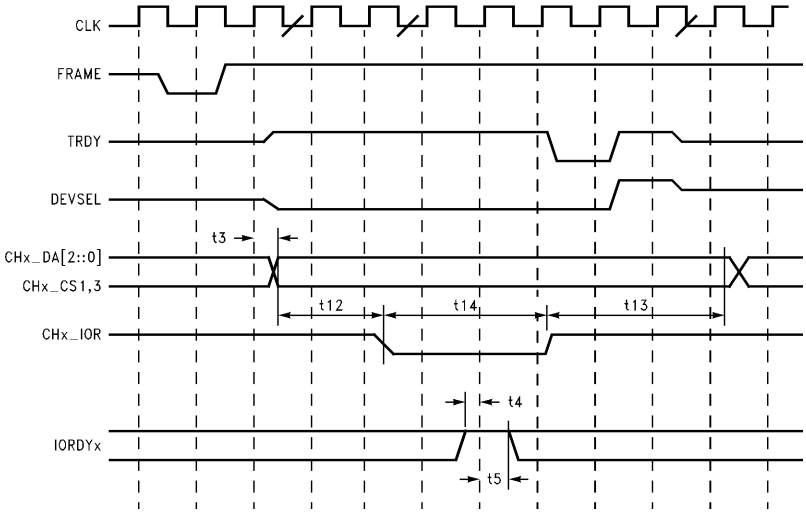
IDE Non Data Cycles (read or write)



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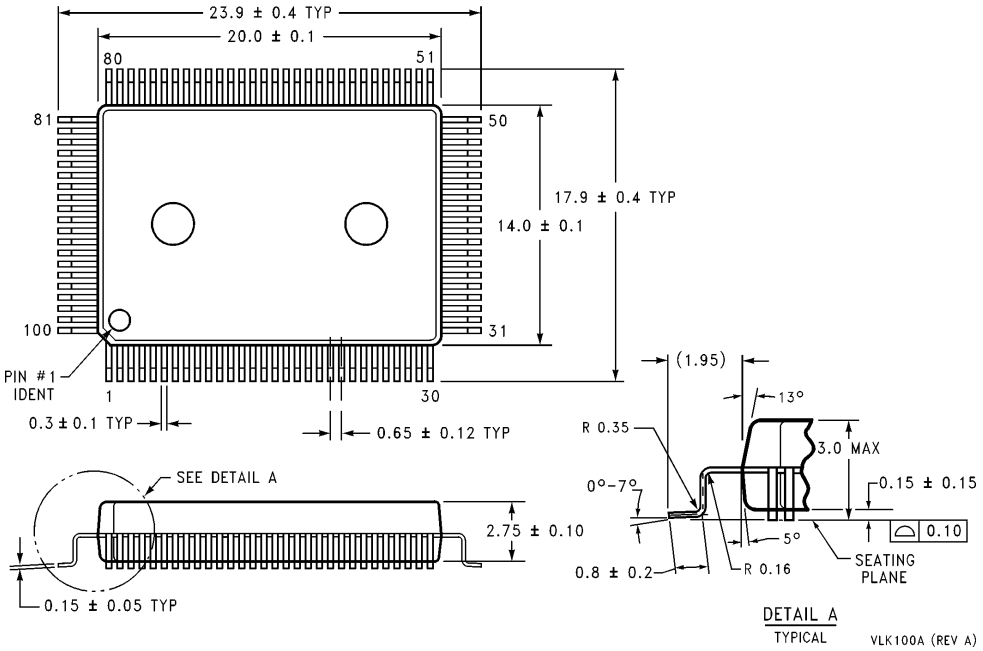
Physical Dimensions inches (millimeters)



100-Lead (14m x 20 mm) Molded Quad Flat Package, EIAJ
Order Number PC87410VLK
NS Package Number VLK100A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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