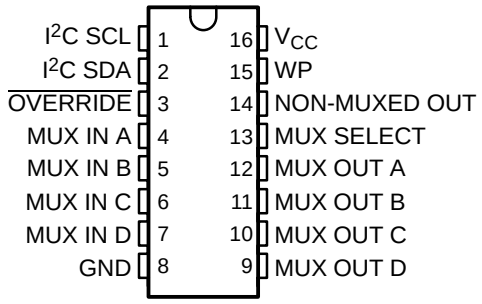
PCA8550
NONVOLATILE 5-BIT REGISTER WITH I²C INTERFACE

SCPS050C–MARCH 1999–REVISED MAY 2005

FEATURES

- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Useful for Jumperless Configuration of PC Motherboard**
- **Inputs Accept Voltages to 5.5 V**
- **MUX OUT Signals are 2.5-V Outputs**
- **NON-MUXED OUT Signal is a 3.3-V Output**
- **Minimum of 1000 Write Cycles**
- **Minimum of 10 Years Data Retention**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

D, DB, OR PW PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This 4-bit 1-of-2 multiplexer with I^2C input interface is designed for 3-V to 3.6-V V_{CC} operation.

The PCA8550 is designed to multiplex four bits of data from parallel inputs or from I^2C input data stored in a nonvolatile register. An additional bit of register output also is provided, which is latched to prevent changes in the output value during the write cycle. The factory default for the contents of the register is all low. These stored values can be read from, or written to, using the I^2C bus. The ability to control writing to the register is provided by the write protect (WP) input. The override ($\overline{\text{OVERRIDE}}$) input forces all the register outputs to a low.

This device provides a fast-mode (400 kbit/s) or standard-mode (100 kbit/s) I^2C serial interface for data input and output. The implementation is as a slave. The device address is specified in the I^2C interface definition table. Both of the I^2C Schmitt-trigger inputs (SCL and SDA) provide integrated pullup resistors and are 5-V tolerant.

The PCA8550 requires a monotonic power-supply ramp at start-up in the region of 1.1 V to 2.5 V. The nonvolatile registers and I^2C state machine initialize to their default states after this V_{CC} level is passed.

The PCA8550 is characterized for operation from 0°C to 70°C.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SOIC – D	Tube of 40	PCA8550D	PCA8550
		Reel of 2500	PCA8550DR	
	SSOP – DB	Reel of 2000	PCA8550DBR	
	TSSOP – PW	Reel of 2000	PCA8550PWR	

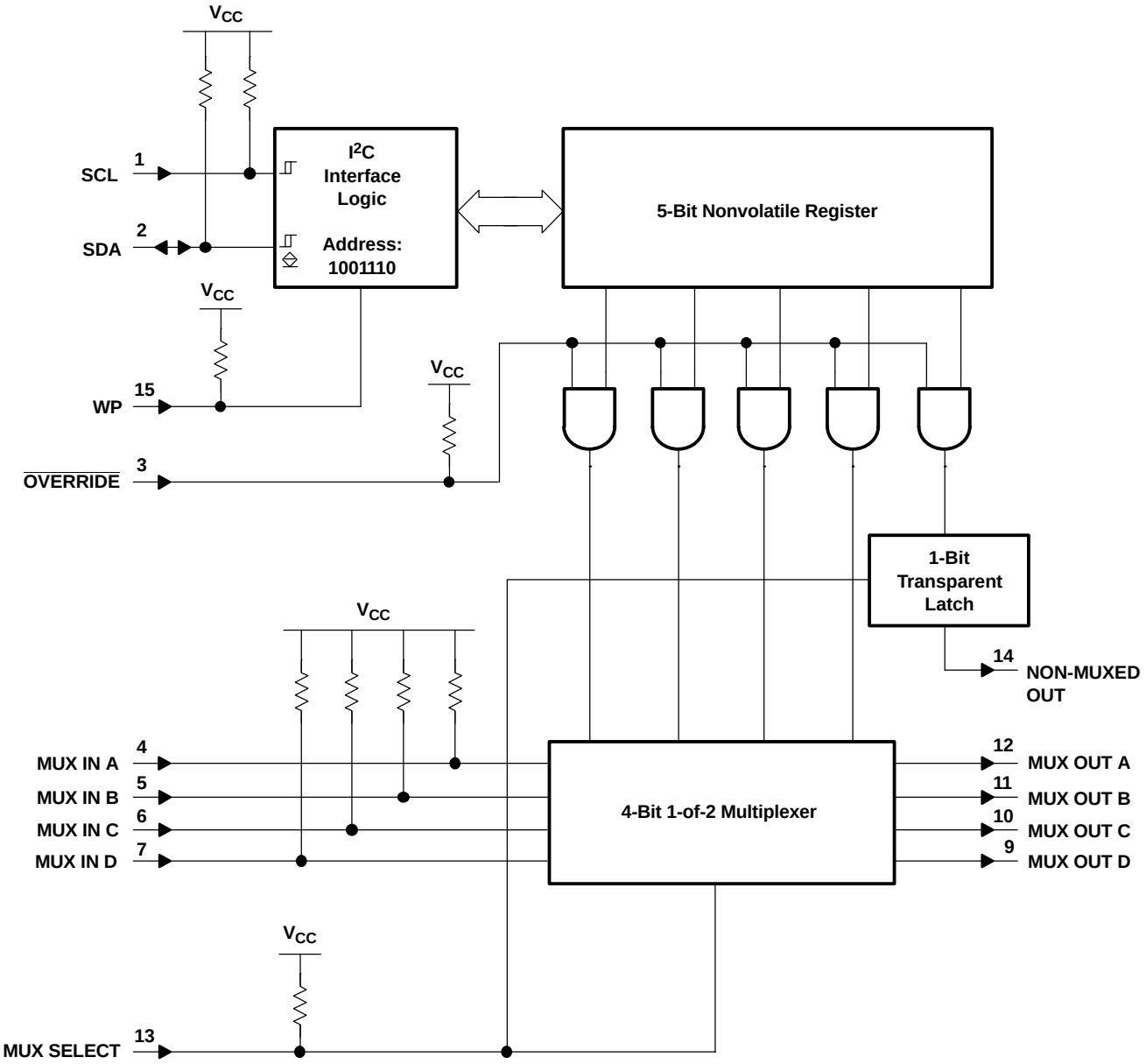
(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS		OUTPUTS	
MUX SELECT	$\overline{\text{OVERRIDE}}$	MUX OUT	NON-MUXED OUT
L	L	L	L
L	H	Nonvolatile register	Nonvolatile register
H	X	MUX IN	Latched NON-MUXED OUT (1)

(1) The latched NON-MUXED OUT state is the value present on the NON-MUXED OUT output at the time the MUX SELECT input transitions from the low to the high state.

LOGIC DIAGRAM (POSITIVE LOGIC)



I²C Interface

I²C communication with this device is initiated by a master sending a start condition, a high-to-low transition on the serial data (SDA) input/output while the serial clock (SCL) input is high. After the start condition, the device address byte is sent, MSB first, including the data-direction bit (R/$\overline{W}$). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an acknowledge, a low on the SDA input/output during the high of the acknowledge-related clock pulse.

The data byte follows the address acknowledge. If the R/$\overline{W}$ bit is high, the data from this device are the values read from the nonvolatile register. If the R/$\overline{W}$ bit is low, the data are from the master, to be written into the register. A valid data byte is one in which the three high-order bits are low. The first valid data byte that is received is written into the register, following the stop condition. If an invalid data byte is received, it is acknowledged, but is not written into the register. The data byte is followed by an acknowledge sent from this device. If other data bytes are sent from the master, following the acknowledge, they are ignored by this device.

A stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master. If the WP input is low during the falling edge of the first valid data byte acknowledge on the SCL input and the R/$\overline{W}$ bit is low, the stop condition causes the I²C interface logic to write the data byte value into the nonvolatile register. Data are written only if complete bytes are received and acknowledged. Writing to the register takes time (t_{wr}), during which the device does not respond to its slave address. If the WP input is high, the I²C interface logic does not write to the register.

I²C Interface Definition Table

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Address	H	L	L	H	H	H	L	R/$\overline{W}$
Data	L	L	L	NON-MUXED OUT	MUX OUT D	MUX OUT C	MUX OUT B	MUX OUT A

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range(2)		–0.5	6.5	V
V_O	Output voltage range	SDA(2)	–0.5	6.5	V
		MUX OUT outputs(2)	–0.5	2.9	
		NON-MUXED OUT output(2)(3)	–0.5	V_{CC} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{CC}(3)		–50, +10	mA
I_{IOK}	Input/output clamp current	V_O < 0		–50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}(3)		±15	mA
	Continuous current through V_{CC} or GND			±30	mA
θ_{JA}	Package thermal impedance(4)	D package		113	°C/W
		DB package		131	
		PW package		149	
T_{stg}	Storage temperature range		–65	85	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the recommended operating conditions table.
(4) The package thermal impedance is calculated in accordance with JESD 51.

Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3	3.6	V
V_{IH}	High-level input voltage	SCL, SDA	2.7	4	V
		$\overline{\text{OVERRIDE}}$, MUX IN, MUX SELECT, WP	2	4	
V_{IL}	Low-level input voltage	SCL, SDA	–0.5	0.9	V
		$\overline{\text{OVERRIDE}}$, MUX IN, MUX SELECT, WP	–0.5	0.8	
I_{OH}	High-level output current	MUX OUT, NON-MUXED OUT		–2	mA
I_{OL}	Low-level output current	SDA		6	mA
		MUX OUT, NON-MUXED OUT		2	
$\Delta t/\Delta v$	Input transition rise or fall rate	$\overline{\text{OVERRIDE}}$, MUX IN, MUX SELECT, WP		10	ns/V
T_A	Operating free-air temperature		0	70	°C

Electrical Characteristics

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I = –18 mA	–1.5		V
V_{hys} (1)	SCL, SDA		0.19		V
V_{OH}	MUX OUT	I_{OH} = –100 µA	2	2.625	V
		I_{OH} = –1 mA	1.7	2.625	
	NON-MUXED OUT	I_{OH} = –100 µA	2.4	3.6	
		I_{OH} = –2 mA	2	3.6	
V_{OL}	MUX OUT	I_{OL} = 100 µA	–0.3	0.4	V
		I_{OL} = 2 mA	–0.3	0.7	
	NON-MUXED OUT	I_{OL} = 100 µA	–0.5	0.4	
		I_{OL} = 2 mA	–0.5	0.7	
	SDA	I_{OL} = 3 mA		0.4	
		I_{OL} = 6 mA		0.6	
I_{IH}	SCL, SDA	V_{IH} = 2.4 V	–1.5	–12	µA
	$\overline{\text{OVERRIDE}}$, MUX SELECT, WP		–20	–100	
	MUX IN		–0.166	–0.75	mA
I_{IL}	SCL, SDA	V_{IL} = 0.4 V	–7	–32	µA
	$\overline{\text{OVERRIDE}}$, MUX SELECT, WP		–86	–267	
	MUX IN		–0.72	–2	mA
I_{CC}	During read or write cycle	V_I = 0 to V_{CC}, I_O = 0, V_{CC} = 3.3 V		10	mA
	Not during read or write cycle	V_I = V_{CC}, I_O = 0		500	µA
C_i		V_I = V_{CC} or GND		10	pF

(1) V_{hys} is the hysteresis of Schmitt-trigger inputs.

Nonvolatile Storage Specifications

PARAMETER	SPECIFICATIONS
Write time (t_{wr})	10 ms, typical
Memory-cell data retention	10 years, minimum
Maximum number of memory-cell write cycles	1000 cycles, minimum

I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V_{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	
f_{scl}	I²C clock frequency	10	400	kHz
t_{sch}	I²C clock high time	600		ns
t_{scl}	I²C clock low time	1.3		µs
t_{sp}	I²C spike time	0	50	ns
t_{sds}	I²C serial data setup time	100		ns
t_{sdh}	I²C serial data hold time	0	900	ns
t_{icr}	I²C input rise time	20	300	ns
t_{icf}	I²C input fall time	20	300	ns
t_{ocf}	I²C output fall time (10-pF to 400-pF bus)	20 + 0.1 C_b (1)	250	ns
t_{buf}	I²C bus free time between stop and start	1.3		µs
t_{sts}	I²C start or repeated start condition setup	600		ns
t_{sth}	I²C start or repeated start condition hold	600		ns
t_{sps}	I²C stop condition setup	600		ns
C_b (1)	I²C bus capacitive load		400	pF

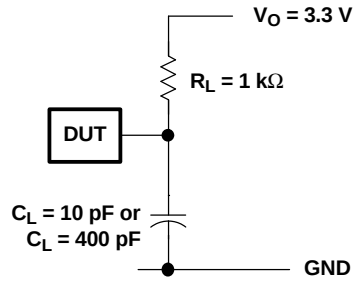
(1) C_b = capacitance of one bus line in pF

Switching Characteristics

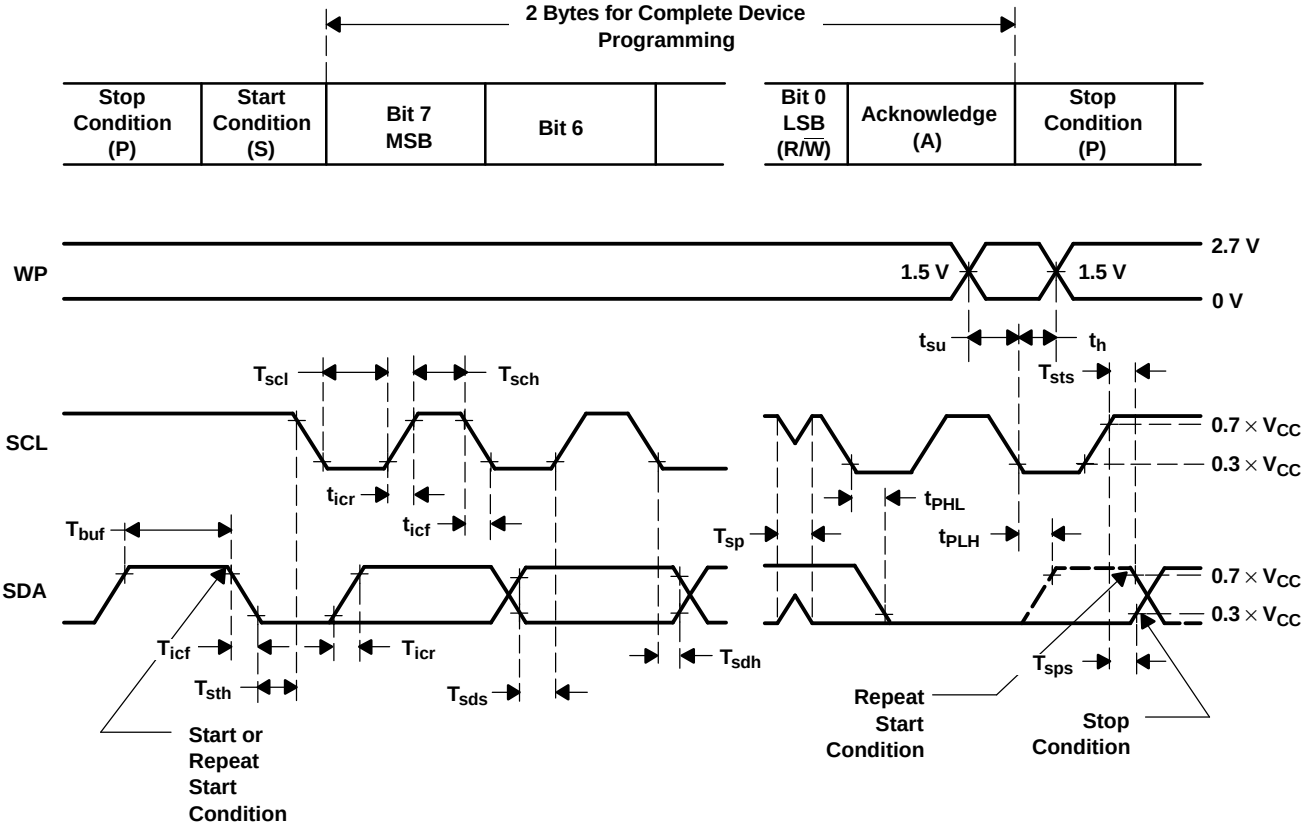
over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	
t_{mpd}	Mux input to output propagation delay	MUX IN	MUX OUT		20	ns
t_{sov}	MUX SELECT to output valid	MUX SELECT	Output valid		22	ns
t_{ovn}	$\overline{\text{OVERRIDE}}$ to NON-MUXED OUT output delay	$\overline{\text{OVERRIDE}}$	NON-MUXED OUT		15	ns
t_{ovm}	$\overline{\text{OVERRIDE}}$ to MUX OUT output delay	$\overline{\text{OVERRIDE}}$	MUX OUT		25	ns
t_{su}	Setup time	WP	Falling edge of first valid data byte acknowledge on the SCL input	30		ns
t_h	Hold time	WP	Falling edge of first valid data byte acknowledge on the SCL input	120		ns
t_r	Output rise time			1	3	ns/V
t_f	Output fall time			1	3	ns/V

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

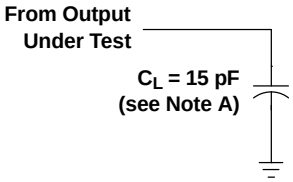


VOLTAGE WAVEFORMS

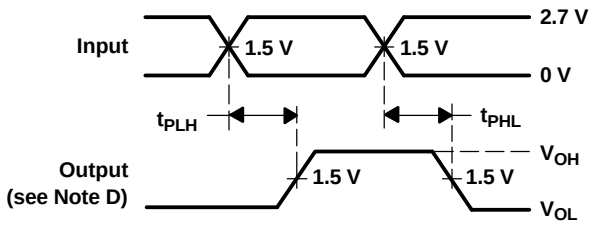
BYTE	DESCRIPTION
1	I²C address
2	Nonvolatile register data

Figure 1. I²C Interface Load Circuit and Voltage Waveforms

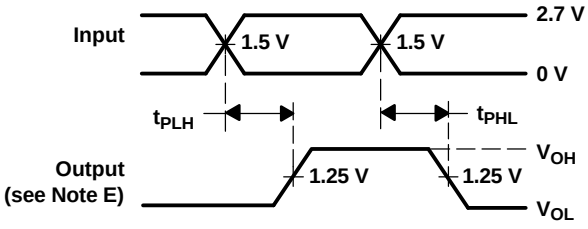
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
FOR NON-MUXED OUT OUTPUT



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
FOR MUXED OUT OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{sov} and t_{ovn}.
E. t_{PLH} and t_{PHL} are the same as t_{mpd}, t_{sov}, and t_{ovm}.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

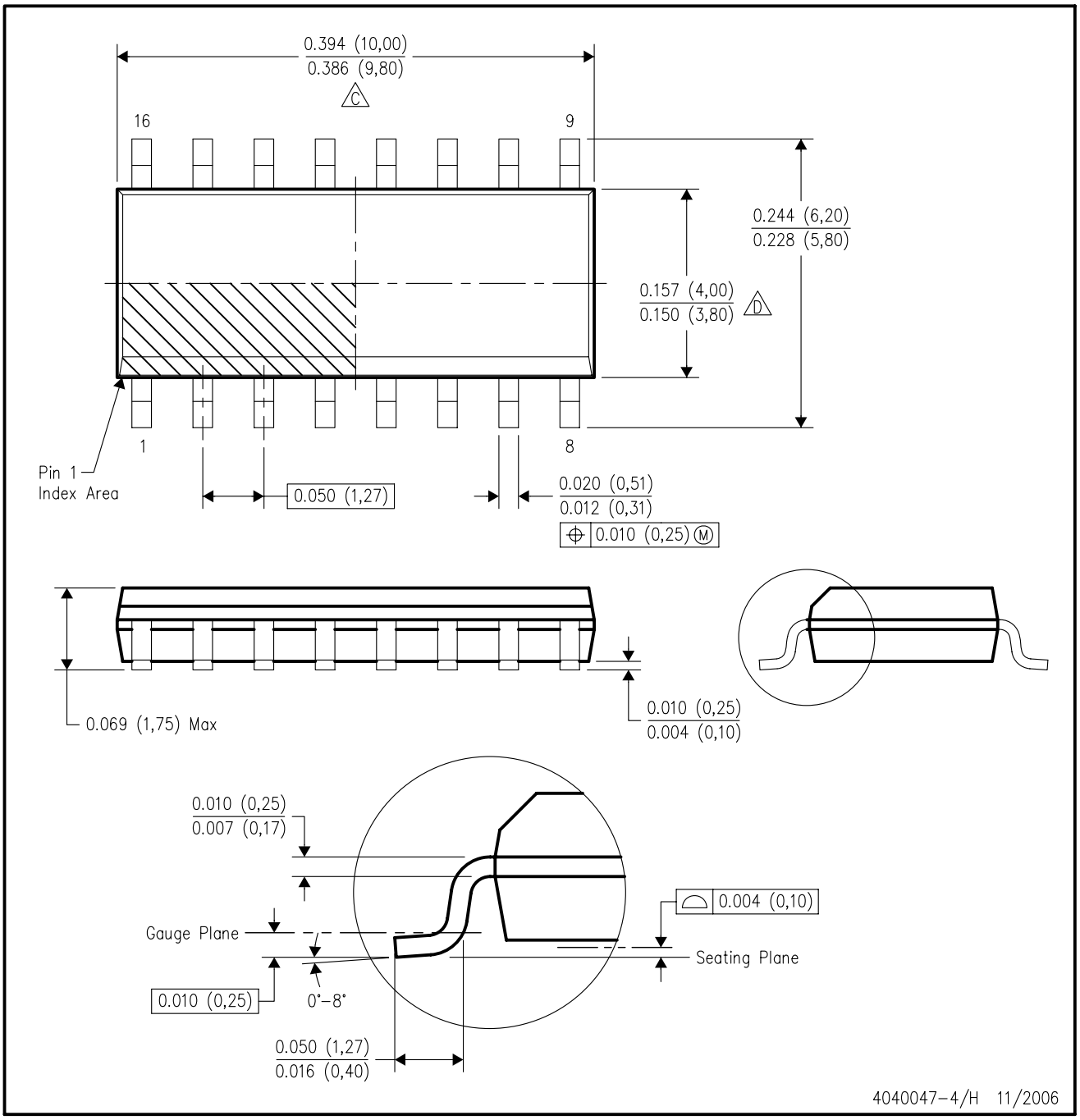
Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
PCA8550D	ACTIVE	SOIC	D	16		TBD	Call TI	Call TI
PCA8550DBR	ACTIVE	SSOP	DB	16		TBD	Call TI	Call TI
PCA8550DBRE4	ACTIVE	SSOP	DB	16		TBD	Call TI	Call TI
PCA8550DE4	ACTIVE	SOIC	D	16		TBD	Call TI	Call TI
PCA8550DR	ACTIVE	SOIC	D	16		TBD	Call TI	Call TI
PCA8550DRE4	ACTIVE	SOIC	D	16		TBD	Call TI	Call TI
PCA8550PWR	ACTIVE	TSSOP	PW	16		TBD	Call TI	Call TI
PCA8550PWRE4	ACTIVE	TSSOP	PW	16		TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AC.

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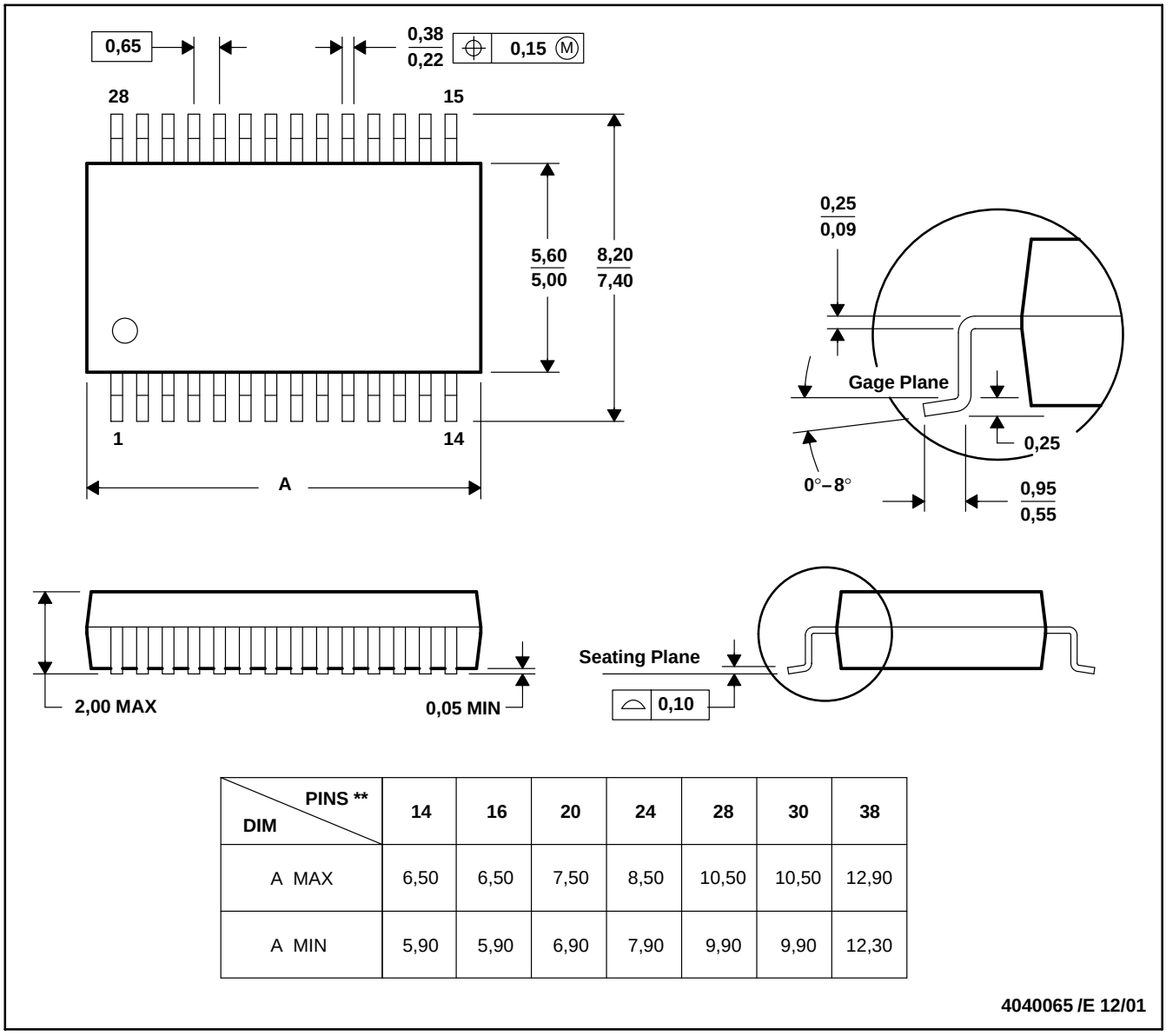
DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



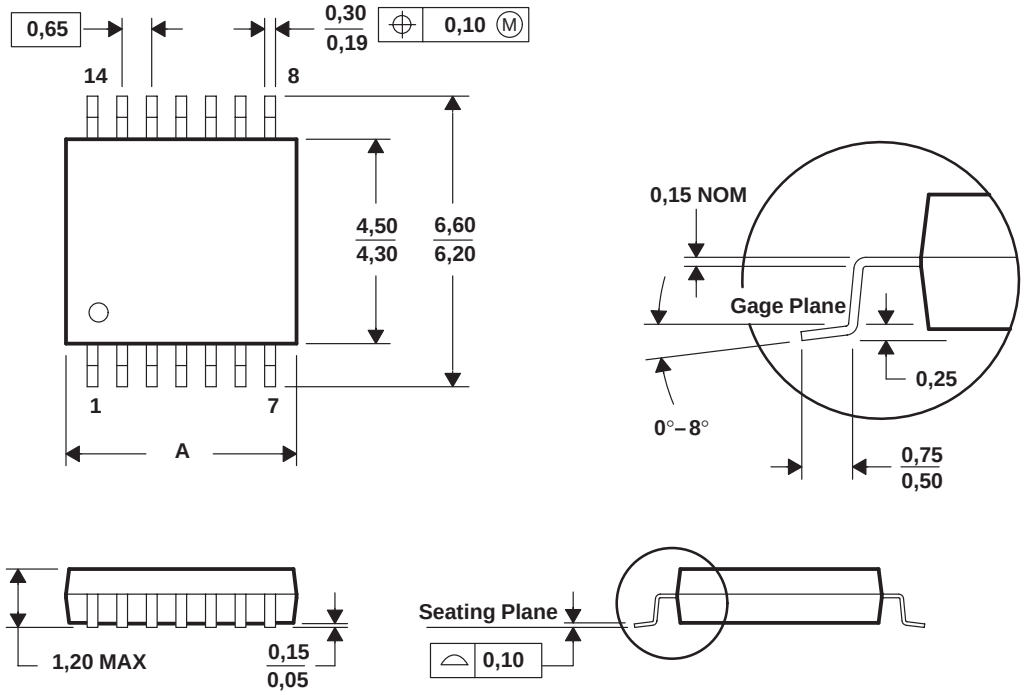
DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
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D. Falls within JEDEC MO-153

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