



PCA9545A

4-channel I²C switch with interrupt logic and reset

Rev. 03 — 3 March 2005

Product data sheet

1. General description

The PCA9545A is a quad bi-directional translating switch controlled via the I²C-bus. The SCL/SDA upstream pair fans out to four downstream pairs, or channels. Any individual SCx/SDx channel or combination of channels can be selected, determined by the contents of the programmable control register. Four interrupt inputs, $\overline{INT0}$ to $\overline{INT3}$, one for each of the downstream pairs, are provided. One interrupt output, \overline{INT} , acts as an AND of the four interrupt inputs.

An active LOW reset input allows the PCA9545A to recover from a situation where one of the downstream I²C-buses is stuck in a LOW state. Pulling the \overline{RESET} pin LOW resets the I²C-bus state machine and causes all the channels to be deselected as does the internal Power-on reset function.

The pass gates of the switches are constructed such that the V_{DD} pin can be used to limit the maximum high voltage which will be passed by the PCA9545A. This allows the use of different bus voltages on each pair, so that 1.8 V or 2.5 V or 3.3 V parts can communicate with 5 V parts without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5 V tolerant.

2. Features

- 1-of-4 bi-directional translating switches
- I²C-bus interface logic; compatible with SMBus standards
- 4 active LOW interrupt inputs
- Active LOW interrupt output
- Active LOW reset input
- 2 address pins allowing up to 4 devices on the I²C-bus
- Channel selection via I²C-bus, in any combination
- Power-up with all switch channels deselected
- Low R_{on} switches
- Allows voltage level translation between 1.8 V, 2.5 V, 3.3 V and 5 V buses
- No glitch on power-up
- Supports hot insertion
- Low stand-by current
- Operating power supply voltage range of 2.3 V to 5.5 V
- 5 V tolerant Inputs
- 0 kHz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up protection exceeds 100 mA per JESD78

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- Three packages offered: SO20, TSSOP20, and HVQFN20

3. Ordering information

Table 1: Ordering information

$T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$

Type number	Package		
	Name	Description	Version
PCA9545ABS	HVQFN20	plastic thermal enhanced very thin quad flat package; no leads; 20 terminals; body $5 \times 5 \times 0.85$ mm	SOT662-1
PCA9545AD	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
PCA9545APW	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

Standard packing quantities and other packaging data are available at www.standardproducts.philips.com/packaging.

4. Marking

Table 2: Marking codes

Type number	Topside mark
PCA9545ABS	9545A
PCA9545AD	PCA9545AD
PCA9545APW	PA9545A

5. Block diagram

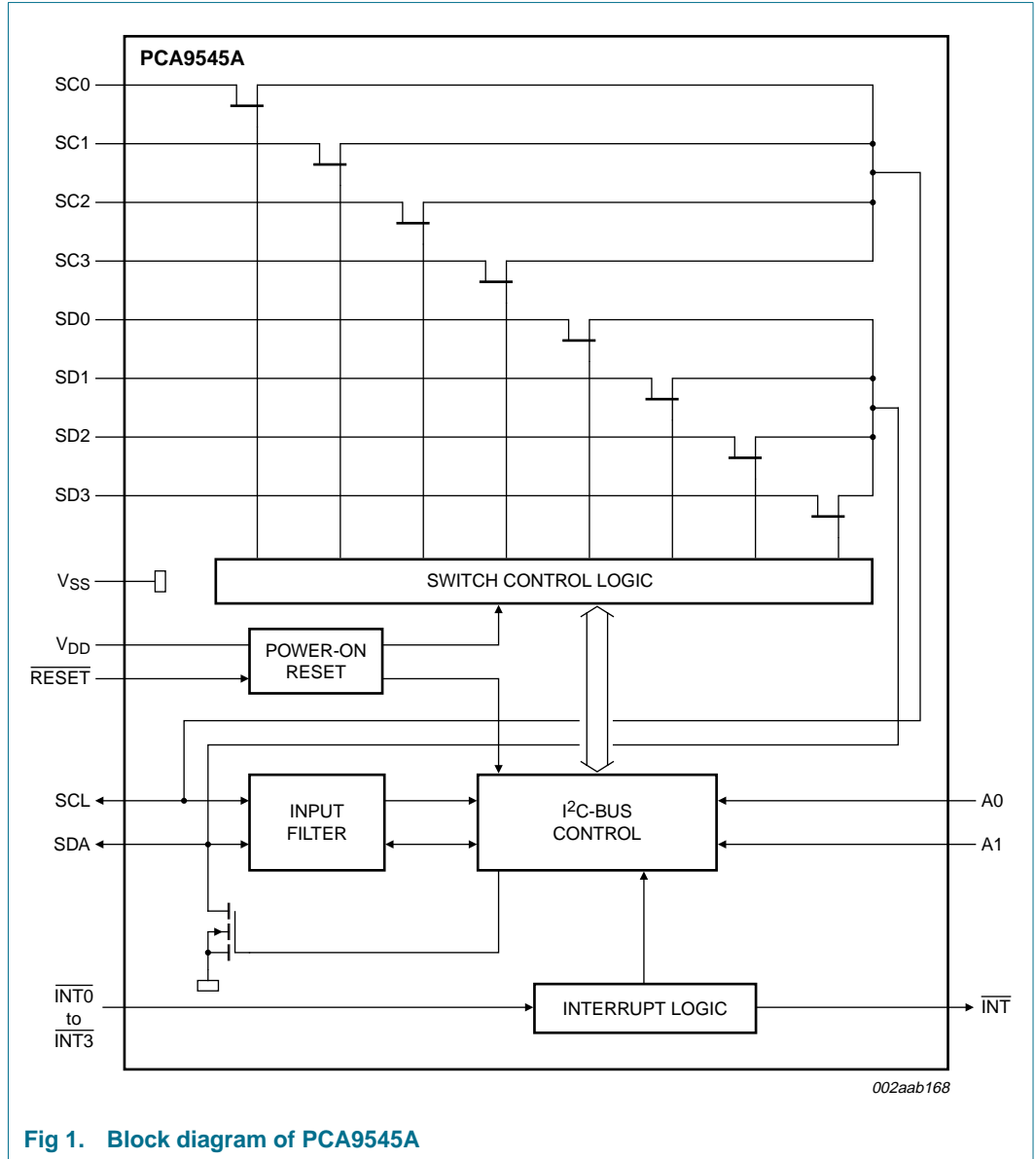
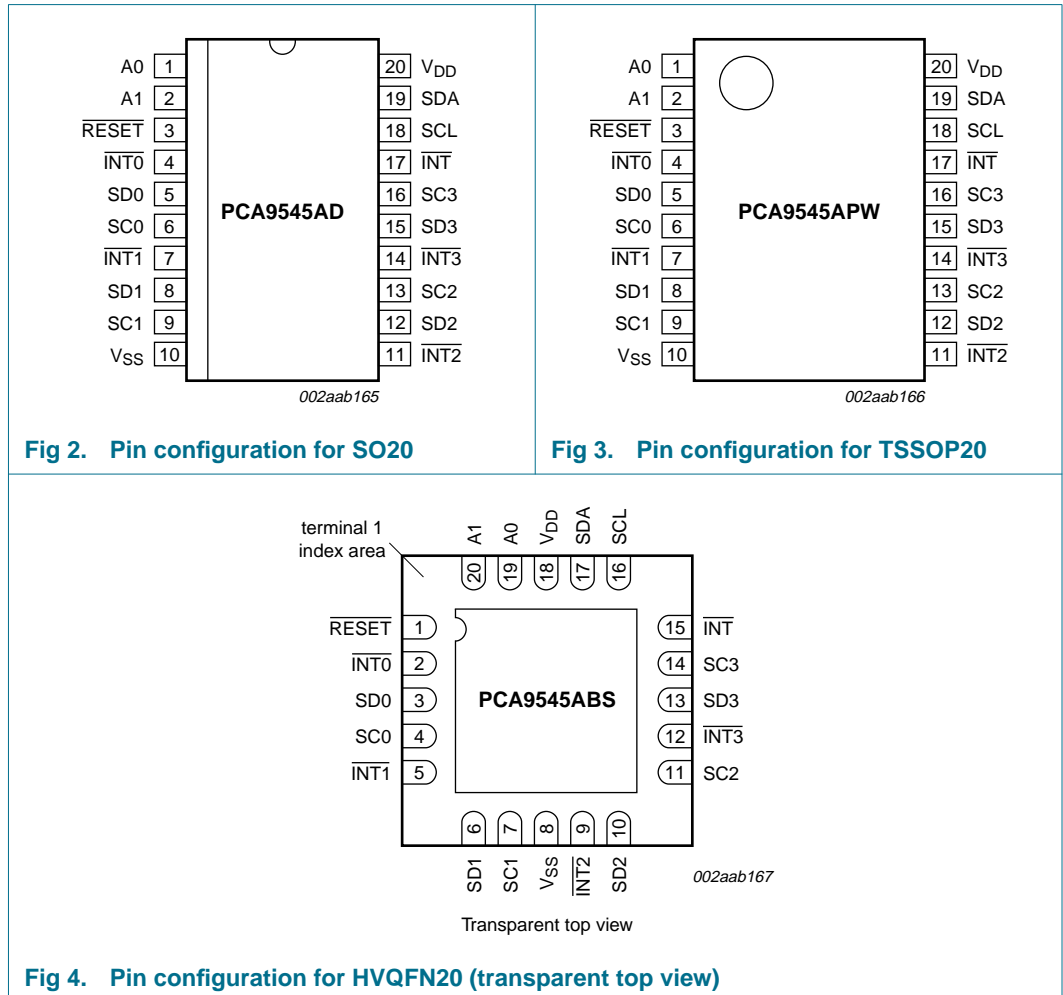


Fig 1. Block diagram of PCA9545A

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3: Pin description

Symbol	Pin		Description
	SO, TSSOP	HVQFN	
A0	1	19	address input 0
A1	2	20	address input 1
RESET	3	1	active LOW reset input
INT0	4	2	active LOW interrupt input 0
SD0	5	3	serial data 0
SC0	6	4	serial clock 0
INT1	7	5	active LOW interrupt input 1
SD1	8	6	serial data 1

Table 3: Pin description ...continued

Symbol	Pin		Description
	SO, TSSOP	HVQFN	
SC1	9	7	serial clock 1
V _{SS}	10	8 [1]	supply ground
$\overline{\text{INT}}2$	11	9	active LOW interrupt input 2
SD2	12	10	serial data 2
SC2	13	11	serial clock 2
$\overline{\text{INT}}3$	14	12	active LOW interrupt input 3
SD3	15	13	serial data 3
SC3	16	14	serial clock 3
$\overline{\text{INT}}$	17	15	active LOW interrupt output
SCL	18	16	serial clock line
SDA	19	17	serial data line
V _{DD}	20	18	supply voltage

[1] HVQFN package die supply ground is connected to both the V_{SS} pin and the exposed center pad. The V_{SS} pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias need to be incorporated in the PCB in the thermal pad region.

7. Functional description

Refer to [Figure 1 “Block diagram of PCA9545A” on page 3](#).

7.1 Device address

Following a START condition, the bus master must output the address of the slave it is accessing. The address of the PCA9545A is shown in [Figure 5](#). To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

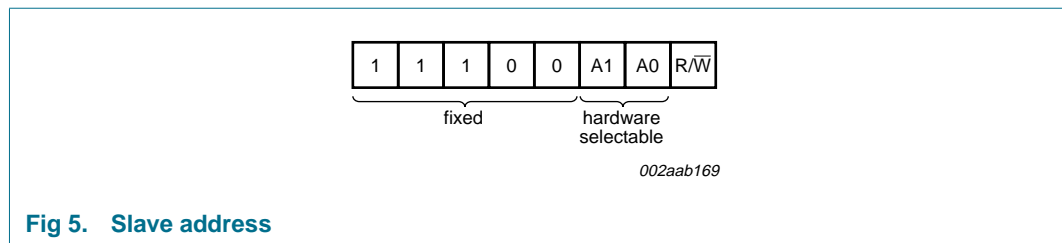


Fig 5. Slave address

The last bit of the slave address defines the operation to be performed. When set to logic 1, a read is selected while a logic 0 selects a write operation.

7.2 Control register

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9545A, which will be stored in the control register. If multiple bytes are received by the PCA9545A, it will save the last byte received. This register can be written and read via the I²C-bus.

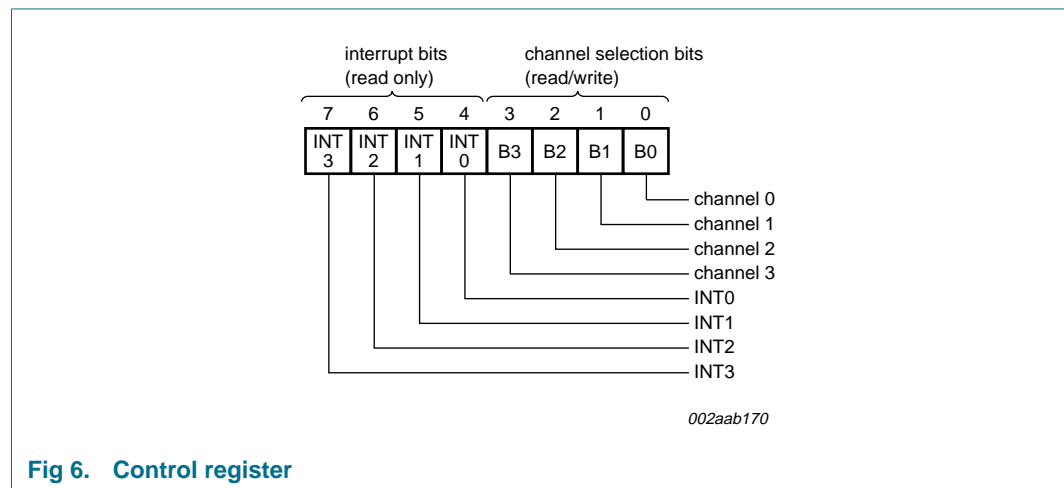


Fig 6. Control register

7.2.1 Control register definition

One or several SCx/SDx downstream pair, or channel, is selected by the contents of the control register. This register is written after the PCA9545A has been addressed. The 4 LSBs of the control byte are used to determine which channel is to be selected. When a channel is selected, the channel will become active after a STOP condition has been placed on the I²C-bus. This ensures that all SCx/SDx lines will be in a HIGH state when the channel is made active, so that no false conditions are generated at the time of connection.

Table 4: Control register: Write—channel selection; Read—channel status

INT3	INT2	INT1	INT0	B3	B2	B1	B0	Command
X	X	X	X	X	X	X	0	channel 0 disabled
							1	channel 0 enabled
X	X	X	X	X	X	0	X	channel 1 disabled
						1		channel 1 enabled
X	X	X	X	X	0	X	X	channel 2 disabled
					1			channel 2 enabled
X	X	X	X	0	X	X	X	channel 3 disabled
				1				channel 3 enabled
0	0	0	0	0	0	0	0	no channel selected; power-up/reset default state

Remark: Several channels can be enabled at the same time. Example: B3 = 0, B2 = 1, B1 = 1, B0 = 0, means that channel 0 and channel 3 are disabled and channel 1 and channel 2 are enabled. Care should be taken not to exceed the maximum bus capacity.

7.2.2 Interrupt handling

The PCA9545A provides 4 interrupt inputs, one for each channel, and one open-drain interrupt output. When an interrupt is generated by any device, it will be detected by the PCA9545A and the interrupt output will be driven LOW. The channel does not need to be active for detection of the interrupt. A bit is also set in the control register.

Bit 4 through bit 7 of the control register corresponds to channel 0 through channel 3 of the PCA9545A, respectively. Therefore, if an interrupt is generated by any device connected to channel 1, the state of the interrupt inputs is loaded into the control register when a read is accomplished. Likewise, an interrupt on any device connected to channel 0 would cause bit 4 of the control register to be set on the read. The master can then address the PCA9545A and read the contents of the control register to determine which channel contains the device generating the interrupt. The master can then reconfigure the PCA9545A to select this channel, and locate the device generating the interrupt and clear it.

It should be noted that more than one device can provide an interrupt on a channel, so it is up to the master to ensure that all devices on a channel are interrogated for an interrupt.

The interrupt inputs may be used as general purpose inputs if the interrupt function is not required.

If unused, interrupt input(s) must be connected to V_{DD} through a pull-up resistor.

Table 5: Control register: Read—interrupt

INT3	INT2	INT1	INT0	B3	B2	B1	B0	Command
X	X	X	$\begin{matrix} 0 \\ 1 \end{matrix}$	X	X	X	X	$\begin{matrix} \text{no interrupt on channel 0} \\ \text{interrupt on channel 0} \end{matrix}$
X	X	$\begin{matrix} 0 \\ 1 \end{matrix}$	X	X	X	X	X	$\begin{matrix} \text{no interrupt on channel 1} \\ \text{interrupt on channel 1} \end{matrix}$
X	$\begin{matrix} 0 \\ 1 \end{matrix}$	X	X	X	X	X	X	$\begin{matrix} \text{no interrupt on channel 2} \\ \text{interrupt on channel 2} \end{matrix}$
$\begin{matrix} 0 \\ 1 \end{matrix}$	X	X	X	X	X	X	X	$\begin{matrix} \text{no interrupt on channel 3} \\ \text{interrupt on channel 3} \end{matrix}$

Remark: Several interrupts can be active at the same time. Example: INT3 = 0, INT2 = 1, INT1 = 1, INT0 = 0, means that there is no interrupt on channel 0 and channel 3, and there is interrupt on channel 1 and channel 2.

7.3 RESET input

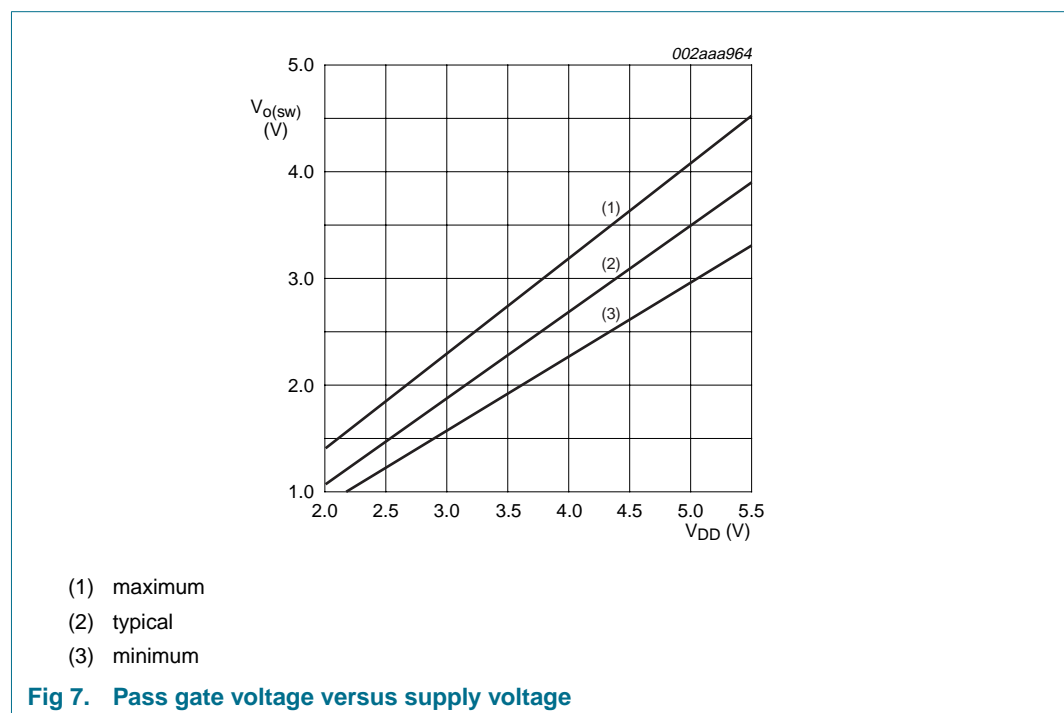
The $\overline{\text{RESET}}$ input is an active LOW signal which may be used to recover from a bus fault condition. By asserting this signal LOW for a minimum of t_{WL} , the PCA9545A will reset its registers and I²C-bus state machine and will deselect all channels. The $\overline{\text{RESET}}$ input must be connected to V_{DD} through a pull-up resistor.

7.4 Power-On Reset

When power is applied to V_{DD} , an internal Power-On Reset (POR) holds the PCA9545A in a reset condition until V_{DD} has reached V_{POR} . At this point, the reset condition is released and the PCA9545A registers and I²C-bus state machine are initialized to their default states—all zeroes—causing all the channels to be deselected. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

7.5 Voltage translation

The pass gate transistors of the PCA9545A are constructed such that the V_{DD} voltage can be used to limit the maximum voltage that will be passed from one I²C-bus to another.



[Figure 7](#) shows the voltage characteristics of the pass gate transistors (note that the graph was generated using the data specified in [Section 11 “Static characteristics”](#) of this data sheet). In order for the PCA9545A to act as a voltage translator, the $V_{O(sw)}$ voltage should be equal to, or lower than the lowest bus voltage. For example, if the main bus was running at 5 V, and the downstream buses were 3.3 V and 2.7 V, then $V_{O(sw)}$ should be equal to or below 2.7 V to effectively clamp the downstream bus voltages. Looking at [Figure 7](#), we see that $V_{O(sw)(max)}$ will be at 2.7 V when the PCA9545A supply voltage is 3.5 V or lower, so the PCA9545A supply voltage could be set to 3.3 V. Pull-up resistors can then be used to bring the bus voltages to their appropriate levels (see [Figure 14](#)).

More Information can be found in Application Note *AN262: PCA954X family of I²C/SMBus multiplexers and switches*.

8. Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see [Figure 8](#)).

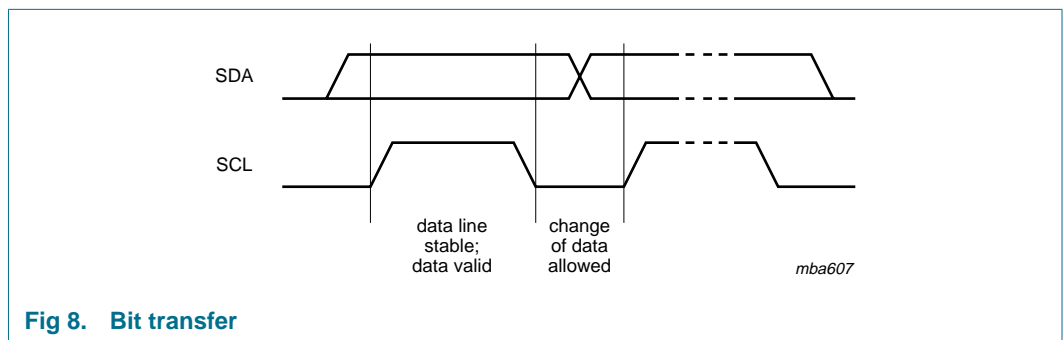


Fig 8. Bit transfer

8.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see [Figure 9](#)).

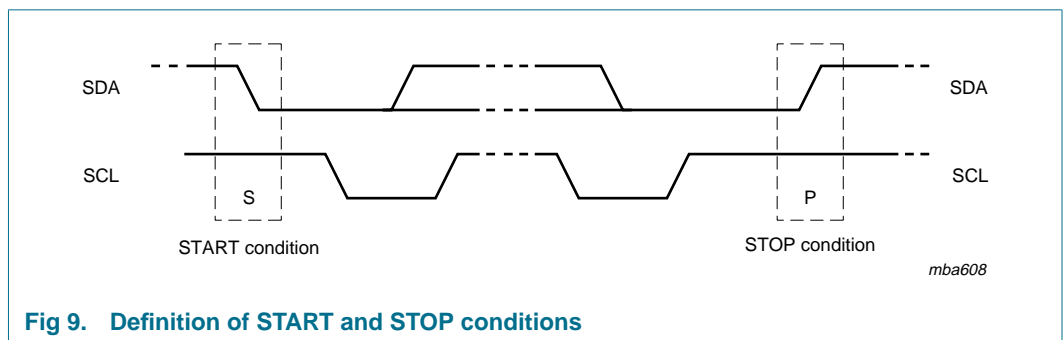


Fig 9. Definition of START and STOP conditions

8.3 System configuration

A device generating a message is a 'transmitter', a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see [Figure 10](#)).

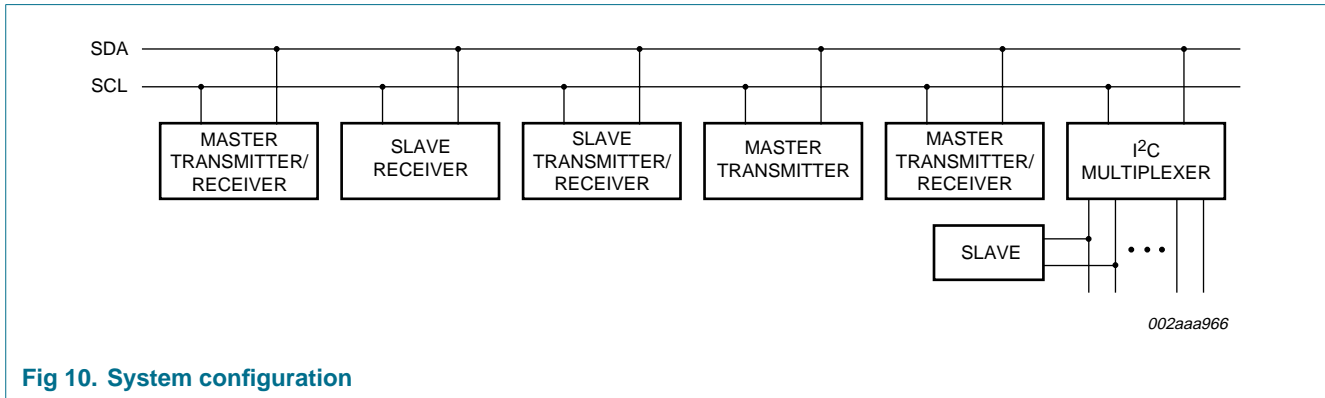


Fig 10. System configuration

8.4 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; setup and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

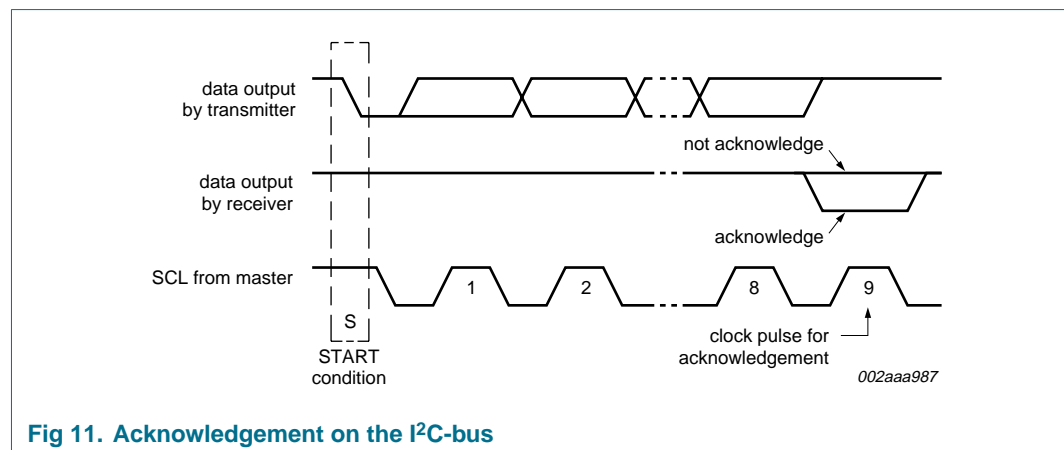


Fig 11. Acknowledgement on the I²C-bus

8.5 Bus transactions

Data is transmitted to the PCA9545A control register using the Write mode as shown in [Figure 12](#).

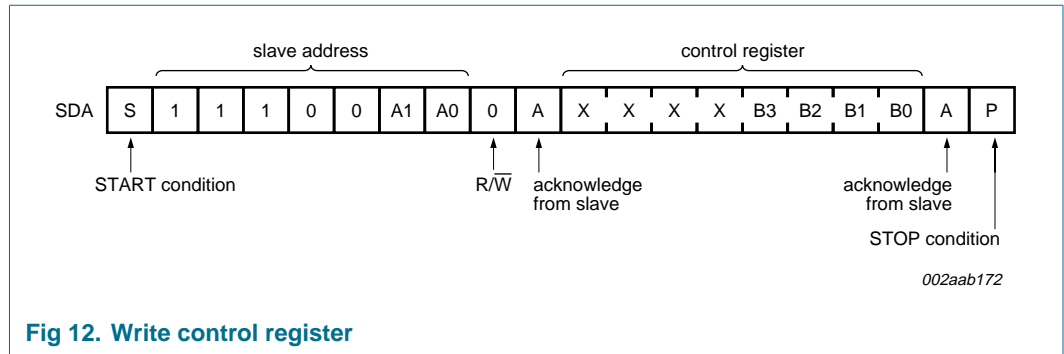


Fig 12. Write control register

Data is read from PCA9545A using the Read mode as shown in [Figure 13](#).

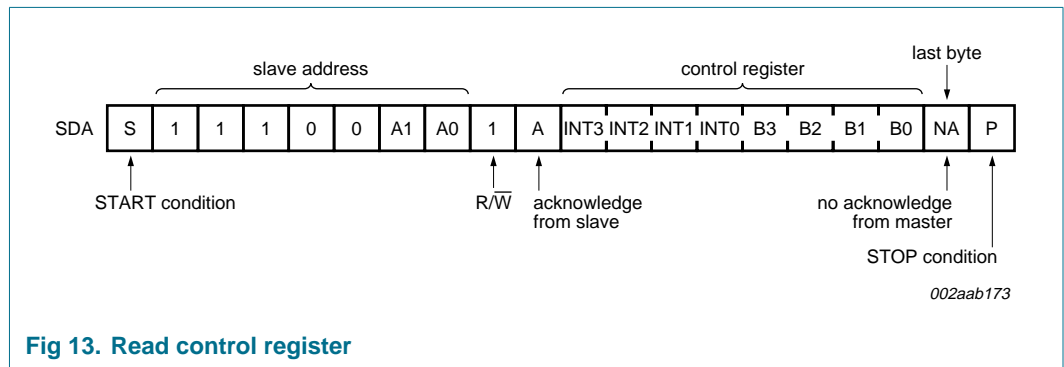
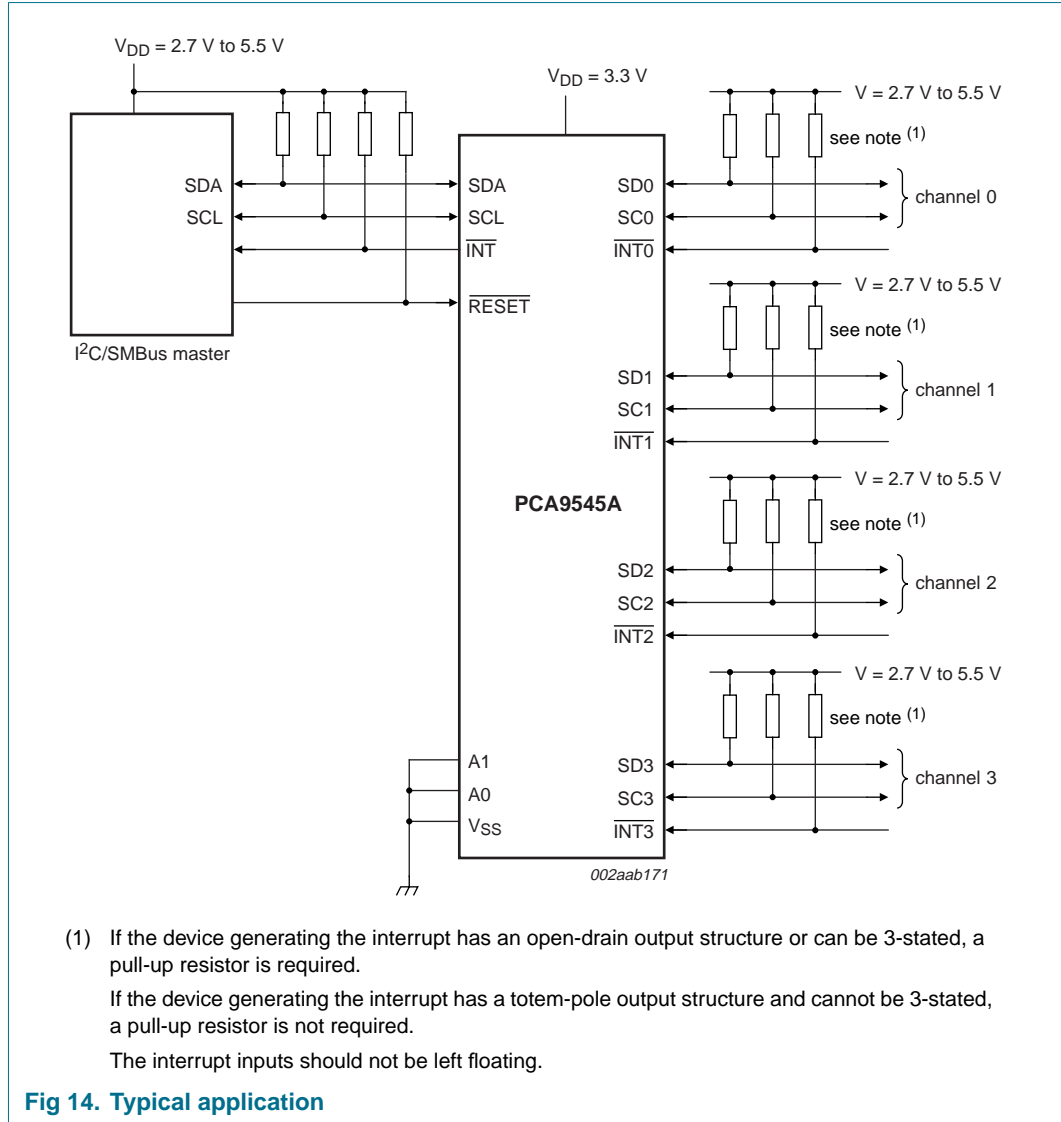


Fig 13. Read control register

9. Application design-in information



10. Limiting values

Table 6: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to V_{SS} (ground = 0 V). [\[1\]](#)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+7.0	V
V_I	input voltage		-0.5	+7.0	V
I_I	input current		-	±20	mA
I_O	output current		-	±25	mA
I_{DD}	supply current		-	±100	mA
I_{SS}	ground supply current		-	±100	mA
P_{tot}	total power dissipation		-	400	mW
T_{stg}	storage temperature		-60	+150	°C
T_{amb}	operating ambient temperature		-40	+85	°C

- [1] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

11. Static characteristics

Table 7: Static characteristics

$V_{DD} = 2.3\text{ V to }3.6\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -40\text{ °C to }+85\text{ °C}$; unless otherwise specified.

See [Table 8 on page 15](#) for $V_{DD} = 4.5\text{ V to }5.5\text{ V}$.^[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_{DD}	supply voltage		2.3	-	3.6	V
I_{DD}	supply current	operating mode; $V_{DD} = 3.6\text{ V}$; no load; $V_I = V_{DD}$ or V_{SS} ; $f_{SCL} = 100\text{ kHz}$	-	10	30	μA
I_{stb}	standby current	standby mode; $V_{DD} = 3.6\text{ V}$; no load; $V_I = V_{DD}$ or V_{SS}	-	0.1	1	μA
V_{POR}	power-on reset voltage	no load; $V_I = V_{DD}$ or V_{SS}	[2] -	1.6	2.1	V
Input SCL; input/output SDA						
V_{IL}	LOW-level input voltage		-0.5	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	6	V
I_{OL}	LOW-level output current	$V_{OL} = 0.4\text{ V}$	3	7	-	mA
		$V_{OL} = 0.6\text{ V}$	6	10	-	mA
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	-1	-	+1	μA
C_i	input capacitance	$V_I = V_{SS}$	-	10	13	pF
Select inputs A0, A1, INT0 to INT3, RESET						
V_{IL}	LOW-level input voltage		-0.5	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	$V_{DD} + 0.5$	V
I_{LI}	input leakage current	pin at V_{DD} or V_{SS}	-1	-	+1	μA
C_i	input capacitance	$V_I = V_{SS}$	-	1.6	3	pF
Pass gate						
R_{on}	on-state resistance	$V_{DD} = 3.67\text{ V}$; $V_O = 0.4\text{ V}$; $I_O = 15\text{ mA}$	5	11	30	Ω
		$V_{DD} = 2.3\text{ V to }2.7\text{ V}$; $V_O = 0.4\text{ V}$; $I_O = 10\text{ mA}$	7	16	55	Ω
$V_{O(sw)}$	switch output voltage	$V_{i(sw)} = V_{DD} = 3.3\text{ V}$; $I_{O(sw)} = -100\text{ }\mu\text{A}$	-	1.9	-	V
		$V_{i(sw)} = V_{DD} = 3.0\text{ V to }3.6\text{ V}$; $I_{O(sw)} = -100\text{ }\mu\text{A}$	1.6	-	2.8	V
		$V_{i(sw)} = V_{DD} = 2.5\text{ V}$; $I_{O(sw)} = -100\text{ }\mu\text{A}$	-	1.5	-	V
		$V_{i(sw)} = V_{DD} = 2.3\text{ V to }2.7\text{ V}$; $I_{O(sw)} = -100\text{ }\mu\text{A}$	1.1	-	2.0	V
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	-1	-	+1	μA
C_{io}	input/output capacitance	$V_I = V_{SS}$	-	3	5	pF
INT output						
I_{OL}	LOW-level output current	$V_{OL} = 0.4\text{ V}$	3	-	-	mA
I_{OH}	HIGH-level output current		-	-	+10	μA

[1] For operation between published voltage ranges, refer to the worst-case parameter in both ranges.

[2] V_{DD} must be lowered to 0.2 V in order to reset part.

Table 8: Static characteristics

$V_{DD} = 4.5\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -40\text{ °C to }+85\text{ °C}$; unless otherwise specified.

See [Table 7 on page 14](#) for $V_{DD} = 2.3\text{ V to }3.6\text{ V}$. [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_{DD}	supply voltage		4.5	-	5.5	V
I_{DD}	supply current	operating mode; $V_{DD} = 5.5\text{ V}$; no load; $V_I = V_{DD}$ or V_{SS} ; $f_{SCL} = 100\text{ kHz}$	-	25	100	μA
I_{stb}	standby current	standby mode; $V_{DD} = 5.5\text{ V}$; no load; $V_I = V_{DD}$ or V_{SS}	-	0.3	1	μA
V_{POR}	power-on reset voltage	no load; $V_I = V_{DD}$ or V_{SS}	[2]	1.7	2.1	V
Input SCL; input/output SDA						
V_{IL}	LOW-level input voltage		-0.5	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	6	V
I_{OL}	LOW-level output current	$V_{OL} = 0.4\text{ V}$	3	-	-	mA
		$V_{OL} = 0.6\text{ V}$	6	-	-	mA
I_L	leakage current	$V_I = V_{SS}$	-1	-	1	μA
C_i	input capacitance	$V_I = V_{SS}$	-	10	13	pF
Select inputs A0, A1, INT0 to INT3, RESET						
V_{IL}	LOW-level input voltage		-0.5	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	$V_{DD} + 0.5$	V
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	-1	-	+1	μA
C_i	input capacitance	$V_I = V_{SS}$	-	2	5	pF
Pass gate						
R_{on}	on-state resistance	$V_{DD} = 4.5\text{ V to }5.5\text{ V}$; $V_O = 0.4\text{ V}$; $I_O = 15\text{ mA}$	4	9	24	Ω
$V_{o(sw)}$	switch output voltage	$V_{i(sw)} = V_{DD} = 5.0\text{ V}$; $I_{o(sw)} = -100\text{ }\mu\text{A}$	-	3.6	-	V
		$V_{i(sw)} = V_{DD} = 4.5\text{ V to }5.5\text{ V}$; $I_{o(sw)} = -100\text{ }\mu\text{A}$	2.6	-	4.5	V
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	-1	-	+1	μA
C_{io}	input/output capacitance	$V_I = V_{SS}$	-	3	5	pF
INT output						
I_{OL}	LOW-level output current	$V_{OL} = 0.4\text{ V}$	3	-	-	mA
I_{OH}	HIGH-level output current		-	-	+10	μA

[1] For operation between published voltage ranges, refer to the worst-case parameter in both ranges.

[2] V_{DD} must be lowered to 0.2 V in order to reset part.

12. Dynamic characteristics

Table 9: Dynamic characteristics

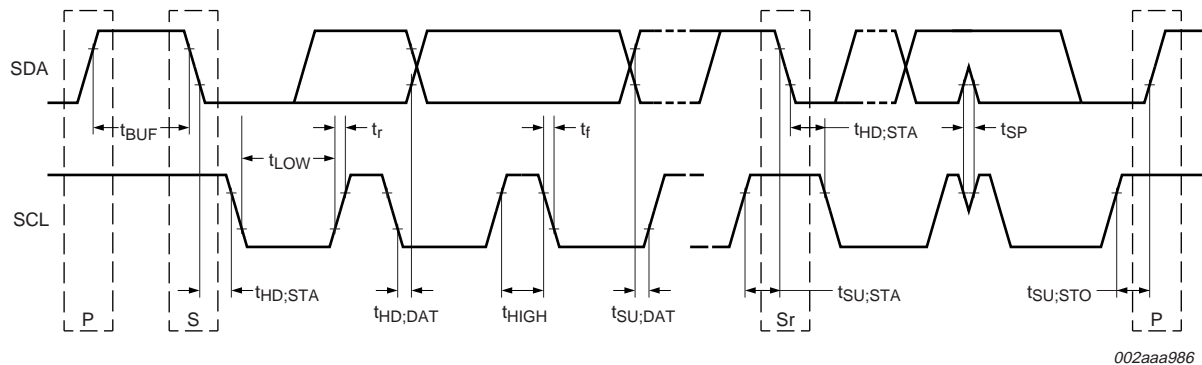
Symbol	Parameter	Conditions	Standard-mode I ² C-bus		Fast-mode I ² C-bus		Unit
			Min	Max	Min	Max	
t _{PD}	propagation delay from SDA to SDn, or SCL to SCn		-	0.3 [1]	-	0.3 [1]	ns
f _{SCL}	SCL clock frequency		0	100	0	400	kHz
t _{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	μs
t _{HD;STA}	hold time (repeated) START condition. After this period, the first clock pulse is generated.		4.0	-	0.6	-	μs
t _{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	μs
t _{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	μs
t _{SU;STA}	setup time for a repeated START condition		4.7	-	0.6	-	μs
t _{SU;STO}	setup time for STOP condition		4.0	-	0.6	-	μs
t _{HD;DAT}	data hold time		0 [2]	3.45	0 [2]	0.9	μs
t _{SU;DAT}	data setup time		250	-	100	-	ns
t _r	rise time of both SDA and SCL signals		-	1000	20 + 0.1C _b [3]	300	ns
t _f	fall time of both SDA and SCL signals		-	300	20 + 0.1C _b [3]	300	μs
C _b	capacitive load for each bus line		-	400	-	400	μs
t _{SP}	pulse width of spikes which must be suppressed by the input filter		-	50	-	50	ns
t _{VD;DAT}	data valid time	HIGH-to-LOW [4]	-	1	-	1	μs
		LOW-to-HIGH [4]	-	0.6	-	0.6	μs
t _{VD;ACK}	data valid Acknowledge		-	1	-	1	μs
INT							
t _{v(INTnN-INTN)}	valid time from $\overline{\text{INTn}}$ to $\overline{\text{INT}}$ signal		-	4	-	4	μs
t _{d(INTnN-INTN)}	delay time from $\overline{\text{INTn}}$ to $\overline{\text{INT}}$ inactive		-	2	100	2	μs
t _{w(rej)L}	LOW-level rejection time	$\overline{\text{INTn}}$ inputs	1	-	1	-	μs
t _{w(rej)H}	HIGH-level rejection time	$\overline{\text{INTn}}$ inputs	0.5	-	0.5	-	μs
RESET							
t _{w(rst)L}	LOW-level reset time		4	-	4	-	ns
t _{rst}	reset time (SDA clear)		500	-	500	-	ns
t _{REC;STA}	recovery time to START condition		0	-	0	-	ns

[1] Pass gate propagation delay is calculated from the 20 Ω typical R_{on} and the 15 pF load capacitance.

[2] A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH(min)} of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

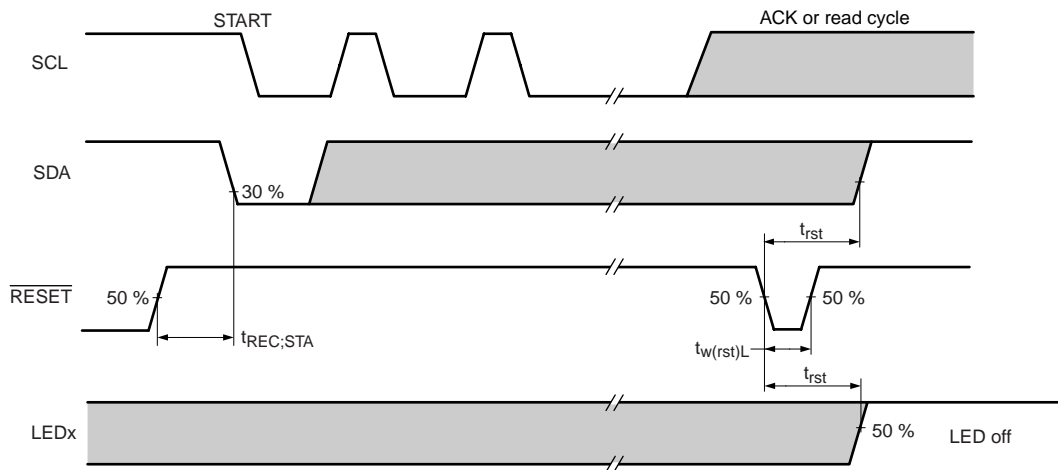
[3] C_b = total capacitance of one bus line in pF.

[4] Measurements taken with 1 kΩ pull-up resistor and 50 pF load.



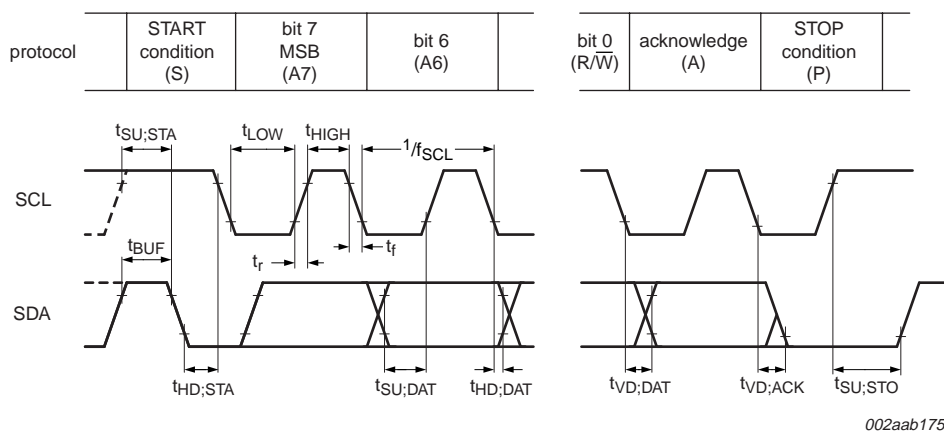
002aaa986

Fig 15. Definition of timing on the I²C-bus



002aab174

Fig 16. Definition of RESET timing



002aab175

Rise and fall times, refer to V_{IL} and V_{IH} .

Fig 17. I²C-bus timing diagram

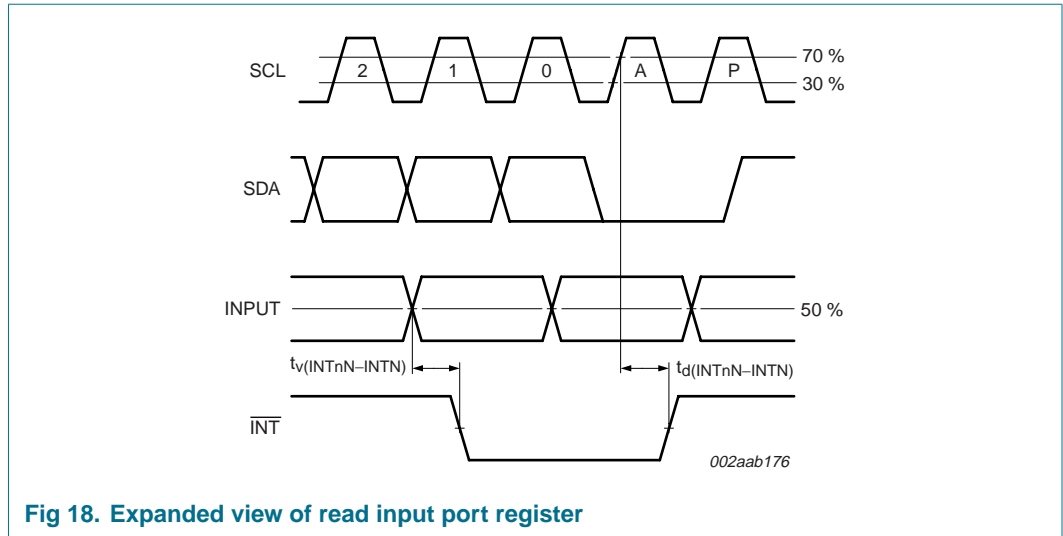


Fig 18. Expanded view of read input port register

13. Test information

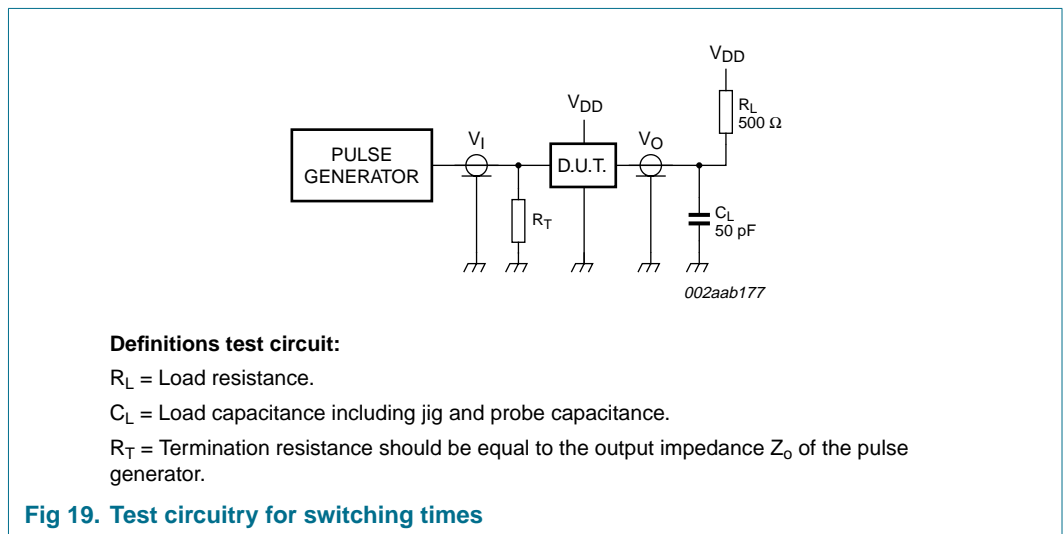


Fig 19. Test circuitry for switching times

14. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

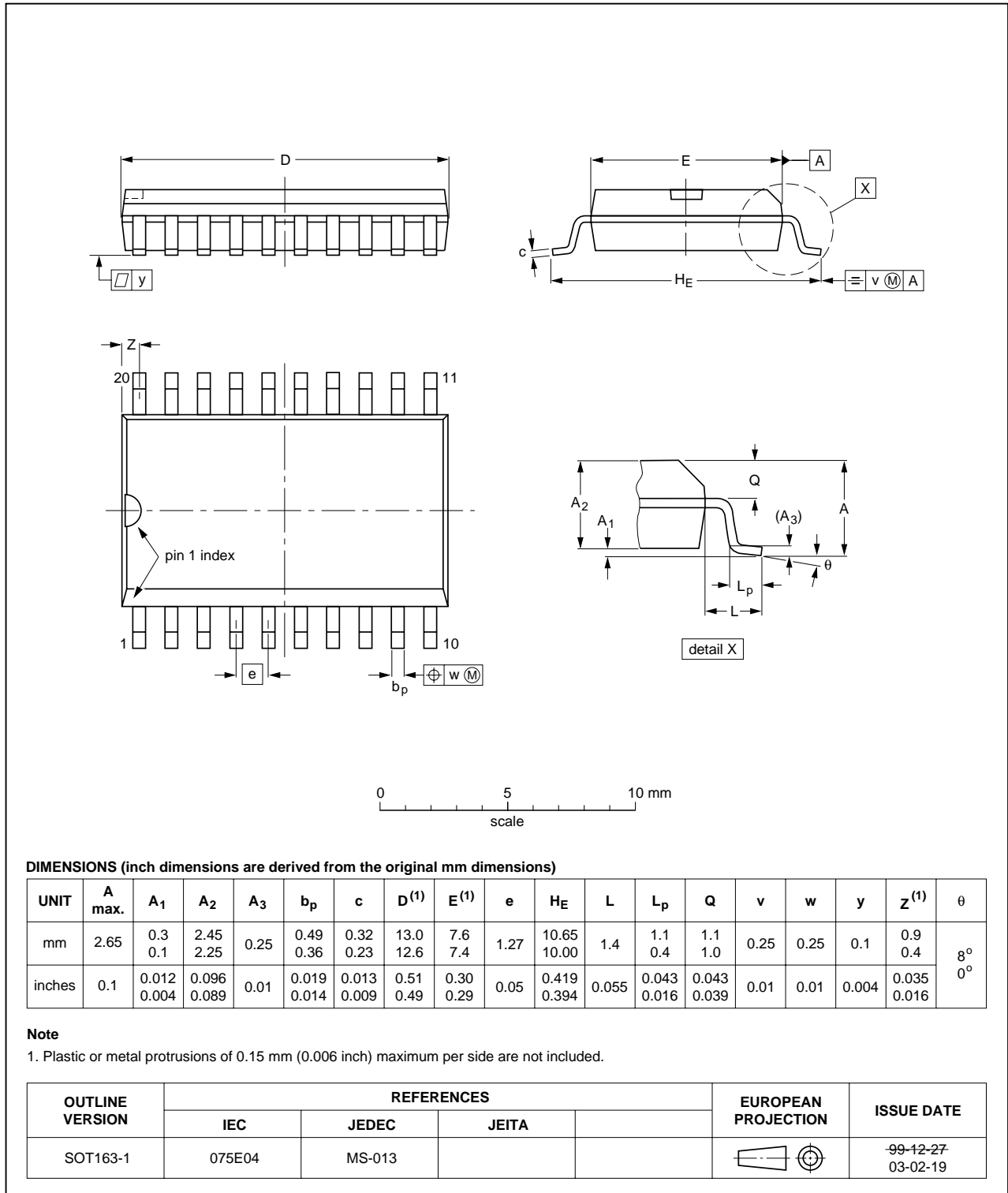


Fig 20. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

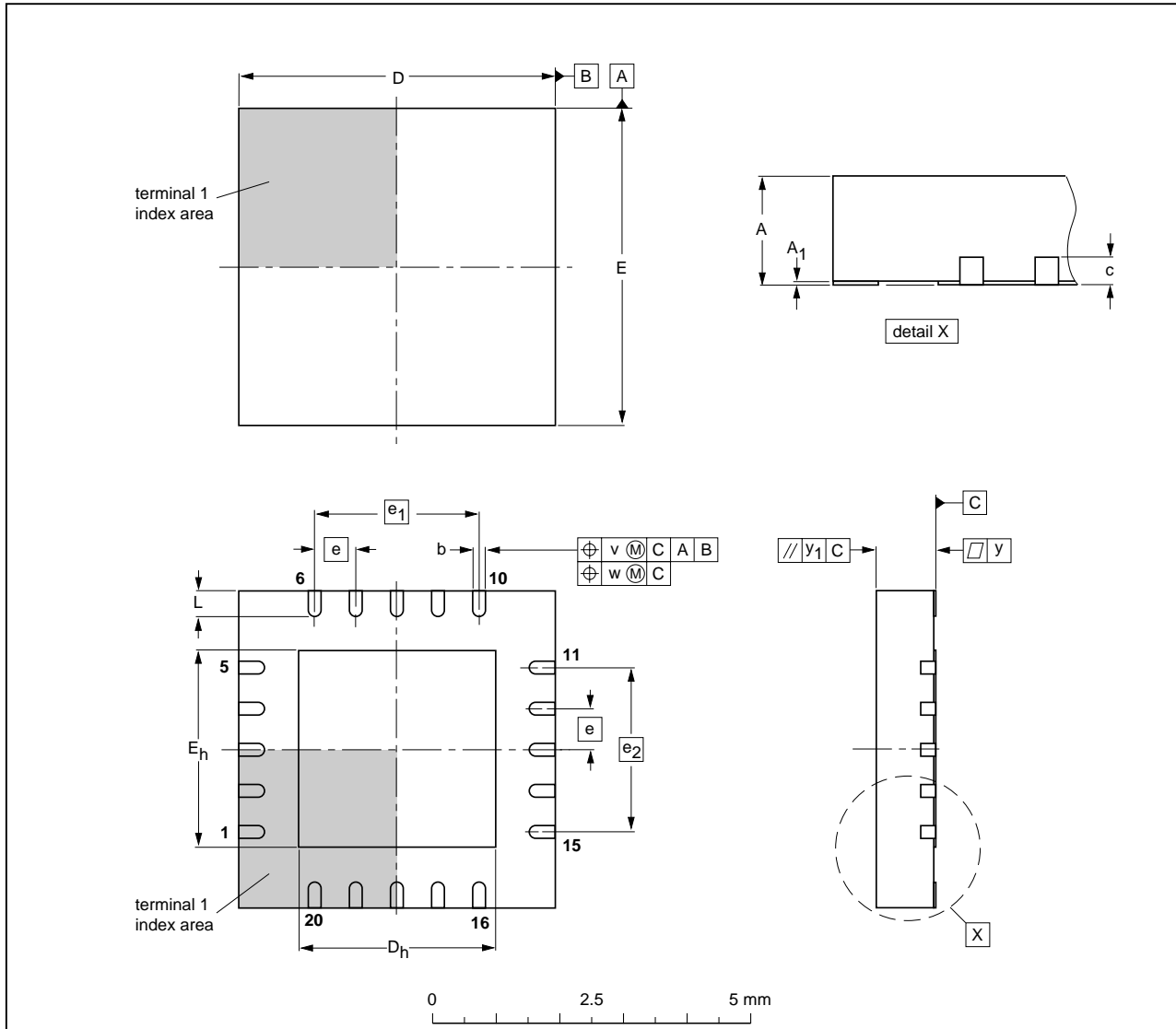
SOT360-1



Fig 21. Package outline SOT360-1 (TSSOP20)

HVQFN20: plastic thermal enhanced very thin quad flat package; no leads; 20 terminals; body 5 x 5 x 0.85 mm

SOT662-1



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾ max.	A ₁	b	c	D ⁽¹⁾	D _h	E ⁽¹⁾	E _h	e	e ₁	e ₂	L	v	w	y	y ₁
mm	1	0.05 0.00	0.38 0.23	0.2	5.1 4.9	3.25 2.95	5.1 4.9	3.25 2.95	0.65	2.6	2.6	0.75 0.50	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT662-1	---	MO-220	---			01-08-08 02-10-22

Fig 22. Package outline SOT662-1 (HVQFN20)

15. Soldering

15.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

15.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
 - for all BGA, HTSSON..T and SSOP..T packages
 - for packages with a thickness ≥ 2.5 mm
 - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm³ so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm³ so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

15.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

- smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

15.5 Package related soldering information

Table 10: Suitability of surface mount IC packages for wave and reflow soldering methods

Package ^[1]	Soldering method	
	Wave	Reflow ^[2]
BGA, HTSSON..T ^[3] , LBGA, LFBGA, SQFP, SSOP..T ^[3] , TFBGA, USON, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable ^[4]	suitable
PLCC ^[5] , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ^[5] ^[6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended ^[7]	suitable
CWQCCN..L ^[8] , PMFP ^[9] , WQCCN..L ^[8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note (AN01026)*; order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

- [4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- [5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- [6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- [7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
- [8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
- [9] Hot bar soldering or manual soldering is suitable for PMFP packages.

16. Abbreviations

Table 11: Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	Electro Static Discharge
HBM	Human Body Model
IC	Integrated Circuit
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit
PCB	Printed-Circuit Board
POR	Power-On Reset

17. Revision history

Table 12: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PCA9545A_3	20050303	Product data sheet	-	9397 750 14311	PCA9545A_2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. Section 2 “Features” on page 1: 9th bullet: changed “RDS_{ON}” to “R_{on}” Figure 4 “Pin configuration for HVQFN20 (transparent top view)” on page 4: added pin 1 indicator notch and center pad. Table 3 “Pin description” on page 4: added Table note 1 and its reference at HVQFN pin 8. Section 7.5 “Voltage translation” on page 8: <ul style="list-style-type: none"> Figure 7: title changed from “V_{pass} voltage versus V_{DD}” to “Pass gate voltage versus supply voltage”; within graphic changed “V_{pass} (V)” to “V_{o(sw)} (V)” 2nd paragraph: changed “V_{pass}” to “V_{o(sw)}”; changed “V_{pass(max)}” to “V_{o(sw)(max)}” Table 6 “Limiting values” on page 13: remove (old) table note [1], as it is now covered by Section 19 “Definitions” on page 26. Table 7 “Static characteristics” on page 14: <ul style="list-style-type: none"> changed symbol “R_{ON}” to “R_{on}”; changed parameter from “switch resistance” to “on-state resistance” changed symbol “V_{pass}” to “V_{o(sw)}” under Conditions column for V_{o(sw)}: changed “V_{swin}” to “V_{i(sw)}”; changed “I_{swout}” to “I_{o(sw)}” Added (new) Table note 1. Table 8 “Static characteristics” on page 15: <ul style="list-style-type: none"> changed symbol “R_{ON}” to “R_{on}”; changed parameter from “switch resistance” to “on-state resistance” changed symbol “V_{pass}” to “V_{o(sw)}” under Conditions column for V_{o(sw)}: changed “V_{swin}” to “V_{i(sw)}”; changed “I_{swout}” to “I_{o(sw)}” Table 9 “Dynamic characteristics” on page 16: <ul style="list-style-type: none"> changed symbol “t_R” to “t_r”; changed symbol “t_F” to “t_f” (also in Figure 15 on page 17) changed symbols “t_{VD;DATL}” and “t_{VD;DATH}” to “t_{VD;DAT}” and added Conditions indicating HIGH-to-LOW and LOW-to-HIGH transitions changed symbol “t_{IV}” to “t_{v(INTn-INTN)}” (also in Figure 18 on page 18) changed symbol “t_{IR}” to “t_{d(INTn-INTN)}” (also in Figure 18 on page 18) changed symbol “L_{pwr}” to “t_{w(rej)L}” changed symbol “H_{pwr}” to “t_{w(rej)H}” changed symbol “t_{WL(rst)}” to “t_{w(rst)L}” (also in Figure 16 on page 17) Added Section 16 “Abbreviations”. 				
PCA9545A_2	20040929	Objective data sheet	-	9397 750 13989	PCA9545A_1
PCA9545A_1	20040728	Objective data sheet	-	9397 750 13309	-

18. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

19. Definitions

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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