PDSP16330 MC

Pythagoras Processor

DS3240 ISSUE 3.1 November 1998

The PDSP16330 is a high speed digital CMOS IC that converts Cartesian data (Real and Imaginary) into Polar form (Magnitude and Phase), at rates up to 10MHz. Cartesian 16+16 bit 2's complement or Sign-Magnitude data is converted into 16 bit Phase format. The Magnitude output may be scaled in amplitude by powers of 2. The Phase output represents a full 2 x π field to eliminate phase ambiguities.

Polyimide is used as an inter-layer dielectric and as glassivation.

FEATURES

- 10MHz Cartesian to Polar Conversion
- 16-Bit Cartesian Inputs
- 16-Bit Magnitude Output
- 12-Bit Phase Output
- 2’s Complement or Sign-Magnitude Input Formats
- Three-state Outputs and Independent Data Enables Simplify System Interfacing
- Magnitude Scaling Facility with Overflow Flag
- Less than 400 mW Power Dissipation at 10MHz
- 100 pin CQFP Package

APPLICATIONS

- Digital Signal Processing
- Digital Radio
- Radar Processing
- Sonar Processing
- Robotics

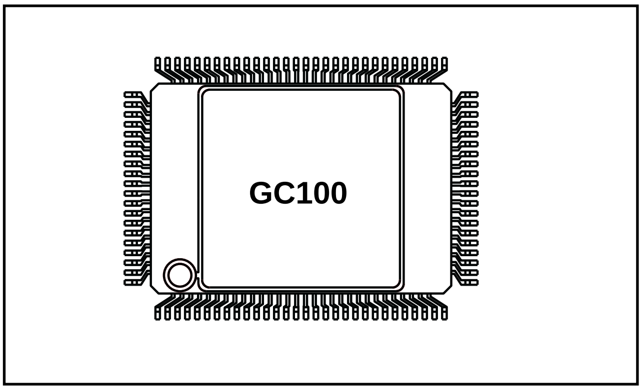


Fig.1 Pin connections - QFP Package

Rev	A	B	C	D
Date	FEB 1992	MAR 1993	OCT 1995	NOV 1998

ASSOCIATED PRODUCTS

PDSP16112 16 X 12 Complex Multiplier
PDSP16116 16 X 16 Complex Multiplier
PDSP16318 Complex Accumulator
PDSP16350 I/Q Splitter and NCO
PDSP16510A Stand Alone FFT Processor

ORDERING INFORMATION

PDSP16330/MC/GC1R (10MHz - QFP Package, MIL-STD-883 Screening)

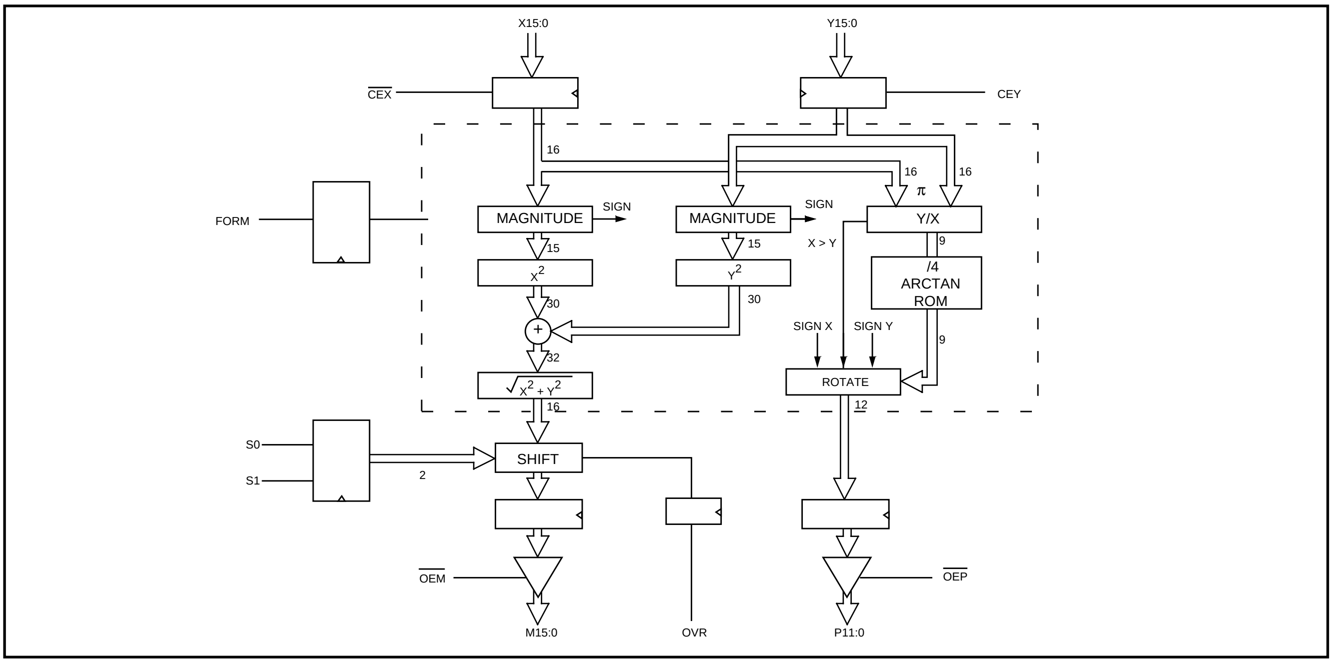


Fig.2 Block diagram

FUNCTIONAL DESCRIPTION

The PDSP16330 converts incoming Cartesian Data into the equivalent Polar Values. The device accepts new 16 + 16 bit complex data every cycle, and delivers a 16 bit + 12 bit Polar equivalent after 24 clock cycles.The input data can be in 2s' Complement or Sign Magnitude format selected via the FORM input. The output is in a magnitude format for both the Magnitude output and the Phase. Phase data is zero for data with a zero Y input and positive X, and is 400 hex for zero X data and positive Y, is 800 hex for zero Y data and negative X, and is C00 hex for zero X and negative Y. The LSB weighting (bit 0) is 2 x π/4096 radians. The 16 bit Magnitude result may be scaled by shifting one, two, or three places in the more significant direction, effectively multiplying the Magnitude result by 2,4 or 8 respectively. Any of these shifts can under certain conditions cause an invalid result to be output from the device. Under these circumstances the OVR output will become active. The PDSP16330 has independent clock enables and three state output controls for all ports.

FORM

This input selects the format of the X and Y input data. A low level on FORM indlcates that the Input data is twos' complement format (Note: input data 8000 hex is not valid in 2s' complement mode). This input refers to the format of the current Input data and may be changed on a per cycle basis if desired. The level of FORM is latched at the same time as the data to which it refers.

S1-0

These inputs select the scaling factor to be applied to the Magnitude output. They are latched by the rising edge of CLK and determine the scaling of the output in the cycle after they are loaded into the device. The scale factor applied is determined by the table. Should the scaling factor applied cause an invalid Magnitude result to be output on the M Port, then the OVR Flag will become active for the period that the M Port output is invalid.

S1	S0	Scaling Factor
0	0	x1
0	1	x2
1	0	x4
1	1	x8

The output number range is from 0 to 2 when the scaling factor is set at x1.

PIN DESCRIPTIONS

Symbol	Pin Name and Description
CLK	**Clock:** Common Clock to device Registers. Register contents change on the rising edge of clock. Both pins must be connected.
$\overline{CEX}$	**Clock Enable:** Clock Enable for X Port. The clock to the X port is enabled by a low level.
$\overline{CEY}$	**Clock Enable:** Clock Enable for Y Port The clock to the Y port is enabled by a low level.
X15-X0	**X Data Input** Data presented to this input is loaded into the device by the rising edge of CLK. X15 is the MSB
Y15-Y0	**Y Data Input** Data presented to this input is loaded into the device by the rising edge of CLK. Y15 is the MSB
M15-M0	**M Data Output:** Magnitude data generated by the device is output on this port. Data changes on the rising edge of CLK, M15 is the MSB. The weighting of M15 is determined by the Scale factor selected .
P11-P0	**P Data Output:** Phase data generated by the device is output on this port. Data changes on the rising edge of CLK, P11 is the MSB. The weighting of P11 is π radians.
$\overline{OEM}$	**Output Enable:** Output Enable for M Port. The M Port is in a high impedance state when this input is high.
$\overline{OEP}$	**Output Enable:** Output Enable for P Port. The P Port is in a high impedance state when this input is high.
FORM	**Format Select** This input selects the format of the Cartesian Data input on the X and Y ports. This input is latched by the rising edge of CLK, and is applied at the same time as the data to which it refers. A low !evel indicates that two's complement data is applied, a high indicates Sign-Magnitude
S1-S0	**Scaling Control:** Control input for scaling of Magnitude Data. This input is latched by the rising edge of CLK, and determines the scaling to be applied to the Magnitude result. The Scaling is applied to the output data in the cycle following the cycle in which the control was latched.
OVR	**Overflow:** Overflow flag. This signal becomes active if the scaling currently selected causes an invalid value to be presented to the Magnitude output.
Vcc	+**5V supply.** All Vcc pins must be connected.
GND	**0V supply.** All GND pins must be connected.

INPUT DATA RANGE

2's Complement	Sign Magnitude
7FFF	7FFF
.	.
.	.
.	.
0001	0001
0000	0000
FFFF	8000
.	.
.	.
.	.
8001	FFF

PIN FUNCTION

Pin No. GC	Function	Pin No. GC	Function	Pin No. GC	Function
91	M7	23	YO	59	X1
92	M6	24	$\overline{CEY}$	60	X2
93	M5	25	CLK	61	X3
94	M4	26	Vcc	62	X4
95	M3	31	GND	63	X5
96	M2	32	GND	64	X6
97	M1	33	GND	65	X7
98	M0	34	GND	66	X8
99	S0	35	GND	67	X9
100	S1	36	GND	68	X10
1	GND	37	GND	69	X11
6	Vcc	38	$\overline{OEP}$	70	X12
7	FORM	39	P0	71	X13
8	Y15	40	P1	72	X14
9	Y14	41	P2	73	X15
10	Y13	42	P3	74	CLK
11	Y12	43	P4	75	OVR
12	Y11	44	P5	76	Vcc
13	Y10	45	P6	81	GND
14	Y9	46	P7	82	$\overline{OEM}$
15	Y8	47	P8	83	M15
16	Y7	48	P9	84	M14
17	Y6	49	P10	85	M13
18	Y5	50	P11	86	M12
19	Y4	51	GND	87	M11
20	Y3	52	Vcc	88	M10
21	Y2	57	$\overline{CEX}$	89	M9
22	Y1	58	X0	90	M8

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): T_{amb} (Military) =-55°C to + 125°C
V_{cc} (Military) = 5.0V ± 10%, GND = 0V

STATIC CHARACTERISTICS

Characteristic	Symbol	Value Min.	Value Typ.	Value Max.	Units	Sub-group	Conditions
* Output high voltage	V_{OH}	2.4			V	1,2,3	IOH = 3.2mA
* Output low voltage	V_{OL}			0.6	V	1,2,3	IOL=-3.2mA
* Input high voltage (CMOS)	V_{IH}	3.0			V	1,2,3	Inputs $\overline{CEX}$, $\overline{CEY}$ and CLK only
* Input low voltage (CMOS)	V_{IL}			1.0	V	1,2,3	Inputs $\overline{CEX}$, $\overline{CEY}$ and CLK only
* Input high voltage (TTL)	V_{IH}	2.2			V	1,2,3	All other inputs
* Input low voltage (TTL)	V_{IL}			0.8	V	1,2,3	All other inputs
* Input leakage current (Note 1)	I_{IL}	-10		+ 120	µA	1,2,3	GND ≤ V_{IN}≤V_{CC}
† Input capacitance	C_{IN}		10		pF		
* Output leakage current	I_{oz}	-50		+ 50	µA	1,2,3	GND ≤V_{IN} ≤ V_{CC}
† Output SC current	I_{OS}	-50		230	mA		V_{cc} = Max

NOTES
1. All inputs except clock inputs have high value pull-down resistors
2. All parameters marked * are tested during production. Parameters marked † are guaranteed by design and characterisation.

SWITCHING CHARACTERISTICS

Characteristic	Value PDSP16330 Min.	Value PDSP16330 Max.	Units	Sub-group	Conditions
† Input data setup to clock rising edge	15		ns		
† Input data Hold after clock rising edge	2		ns		
† $\overline{CEX}$, $\overline{CEY}$ Setup to clock rising edge	30		ns		
† $\overline{CEX}$, $\overline{CEY}$ Hold aher clock rising edge	0		ns		
† FORM, S1:0 Setup to clock rising edge	15		ns		
† FORM, S1:0 Hold after clock rising edge	7		ns		
† Clock rising edge to valid data	5	40	ns		2 x LSTTL + 20pF
* Clock period	100		ns	9,10,11	
† Clock high time	25		ns		
† Clock low time	25		ns		
† Latency	24	24	cycles		
† $\overline{OEM}$, $\overline{OEP}$ low to data high data valid		30	ns		2 x LSTTL + 20pF
† $\overline{OEM}$, $\overline{OEP}$ low to data low data valid		30	ns		2 x LSTTL + 20pF
† $\overline{OEM}$, $\overline{OEP}$ high to data high impedance		30	ns		2 x LSTTL + 20pF
† $\overline{OEM}$, $\overline{OEP}$ low to data high impedance		30	ns		2 x LSTTL + 20pF
† Vcc current (TTL input levels)		110	mA		V_{CC} = Max Outputs unloaded Clock freq. = Max
† Vcc current (CMOS input levels)		70	mA		V_{CC} = Max Outputs unloaded Clock freq. = Max

NOTES
1. LSTTL is equivalent to I_{OH} = 20µA, I_{OL} = -0.4mA
2. Current is defined as negative into the device
3. CMOS input levels are defined as: $V_{IH} = V_{DD}$ - 0.5V, V_{IL} = +0.5V
4. All parameters marked * are tested during production.
   Parameters marked † are guaranteed by design and characterisation.
5. All timings are dependent on silicon speed. This speed is tested by measuring clock period.
   This guarantees all other timings by characterisation and design.

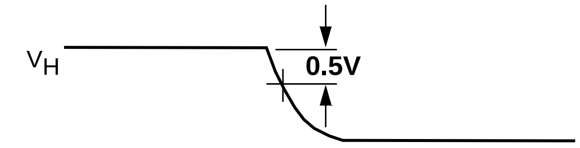
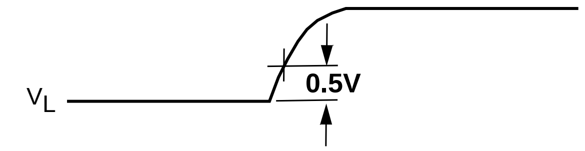
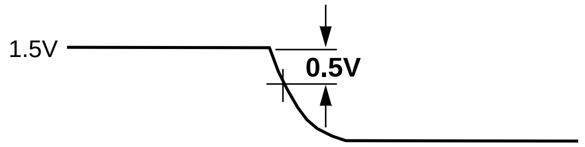
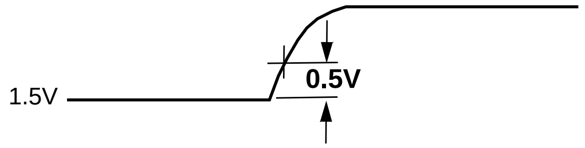
ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{cc}	-0.5V to + 7.0V
Input voltage, V_{IN}	-0.5V to VCC + 0.5V
Output voltage, V_{our}	-0.5V to VCC + 0.5V
Clamp diode current per pin, I_K (see Note 2)	±18mA
Static discharge voltage (HMB), V_{STAT}	500V
Storage temperature. T_{stg}	-65°C to + 150°C
Ambient temperature with power applied T_{amb}:	
Military	-55 °C to + 125 °C
Package power dissipation P_{TOT}	1200mW
Junction temperature	150 °C

THERMAL CHARACTERISTICS

Package Type	θ_{JC}°**C/W**
GC	12

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operatlon under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded; only one output to be tested at any one time.
3. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability

Test	Waveform - measurement level
Delay from ouput high to output high impedance	
Delay from ouput low to output high impedance	
Delay from ouput high impedance to Output low	
Delay from ouput high impedance to Output high	

NOTES
1. V_H - Voltage reached when output driven high
2. V_L - Voltage reached when output driven low

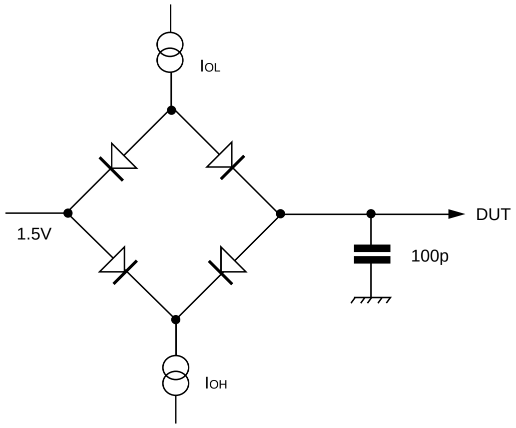


Fig.2 Three state delay measurement load

Part No: PDSP16330/A Pythagoras Processor

Package Type: AC84/GC100

Pin No.4 GC	Con.	Pin No. GC	Con.	Pin No. GC	Con.	Pin No. GC	Con.
76	V1	49	N/C	41	N/C	6	V1
74	V1	84	N/C	37	0v	7	0v
73	0v	82	0v	42	N/C	10	V1
71	0v	70	0v	93	N/C	13	V1
68	0v	66	0v	94	N/C	15	V1
67	0v	65	0v	92	N/C	19	V1
64	0v	50	N/C	40	N/C	22	V1
61	0v	48	N/C	38	0v	25	V1
59	0v	86	N/C	39	N/C	31	0v
58	0v	85	N/C	96	N/C	33	0v
51	0v	47	N/C	97	N/C	1	0v
83	N/C	46	N/C	35	0v	8	V1
81	0v	89	N/C	36	0v	9	V1
75	N/C	88	N/C	98	N/C	11	V1
72	0v	87	N/C	100	V1	14	V1
69	0v	45	N/C	12	V1	20	V1
62	0v	44	N/C	16	V1	18	V1
63	0v	43	N/C	17	V1	21	V1
60	0v	95	N/C	32	0v	23	V1
57	0v	90	N/C	34	0v	24	0v
52	V1	91	N/C	99	V1	26	V1

VDD max = +5.0V = V1

N/C = not connected

(All GC100 pins not specified are N/C)

Fig.3 Life Test/Burn-in connections
NOTE: PDA is 5% and based on groups 1 and 7

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