

DATA SHEET



PDTTC143ES NPN resistor-equipped transistor

Product specification
Supersedes data of 1997 Jul 03
File under Discrete Semiconductors, SC04

1998 May 20

NPN resistor-equipped transistor

PDTC143ES

FEATURES

- Built-in bias resistors R1 and R2 (typ. 4.7 kΩ each)
- Simplification of circuit design
- Reduces number of components and board space.

APPLICATIONS

- Especially suitable for space reduction in interface and driver circuits
- Inverter circuit configurations without use of external resistors.

DESCRIPTION

NPN resistor-equipped transistor in a TO-92; SOT54 plastic package.
PNP complement: PDTA143ES.

PINNING

| PIN | DESCRIPTION |
|-----|------------------|
| 1 | base/input |
| 2 | collector/output |
| 3 | emitter/ground |

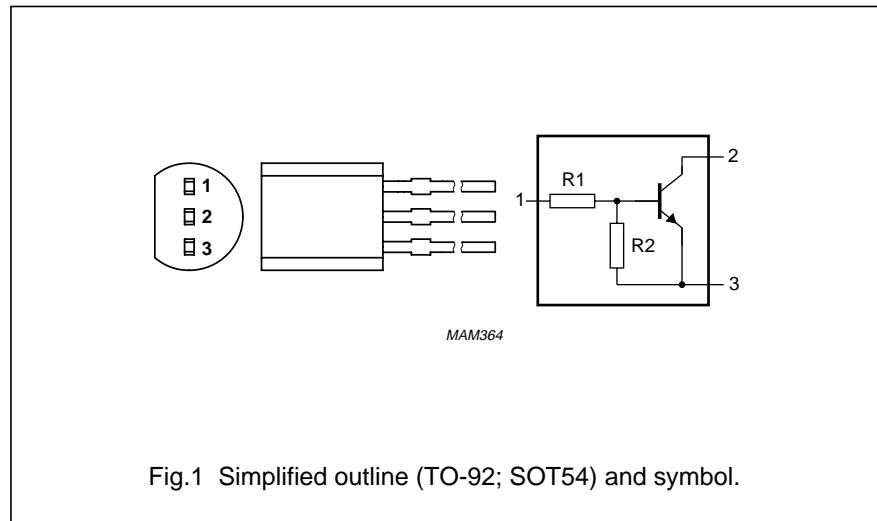


Fig.1 Simplified outline (TO-92; SOT54) and symbol.

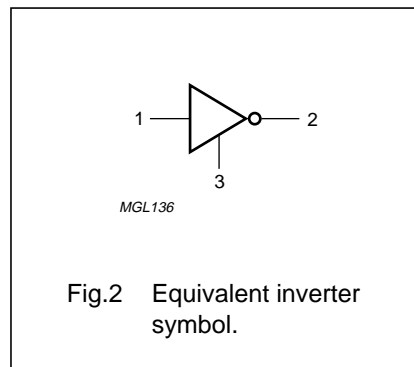


Fig.2 Equivalent inverter symbol.

QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------------|---------------------------|---|------|------|------|------|
| V_{CE0} | collector-emitter voltage | open base | – | – | 50 | V |
| I_O | output current (DC) | | – | – | 100 | mA |
| I_{CM} | peak collector current | | – | – | 100 | mA |
| P_{tot} | total power dissipation | $T_{amb} \leq 25\text{ }^\circ\text{C}$ | – | – | 500 | mW |
| h_{FE} | DC current gain | $I_C = 10\text{ mA}; V_{CE} = 5\text{ V}$ | 30 | – | – | |
| R1 | input resistor | | 3.3 | 4.7 | 6.1 | kΩ |
| $\frac{R2}{R1}$ | resistor ratio | | 0.8 | 1 | 1.2 | |

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|-----------|---------------------------------------|--------------------------------------|------|------|------|
| V_{CBO} | collector-base voltage | open emitter | – | 50 | V |
| V_{CEO} | collector-emitter voltage | open base | – | 50 | V |
| V_{EBO} | emitter-base voltage | open collector | – | 10 | V |
| V_i | input voltage positive negative | | – | +30 | V |
| | | | – | –10 | V |
| I_O | output current (DC) | | – | 100 | mA |
| I_{CM} | peak collector current | | – | 100 | mA |
| P_{tot} | total power dissipation | $T_{amb} \leq 25\text{ °C}$; note 1 | – | 500 | mW |
| T_{stg} | storage temperature | | –65 | +150 | °C |
| T_j | junction temperature | | – | 150 | °C |
| T_{amb} | operating ambient temperature | | –65 | +150 | °C |

Note

1. Transistor mounted on an FR4 printed-circuit board.

THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | CONDITIONS | VALUE | UNIT |
|---------------|---|------------|-------|------|
| $R_{th\ j-a}$ | thermal resistance from junction to ambient | note 1 | 250 | K/W |

Note

1. Transistor mounted on an FR4 printed-circuit board.

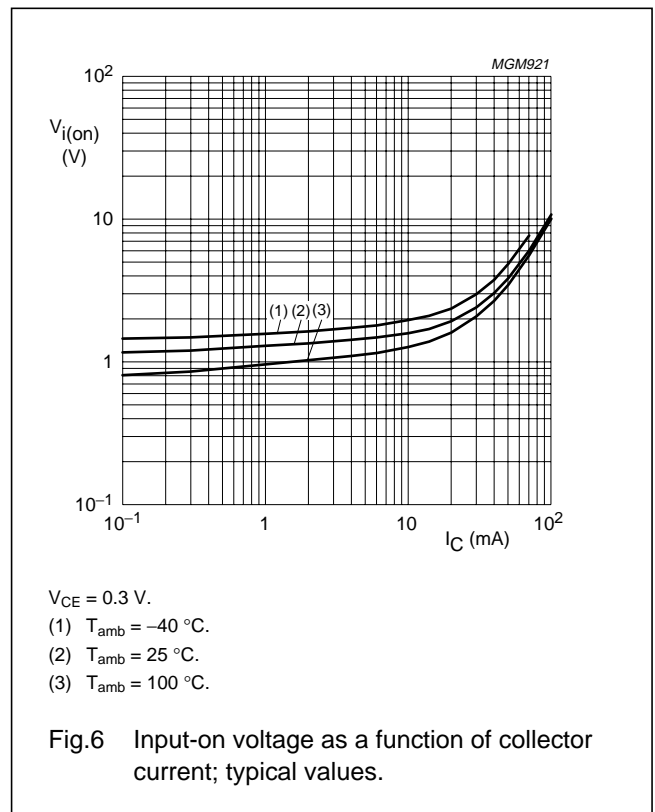
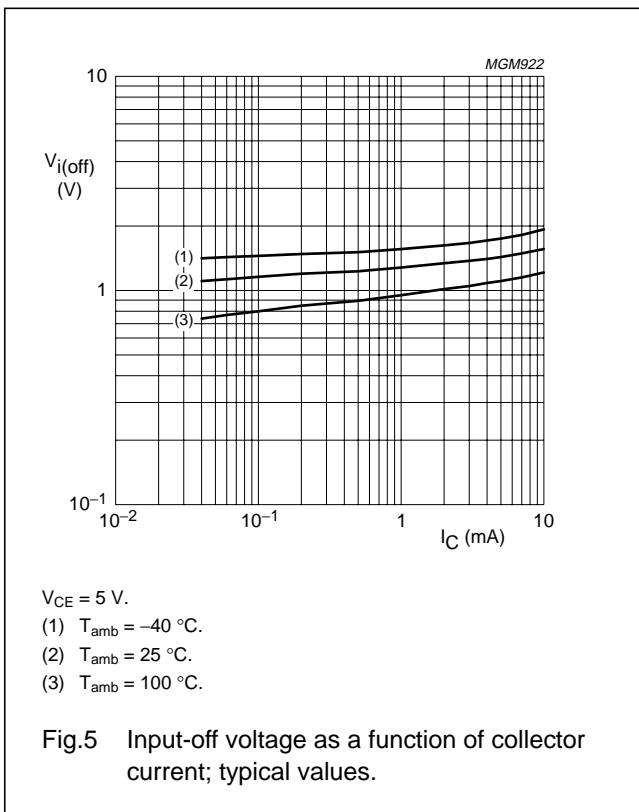
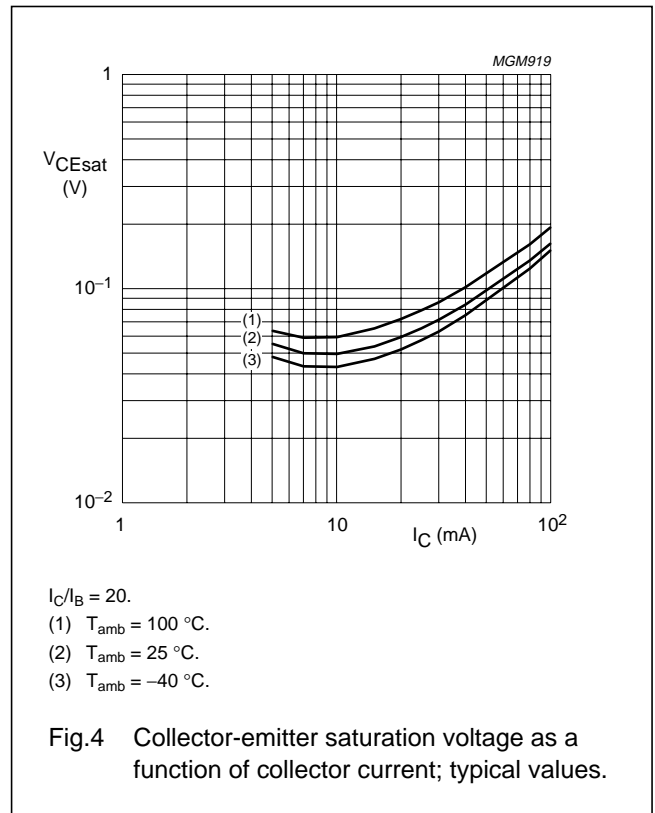
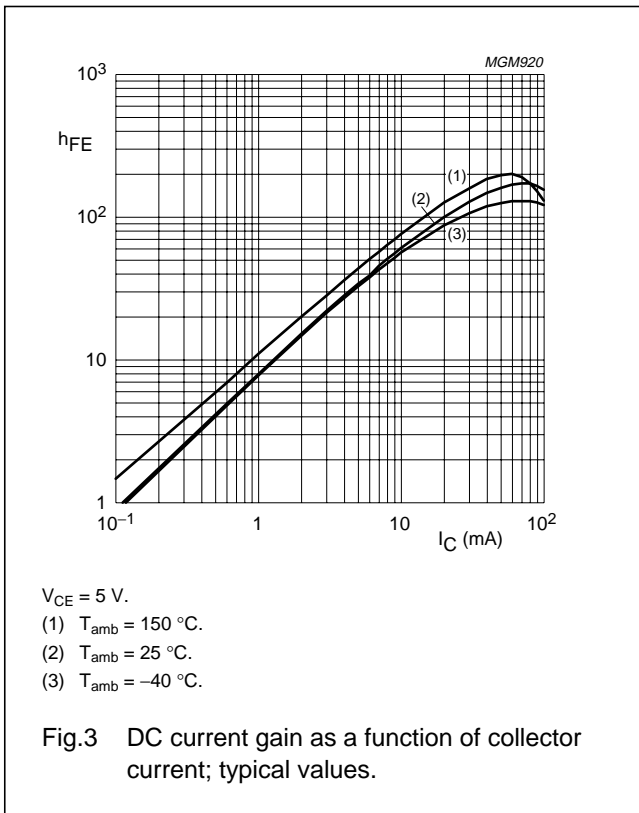
CHARACTERISTICS

$T_{amb} = 25\text{ °C}$ unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------------|--------------------------------------|---|------|------|------|---------------|
| I_{CBO} | collector cut-off current | $I_E = 0$; $V_{CB} = 50\text{ V}$ | – | – | 100 | nA |
| I_{CEO} | collector cut-off current | $I_B = 0$; $V_{CE} = 30\text{ V}$ | – | – | 1 | μA |
| | | $I_B = 0$; $V_{CE} = 30\text{ V}$; $T_j = 150\text{ °C}$ | – | – | 50 | μA |
| I_{EBO} | emitter cut-off current | $I_C = 0$; $V_{EB} = 5\text{ V}$ | – | – | 0.9 | mA |
| h_{FE} | DC current gain | $I_C = 10\text{ mA}$; $V_{CE} = 5\text{ V}$ | 30 | – | – | |
| V_{CEsat} | collector-emitter saturation voltage | $I_C = 10\text{ mA}$; $I_B = 0.5\text{ mA}$ | – | – | 150 | mV |
| $V_{i(off)}$ | input-off voltage | $I_C = 100\text{ }\mu\text{A}$; $V_{CE} = 5\text{ V}$ | – | 1.1 | 0.5 | V |
| $V_{i(on)}$ | input-on voltage | $I_C = 20\text{ mA}$; $V_{CE} = 300\text{ mV}$ | 2.5 | 1.9 | – | V |
| R1 | input resistor | | 3.3 | 4.7 | 6.1 | k Ω |
| $\frac{R2}{R1}$ | resistor ratio | | 0.8 | 1 | 1.2 | |
| C_c | collector capacitance | $I_E = I_B = 0$; $V_{CB} = 10\text{ V}$; $f = 1\text{ MHz}$ | – | – | 2.5 | pF |

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PDTC143ES



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PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



DIMENSIONS (mm are the original dimensions)

| UNIT | A | b | b ₁ | c | D | d | E | e | e ₁ | L | L ₁ ⁽¹⁾ |
|------|------------|--------------|----------------|--------------|------------|------------|------------|------|----------------|--------------|-------------------------------|
| mm | 5.2 5.0 | 0.48 0.40 | 0.66 0.56 | 0.45 0.40 | 4.8 4.4 | 1.7 1.4 | 4.2 3.6 | 2.54 | 1.27 | 14.5 12.7 | 2.5 |

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

| OUTLINE VERSION | REFERENCES | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|-------|-------|---------------------|------------|
| | IEC | JEDEC | EIAJ | | |
| SOT54 | | TO-92 | SC-43 | | 97-02-28 |

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DEFINITIONS

| | |
|---|---|
| Data sheet status | |
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |

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