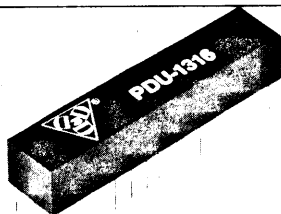


Digitally Programmable Delay Units

SERIES: PDU-1316
(4-Bit) TTL Interfaced

data delay devices, inc.



Features:

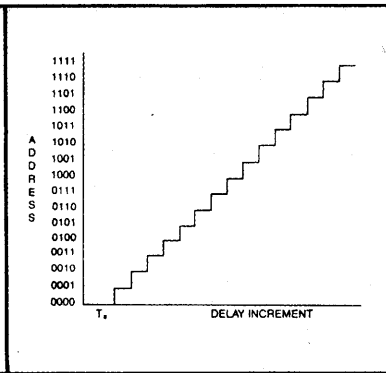
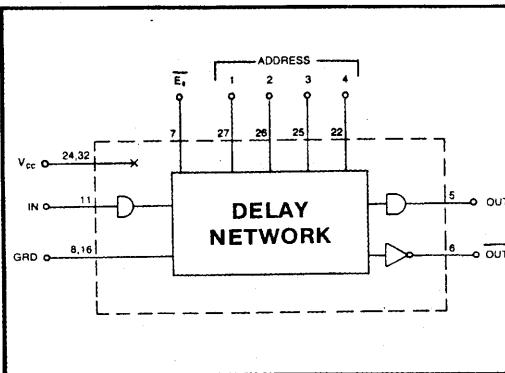
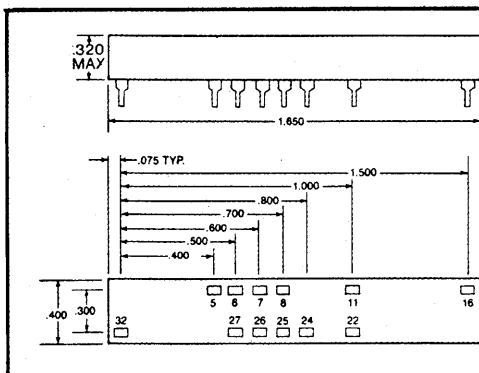
- Input & output TTL buffered
- 4-BIT TTL programmable delay line
- Two (2) separate outputs; inverting & non-inverting
- Completely interfaced
- Compact & low profile

Specifications:

- Input signal requirement: TTL logic.
- Output fan-out: TTL Schottky loads.
- Delay variation: Monotonic in one direction.
- Programmed delay tolerance: $\pm 5\%$ or 1 ns whichever is greater.
- Inherent delay (T_{D0}):
 - 19 ns \pm 1 ns on pin 5 } for PDU-1316-1 thru -10
 - 15 ns \pm 1 ns on pin 6 }
 greater for rest of Part Numbers.
- Propagation delay:
 - Address to output (T_{SUA}) = 12 ns typ.
 - Enable to output (T_{SUE}) = 12 ns typ.
- Power dissipation: 740 mw max.
- Supply voltage: 5 Vdc \pm 5%.
- Operating temperature: 0-70°C.
- Temperature coefficient: 100 PPM/°C.

Test Conditions:

- Input pulse-width: $\geq 150\%$ of Max. delay.
- Input pulse spacing: ≥ 3 times of Max. delay.
- Input pulse voltage: TTL logic.
- Measurements taken @ $T_a = 25^\circ\text{C}$; $V_{CC} = 5\text{V}$.



TRUTH TABLE

Enable (E0)	Address				Delay Out
	4	3	2	1	
0	0	0	0	0	T_0
0	0	0	0	1	T_1
0	0	0	1	0	T_2
0	0	0	1	1	T_3
0	0	1	0	0	T_4
0	0	1	0	1	T_5
0	0	1	1	0	T_6
0	0	1	1	1	T_7
0	1	0	0	0	T_8
0	1	0	0	1	T_9
0	1	0	1	0	T_{10}
0	1	0	1	1	T_{11}
0	1	1	0	0	T_{12}
0	1	1	0	1	T_{13}
0	1	1	1	0	T_{14}
0	1	1	1	1	T_{15}
1	ϕ	ϕ	ϕ	ϕ	0

Part No.	Incremental Delay Per Step (ns)	Total Programmed Delay (ns)
PDU-1316-5	.5 \pm .3	7.5
PDU-1316-1	1 \pm .5	15.0
PDU-1316-2	2 \pm .5	30.0
PDU-1316-3	3 \pm 1.0	45.0
PDU-1316-4	4 \pm 1.0	60.0
PDU-1316-5	5 \pm 1.0	75.0
PDU-1316-6	6 \pm 1.0	90.0
PDU-1316-8	8 \pm 1.0	120.0
PDU-1316-10	10 \pm 1.5	150.0
PDU-1316-12	12 \pm 1.5	180.0
PDU-1316-15	15 \pm 1.5	225.0
PDU-1316-20	20 \pm 2.0	300.0
PDU-1316-25	25 \pm 2.5	375.0
PDU-1316-30	30 \pm 3.0	450.0
PDU-1316-35	35 \pm 3.5	525.0
PDU-1316-40	40 \pm 4.0	600.0
PDU-1316-45	45 \pm 4.5	675.0
PDU-1316-50	50 \pm 5.0	750.0
PDU-1316-60	60 \pm 6.0	900.0
PDU-1316-80	80 \pm 8.0	1,200.0
PDU-1316-100	100 \pm 10.0	1,500.0

0 = Logic 0 1 = Logic 1 ϕ = Don't care.
 T_0 = Reference or inherent delay of unit
 $T_1 \rightarrow T_{15}$ = Multiplier of incremental delay.