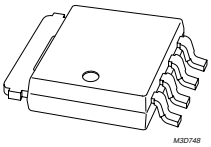


PH6325L

N-channel TrenchMOS™ logic level FET

Rev. 01 — 28 April 2004 **Preliminary data**

1. Product profile

1.1 Description

Logic level N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- Optimized for use in DC-to-DC converters
- Low threshold voltage
- Very low switching and conduction losses
- Low thermal resistance.

1.3 Applications

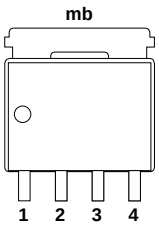
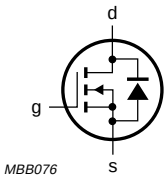
- DC-to-DC converters
- Voltage regulators
- Switched-mode power supplies
- Notebook computers.

1.4 Quick reference data

- $V_{DS} \leq 25$ V
- $Q_{gd} = 3.3$ nC (typ)
- $R_{DSon} \leq 6.3$ mΩ ($V_{GS} = 10$ V)
- $I_D \leq 78.7$ A
- $Q_{g(tot)} = 13.3$ nC (typ)
- $R_{DSon} \leq 9.5$ mΩ ($V_{GS} = 4.5$ V).

2. Pinning information

Table 1: Pinning - SOT669 (LFPAK), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)		
4	gate (g)		
mb	mounting base; connected to drain (d)		

SOT669 (LFPAK)

3. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
PH6325L	LFPAK	Plastic single-ended surface mounting package; 4 leads	SOT669

4. Limiting values

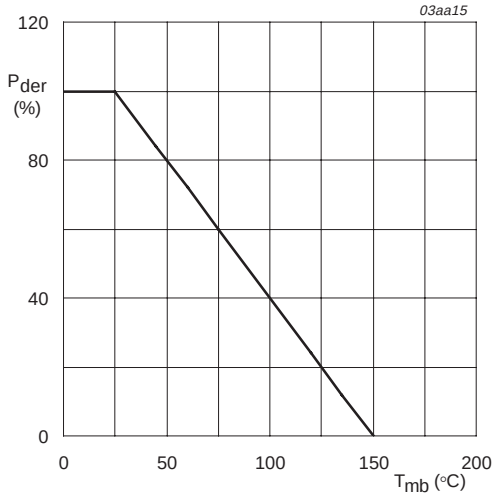
Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage (DC)	25 °C ≤ T_j ≤ 150 °C		-	25	V
V_{GS}	gate-source voltage			-	±20	V
I_D	drain current (DC)	T_{mb} = 25 °C; V_{GS} = 10 V; Figure 2 and 3		-	78.7	A
		T_{mb} = 100 °C; V_{GS} = 10 V; Figure 2		-	49.6	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs; Figure 3		-	236	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Figure 1		-	62.5	W
T_{stg}	storage temperature			–55	+150	°C
T_j	junction temperature			–55	+150	°C
Source-drain diode						
I_S	source (diode forward) current (DC)	T_{mb} = 25 °C		-	52	A
I_{SM}	peak source (diode forward) current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs		-	208	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; I_D = 34 A; t_p = 0.15 ms; V_{DD} = 25 V; R_{GS} = 50 Ω; V_{GS} = 10 V; starting at T_j = 25 °C		-	115	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	unclamped inductive load; I_D = 3.4 A; t_p = 0.015 ms; V_{DD} = 25 V; R_{GS} = 50 Ω; V_{GS} = 10 V; starting at T_j = 25 °C	[1] [2]	-	1.2	mJ

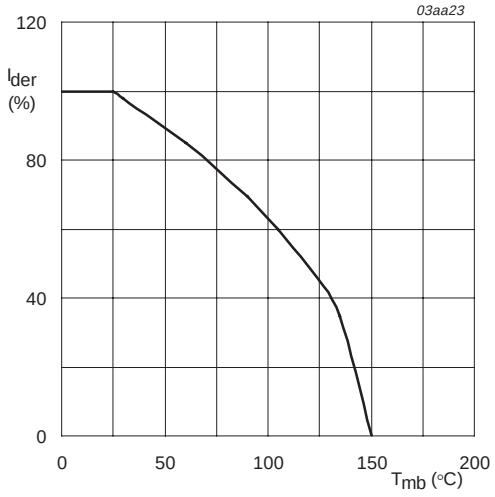
[1] Duty cycle is limited by the maximum junction temperature.

[2] Repetitive avalanche failure is not determined simply by thermal effects. Repetitive avalanche transients should only be applied for short bursts, not every switching cycle.



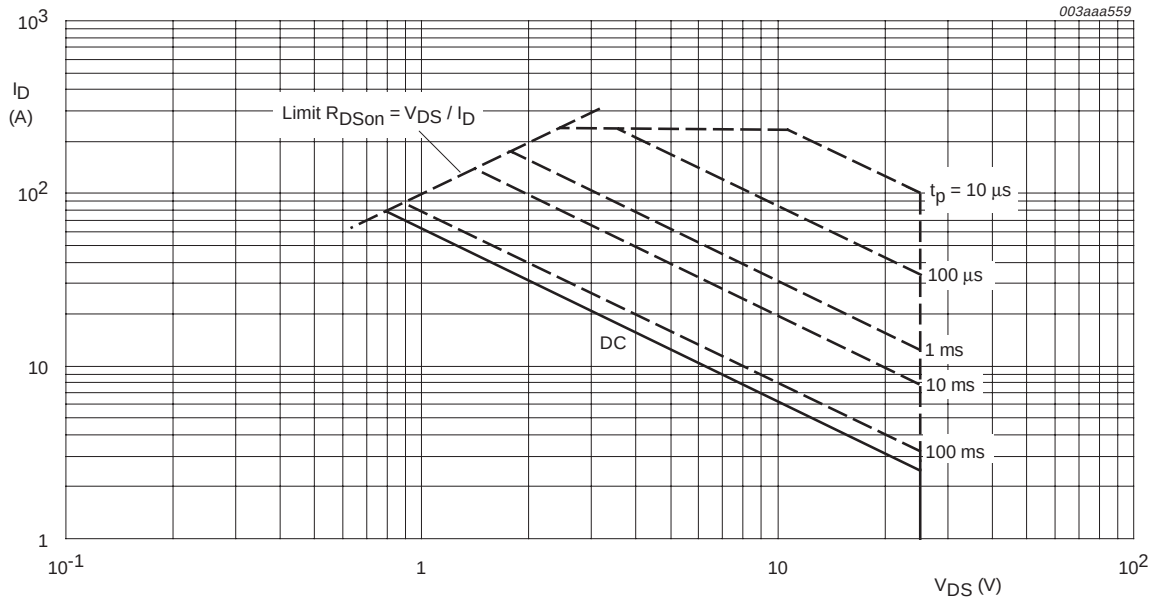
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T_{mb} = 25 °C; I_{DM} is single pulse; V_{GS} = 10 V

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	2	K/W

5.1 Transient thermal impedance

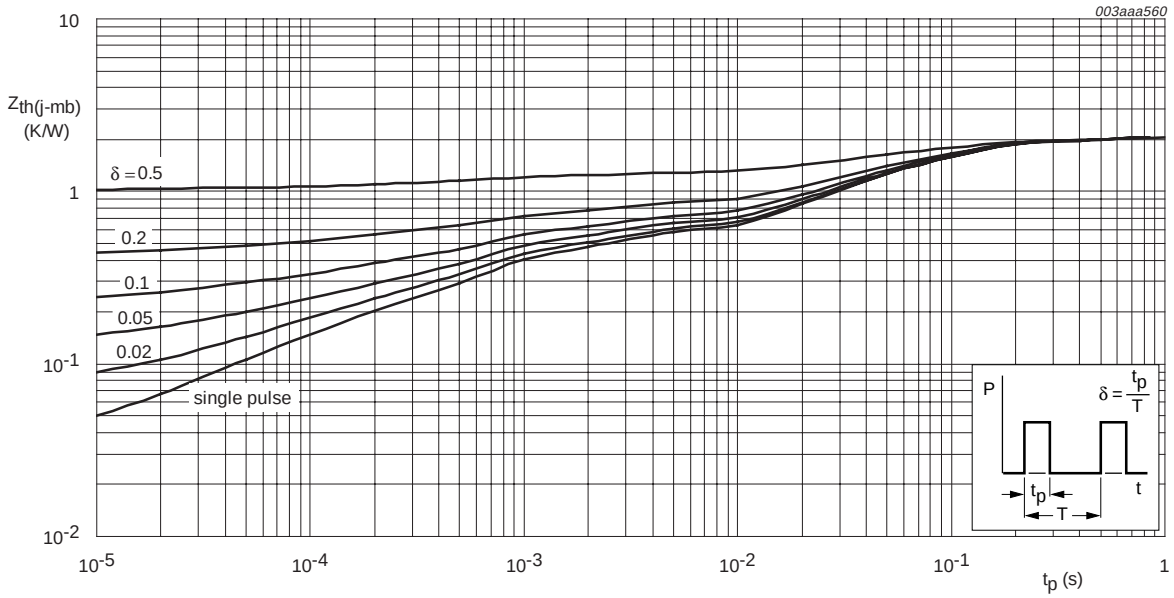


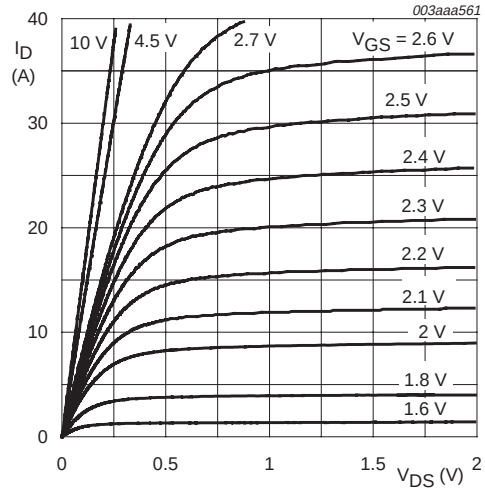
Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

6. Characteristics

Table 5: Characteristics

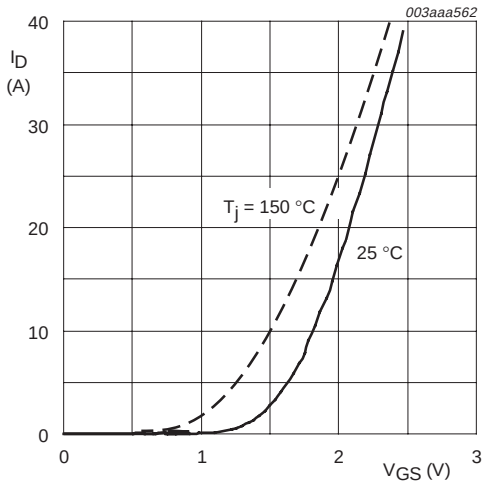
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V	25	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 9 and 10				
		T_j = 25 °C	1	1.5	2	V
		T_j = 150 °C	0.5	-	-	V
I_{DSS}	drain-source leakage current	V_{DS} = 25 V; V_{GS} = 0 V				
		T_j = 25 °C	-	0.06	1	µA
		T_j = 150 °C	-	-	500	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±16 V; V_{DS} = 0 V	-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 25 A; Figure 7 and 8				
		T_j = 25 °C	-	7.4	9.5	mΩ
		T_j = 150 °C	-	11.8	15.2	mΩ
		V_{GS} = 10 V; I_D = 25 A; Figure 7 and 8				
		T_j = 25 °C	-	4.7	6.3	mΩ
		T_j = 150 °C	-	7.5	10.1	mΩ
$R_{G(int)}$	internal gate resistance	f = 1 MHz	-	1.8	-	Ω
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 12 V; V_{GS} = 4.5 V; Figure 11 and 12	-	13.3	-	nC
Q_{gs}	gate-source charge		-	4.9	-	nC
Q_{gs1}	pre-$V_{GS(th)}$ gate-source charge		-	2.6	-	nC
Q_{gs2}	post-$V_{GS(th)}$ gate-source charge		-	2.3	-	nC
Q_{gd}	gate-drain (Miller) charge		-	3.3	-	nC
V_{plat}	plateau voltage		-	2.4	-	V
$Q_{g(tot)}$	total gate charge	I_D = 0 A; V_{DS} = 0 V; V_{GS} = 4.5 V	-	11.1	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 12 V; f = 1 MHz; Figure 13 and 14	-	1871	-	pF
C_{oss}	output capacitance		-	517	-	pF
C_{rss}	reverse transfer capacitance		-	179	-	pF
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 0 V; f = 1 MHz	-	2420	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 12 V; I_D = 25 A; V_{GS} = 4.5 V; R_G = 4.7 Ω	-	25	-	ns
t_r	rise time		-	25	-	ns
$t_{d(off)}$	turn-off delay time		-	32	-	ns
t_f	fall time		-	12	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 25 A; V_{GS} = 0 V; Figure 15	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = –100 A/µs; V_{GS} = 0 V; V_R = 25 V	-	33	-	ns
Q_r	recovered charge		-	13	-	nC



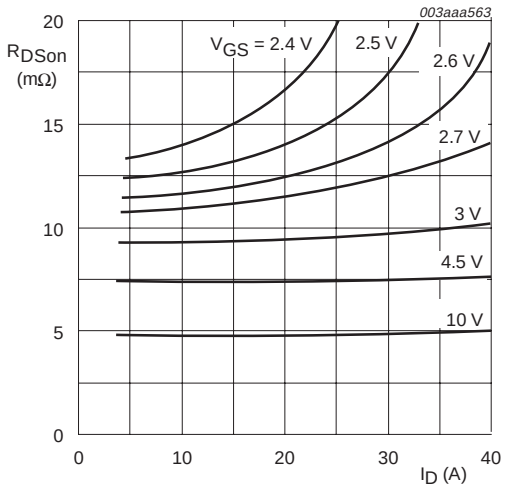
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



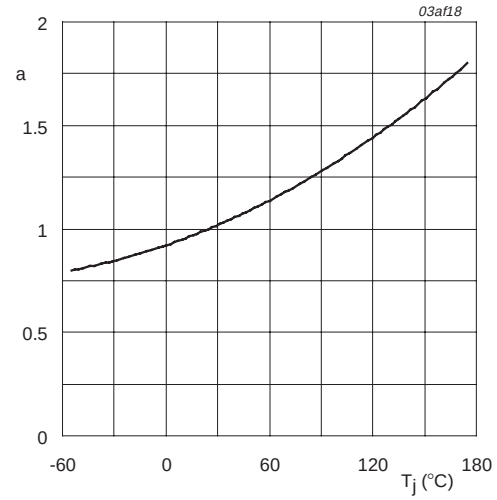
T_j = 25 °C and 150 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



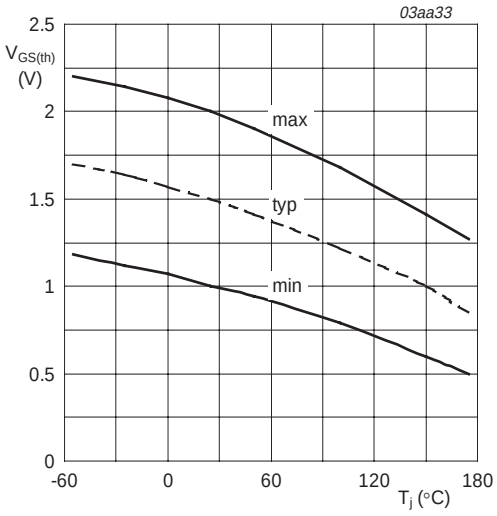
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



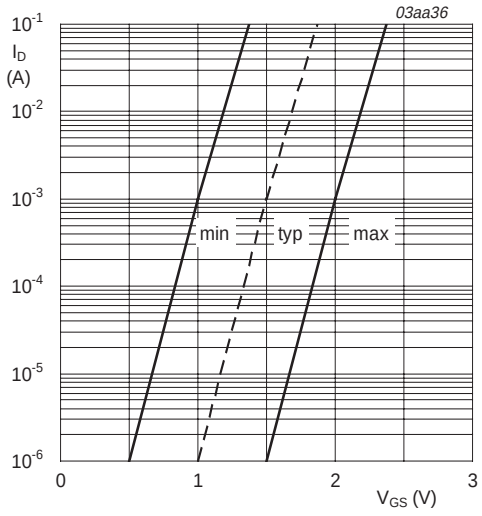
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



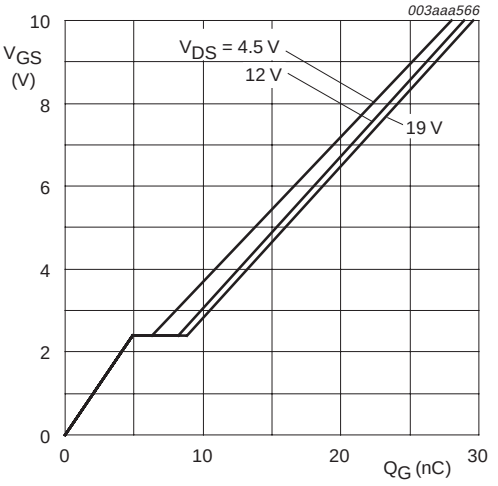
I_D = 1 mA; V_{DS} = V_{GS}

Fig 9. Gate-source threshold voltage as a function of junction temperature.



T_j = 25 °C; V_{DS} = 5 V

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



I_D = 25 A; V_{DS} = 4.5 V, 12 V and 19 V

Fig 11. Gate-source voltage as a function of gate charge; typical values.

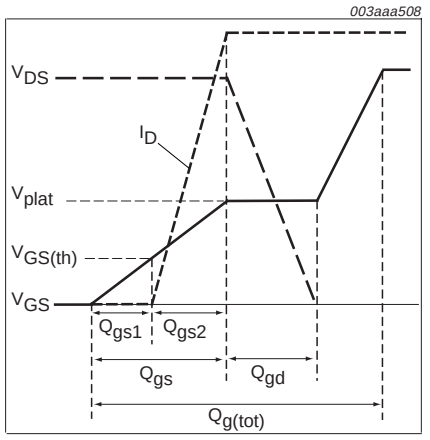
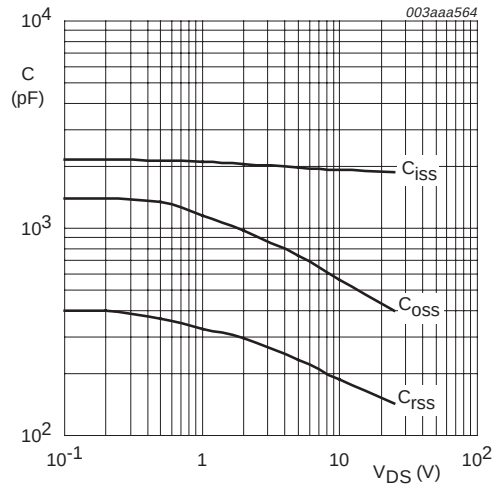
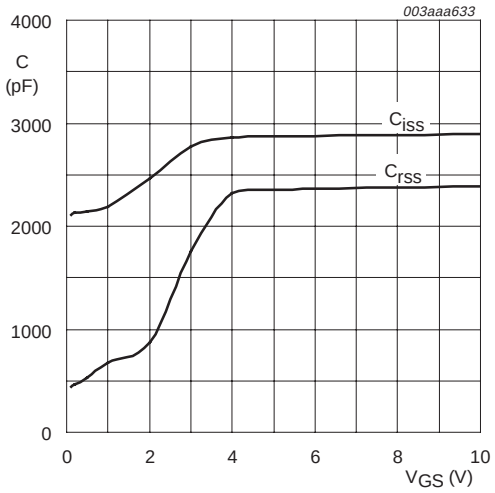


Fig 12. Gate charge waveform definitions.



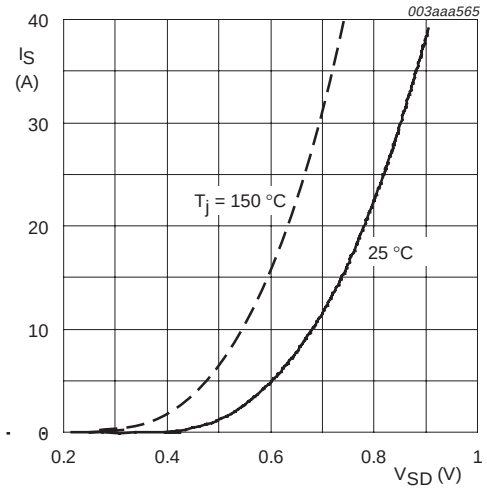
V_{GS} = 0 V; f = 1 MHz

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



T_j = 25 °C and 150 °C; V_{DS} = 0 V

Fig 14. Input and reverse transfer capacitances as a function of gate-source voltage; typical values.

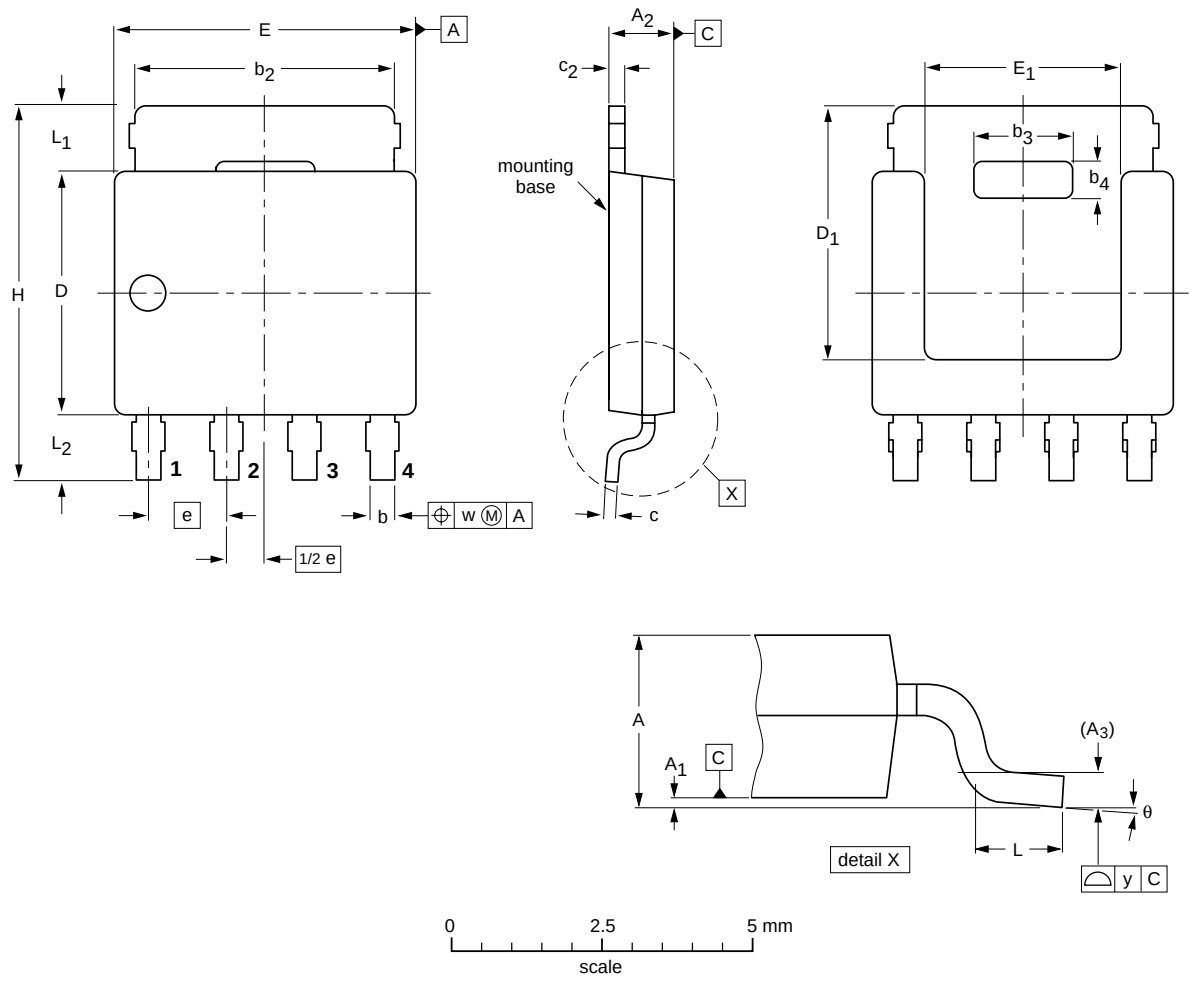


T_j = 25 °C and 150 °C; V_{GS} = 0 V

Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.

7. Package outline

Plastic single-ended surface mounted package (Philips version LFPAK); 4 leads **SOT669**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	A_2	A_3	b	b_2	b_3	b_4	c	c_2	$D^{(1)}$	$D_1^{(1)}$ max	$E^{(1)}$	$E_1^{(1)}$	e	H	L	L_1	L_2	w	y	θ
mm	1.20 1.01	0.15 0.00	1.10 0.95	0.25	0.50 0.35	4.41 3.62	2.2 2.0	0.9 0.7	0.25 0.19	0.30 0.24	4.10 3.80	4.20	5.0 4.8	3.3 3.1	1.27	6.2 5.8	0.85 0.40	1.3 0.8	1.3 0.8	0.25	0.1	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT669		MO-235				~~03-02-05~~ 03-09-15

Fig 16. SOT669 (LFPAK).

8. Soldering

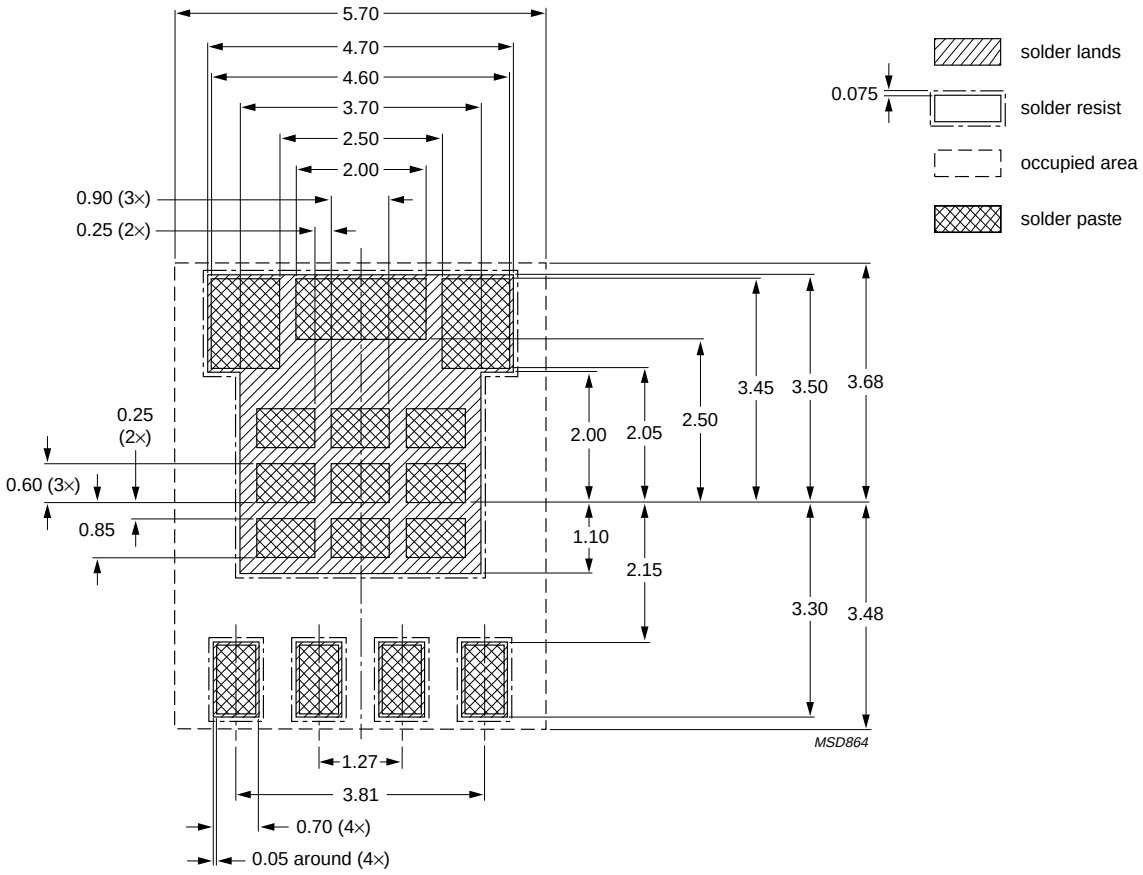


Fig 17. SOT669 (LFPAK) optimized soldering footprint

9. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20040428	-	Preliminary data (9397 750 12307)

10. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

11. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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