

PHK24NQ04LT

TrenchMOS™ logic level FET

Rev. 01 — 12 September 2003

Product data

1. Product profile

1.1 Description

N-channel logic level field-effect transistor in a plastic package using TrenchMOS™ technology.

Product availability:

PHK24NQ04LT in SOT96-1 (SO8).

1.2 Features

- Logic level compatible
- Low gate charge.

1.3 Applications

- DC-to-DC converters
- Switched-mode power supplies.

1.4 Quick reference data

- $V_{DS} \leq 40\text{ V}$
- $I_D \leq 21.2\text{ A}$
- $P_{tot} \leq 6.25\text{ W}$
- $R_{DS(on)} \leq 7.7\text{ m}\Omega$.

2. Pinning information

Table 1: Pinning - SOT96-1 (SO8) simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)	<p>Top view MBK187</p> <p>SOT96-1 (SO8)</p>	<p>MBB076</p>
4	gate (g)		
5,6,7,8	drain (d)		



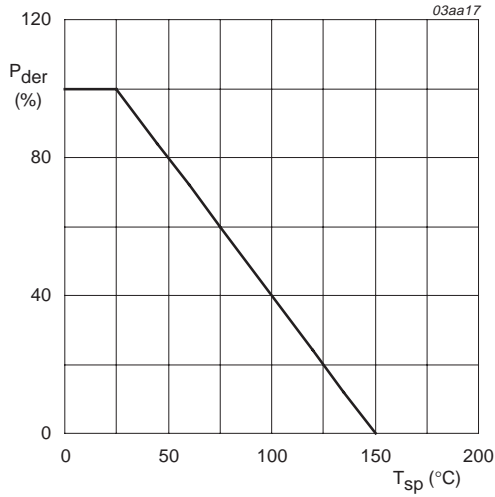
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3. Limiting values

Table 2: Limiting values

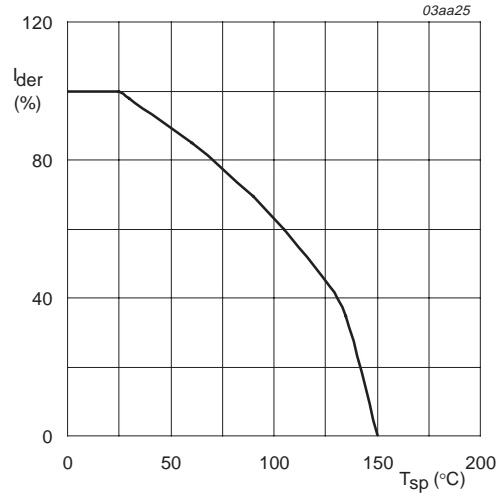
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	40	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	40	V
V_{GS}	gate-source voltage (DC)		-	± 20	V
I_D	drain current (DC)	$T_{sp} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; Figure 2 and 3	-	21.2	A
		$T_{sp} = 80\text{ °C}$; $V_{GS} = 10\text{ V}$; Figure 2	-	15.9	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	-	60	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; Figure 1	-	6.25	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	$T_{sp} = 25\text{ °C}$	-	5.2	A
I_{SM}	peak source (diode forward) current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	20.8	A



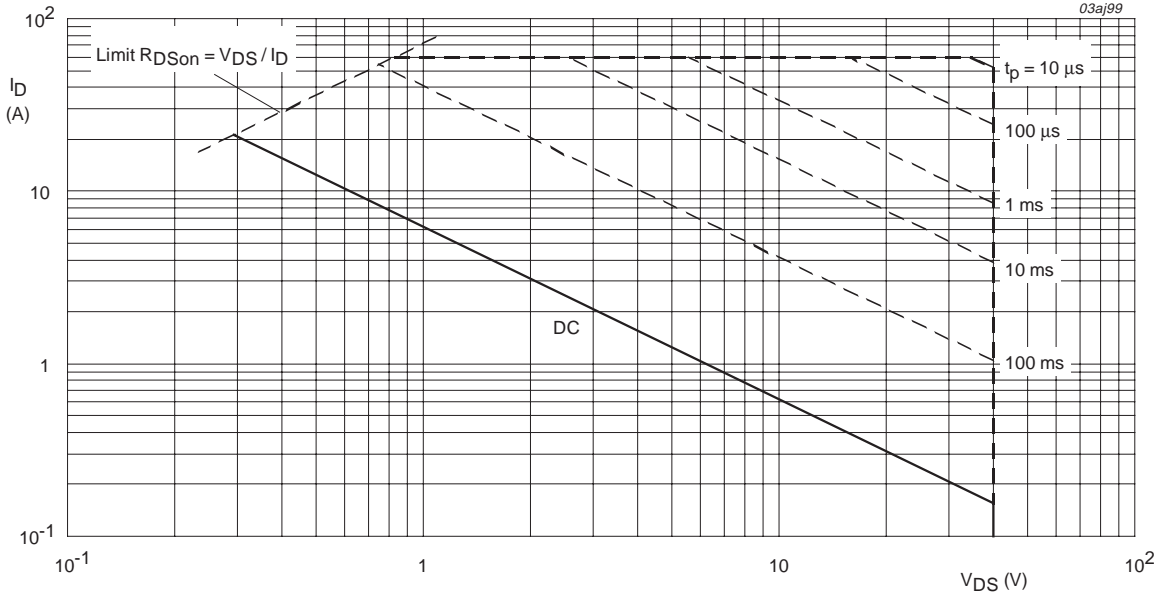
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



T_{sp} = 25 °C; I_{DM} is single pulse; V_{GS} = 10 V.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

4. Thermal characteristics

Table 3: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Figure 4	-	-	20	K/W

4.1 Transient thermal impedance

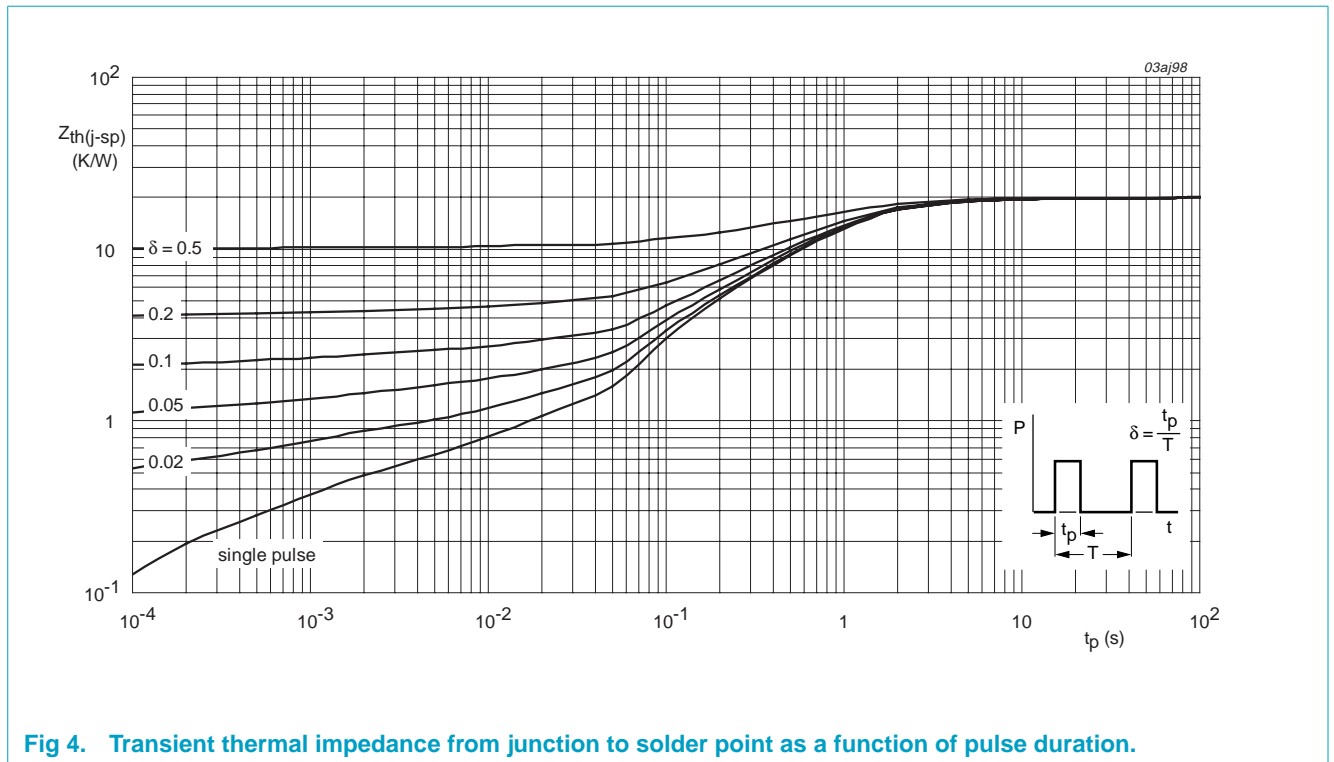
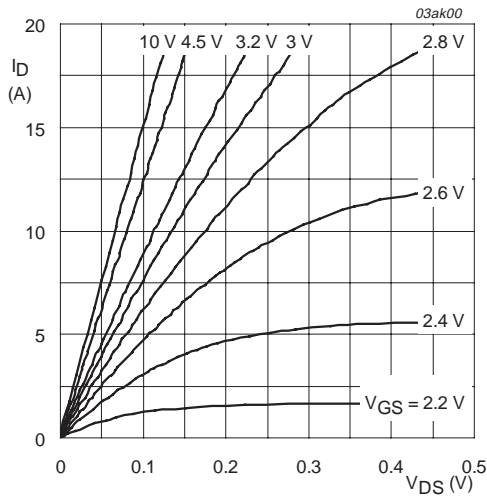


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration.

5. Characteristics

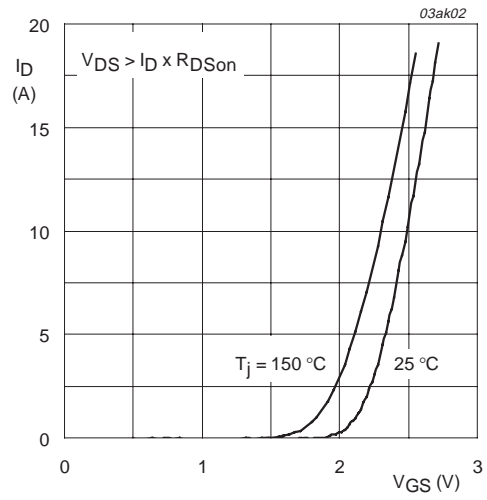
Table 4: Characteristics
 $T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$ $T_j = 25\text{ °C}$	40	-	-	V
		$T_j = -55\text{ °C}$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}$; $V_{DS} = V_{GS}$; Figure 9 $T_j = 25\text{ °C}$	1	1.5	2	V
		$T_j = 150\text{ °C}$	0.6	-	-	V
		$T_j = -55\text{ °C}$	-	-	2.2	V
I_{DSS}	drain-source leakage current	$V_{DS} = 40\ \text{V}$; $V_{GS} = 0\ \text{V}$ $T_j = 25\text{ °C}$	-	0.05	1	μA
		$T_j = 150\text{ °C}$	-	-	500	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 16\ \text{V}$; $V_{DS} = 0\ \text{V}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\ \text{V}$; $I_D = 12\ \text{A}$; Figure 7 and 8 $T_j = 25\text{ °C}$	-	7.8	9.2	m Ω
		$T_j = 150\text{ °C}$	-	14	16.6	m Ω
		$V_{GS} = 10\ \text{V}$; $I_D = 14\ \text{A}$; Figure 7 and 8	-	6.5	7.7	m Ω
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$I_D = 14\ \text{A}$; $V_{DD} = 20\ \text{V}$; $V_{GS} = 10\ \text{V}$; Figure 13	-	64	-	nC
Q_{gs}	gate-source charge		-	7.7	-	nC
Q_{gd}	gate-drain (Miller) charge		-	11.5	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\ \text{V}$; $V_{DS} = 25\ \text{V}$; $f = 1\ \text{MHz}$; Figure 11	-	2985	-	pF
C_{oss}	output capacitance		-	490	-	pF
C_{riss}	reverse transfer capacitance		-	240	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 20\ \text{V}$; $I_D = 1\ \text{A}$; $V_{GS} = 5\ \text{V}$; $R_G = 6\ \Omega$	-	30	-	ns
t_r	rise time		-	30	-	ns
$t_{d(off)}$	turn-off delay time		-	60	-	ns
t_f	fall time		-	40	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 2.3\ \text{A}$; $V_{GS} = 0\ \text{V}$; Figure 12	-	0.75	1.2	V
t_{rr}	reverse recovery time	$I_S = 2\ \text{A}$; $di_S/dt = -100\ \text{A}/\mu\text{s}$; $V_{GS} = 0\ \text{V}$	-	49	-	ns
Q_r	recovered charge		-	36	-	nC



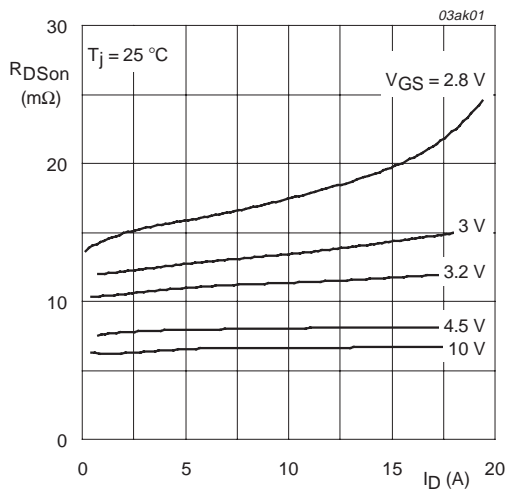
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



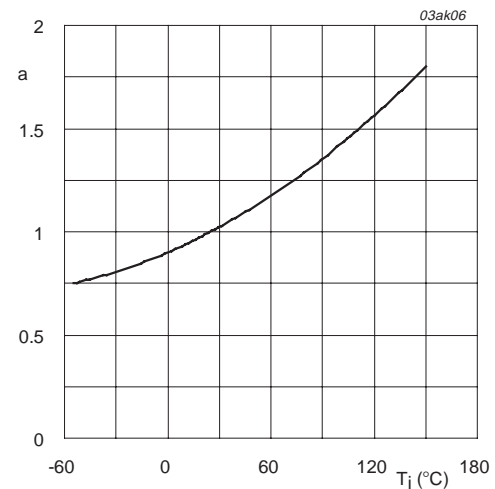
$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



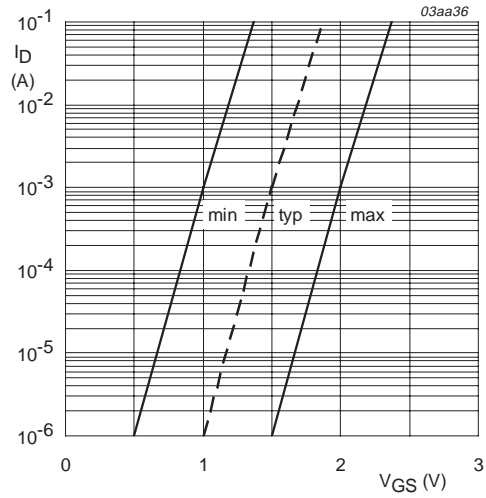
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



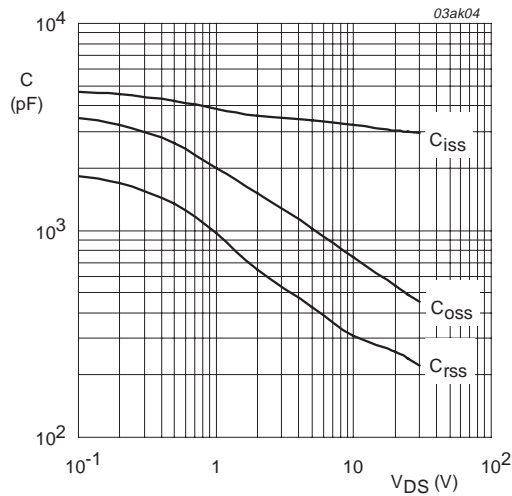
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



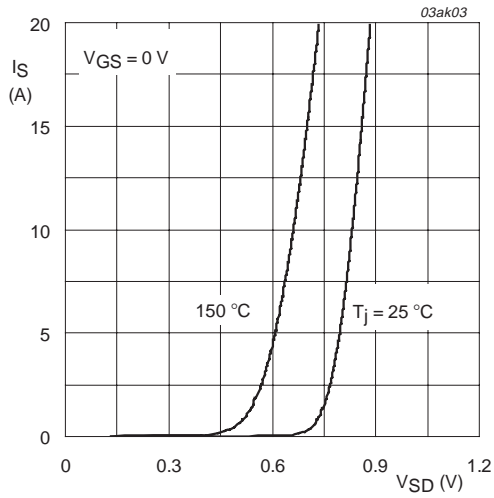
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



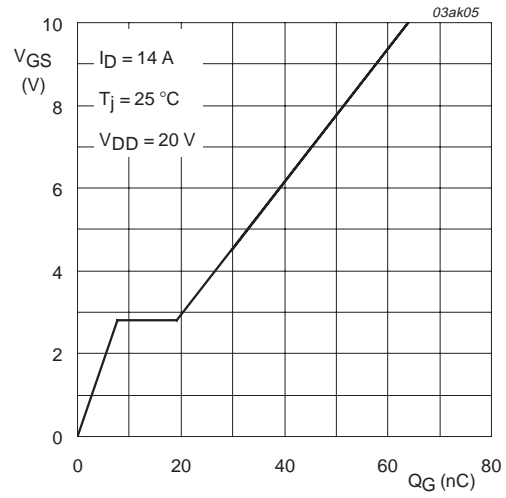
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{GS} = 0\text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 14\text{ A}$; $V_{DD} = 20\text{ V}$

Fig 13. Gate-source voltage as a function of gate charge; typical values.

6. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

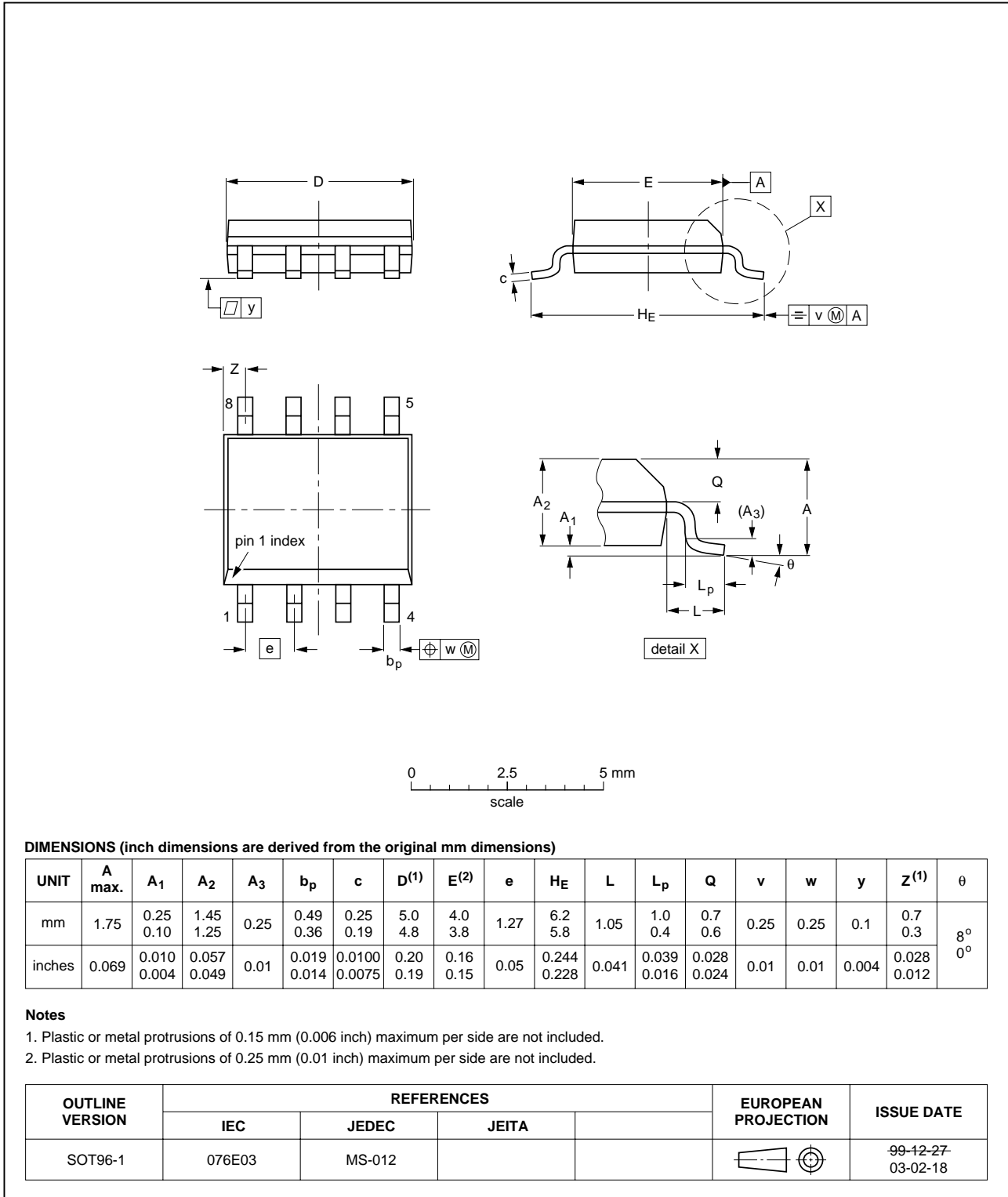


Fig 14. SOT96-1 (SO8).

7. Revision history

Table 5: Revision history

Rev	Date	CPCN	Description
01	20030912	-	Product data (9397 750 11709)

8. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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