

**Product Features**

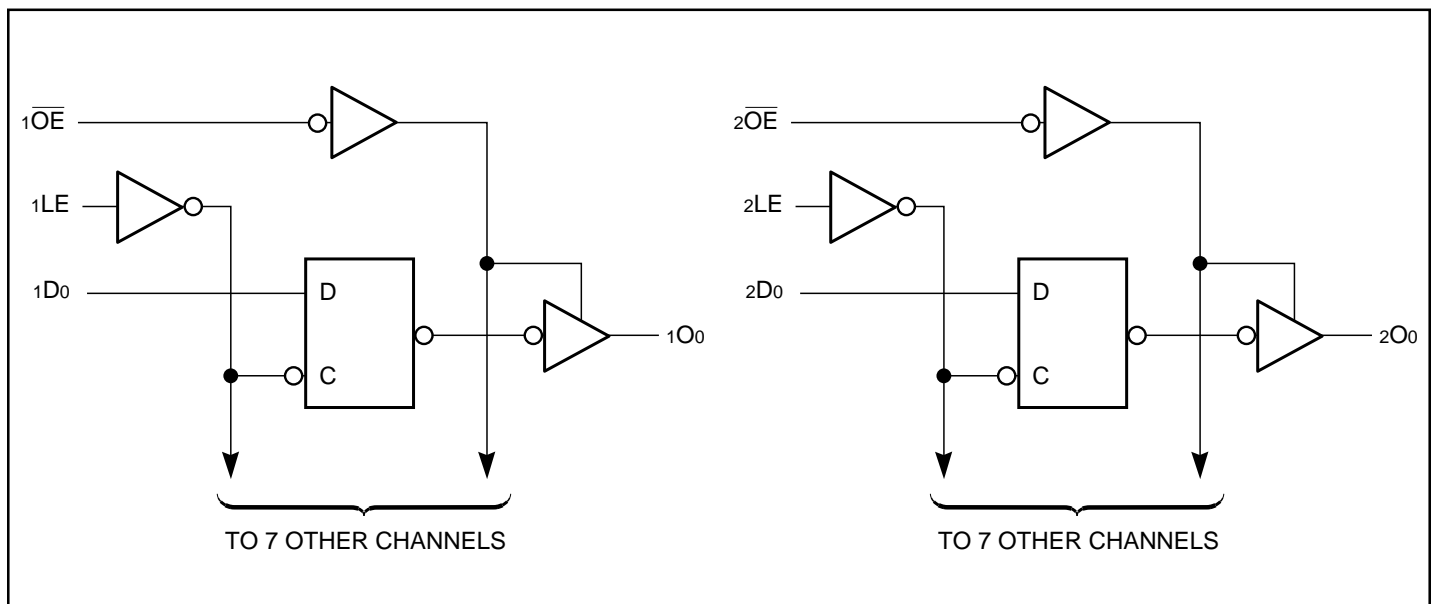
- Advanced Low Power CMOS Operation
- Can serve as a 5V to 3V translator
- Excellent output drive capability:  
Balanced drives (24mA sink and source)  
Compatible with LVC™ class of products.
- Pin compatible with industry standard double-density pinouts
- Low ground bounce outputs
- Hysteresis on all inputs
- Industrial operating temperature range: -40°C to +85°C
- Inputs can be driven by 3.3V or 5V devices
- Multiple center pin and distributed Vcc/GND pins minimizing switching noise
- Packages available:  
-48-pin 240 mil wide plastic TSSOP (A)  
-48-pin 300 mil wide plastic SSOP (V)  
-48-pin 173 mil wide plastic TVSOP (K)
- Device models available on request

**Product Description**

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT163373 is a 16-bit transparent latch designed with 3-state outputs and are intended for bus oriented applications. The Output Enable and Latch Enable controls are organized to operate as two 8-bit latches or one 16-bit latch. When Latch Enable (LE) is HIGH, the flip-flops appear transparent to the data. The data that meets the set-up time when LE is LOW is latched. When OE is HIGH, the bus output is in the high impedance state.

**Logic Block Diagram**



### Product Pin Description

Pin Name	Description
$\overline{xOE}$	3-State Output Enable Inputs (Active LOW)
$xLE$	Latch Enable Inputs (Active HIGH)
$xDx$	Data Inputs
$xOx$	3-State Outputs
GND	Ground
Vcc	Power

### Truth Table

Inputs <sup>(1)</sup>			Outputs <sup>(1)</sup>
$xDx$	$xLE$	$\overline{xOE}$	$xOx$
H	H	L	H
L	H	L	L
X	X	H	Z

**Note:**

1. H = High Voltage Level, X = Don't Care, L = Low Voltage Level, Z = High Impedance

### Product Pin Configuration

$\overline{1OE}$	1	48-PIN V48 A48 K48	48	1LE
1O0	2		47	1D0
1O1	3		46	1D1
GND	4		45	GND
1O2	5		44	1D2
1O3	6		43	1D3
Vcc	7		42	Vcc
1O4	8		41	1D4
1O5	9		40	1D5
GND	10		39	GND
1O6	11		38	1D6
1O7	12		37	1D7
2O0	13	36	2D0	
2O1	14	35	2D1	
GND	15	34	GND	
2O2	16	33	2D2	
2O3	17	32	2D3	
Vcc	18	31	Vcc	
2O4	19	30	2D4	
2O5	20	29	2D5	
GND	21	28	GND	
2O6	22	27	2D6	
2O7	23	26	2D7	
$\overline{2OE}$	24	25	2LE	

### Capacitance (T<sub>A</sub> = 25°C, f = 1 MHz)

Parameters <sup>(1)</sup>	Description	Test Conditions	Typ.	Max.	Units
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4.5	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	5.5	8	pF

**Note:**

1. This parameter is determined by device characterization but is not production tested.

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-55°C to +125°C
Ambient Temperature with Power Applied .....	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only) ..	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage .....	-0.5V to +7.0V
DC Output Current .....	120 mA
Power Dissipation .....	1.0W

#### Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### DC Electrical Characteristics (Over the Operating Range, TA = -40°C to +85°C, VCC = 2.7V to 3.6V)

Parameters	Description	Test Conditions <sup>(1)</sup>		Min.	Typ <sup>(2)</sup>	Max.	Units
VIH	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level		2.2	—	5.5	V
	Input HIGH Voltage (I/O pins)			2.0	—	VCC+0.5	V
VIL	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level		-0.5	—	0.8	V
IIH	Input HIGH Current (Input pins)	VCC = Max.	VIN = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)	VCC = Max.	VIN = VCC	—	—	±1	µA
IIL	Input LOW Current (Input pins)	VCC = Max.	VIN = GND	—	—	±1	µA
	Input LOW Current (I/O pins)	VCC = Max.	VIN = GND	—	—	±1	µA
IOZH	High Impedance Output Current (3-State Output pins)	VCC = Max.	VOUT = VCC	—	—	±1	µA
IOZL		VCC = Max.	VOUT = GND	—	—	±1	µA
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18 mA		—	-0.7	-1.2	V
IODH	Output HIGH Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V <sup>(3)</sup>		-36	-60	-110	mA
IODL	Output LOW Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V <sup>(3)</sup>		50	90	200	mA
VOH	Output HIGH Voltage	VCC = Min.	I <sub>OH</sub> = -0.1mA	VCC-0.2	—	—	V
		VIN = VIH or VIL	I <sub>OH</sub> = -3mA	2.4	3.0	—	V
		VCC = 3.0V,	I <sub>OH</sub> = -8mA	2.4 <sup>(5)</sup>	3.0	—	V
		VIN = VIH or VIL	I <sub>OH</sub> = -24mA	2.0	—	—	V
VOL	Output LOW Voltage	VCC = Min.	I <sub>OL</sub> = 0.1mA	—	—	0.2	V
		VIN = VIH or VIL	I <sub>OL</sub> = 16mA	—	0.2	0.4	V
			I <sub>OL</sub> = 24mA	—	0.3	0.5	V
Ios mA	Short Circuit Current <sup>(4)</sup>	VCC = Max. <sup>(3)</sup> , VOUT = GND		—	-60	-85	-240
VH	Input Hysteresis			—	150	—	mV

#### Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at VCC = 3.3V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. VOH = VCC - 0.6V at rated current.

**Power Supply Characteristics**

Parameters	Description	Test Conditions <sup>(1)</sup>		Min.	Typ <sup>(2)</sup>	Max.	Units
I <sub>CC</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = Max.	V <sub>IN</sub> = GND or V <sub>CC</sub>		0.1	10	μA
ΔI <sub>CC</sub>	Quiescent Power Supply Current TTL Inputs HIGH	V <sub>CC</sub> = Max.	V <sub>IN</sub> = V <sub>CC</sub> – 0.6V <sup>(3)</sup>		2.0	30	μA
I <sub>CCD</sub>	Dynamic Power Supply <sup>(4)</sup>	V <sub>CC</sub> = Max., Outputs Open x $\overline{\text{OE}}$ = GND xLE = V <sub>CC</sub> One Bit Toggling 50% Duty Cycle	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND		50	75	μA/ MHz
I <sub>C</sub>	Total Power Supply Current <sup>(6)</sup>	V <sub>CC</sub> = Max., Outputs Open f <sub>i</sub> = 10 MHz 50% Duty Cycle x $\overline{\text{OE}}$ = GND xLE = V <sub>CC</sub> One Bit Toggling	V <sub>IN</sub> = V <sub>CC</sub> – 0.6V V <sub>IN</sub> = GND		0.5	0.8	mA
		V <sub>CC</sub> = Max., Outputs Open f <sub>i</sub> = 2.5 MHz 50% Duty Cycle x $\overline{\text{OE}}$ = GND xLE = V <sub>CC</sub> 16 Bits Toggling	V <sub>IN</sub> = V <sub>CC</sub> – 0.6V V <sub>IN</sub> = GND		2.0	3.3 <sup>(5)</sup>	

**Notes:**

- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.
- Per TTL driven input; all other inputs at V<sub>CC</sub> or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.
- I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>

$$I_C = I_{CC} + \Delta I_{CC} \text{ DHNT} + I_{CCD} (f_{CP}/2 + f_i N_i)$$

$$I_{CC} = \text{Quiescent Current (ICCL, ICCH and ICCZ)}$$

$$\Delta I_{CC} = \text{Power Supply Current for a TTL High Input}$$

$$\text{DH} = \text{Duty Cycle for TTL Inputs High}$$

$$\text{NT} = \text{Number of TTL Inputs at DH}$$

$$I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$$

$$f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$$

$$\text{NCP} = \text{Number of Clock Inputs at } f_{CP}$$

$$f_i = \text{Input Frequency}$$

$$N_i = \text{Number of Inputs at } f_i$$

All currents are in milliamps and all frequencies are in megahertz.

**Switching Characteristics over Operating Range<sup>(1)</sup>**

Parameters	Description	Conditions <sup>(2)</sup>	FCT163373		FCT163373A		FCT163373C		Units
			Com.		Com.		Com.		
			Min. <sup>(3)</sup>	Max.	Min. <sup>(3)</sup>	Max.	Min. <sup>(3)</sup>	Max.	
tPLH tPHL	Propagation Delay xDx to xOx	CL = 50 pF RL = 500Ω	1.5	8.0	1.5	5.2	1.5	4.2	ns
tPLH tPHL	Propagation Delay xLE to xOx		2.0	13.0	2.0	8.5	2.0	5.5	ns
tPZH tPZL	Output Enable Time xOE to xOx		1.5	12.0	1.5	6.5	1.5	5.5	ns
tPHZ tPLZ	Output Disable Time <sup>(4)</sup> xOE to xOx		1.5	7.5	1.5	5.5	1.5	5.0	ns
tSU	Setup Time HIGH or LOW, xDx to xLE		2.0		2.0		2.0		ns
tH	Hold Time HIGH or LOW, xDx to xLE		1.5		1.5		1.5		ns
tW	xLE Pulse Width HIGH		6.0		5.0		5.0		ns
tSK(o)	Output Skew <sup>(5)</sup>			0.5		0.5		0.5	ns

**Notes:**

1. Propagation Delays and Enable/Disable times are with  $V_{CC} = 3.3V \pm 0.3V$ , normal range. For  $V_{CC} = 2.7V$ , extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
2. See test circuit and wave forms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.
4. This parameter is guaranteed but not production tested.
5. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.