PLL620-05/-06/-07/-08/-09

Low Phase Noise XO with multipliers (for 100-200MHz Fund or 3rdOT Xtal)

Universal Low Phase Noise IC's

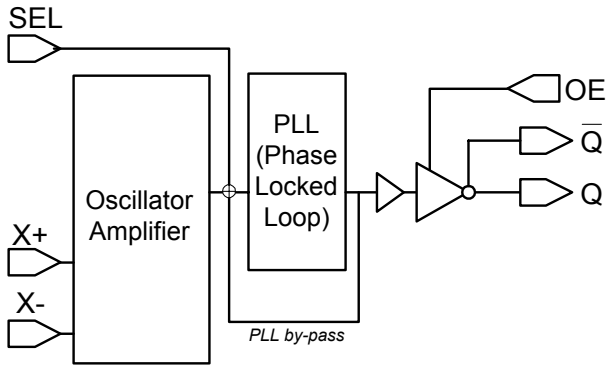
FEATURES

- 100MHz to 200MHz Fundamental or 3rd Overtone Crystal.
- Output range: 100 – 200MHz (no multiplication), 200 – 400MHz (2x multiplier), 400 – 700MHz (4x multiplier), or 800MHz-1GHz(PLL620-09 only, 8x multiplier).
- CMOS (Standard drive PLL620-07 or Selectable Drive PLL620-06), PECL (Enable low PLL620-08 or Enable high PLL620-05) or LVDS output (PLL620-09).
- Supports 3.3V-Power Supply.
- Available in 16-Pin (TSSOP or 3x3mm QFN)
  Note: PLL620-06 only available in 3x3mm.
  Note: PLL620-07 only available in TSSOP.

DESCRIPTION

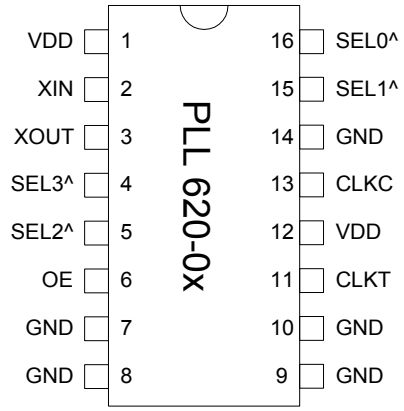
The PLL620-0x family of XO IC's is specifically designed to work with high frequency fundamental and third overtone crystals. Their low jitter and low phase noise performance make them well suited for high frequency XO requirements. They achieve very low current into the crystal resulting in better overall stability.

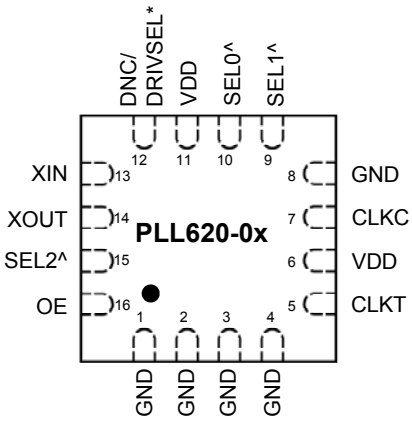
BLOCK DIAGRAM



PIN CONFIGURATION

(Top View)





^: Internal pull-up

*: PLL620-06 pin 12 is output drive select (DRIVSEL)
(0 for High Drive CMOS, 1 for Standard Drive CMOS)
The pin remains 'Do Not Connect (DNC)' for PLL620-05/07/08/09.

OUTPUT ENABLE LOGICAL LEVELS

Part #	OE	State
PLL620-08	0 (Default)	Output enabled
	1	Tri-state
PLL620-05	0	Tri-state
PLL620-06 PLL620-07 PLL620-09	1 (Default)	Output enabled

OE input: Logical states defined by PECL levels for PLL620-08
Logical states defined by CMOS levels for PLL620-05/-06/-07/-09

PIN DESCRIPTIONS

Name	TSSOP* Pin number	3x3mm QFN* Pin number	Type	Description
VDD	1, 12	6,11	P	+3.3V power supply.
XIN	2	13	I	Crystal input. See Crystal Specification on page 3.
XOUT	3	14	I	Crystal output. See Crystal Specification on page 3.
OE	6	16	I	Output enable.
GND	7,8,9, 10, 14	1,2,3,4,8	P	Ground (except pin 12 on PLL620-06: DRIVSEL see below).
DRIVSEL**	-	12	I	PLL620-06 only: Drive Select Input. This pin has an internal pull-up that will default DRIVSEL to '1' when not connect to GND. CMOS output of PLL620-06 will be high drive CMOS when DRIVSEL is set to '0', and will be standard CMOS otherwise. The pin remains 'Do Not Connect (DNC)' for PLL620-05/07/08/09.
CLKT	11	5	O	True output PECL (PLL620-08) or LVDS (PLL620-09) (N/C for PLL620-07)
CLKC	13	7	O	Complementary output PECL (PLL620-08) or LVDS (PLL620-09) (CMOS out for PLL620-07).
SEL0	16	10	I	Multiplier selector pins. These pins have an internal pull-up that will default SEL to '1' when not connected to GND.
SEL1	15	9	I	
SEL2	5	15	I	
SEL3	4	Not available	I	

* Note: PLL620-06 only available in 3x3mm QFN, PLL620-07 only available in TSSOP.
** Note: DRIVSEL on pin 12 on PLL620-06 only. The pin remains 'Do Not Connect (DNC)' for PLL620-05/07/08/09.

FREQUENCY SELECTION TABLE

SEL3	SEL2	SEL1	SEL0	Selected Multiplier
0	0	1	1	Fin x 8(PLL620-09 only)
1	0	1	1	Fin x 4
1	1	1	0	Fin x 2
1	1	1	1	No multiplication

Note: SEL3 is not available (always "1") in 3x3mm package
All pins have internal pull-ups (default value is 1). Connect to GND to set to 0.

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note**: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

2. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	F_{XIN}	Fundamental or 3rd overtone*	100		200	MHz
Crystal Loading Rating	$C_{L\ (xtal)}$			5		pF
Interelectrode Capacitance	C_0				5	pF
Recommended ESR	R_E	AT cut			30	Ω

* **Note**: 3rd overtone crystals require an external resistor between XIN and XOUT to prevent the fundamental from oscillating.

3. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current (Loaded Outputs)	I_{DD}	PECL/LVDS/CMOS			100/80/40	mA
Operating Voltage	V_{DD}		2.97		3.63	V
Output Clock Duty Cycle		@ 50% V_{DD} (CMOS) @ 1.25V (LVDS) @ V_{DD} – 1.3V (PECL)	45 45 45	50 50 50	55 55 55	%
Short Circuit Current				±50		mA

4. Jitter Specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Period jitter RMS	At 155.52MHz, with capacitive decoupling between VDD and GND. Over 10,000 cycles		2.5		ps
Period jitter peak-to-peak			18.5	20	
Accumulated jitter RMS	At 155.52MHz, with capacitive decoupling between VDD and GND. Over 1,000,000 cycles.		2.5		ps
Accumulated jitter peak-to-peak			24	27	
Random Jitter	"RJ" measured on Wavecrest SIA 3000		2.5		ps
Integrated jitter RMS at 155MHz	Integrated 12 kHz to 20 MHz		0.3	0.4	ps
Period jitter RMS	At 622.08MHz, with capacitive decoupling between VDD and GND. Over 10,000 cycles		11		ps
Period jitter peak-to-peak			45	49	
Accumulated jitter RMS	At 622.08MHz, with capacitive decoupling between VDD and GND. Over 1,000,000 cycles.		11		ps
Accumulated jitter peak-to-peak			24	27	
Random Jitter	"RJ" measured on Wavecrest SIA 3000		3		ps
Integrated jitter RMS at 622MHz	Integrated 12 kHz to 20 MHz		1.6	1.8	ps

5. Phase Noise Specifications

PARAMETERS	FREQUENCY	@10Hz	@100Hz	@1kHz	@10kHz	@100kHz	UNITS
Phase Noise relative to carrier	155.52MHz	-75	-95	-125	-140	-145	dBc/Hz
	622.08MHz	-75	-95	-110	-125	-120	

6. CMOS Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output drive current (High Drive)	I_{OH}	V_{OH}= V_{DD}-0.4V, V_{DD}=3.3V	30			mA
	I_{OL}	V_{OL} = 0.4V, V_{DD} = 3.3V	30			mA
Output drive current (Standard Drive)	I_{OH}	V_{OH}= V_{DD}-0.4V, V_{DD}=3.3V	10			mA
	I_{OL}	V_{OL} = 0.4V, V_{DD} = 3.3V	10			mA
Output Clock Rise/Fall Time (Standard Drive)		0.3V ~ 3.0V with 15 pF load		2.4		ns
Output Clock Rise/Fall Time (High Drive)		0.3V ~ 3.0V with 15 pF load		1.2		

* Note: High Drive CMOS is available on PLL620-06 through DRIVSEL selector input on pin 12.

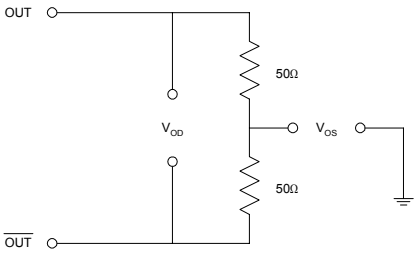
7. LVDS Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	V_{OD}	R_L = 100 Ω (see figure)	247	355	454	mV
V_{DD} Magnitude Change	ΔV_{OD}		-50		50	mV
Output High Voltage	V_{OH}			1.4	1.6	V
Output Low Voltage	V_{OL}		0.9	1.1		V
Offset Voltage	V_{OS}		1.125	1.2	1.375	V
Offset Magnitude Change	ΔV_{OS}		0	3	25	mV
Power-off Leakage	I_{OXD}	V_{out} = V_{DD} or GND, V_{DD} = 0V		±1	±10	uA
Output Short Circuit Current	I_{OSD}			-5.7	-8	mA

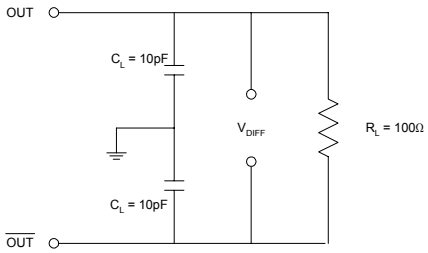
8. LVDS Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	t_r	R_L = 100 Ω, C_L = 10 pF (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	t_f		0.2	0.7	1.0	ns

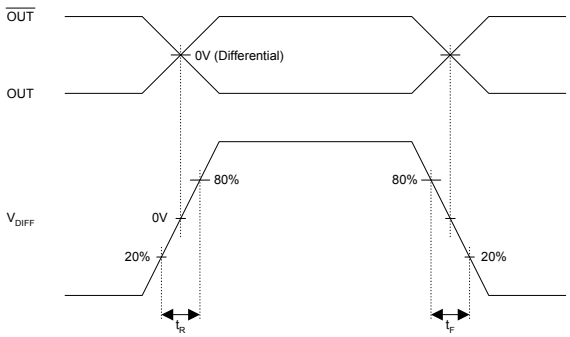
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transistion Time Waveform



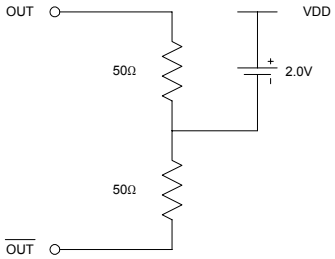
9. PECL Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Output High Voltage	V_{OH}	R_L = 50 Ω to (V_{DD} – 2V) (see figure)	V_{DD} – 1.025		V
Output Low Voltage	V_{OL}			V_{DD} – 1.620	V

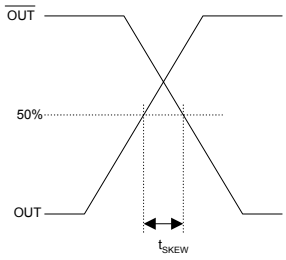
19. PECL Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Clock Rise Time	t_r	@20/80% - PECL		0.6	1.5	ns
Clock Fall Time	t_f	@80/20% - PECL		0.5	1.5	ns

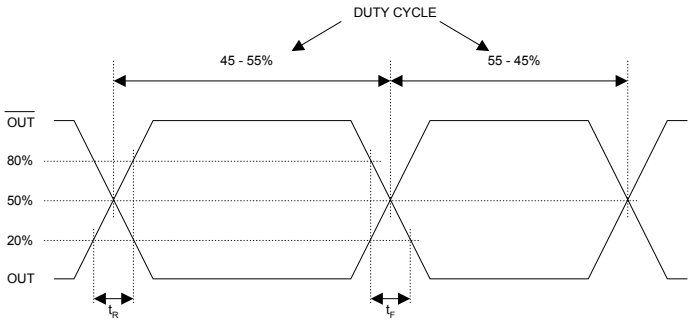
PECL Levels Test Circuit



PECL Output Skew

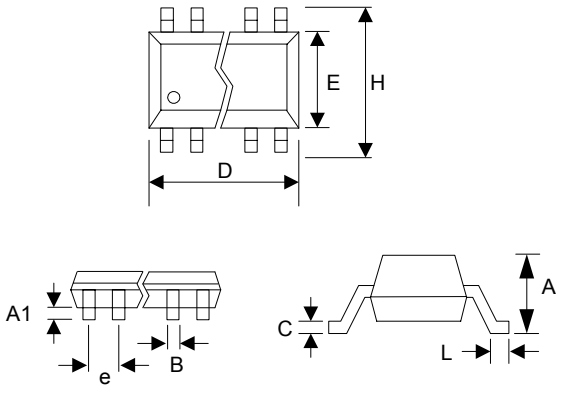


PECL Transistion Time Waveform



PACKAGE INFORMATION

16 PIN TSSOP (mm)		
Symbol	Min.	Max.
A	-	1.20
A1	0.05	0.15
B	0.19	0.30
C	0.09	0.20
D	4.90	5.10
E	4.30	4.50
H	6.40 BSC	
L	0.45	0.75
e	0.65 BSC	



3mm x 3mm, QFN

VARIATIONS.

SYMBOL	16 LD		
	MIN	NOM	MAX
e	0.50 BSC		
b	0.18	0.23	0.30
L	0.30	0.40	0.50
ND	4		
NE	4