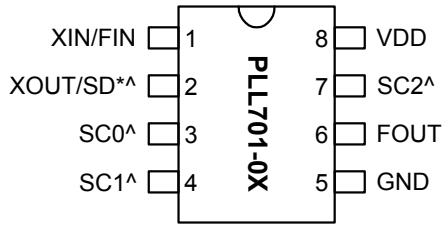
PLL701-01/02/04/06

Low EMI Spread Spectrum Multiplier Clock

FEATURES

- Spread Spectrum Clock Generator with selectable multiplier from 1x to 6x outputs.
- Output frequency ranges: 10MHz to 180MHz.
- Accepts input from crystal or reference clock.
- Selectable Center, Down or Asymmetric Spread Modulation.
- Selectable Modulation rate.
- TTL/CMOS compatible outputs.
- 3.3V Operating Voltage.
- Low short term jitter.
- Available in 8-Pin 150mil SOIC.

PIN CONFIGURATION



XIN/FIN = 10 ~ 30 MHz

Note: ^: Internal pull-up resistor (120kΩ for SD, 30 kΩ for SC0-SC2).

*: The value of SD is latched upon power-up. The internal pull-up resistor results in a default high value when no pull-down resistor is connected to this pin (recommended external pull-down resistor of 27 kΩ).

DESCRIPTION

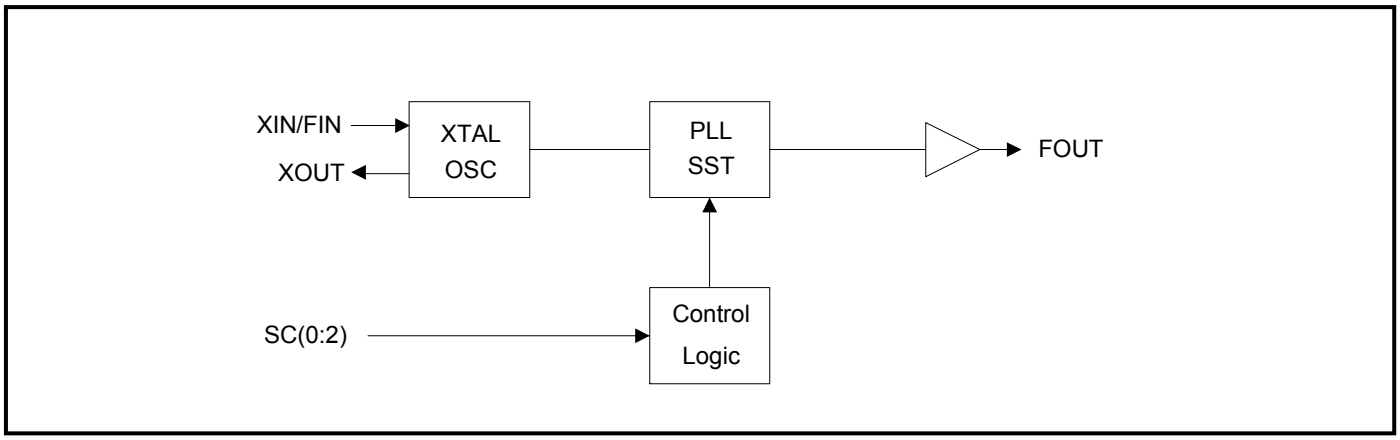
The PLL701-01/02/04/06 are Spread Spectrum Clock Generators designed for the purpose of reducing EMI in high-speed digital systems. Any output frequency from 10 to 180MHz can be selected by programming 6 multiplier modes. The device is designed to operate from a crystal or reference clock input and provides 1x to 6x modulated clock outputs.

OUTPUT CLOCK (FOUT) SELECTION

SD	SC2	SC1	SC0	FOUT (-01)	FOUT (-02)	FOUT (-04)	FOUT (-06)	SST Modulation			
								Magnitude	Freq.	Type	
1	0	0	0	X1	X2	X4	X6	0.50%	Fin / 512	C	±0.25%
1	0	0	1	X1	X2	X4	X6	1.00%		C	±0.5%
0	0	0	1	X1	X2	X4	X6			D	-1.0%
1	0	1	0	X1	X2	X4	X6	1.50%		C	±0.75%
0	0	1	0	X1	X2	X4	X6			A	+0.25% ~ -1.25%
1	0	1	1	X1	X2	X4	X6	2.00%		C	±1.0%
0	0	1	1	X1	X2	X4	X6			A	+0.5% ~ -1.5%
1	1	0	0	X1	X2	X4	X6	2.50%		C	±1.25%
0	1	0	0	X1	X2	X4	X6			A	+0.75% ~ -1.75%
1	1	0	1	X1	X2	X4	X6	3.00%		C	±1.5%
0	1	0	1	X1	X2	X4	X6			A	+1.0% ~ -2.0%
1	1	1	0	X1	X2	X4	X6	3.50%		C	±1.75%
0	1	1	0	X1	X2	X4	X6			A	+1.25% ~ -2.25%
1	1	1	1	X1	X2	X4	X6	OFF			

Notes: C: Center Spread. A: Asymmetric Spread. D: Down Spread.

BLOCK DIAGRAM



PIN DESCRIPTIONS

Name	Number	Type	Description
XIN/FIN	1	I	Crystal input to be connected to fundamental parallel mode crystal.(C_L=18pF) or clock input.
XOUT/SD	2	B	At power-up, this pin is an input pin to select modulation type. After input sampling, this pin is crystal output. Has internal pull up resistor.
SC0	3	I	Digital control input to select modulation magnitude. Has internal pull-up.
SC1	4	I	Digital control input to select modulation magnitude. Has internal pull-up.
GND	5	P	Ground.
FOUT	6	O	Modulated Clock Frequency Output. The frequency before modulation is synthesized by multiplying the input frequency by 1X, 2X, 4X, 6X depending on the part number (PLL701-01, -02, -04, -06).
SC2	7	I	Digital control input to select modulation magnitude. Has internal pull-up.
VDD	8	P	Power Supply.

FUNCTIONAL DESCRIPTION

Selectable spread spectrum and modulation magnitudes

The PLL701-01/02/04/06 provides selectable spread spectrum modulation type, as well as selectable modulation magnitude. Selection is made by connecting specific pins to a logical “zero” or “one” according to the output clock selection table on page 1.

In order to reduce the number of pins on the chip, the PLL701-01/02/04/06 uses pin 2 (XOUT/SD) as a bi-directional pin. The pin serves as modulation type selector input (SD) upon power-up (see output clock selection table on page 1), and as XOUT crystal connection as soon as the input has been latched.
Pins 3 (SC0), 4 (SC1), and 7 (SC2) are used as inputs to select the spread spectrum modulation magnitude as shown on the output clock selection table (page 1).

Connecting a selection pin to a logical "one"

All selection pins have an internal pull-up resistor (30kΩ for pins 3, 4, 7, and 120kΩ for pin 2). This internal pull-up resistor will pull the input value to a logical "one" (pull-up) by default, i.e. when no resistive load is connected between the pin and GND. No external pull-up resistor is therefore required for connecting a logical "one" upon power-up.

Connecting a selection pin to a logical "zero"

For an input only pin, i.e. pins 3 (SC0), 4 (SC1), and 7 (SC2), the pin simply needs to be grounded to pull the input down to a logical "zero". Connecting the bi-directional pin (SD) to a logical "zero" will however require the use of a 27kΩ loading resistor between the pin and GND.

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note**: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

2. Timing Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Rise Time	T_r	Measured at 0.8V ~ 2.0V @ 3.3V	0.8	0.95	1.1	ns
Fall Time	T_f	Measured at 2.0V ~ 0.8V @ 3.3V	0.78	0.85	0.9	ns
Output Duty Cycle	D_T		45	50	55	%
Cycle to Cycle Jitter	$T_{cyc-cyc}$	FOUT=48MHz @ 3.3V			100	ps
Cycle to Cycle Jitter	$T_{cyc-cyc}$	FOUT=72MHz @ 3.3V			100	ps

3. DC/AC Specifications

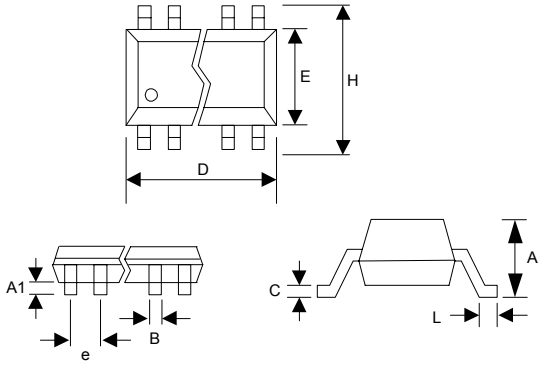
PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_{DD}		2.97		3.63	V
Input High Voltage	V_{IH}		0.7*VDD			V
Input Low Voltage	V_{IL}				0.3*VDD	V
Input High Current	I_{IH}				100	μA
Input Low Current	I_{IL}				100	μA
Output High Voltage	V_{OH}	I_{OH}=5mA, VDD=3.3V	2.4			
Output Low Voltage	V_{OL}	I_{OL}=6mA, VDD=3.3V			0.4	
Input Frequency	F_{XIN}	When using a crystal	10		30	MHz
	F_{IN}	When using reference clock	10		30	MHz
Maximum interruption of F_{IN}		When using reference clock			100	μs
Load Capacitance	C_L	Between Pin XIN and XOUT*		18		pF
Pull-up Resistor	R_{up}	PIN 2		120		kΩ
Pull-up Resistor	R_{up}	PIN 3, 4, 7		30		kΩ
Short Circuit Current	I_{sc}			50		mA
3.3V Dynamic Supply Current	I_{CC}	No Load		20		mA

***Note:** Pin XIN and XOUT each has a 36pF capacitance. When used with a XTAL, the two capacitors combined load the crystal with 18pF. If driving XIN with a reference clock signal, the load capacitance will be 36pF (typical).

PACKAGE INFORMATION

8 PIN Narrow SOIC (mm)

	SOIC	
Symbol	Min.	Max
A	1.47	1.73
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	4.95
E	3.80	4.00
H	5.80	6.20
L	0.38	1.27
e	1.27 BSC	

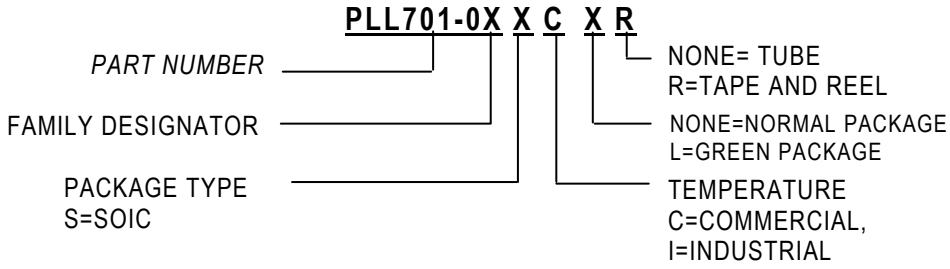


ORDERING INFORMATION

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of Device number, Package type and Operating temperature range



Part / Order Number	Marking	Package Option	Temperature
PLL701-0XSCR	P701-0XXC	SOIC -Tape and Reel	0 to +70° C
PLL701-0XSC	P701-0XXC	SOIC -Tube	0 to +70° C
PLL701-0XSCLR	P701-0XXCL	SOIC -Tape and Reel (GREEN)	0 to +70° C
PLL701-0XSCL	P701-0XXCL	SOIC –Tube (GREEN)	0 to +70° C