PM3386

S/UNI-2xGE

DUAL GIGABIT ETHERNET CONTROLLER

DATASHEET

PROPRIETARY AND CONFIDENTIAL

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1 DEFINITIONS

CSMA/CD	Carrier Sense Multiple Access with Collision Detection.
1000BASE-T	IEEE 802.3-1998 Physical Layer specification for 1000 Mb/s CSMA/CD LAN using four pairs of Category 5 balanced copper cabling.
1000BASE-SX	IEEE 802.3-1998 using short wavelength laser devices over multimode fiber
1000BASE-LX	IEEE 802.3-1998 using long wavelength laser devices over multimode and single-mode fiber.
Auto-Negotiation	The algorithm that allows two devices at either end of a link segment to negotiate common data service functions.
Base Page	The first 16-bit message exchanged during IEEE 802.3-1998 Auto-Negotiation.
Comma	The seven-bit sequence that is part of an 8B/10B code-group that is used for the purpose of code-group alignment.
Comma-	The seven-bit sequence (1100000) of an encoded data stream.
Comma+	The seven-bit sequence (0011111) of an encoded data stream.
Data Frame	Consists of Destination Address, Source Address, Length Field, logical link control (LLC) Data, PAD, and Frame Check Sequence.
DTE	Any source or destination of data connected to the local area network.
EOF	End of frame.
EOP	End of packet
Even Parity	The count of the number of 1's in the data word of n bits. If there are an odd number of 1s, then the parity bit will be a 1 so that including the parity bit, the number of 1s are an even number.
Frame	Same as Data Frame
Full Duplex	A mode of operation that supports simultaneous communication between a pair of stations, provided that the Physical Layer is capable of supporting simultaneous transmission and reception without interference.
GMII	Gigabit Media Independent Interface.
IPG	Inter-Packet Gap (IPG): A delay or time gap between CSMA/CD physical packets intended to provided interframe recovery time for other CSMA/CD sublayers and for the Physical Medium.
MIB	Management Information Base (MIB): A repository of information to describe the operation of specific network device.

MAC	Media Access Control (MAC): The data link sublayer that is responsible for transferring data to and from the Physical Layer.
MII	Media independent Interface (MII): A transparent signal interface at the bottom of the Reconciliation sublayer.
Next Page	General class of pages optionally transmitted by Auto-Negotiation able devices following the base page word negotiation.
Nibble	A group of four data bits. The unit of exchange on the MII.
Packet	The logical unit of data transferred across the POS-PHY Level 3 interface. This generally corresponds to the Data Frame as defined previously, although the CRC may or may not be present in the POS-PHY Level 3 egress direction.
Physical Packet	Consists of a Data Frame as defined previously, preceded by the Preamble and the Start Frame Delimiter, encoded, as appropriate, for the Physical Layer (PHY) type.
POS-PHY	SATURN compatible Packet over SONET interface specification for physical layer devices. POS-PHY level 3 defines an interface for bit rates up to and including 2.488 Gbit/s.
PL3	Short hand notation for the POS-PHY Level 3 term.
Odd Parity	The count of the number of 1's in the data word of n bits. If there are an odd number of 1s, then the parity bit will be a 0 so that including the parity bit, the number of 1s are an odd number
SOF	Start of Frame.
SOP	Start of Packet.

2 FEATURES

2.1 General

- Two port full-duplex Gigabit Ethernet Controller with an industry standard POS-PHY Level 3 system interface.
- Provides direct connect to optics via two internal Serializer/Deserializer (SERDES)
- Provides connection to copper Gigabit Ethernet physical layer devices via two GMII interfaces.
- Incorporates dual SERDES, compatible to IEEE 802.3 1998 PMA physical layer specification.
- Provides on-chip data recovery and clock synthesis.
- Supports dual IEEE 802.3 -1998 GMII interfaces for connection to copper Gigabit Ethernet physical layer devices.
- Provides dual standard IEEE 802.3 Gigabit Ethernet MACs for frame verification.
- Enables frame filtering on 8 unicast or 64 multicast entries.
- Internal 16k byte egress and 64k byte ingress FIFOs per channel to accommodate system latencies.
- Incorporates SATURN POS-PHY Level 3 32-bit System Interface clocked up to 104 MHz (32 bit mode only).
- Line side loopback capability for system level diagnostic capability.
- Includes 16 bit generic microprocessor interface for device initialization, control, register and per port statistics access.
- Provides a standard 5 signal P1149.1 JTAG test port for boundary scan board test purposes.
- Low power 1.8V CMOS device with 3.3V TTL compatible digital inputs (5V TTL compatible microprocessor inputs) and 3.3V CMOS/TTL compatible digital outputs within a 352 pin 27mm by 27mm UBGA package.
- Industrial temperature range (-40°C to +85°C).

2.2 Line Side Interface

- SERDES interface provides 2 differential pairs at 1250 MHz for connection to electrical optical modules.
- GMII interface provides 8 bit wide TX & RX data interfaces at 125 MHz with control signals for connection to copper Gigabit Ethernet physical layer devices.
- Allows selection between SERDES and GMII interface on a per channel basis.

2.3 Gigabit Ethernet MAC

- Verifies frame integrity (i.e. FCS and length checks).
- Erred frames can be filtered or passed to higher layer device.
- Automatic Base page Auto-Negotiation, extended Auto-Negotiation (Next Page) supported via host.
- Egress Ethernet physical frame encapsulation (pad to min size, add preamble, IFG and CRC generation).
- Supports Ethernet 2.0, IEEE 802.3 LLC and IEEE 802.3 SNAP/LLC encoding formats and VLAN tagged frames.
- Provides 8 unicast exact-match address filters to filter frames based on DA or SA with optional VID.
- Each address filter can be programmed to indicate whether to accept or discard based on a match.
- Provides a 64 group multicast address filter.
- Supports 64 byte minimum size frames and jumbo frames up to 9.6K bytes.
- Programmable Inter-packet gap (IPG).
- System side loopback through GMAC for diagnostic capability.

2.4 Flow Control

- Supports IEEE 802.3-1998 flow control at each Ethernet port if enabled.
- Programmable watermarks for full/empty FIFO thresholds.
- Automatic generation of PAUSE frames based on FIFO fill levels.
- Upper layer device can flow control Ethernet ports using side-band or host signaling to cause generation of a PAUSE frame.
- Provides side-band Paused state indication to upstream devices.
- Loss-less flow control on all valid frames up to 9.6k bytes.

2.5 Statistics

- 40 bit counters are used to ensure rollover compliance with IEEE 802.3–1998.
- Minimum 58 minutes before rollover.
- Provides port statistic counters needed to support the standard 802.3-1998, SNMP, and RMON Management Information Base (MIB) implementations.

3 APPLICATIONS

- Core Routers
- Edge Routers
- Enterprise Edge Routers
- Multi-Service Switches/Routers
- SONET/SDH Transport Muxes

4 REFERENCES

- IEEE 802.3-1998 Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications
- PMC-980495 SATURN Compatible Interface For Packet Over SONET Physical Layer And Link Layer Devices (Level 3)
- RFC 1757 Remote Network Monitoring Management Information Base
- RFC 1213 Management Information Base for Network Management of TCP/IP-based internets: MIB-II
- RFC 2233 The Interfaces Group MIB using SMIv2
- RFC 2665 Definitions of Managed Objects for the Ethernet-like Interface Types

5 APPLICATION EXAMPLES

The PM3386 S/UNI-2xGE is applicable to equipment implementing high density Gigabit Ethernet interfaces. The PM3386 is a dual channel SERDES and GMAC with embedded FIFOs that provides a high density and low power Gigabit Ethernet solution for direct connection to electrical optical modules. Alternatively, a GMII interface is provided for connection to copper Gigabit Ethernet physical layer devices.

On the system side, the POS-PHY Level 3 (32 bit synchronous FIFO style interface clocked up to 104 MHz) allows a common connection to higher layer devices. A common system interface simplifies multi-service equipment utilizing some or all of the following physical layer options:

- OC-48 POS/ATM
- 4xOC-12 POS/ATM
- 16xOC-3 POS/ATM
- Channelized POS/ATM
- High density DS3
- Gigabit Ethernet

The PM3386 is particularly suited for the following applications:

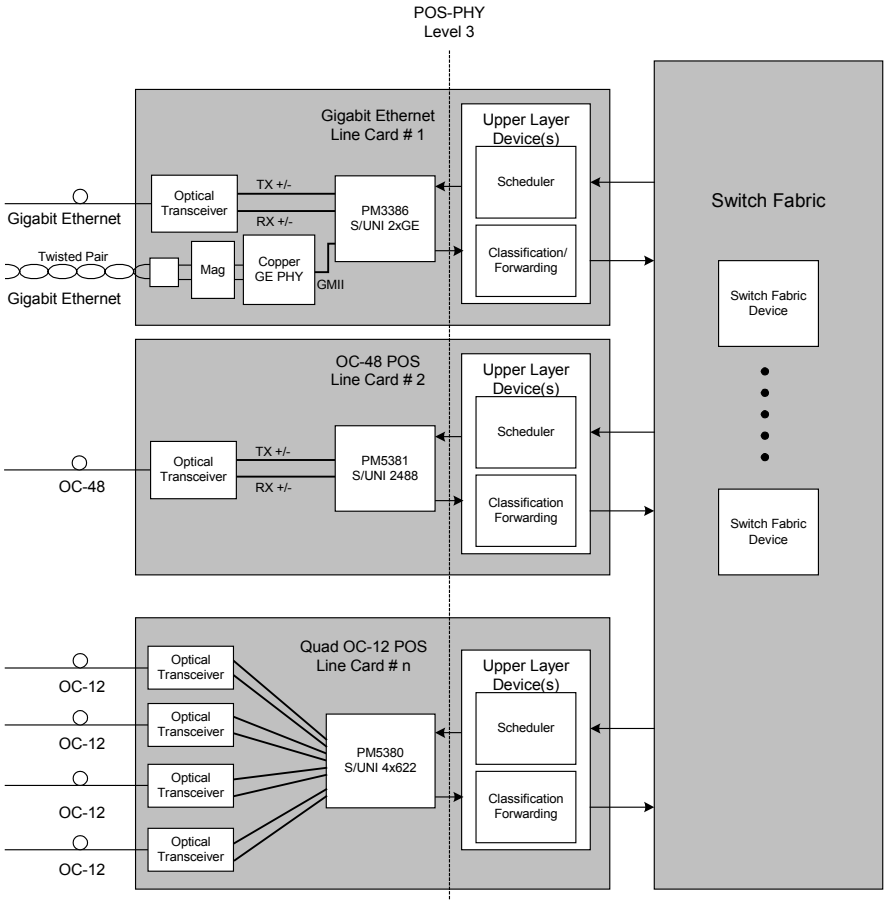
- Core Routers
- Edge Routers
- Enterprise Edge Routers
- Multi-Service Switches/Routers
- SONET/SDH Transport Muxes

These applications require various interfaces (Gigabit Ethernet, ATM, POS, DS3) which use the POS-PHY Level 3 interface. Service cards for various physical layer options can re-use upper layer devices and board design to improve time-to market. The use of Gigabit Ethernet within Internet points of presence (POPs), Super POPs and Transport POPs is increasing due to the requirement of inexpensive high-speed Layer 2 interconnect. Thus, connections between

Edge Routers and Core Routers within a POP are provided via Gigabit Ethernet. Co-located server clusters are also connected via Gigabit Ethernet to POP routers. Similarly, Gigabit Ethernet is becoming the choice for connection between Enterprise Routers and Multi-Service switches. Transport equipment is looking to provide Ethernet directly over SONET/SDH for wide area transparent bridging.

In a typical application the S/UNI-2xGE performs data recovery on the Gigabit Ethernet stream, MAC level frame checks and sends the frame to an upper layer device (such as an IP processor) for forwarding via the POS-PHY level 3 interface. The S/UNI-2xGE maintains extensive statistics for SNMP and RMON applications. On egress, frames are formatted into physical frames with the proper inter-frame gap, preamble and start of frame delimiter. The physical packet is then serialized for transmission over an external electrical optical module. The initial configuration and ongoing control and monitoring of the S/UNI-2xGE are provided via a generic microprocessor interface. The following diagram shows a typical multi-service card application for the PM3386 S/UNI-2xGE with similar cards for OC48 and Quad OC-12 ports.

Figure 1 PM3386 Typical Application Example



6 BLOCK DIAGRAM

Figure 2 - PM3386 Dual Gigabit Ethernet to POS-PHY Level 3

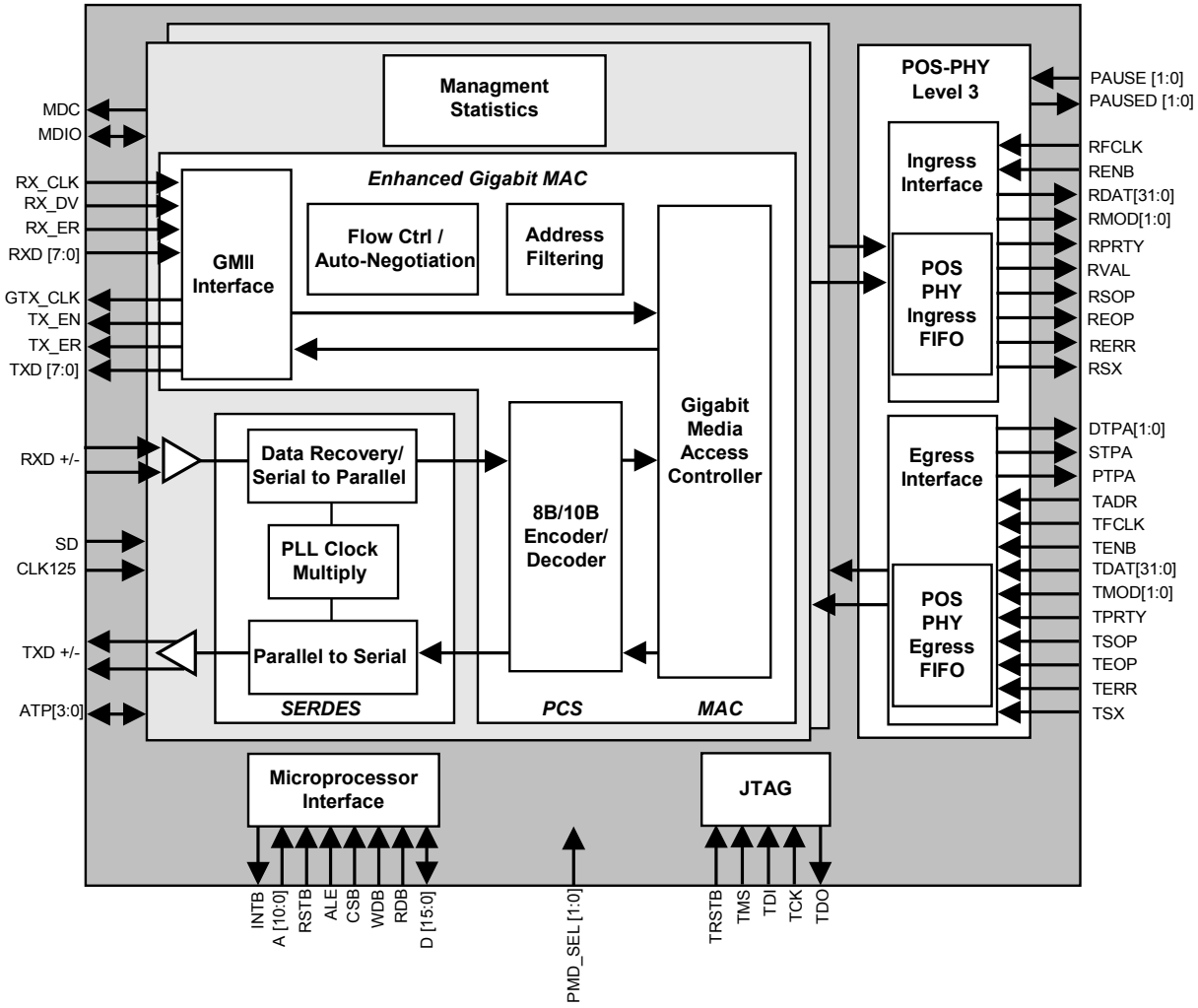
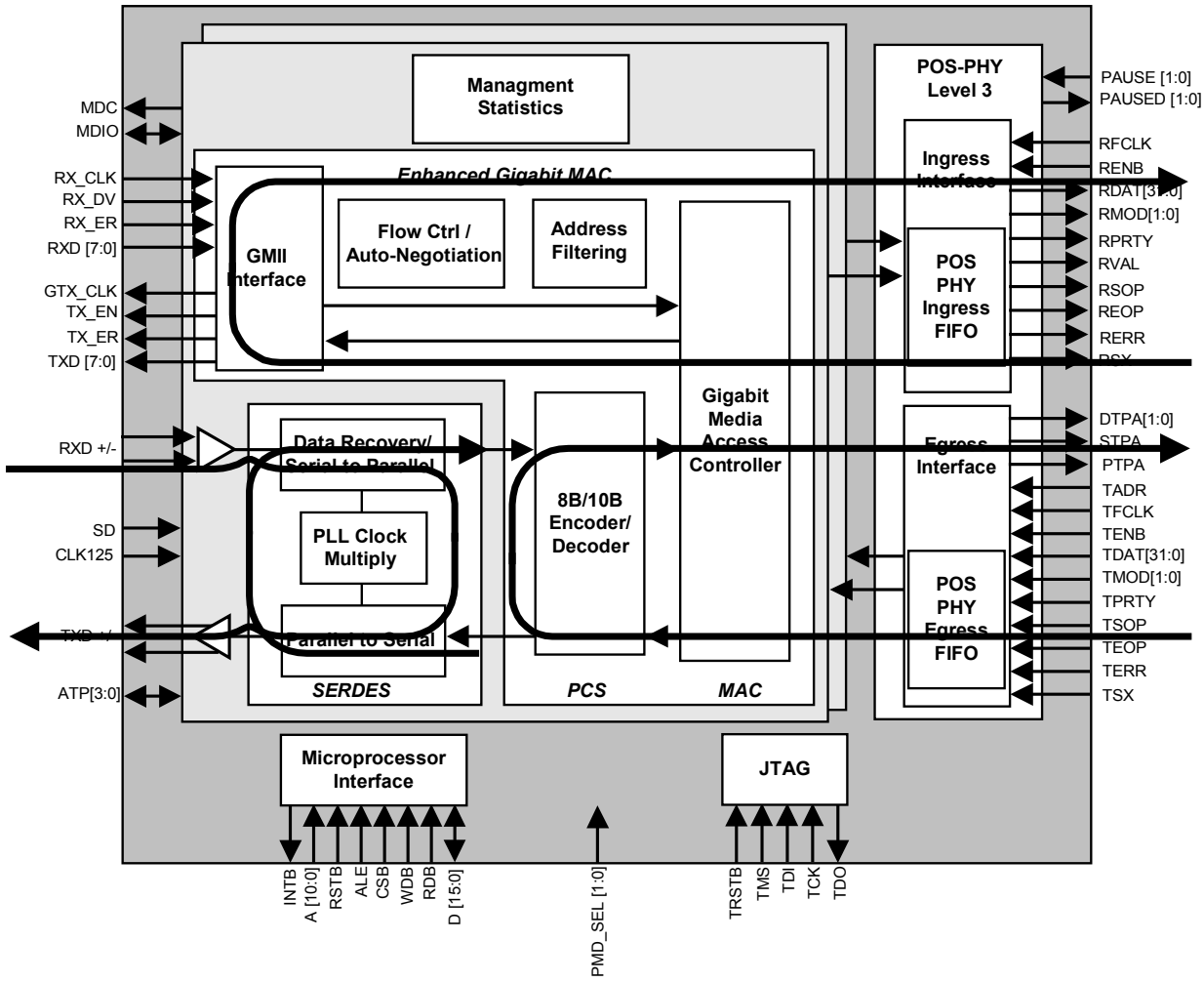


Figure 3 PM3386 Device Loop Back Paths



7 DESCRIPTION

The PM3386 is a monolithic integrated circuit that implements a two port full duplex 1000 Mbit/s Gigabit Ethernet MAC data transport device. The PM3386 provides line interface connectivity provided by an on-chip SERDES and GMII functions and data transport to the up stream device via the industry standard POS-PHY Level 3 interface.

Serializer-Deserializer (SERDES)

The PM3386 has two internal serializer-deserializer transceivers. The SERDES are IEEE 802.3-1998 Gigabit Ethernet compatible supporting gigabit data transfer flows. The SERDES is based on the X3T11 10 Bit specification. The PM3386 receives and transmits Gigabit Ethernet streams using a bit serial interface for direct connection to optical transceiver devices. The SERDES performs data recovery and serial to parallel conversion for connection to the Enhanced Gigabit Media Access Control block.

Gigabit Media Independent Interface (GMII)

For Gigabit Ethernet over copper support, the PM3386 provides dual standard GMII interfaces. A copper Gigabit Ethernet physical layer device can be connected to the PM3386 via this interface.

Enhanced Gigabit Media Access Control (EGMAC)

The Enhanced Gigabit Media Access Control (EGMAC) block provides an integrated IEEE 802.3-1998 Gigabit Ethernet Media Access Control (MAC) supporting high performance 1000Base capability. The EGMAC has line side interfaces for connection to internal (SERDES) and external Gigabit PHY via GMII on each Gigabit Ethernet port. The Enhanced Gigabit MAC (EGMAC) incorporates all of the Gigabit Ethernet MAC functions including Auto-Negotiation, statistics, and the MAC Control Sub-layer that adheres to IEEE 802.3-1998 providing support for PAUSE control frames. The EGMAC provides basic frame integrity checks to validate incoming frames. The EGMAC also provides simple line rate ingress address filtering support via 8 exact-match MAC address and VID unicast filters, one 64-bin hash-based multicast filter, and the ability to filter or accept matched frames on a per instance programmable fashion. All inquires for filtering are done at line rate with no system latency introduced for look up cycles.

Management Statistics (MSTAT)

The PM3386 also incorporates a rich set of per port RMON, SNMP, and Etherlike Management Information Base counters. Deep statistical counters are used for management counts providing a minimum rollover time of greater than 58 minutes. All counts are easily managed via the Management Statistics (MSTAT) block.

POS-PHY Level 3 Interface (PL3)

The PM3386 can connect to a single upper layer device through a POS-PHY Level 3 Interface. The POS-PHY Level 3 interface is a 32-bit wide interface with a clock rate from 60 to 104 MHz. POS-PHY Level 3 was developed with the cooperation of the SATURN Development Group to cover all application bit rates up to and including 3.2 Gbit/s. This interface provides standards support for interoperation between the PM3386, a multiple PHY layer device, connecting to one Link Layer device. The interface stresses simplicity of operation to allow forward migration to more elaborate PHY and Link Layer devices. The POS-PHY interface contains 64KB receive and 16KB transmit FIFOs per channel. These FIFOs contain programmable thresholds specifying full and empty conditions.

Receive Direction

In the receive direction, the PM3386 can be configured to use the internal SERDES or the GMII interface on a per channel basis. For SERDES operation, a Gigabit Ethernet bit stream is received from an external optical transceiver. The data is recovered and converted from serial to parallel data for connection to the EGMAC block. The EGMAC terminates the 8B/10B line codes and performs frame integrity checks (frame length, FCS etc). For GMII operation, the physical packet is sourced from an external copper physical layer device to the PM3386 via the GMII interface (8 bits clocked at 125 MHz). The EGMAC accepts the 8 bit data and performs frame integrity checks once the complete frame is received. The EGMAC can optionally filter erred frames.

Statistics are updated and the frame is sent to the POS-PHY Level 3 interface. The FIFO's in the POS-PHY interface accommodate system latencies and allows for loss-less flow control up to 9.6k bytes. The received frames are then read through the POS-PHY Level 3 (32 bits clocked from 60-104 MHz) system side interface.

Transmit Direction

In the transmit direction, packets to be transmitted are written into the POS-PHY TX FIFO through the POS-PHY Level 3 interface (32 bits clocked from 60-104

MHz) from the upper layer device. The channel is selected by the upper layer device and is indicated in-band on the POS-PHY interface. The EGMAC builds a properly formatted Ethernet physical packet (padding to minimum size and inserting the preamble, start of frame delimiter (SFD) and the inter-packet gap (IPG)). Statistics are updated and the physical packet is sent to the SERDES or the GMII interface.

For SERDES operation, the EGMAC encodes the physical packet using 8B/10B encoding and passes the physical packet to the SERDES block. The SERDES performs parallel to serial conversion using an internally synthesized 1250 MHz clock. The bit stream is sent to an external optical transceiver for transmission over fiber cable. For GMII operation, the EGMAC sends the physical packet byte by byte across the GMII interface (8 bits clocked at 125 MHz) to an external copper Gigabit Ethernet physical layer device. The copper Gigabit Ethernet physical layer device then transmits the physical packet over copper cable.

Flow Control

Flow control is handled in the EGMAC block. When a PAUSE control frame is received, the PM3386 will optionally terminate transmission (after the current frame is sent) and assert the appropriate channel side band flow control output to indicate the paused condition. The received PAUSE control frame can be optionally filtered or passed to the link layer device via the POS-PHY Level 3 interface.

PAUSE control frames are transmitted either under link layer control using channel side band flow control inputs, under link layer control transparent to the PM3386, host based PAUSE frame control or under internal control based on receive FIFO levels. All four methods can provide for loss-less flow control.

General

The PM3386 is configured, controlled and monitored via a generic 16-bit microprocessor bus interface. The PM3386 also provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.

The PM3386 is implemented in low power, +1.8 Volt, CMOS technology with 5V TTL compatible digital inputs and 3.3V TTL/CMOS compatible digital outputs. The PM3386 is packaged in a 352-pin UBGA package.

8 PIN DIAGRAM

The PM3386 is packaged in a 352-pin Ultra Ball Grid Array (UBGA) having a body size of 27mm by 27mm.

Table 1 PM3386 Pin Diagram

26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
VSS	VSS	NC	RXD1[2]	RXD1[6]	RX_ER1	TX_EN1	TXD1[5]	TXD1[2]	VSSQ	ALE	CSB	VSS	VSS	A[6]	A[3]	A[1]	D[13]	D[10]	D[7]	D[4]	D[1]	TDI	NC	VSS	VSS	A
VSS	VDDO	VSS	NC	RXD1[3]	RXD1[7]	RX_CLK1	TX_ER1	TXD1[4]	TXD1[1]	INTB	RDB	A[9]	A[8]	A[5]	A[2]	D[15]	D[11]	D[8]	D[5]	D[2]	TMS	NC	VSS	VDDO	VSS	B
VSS	VSS	VDDO	NC	RXD1[0]	RXD1[4]	RX_DV1	GTX_CLK1	TXD1[7]	TXD1[3]	TXD1[0]	WRB	A[10]	A[7]	A[4]	A[0]	D[12]	D[9]	D[6]	D[3]	TCK	TRSTB	NC	VDDO	VSS	NC	C
VSS	VSS	VDDO	VDDO	NC	RXD1[1]	RXD1[5]	VDDI	VDDO	TXD1[6]	VDDI	VDDQ	NC	VDDO	VDDI	D[14]	VDDI	NC	VDDO	D[0]	TDO	NC	VDDO	NC	NC	NC	D
VSS	NC	VDDO	NC																			NC	NC	NC	NC	E
VSSQ	PMD_SEL1	VDDI	VDDI																			NC	NC	NC	RDAT[0]	F
VSS	CLK125	VDDQ	AVDL																			NC	RSTB	RDAT[1]	VDDI	G
AVDH	AVDQ	AVDL	AVDL																			VDDO	RDAT[2]	RDAT[3]	RDAT[6]	H
VSS	RXSD1	AVDH	VDDO																			NC	RDAT[4]	RDAT[7]	VSSQ	J
RXD1+	RXD1-	AVDL	AVDL																			RDAT[5]	RDAT[8]	RDAT[9]	RDAT[11]	K
VSS	AV	H	NC																			VDDQ	RDAT[10]	RDAT[12]	RDAT[13]	L
TXD1-	TX																					VDDI	RDAT[14]	RDAT[15]	RDAT[16]	M
AVDL	AV		DL																			VDDO	RDAT[17]	RDAT[18]	VSS	N
AVDL	AV																					RDAT[21]	RDAT[20]	RDAT[19]	VSS	P
RXD0-	RXD0+	RXSD0	AVDH																			VDDI	RDAT[24]	RDAT[23]	RDAT[22]	R
VSS	AVDL	AVDL	VDDO																			RDAT[30]	RDAT[28]	RDAT[26]	RDAT[25]	T
TXD0+	TXD0-	AVDH	NC																			RSX	RPRTY	RDAT[29]	RDAT[27]	U
VSS	NC	PMD_SEL0	VDDI																			VDDO	RERR	REOP	RDAT[31]	V
TXD0[3]	TXD0[2]	TXD0[0]	TXD0[1]																			VDDI	RVAL	RMOD[1]	RFCLK	W
VSS	TXD0[5]	TXD0[4]	VDDO																			PAUSE1	PAUSED0	RSOP	RMOD[0]	Y
NC	TXD0[7]	TXD0[6]	VDDI																			NC	VDDQ	PAUSED1	RENB	AA
VSS	NC	VDDO	NC																			NC	NC	VSSQ	PAUSE0	AB
VSS	VSS	VDDO	VDDO	VDDI	RX_CLK0	VDDI	VDDO	NC	TDAT[31]	VDDI	VDDQ	VDDO	NC	TDAT[11]	VDDI	TDAT[2]	VDDO	VDDI	TMOD[1]	VDDI	NC	VDDO	NC	NC	NC	AC
VSS	VSS	VDDO	NC	GTX_CLK0	RXD0[7]	RXD0[4]	RXD0[1]	MDC	TDAT[28]	TDAT[25]	TDAT[21]	TDAT[19]	TDAT[16]	TDAT[13]	TDAT[8]	TDAT[5]	TDAT[1]	TENB	TEOP	TMOD[0]	STPA	NC	VDDO	VSS	NC	AD
VSS	VDDO	VSS	TX_EN0	RX_DV0	RXD0[5]	RXD0[2]	MDIO	TDAT[29]	TDAT[26]	TDAT[23]	TDAT[20]	TDAT[18]	TDAT[17]	TDAT[14]	TDAT[10]	TDAT[7]	TDAT[4]	TDAT[0]	TSX	TPRTY	TADR	DTPA[1]	VSS	VDDO	VSS	AE
VSS	VSS	TX_ER0	RX_ER0	RXD0[6]	RXD0[3]	RXD0[0]	TDAT[30]	TDAT[27]	TDAT[24]	TDAT[22]	VSSQ	VSS	VSS	TDAT[15]	TDAT[12]	TDAT[9]	TDAT[6]	TDAT[3]	TFCLK	TSOP	TERR	PTPA	DTPA[0]	VSS	VSS	AF

Bottom View

9 PIN DESCRIPTION

Table 2 - Serial Line Side Interface Signals

Pin Name	Type	Pin No.	Function
CLK125	Schmitt Input	G25	**PHY Reference Clock (Port 0)** 125 MHz reference clock used to generate GTX_CLK0 or GTX_CLK1 during GMII mode. The Clock Synthesis Unit uses this clock as it's input reference during SERDES mode. Please refer to the Operations section for a discussion of clock mode selection interfacing issues.
RXD0+ RXD0-	Differential PECL Input	R25 R26	**Receive Differential Data (Port 0)** These PECL inputs (RXD0+/-) contain the 8B/10B bit serial receive stream. The receive data is recovered from the RXD0+/- bit stream.
RXSD0	Input	R24	**Receive Signal Detect (Port 0)** RXSD0 indicates the presence of valid receive signal power from the Optical Physical Medium Dependent Device. A logic level high indicates the presence of valid data. A logic low indicates a loss of signal.
RXD1+ RXD1-	Differential PECL Input	K26 K25	**Receive Differential Data (Port 1)** The PECL inputs RXD1+/- contain the 8B/10B bit serial receive stream. The receive data is recovered from the RXD1+/- bit stream.

Pin Name	Type	Pin No.	Function
RXSD1	Input	J25	**Receive Signal Detect (Port 1)** RXSD1 indicates the presence of valid receive signal power from the Optical Physical Medium Dependent Device. A logic level high indicates the presence of valid data. A logic low indicates a loss of signal.
TXD0+ TXD0-	Differential PECL Output	U26 U25	**Transmit Differential Data (Port 0)** The PECL outputs TXD0+/- contain the 1.25 Gbit/s transmit stream. The TXD0+/- outputs are driven using the CSU clock.
TXD1+ TXD1-	Differential PECL Output	M25 M26	**Transmit Differential Data (Port 1)** The PECL outputs TXD1+/- contain the 1.25 Gbit/s transmit stream. The TXD1+/- outputs are driven using the CSU clock.
ATP0 ATP1	Bi-Directional CMOS	M24 M23	**Receive and Transmit Analog Test Ports** The ATP[1:0] pins are used for manufacturing testing only and should be tied to analog ground.

Table 3 -Gigabit Media Independent Interface (GMII)

Signal Name	Direction	Pin No.	Function
GTX_CLK0	Output	AD22	**GMII Transmit Clock (Port 0)** 125 MHz reference clock supplied by the PM3386.
TXD0[0] TXD0[1] TXD0[2] TXD0[3] TXD0[4] TXD0[5] TXD0[6] TXD0[7]	Output	W24 W23 W25 W26 Y24 Y25 AA24 AA25	**GMII Transmit Data (Port 0)** Byte-wide transmit data is output on these pins synchronously to the PHY device. The least significant bit, TXD0[0] is the first bit transferred on the line. This signal is updated on the rising edge of GTX_CLK0.

Signal Name	Direction	Pin No.	Function
TX_EN0	Output	AE23	**Transmit Enable (Port 0)** When in GMII mode this signal is an active high signal asserted when valid data is present on the TXD0[7:0] and TX_ER0 pins. This signal is updated on the rising edge of GTX_CLK0. When in SERDES mode this signal enables operation of the external transmitter. When asserted (default active low) it indicates the potential presence of valid transmit data. When de-asserted indicates the absence of valid transmit data. Note that while in SERDES mode the polarity of this signal is programmable to support interoperability with differing optical transmitters.
TX_ER0	Output	AF24	**GMII Transmit Coding Error (Port 0)** Active high signal asserted when an error is detected during transmission. Please refer to the Operations section for a full listing of error conditions reported by the PM3386 using the TX_ER0 output. This signal is updated on the rising edge of GTX_CLK0.
RX_CLK0	Schmitt Input	AC21	**GMII Receive Clock (Port 0)** 125 MHz GMII reference clock received from the PHY device.
RXD0[0] RXD0[1] RXD0[2] RXD0[3] RXD0[4] RXD0[5] RXD0[6] RXD0[7]	Input	AF20 AD19 AE20 AF21 AD20 AE21 AF22 AD21	**GMII Receive Data (Port 0)** Byte-wide receive data is input on these pins synchronously from the PHY device. The least significant bit, RXD0[0] is expected to contain the first bit received on the line. This signal is synchronized to RX_CLK0.

Signal Name	Direction	Pin No.	Function
RX_DV0	Input	AE22	**GMII Receive Data Valid (Port 0)** Active high signal asserted when valid data is present on the RXD0[7:0] and RX_ER0 pins. This signal is synchronized to RX_CLK0.
RX_ER0	Input	AF23	**GMII Receive Error (Port 0)** Active high signal asserted when there has been an error during the received physical packet. This signal is synchronized to RX_CLK0.
GTX_CLK1	Output	C19	**GMII Transmit Clock (Port 1)** 125 MHz reference clock supplied by the PM3386.
TXD1[0] TXD1[1] TXD1[2] TXD1[3] TXD1[4] TXD1[5] TXD1[6] TXD1[7]	Output	C16 B17 A18 C17 B18 A19 D17 C18	**GMII Transmit Data (Port 1)** Byte-wide transmit data is output on these pins synchronously to the PHY device. The least significant bit, TXD1[0] is the first bit transferred on the line. This signal is updated on the rising edge of GTX_CLK1.

Signal Name	Direction	Pin No.	Function
TX_EN1	Output	A20	**Transmit Enable (Port 1)** When in GMII mode this signal is an active high signal asserted when valid data is present on the TXD1[7:0] and TX_ER1 pins. This signal is updated on the rising edge of GTX_CLK1. When in SERDES mode this signal enables operation of the external transmitter. When asserted (default active low) it indicates the potential presence of valid transmit data. When de-asserted indicates the absence of valid transmit data. Note that while in SERDES mode the polarity of this signal is programmable to support interoperability with differing optical transmitters.
TX_ER1	Output	B19	**GMII Transmit Coding Error (Port 1)** Active high signal asserted when an error is detected during transmission. Please refer to the Operations section for a full listing of error conditions reported by the PM3386 using the TX_ER1 output. This signal is updated on the rising edge of GTX_CLK1.
RX_CLK1	Schmitt Input	B20	**GMII Receive Clock (Port 1)** 125 MHz GMII reference clock received from the PHY device.
RXD1[0] RXD1[1] RXD1[2] RXD1[3] RXD1[4] RXD1[5] RXD1[6] RXD1[7]	Input	C22 D21 A23 B22 C21 D20 A22 B21	**GMII Receive Data (Port 1)** Byte-wide receive data is input on these pins synchronously from the PHY device. The least significant bit, RXD1[0] is expected to contain the first bit received on the line. This signal is synchronized to RX_CLK1.

Signal Name	Direction	Pin No.	Function
RX_DV1	Input	C20	**GMII Receive Data Valid (Port 1)** Active high signal asserted when valid data is present on the RXD1[7:0] and RX_ER1 pins. This signal is synchronized to RX_CLK1
RX_ER1	Input	A21	**GMII Receive Error (Port 1)** Active high signal asserted when there has been an error during the received physical packet. This signal is synchronized to RX_CLK1.
MDC	Output	AD18	**MII Management Data Clock** MDC provides the MII reference clock for communication between the PM3386 and other transceivers.
MDIO	I/O Internal pull-down	AE19	**MII Management Data** When configured as an input, the external PHY supplies status during MII Management read cycles. When configured as an output, the PM3386 supplies control during MII Management write/read cycles and data during MII Management write cycles. Data values on the MDIO pin are updated and sampled on the rising edge of MDC.

Table 4 -POS-PHY Level 3 Transmit Interface

Signal Name	Direction	Pin No.	Function
TFCLK	Schmitt Input	AF7	**POS-PHY Transmit FIFO Write Clock** TFCLK is used to synchronize data transfer transactions between the higher layer device and the PM3386. TFCLK cycles at a 60 to 104 MHz rate.

Signal Name	Direction	Pin No.	Function
TDAT[0]	Input	AE8	**POS-PHY Transmit Packet Data Bus** This bus carries the packet octets that are written to the selected transmit FIFO and the in-band port address to select the desired transmit FIFO. The TDAT bus is considered valid only when TENB is simultaneously asserted. When a 32-bit interface is used, data must be transmitted in big endian order on TDAT[31:0]. TDAT[31:0] is sampled on the rising edge of TFCLK.
TDAT[1]		AD9	
TDAT[2]		AC10	
TDAT[3]		AF8	
TDAT[4]		AE9	
TDAT[5]		AD10	
TDAT[6]		AF9	
TDAT[7]		AE10	
TDAT[8]		AD11	
TDAT[9]		AF10	
TDAT[10]		AE11	
TDAT[11]		AC12	
TDAT[12]		AF11	
TDAT[13]		AD12	
TDAT[14]		AE12	
TDAT[15]		AF12	
TDAT[16]		AD13	
TDAT[17]		AE13	
TDAT[18]		AE14	
TDAT[19]		AD14	
TDAT[20]		AE15	
TDAT[21]		AD15	
TDAT[22]		AF16	
TDAT[23]		AE16	
TDAT[24]		AF17	
TDAT[25]		AD16	
TDAT[26]		AE17	
TDAT[27]		AF18	
TDAT[28]		AD17	
TDAT[29]		AE18	
TDAT[30]		AF19	
TDAT[31]		AC17	

Signal Name	Direction	Pin No.	Function
TERR	Input	AF5	**POS-PHY Transmit Error Indicator** Active high signal used to indicate that the current packet must be aborted. TERR should only be considered valid when TENB and TEOP are simultaneously asserted. TERR is sampled on the rising edge of TFCLK.
TENB	Input	AD8	**POS-PHY Transmit Write Enable** Active low signal used to control the flow of data to the transmit FIFOs. When TENB is high, the TDAT[31:0], TMOD, TSOP, TEOP, TPRTY and TERR signals are invalid and are ignored by the PM3386. However, the TSX signal if asserted is valid and is processed by the PM3386 only when TENB is high. When TENB is low, the TDAT[31:0], TMOD, TSOP, TEOP, TPRTY and TERR signals are valid and are processed by the PM3386. The TSX signal is ignored by the PM3386 when TENB is low. TENB is sampled on the rising edge of TFCLK.
TPRTY	Input	AE6	**POS-PHY Transmit bus parity** The transmit parity (TPRTY) signal indicates the parity calculated over the TDAT bus. TPRTY is considered valid only when TENB or TSX are asserted. By default the PM3386 uses odd parity. The PM3386 supports both even and odd parity. The PM3386 reports any parity error to the host processor via a maskable interrupt, but does not interfere with the transferred data. TPRTY is sampled on the rising edge of TFCLK.

Signal Name	Direction	Pin No.	Function
TMOD[0] TMOD[1]	Input	AD6 AC7	**POS-PHY Transmit Word Modulo** TMOD[1:0] indicates the number of valid bytes of data in TDAT[31:0]. The TMOD bus should always be all zero, except during the last double-word transfer of a packet on TDAT[31:0]. When TEOP and TENB are asserted, the number of valid packet data bytes on TDAT[31:0] is specified by TMOD[1:0]. TMOD[1:0] = “00” TDAT[31:0] valid TMOD[1:0] = “01” TDAT[31:8] valid TMOD[1:0] = “10” TDAT[31:16] valid TMOD[1:0] = “11” TDAT[31:24] valid TMOD [1:0] is sampled on the rising edge of TFCLK.
TSX	Input	AE7	**POS-PHY Transmit Start of Transfer** Active high signal indicating when the in-band port address is present on the TDAT[31:0] bus. When TSX is high and TENB is high (not asserted), the value of contained within TDAT[7:0] is the address of the transmit FIFO to be selected. TDAT[7:0] == 0 selects channel zero. TDAT[7:0] == 1 selects channel one. Subsequent data transfers on the TDAT bus will fill the FIFO specified by this in-band address. If TDAT[7:0] is not 0 or 1 no channel within the PM3386 device will be selected. Subsequent data transfers on the TDAT bus to address outside of 0 or 1 will be dropped at the PL3 interface. TSX is considered valid only when TENB is not asserted. TSX is sampled on the rising edge of TFCLK.

Signal Name	Direction	Pin No.	Function
TSOP	Input	AF6	**POS-PHY Transmit Start of Packet** Active high signal used to delineate the packet boundaries on the TDAT bus. When TSOP is high, the start of the packet is present on the TDAT bus. TSOP is required to be present at the beginning of every packet and is considered valid only when TENB is asserted. TSOP is sampled on the rising edge of TFCLK.
TEOP	Input	AD7	**POS-PHY Transmit End of Packet** Active high signal used to delineate the packet boundaries on the TDAT bus. When TEOP is high, the end of the packet is present on the TDAT bus. Note that TMOD[1:0] indicates the number of valid bytes the last double word is composed of when TEOP and TENB are asserted. TEOP is required to be present at the end of every packet and is considered valid only when TENB is asserted. TEOP is sampled on the rising edge of TFCLK.

Signal Name	Direction	Pin No.	Function
TADR	Input	AE5	**POS-PHY Transmit PHY Address** The TADR signal is used with the PTPA signal to poll the transmit FIFOs packet available status. When TADR is sampled on the rising edge of TFCLK by the PM3386, the polled packet available indication PTPA signal is updated with the status of the port specified by the TADR address on the following rising edge of TFCLK. TADR = 0 = channel 0 TADR = 1 = channel 1 TADR is sampled on the rising edge of TFCLK.
PTPA	Output	AF4	**POS-PHY Polled-PHY Transmit Packet Available** PTPA transitions high when a predefined (user programmable) minimum number of bytes are available in the polled transmit FIFO. Once high, PTPA indicates that the transmit FIFO is not full. When PTPA transitions low, it indicates that the transmit FIFO is full or near full (user programmable). PTPA allows the polling of the PM3386 channel selected by TADR address pin. The port which PTPA reports is updated on the following rising edge of TFCLK after the PM3386 channel address on TADR is sampled by the PM3386 device. PTPA is updated on the rising edge of TFCLK.

Signal Name	Direction	Pin No.	Function
STPA	Output	AD5	**POS-PHY Selected-PHY Transmit Packet Available** STPA transitions high when a predefined (user programmable) minimum number of bytes are available in the transmit FIFO specified by the in-band address on TDAT bus. Once high, STPA indicates the transmit FIFO is not full. When STPA transitions low, it indicates that the transmit FIFO is full or near full (user programmable). STPA always provides status indication for the selected port of the PM3386 device in order to avoid FIFO overflows while polling is performed. The port which STPA reports is updated on the following rising edge of TFCLK after the PM3386 channel address on TDAT is sampled by the PM3386 device. STPA is updated on the rising edge of TFCLK.
DTPA0 DTPA1	Output	AF3 AE4	**POS-PHY Direct Transmit Packet Available** Active high signals that provide direct status indication for the corresponding ports in the PM3386. DTPA[1:0] transitions high when a predefined (user programmable) minimum number of byes are available in the transmit FIFO. Once high, the DTPA[1:0] signals indicate that its corresponding transmit FIFO is not full. When DTPA[1:0] transitions low, it indicates that its transmit FIFO is full or near full. (user programmable). DTPA0 corresponds to channel zero. DTPA1 corresponds to channel one. DTPA0 and DTPA1 are updated on the rising edge of TFCLK.

Table 5 - POS-PHY Level 3 Receive Interface

Signal Name	Direction	Pin No.	Function
RFCLK	Schmitt Input	W1	**POS-PHY Receive FIFO Write Clock** RFCLK is used to synchronize data transfer transactions between the higher layer device and the PM3386. RFCLK cycles at a rate of 60 to 104 MHz.
RVAL	Output	W3	**POS-PHY Receive Data Valid** Active high signal indicating the validity of the receive data signals. RVAL will transition low when a receive FIFO is empty, at the end of a data burst from a given channel. When RVAL is high, the RDAT[31:0], RPRTY, RMOD[1:0], RSOP, REOP and RERR signals are valid. When RVAL is low, the RDAT[31:0], RPRTY, RMOD[1:0], RSOP, REOP and RERR signals are invalid and must be disregarded. The RSX signal is only valid when RVAL is low. RVAL is updated on the rising edge of RFCLK.

Signal Name	Direction	Pin No.	Function
RENB	Input	AA1	**POS-PHY Receive Read Enable** Active low signal used to control the flow of data from the PM3386. The higher layer device may de-assert RENB at anytime if it is unable to accept data from the PM3386. When RENB is sampled low by the PM3386, the upper level device is signaling that it can receive data. RSX may then be asserted to indicate a new address on the RDAT[0] bus pin or RVAL may be asserted indicating validity of read data and control on the RDAT[31:0], RPRTY, RMOD[1:0], RSOP, REOP, and RERR signals. Note that these signals will be updated on the following rising edge of the RFCLK. When RENB is sampled high by the PM3386, the upper level device is signaling that it can no longer accept data. On the following rising edge of RFCLK, if active, the RVAL signal will remain asserted signifying valid data and control on RDAT[31:0], RPRTY, RMOD[1:0], RSOP, REOP, and RERR. RENB is sampled on the rising edge of RFCLK.

Signal Name	Direction	Pin No.	Function
RDAT[0]	Output	F1	**POS-PHY Receive Packet Data Bus** The RDAT[31:0] bus carries the packet octets that are read from the receive FIFO and the in-band port address of the selected receive FIFO. The in-band address on RDAT[0] is considered valid only when RVAL is de-asserted (LOW) and RSX is asserted (HIGH). The data on RDAT[31:0] is considered valid only when RVAL is asserted(HIGH). Data is presented on the data bus in big endian order on RDAT[31:0]. RDAT[31:0] is updated on the rising edge of RFCLK.
RDAT[1]		G2	
RDAT[2]		H3	
RDAT[3]		H2	
RDAT[4]		J3	
RDAT[5]		K4	
RDAT[6]		H1	
RDAT[7]		J2	
RDAT[8]		K3	
RDAT[9]		K2	
RDAT[10]		L3	
RDAT[11]		K1	
RDAT[12]		L2	
RDAT[13]		L1	
RDAT[14]		M3	
RDAT[15]		M2	
RDAT[16]		M1	
RDAT[17]		N3	
RDAT[18]		N2	
RDAT[19]		P2	
RDAT[20]		P3	
RDAT[21]		P4	
RDAT[22]		R1	
RDAT[23]		R2	
RDAT[24]		R3	
RDAT[25]		T1	
RDAT[26]		T2	
RDAT[27]		U1	
RDAT[28]		T3	
RDAT[29]		U2	
RDAT[30]		T4	
RDAT[31]		V1	

Signal Name	Direction	Pin No.	Function
RPRTY	Output	U3	**POS-PHY Receive Parity** The receive parity (RPRTY) signal indicates the parity calculated over the RDAT bus. RPRTY is only valid when RVAL or RSX is asserted. The PM3386 supports both odd and even parity over the RDAT bus. RPRTY is updated on the rising edge of RFCLK.
RMOD[0] RMOD[1]	Output	Y1 W2	**POS-PHY Receive Word Modulo** RMOD[1:0] indicates the number of valid bytes of data in RDAT[31:0]. The RMOD bus must always be zero, except during the last double-word transfer of a packet on RDAT[31:0]. When REOP and RVAL are asserted, the number of valid packet data bytes on RDAT[31:0] is specified by RMOD[1:0]. RMOD[1:0] = “00” RDAT[31:0] valid RMOD[1:0] = “01” RDAT[31:8] valid RMOD[1:0] = “10” RDAT[31:16] valid RMOD[1:0] = “11” RDAT[31:24] valid RMOD[1:0] is considered valid only when RVAL and REOP are asserted. RMOD[1:0] is updated on the rising edge of RFCLK.
RSOP	Output	Y2	**POS-PHY Receive Start of Packet** Active high signal used to delineate the packet boundaries on the RDAT bus. When RSOP is high, the start of the packet is present on the RDAT bus. RSOP is required to be present at the start of every packet and is only considered valid when RVAL is asserted. RSOP is updated on the rising edge of RFCLK.

Signal Name	Direction	Pin No.	Function
REOP	Output	V2	**POS-PHY Receive End Of Packet** Active high signal used to delineate the packet boundaries on the RDAT bus. When REOP is high, the end of the packet is present on the RDAT bus. Note that RMOD[1:0] indicates the number of valid bytes the last double word is composed of when REOP and RVAL are asserted. REOP is required to be present at the end of every packet and is considered valid only when RVAL is asserted. REOP is updated on the rising edge of RFCLK.
RERR	Output	V3	**POS-PHY Receive error indicator** Active high signal used to indicate that the current packet is aborted and should be discarded. RERR shall only be asserted when REOP and RVAL are asserted. Conditions that can cause RERR to be set may be, but are not limited to, FIFO overflow, abort sequence detection and FCS error. RERR is updated on the rising edge of RFCLK.

Signal Name	Direction	Pin No.	Function
RSX	Output	U4	**POS-PHY Receive Start of Transfer** RSX indicates when the in-band port address is present on the RDAT bus. When RSX is high and RVAL is low, the value of RDAT[0] is the address of the receive FIFO to be selected by the PM3386. Subsequent data transfers on the RDAT bus will be from the FIFO specified by this in-band address. RSX is considered valid only when RVAL is not asserted. RSX is considered valid only when RENB was asserted on the previous cycle. RSX is updated on the rising edge of RFCLK.

Table 6 - Side-band Flow Control

Name	Type	Pin No.	Description
PAUSE0 PAUSE1	Input Internal pull-down	AB1 Y4	**PAUSE Control** Assertion of the PAUSE0 or PAUSE1 signals may cause (programmed option) the PM3386 on a per channel basis to transmit 802.3-1998 PAUSE frames and either drop at the MAC layer or pass to the POS-PHY L3 client any further incoming frames (programmed option). De-assertion of the PAUSE0 or PAUSE1 signal can cause the removal of the PAUSE condition on a per channel basis. Due to the programmability options for these pins please see the PAUSE flow control section in the Operations section. PAUSE0 and PAUSE1 are active high signals. PAUSE0 and PAUSE1 are sampled on the rising edge of the RFCLK.

PAUSED0 PAUSED1	Output	Y3 AA2	**PAUSED Status** The PAUSED0 and PAUSED1 signals indicate the reception and execution of 802.3-1998 PAUSE control frames on the given port of the PM3386. An asserted (high) PAUSED0 or PAUSED1 pin indicates that the corresponding channels ingress PAUSE timer is non-zero. This also typically indicates (if enabled via the **FCRX** bit in the **EGMAC GMACC1-Config Register**) that the given channel is in a paused state. De-assertion of the PAUSED0 or PAUSED1 pin indicates that the corresponding channels PAUSE counter is now zero. This also typically indicates that the given channel is no longer pausing on that channel. Please refer to the **FCRX** bit definition for more information. PAUSED0 and PAUSED1 are updated on the rising edge of RFCLK.

Table 7 Microprocessor Interface

Pin Name	Type	Pin No.	Function
CSB	Input	A15	**Active-low chip select** The CSB signal is low during PM3386 register accesses. If CSB is not required (i.e., registers accesses are controlled using the RDB and WRB signals only), CSB must be connected tied low.
RDB	Input	B15	**Active-low read enable** The RDB signal is low during PM3386 register read accesses. The PM3386 drives the D[15:0] bus with the contents of the addressed register while RDB and CSB are low.

Pin Name	Type	Pin No.	Function
WRB	Input	C15	**Active-low write strobe** The WRB signal is low during a PM3386 register write accesses. The D[15:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low.
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7] D[8] D[9] D[10] D[11] D[12] D[13] D[14] D[15]	I/O	D7 A5 B6 C7 A6 B7 C8 A7 B8 C9 A8 B9 C10 A9 D11 B10	**The bi-directional data bus** D[15:0] is used during PM3386 register read and write accesses.
A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7] A[8] A[9] A[10]	Input	C11 A10 B11 A11 C12 B12 A12 C13 B13 B14 C14	**Address bus** A[10:0] selects specific registers during PM3386 register accesses.
ALE	Input Internal pull-up	A16	**Address latch enable** ALE is active-high and latches the address bus A[10:0] when low. When ALE is high, the internal address latches are transparent. It allows the PM3386 to interface to a multiplexed address/data bus. ALE has an integral pull-up resistor.

Pin Name	Type	Pin No.	Function
INTB	Output Open Drain	B16	**Active-low interrupt** INTB is set low when a PM3386 interrupt source is active and that source is unmasked. The PM3386 may be enabled to report many alarms or events via interrupts. INTB is tri-stated when the interrupt is acknowledged via an appropriate register access. INTB is an open drain output.

Table 8 - Device Miscellaneous

Name	Type	Pin No.	Description
RSTB	Schmitt input Internal pull-up	G3	**Master Reset** This active low reset signal input provides an asynchronous reset to the device. RSTB is a Schmitt triggered input with an internal pull-up resistor. When RSTB is forced low, all device registers are forced to their default states.
PMD_SEL0 PMD_SEL1	Input Internal pull-down	V24 F25	**Physical Medium Select** These active high signals select between using the on-board SERDES or external transceiver via the GMII pins. A low (tied to VSS) will select internal SERDES. A high (tied to VDDO) will select external transceiver via the GMII pins. These pins are required to be tied to VDDO or VSS prior to device power up.

Table 9 - JTAG Test Access Port (TAP) Signals

Name	Type	Pin No.	Description
TCK	Input	C6	**JTAG Test Clock** The JTAG test clock (TCK) signal provides clock timing for test operations that are carried out using the IEEE P1149.1 test access port. TCK must be tied to VSS or VDDO when not in JTAG test.
TMS	Input Internal pull-up	B5	**JTAG Test Mode Select** TMS controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an internal pull up resistor.
TDI	Input Internal pull-up	A4	**JTAG test Input** TDI carries test data into the PM3386 via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an internal pull-up resistor
TDO	Output	D6	**JTAG Test Output** TDO carries test data out of the PM3386 via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is inactive except when in the progress of shifting boundary scan data out.
TRSTB	Schmitt Input Internal pull-up	C5	**JTAG Test Reset** TRSTB provides an asynchronous reset for testing via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with and internal put-up resistor. Note that when not being used for JTAG testing the TRSTB pin must be connected to the RSTB input for proper normal mode operation.

Table 10 Power and Grounds

Pin Name	Type	Pin No.	Function
VDDI	Power	F23 F24 V23 AA23 AC22 AC20 AC16 AC11 AC8 AC6 W4 R4 M4 G1 D10 D12 D16 D19	1.8V Digital power to the core logic

Pin Name	Type	Pin No.	Function
VDDO	Power	D23 C24 B25 D18 D13 D8 D4 C3 B2 H4 N4 V4 AC4 AD3 AE2 AC9 AC14 AC19 AC23 AD24 AE25 Y23 T23 J23 D24 E24 AB24 AC24	3.3V Digital power to the I/O

Pin Name	Type	Pin No.	Function
VDDQ	Power	G24 AC15 AA3 L4 D15	3.3V Digital Quite power to the I/O
AVDH	Analog Power	H26 J24 L25 L24 N24 R23 U24	3.3V Analog power to analog cells. Insure these inputs are connected to a well-decoupled +3.3V DC supply.
AVDL	Analog Power	G23 H23 H24 K23 K24 N26 N25 N23 P23 P25 P26 T24 T25	1.8V Analog power to analog cells. Insure these inputs are connected to a well-decoupled +1.8V DC supply.
AVDQ	Analog Power	H25 P24	3.3V Analog Quite power to analog cells. Insure these inputs are connected to a well-decoupled +3.3V DC supply.

Pin Name	Type	Pin No.	Function
VSS	Ground	A26 B26 C25 A25 B24 A14 A13 B3 A2 A1 B1 C2 N1 P1 AD2 AE1 AF1 AF2 AE3 AF13 AF14 AE24 AF25 AF26 AE26 AD25 AD26 AC25 AC26 AB26 Y26 V26 T26 L26 J26 G26 E26 D26 D25 C26 F26 AF15 AB2 J1 A17	Device ground

Notes on Pin Description:

1. All PM3386 inputs and bi-directional signals present minimum capacitive loading and operate at TTL logic levels except the inputs marked as Analog or PECL.

2. The GTX_CLK0, GTX_CLK1, TXD0[7:0], TXD1[7:0], TX_ER0, TX_ER1, TX_EN0, TX_EN1, MDC, MDIO, STPA, PTPA, DTPA[1:0], RVAL, RDATA[31:0], RPRTY, RMOD[1:0], RSOP, REOP, RERR, RSX, PAUSED0, PAUSED1, D[15:0], INTB, and TDO outputs have 6mA drive capability.

3. All digital inputs are 5V tolerant.

4. The PECL inputs and outputs should be terminated in a passive network and interface at PECL levels as described in the Operations section.

5. It is mandatory that every ground pin (VSS) be connected to the printed circuit board ground plane to ensure reliable device operation.

6. It is mandatory that every digital power pin (VDDI, VDDO, and VDDQ) be connected to the printed circuit board power planes to ensure reliable device operation.

7. All analog power pins can be sensitive to noise. They must be isolated from the digital power. Care must be taken to correctly decouple these pins.

8. It is mandatory that every analog power pin (AVDL, AVDH, and AVDQ) be de-coupled from but connected to the printed circuit board power planes to ensure reliable device operation.

8. Due to ESD protection structures in the pads it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions it is possible to damage these ESD protection devices or trigger latch up. Please adhere to the recommended power supply sequencing as described in the Operation section of this document.

10 FUNCTIONAL DESCRIPTION

The PM3386 provides a high density and low power solution for implementing Gigabit Ethernet connectivity. The PM3386 is a dual Gigabit Ethernet controller with integrated SERDES and GMAC functions connecting to a standard POS-PHY Level 3 system interface. The PM3386 accepts serial bit streams from optical transceiver devices or Gigabit Ethernet PHY devices and performs Media Access Control frame verification. Statistics are maintained and the frame is forwarded to internal FIFOs for the POS-PHY Level 3 interface. The PM3386 may be connected to an upper layer device via the POS-PHY Level 3 interface for classification and forwarding.

The PM3386 is partitioned into the following major functional blocks. The operation of each block is described in more detail in subsequent sections.

- SERDES
- Enhanced Gigabit Media Access Control
- Ethernet Statistics
- Address Filtering
- POS-PHY Level 3 System Interface
- Microprocessor Interface

10.1 Serializer-Deserializer (SERDES)

The PM3386 has two internal serializer-deserializer transceivers. The SERDES is IEEE 802.3-1998 Gigabit Ethernet compatible supporting gigabit data transfer flows. The SERDES is based on the X3T11 10 Bit specification. The PECL cells used to implement the SERDES are capable of both 5V and 3.3V low voltage PECL operation as they can be AC coupled within the system design.

The transmitter section of the SERDES accepts 10-bit wide parallel data and serializes this data into a high-speed serial data stream. The parallel data is 8B/10B encoded data. An internally generated reference clock is then multiplied to generate the 1250 MHz serial clock used to clock the encoded data out the high-speed output at a rate of 1250 Mbit/s. The high-speed outputs are capable of interfacing directly to a separate fiber optic module for optical transmission.

The receiver section accepts a serial electrical data stream at 1250 Mbit/s and recovers the original 10-bit wide parallel data. The receiver Clock Recovery Unit (CRU) locks onto the incoming serial signal and facilitates the recovery of the high-speed serial data. The serial data is converted back into 10-bit parallel data, recognizing the 8B/10B comma character to establish byte alignment. The recovered parallel data is presented to the EGMAC.

10.2 Enhanced Gigabit Media Access Control (EGMAC)

10.2.1 EGMAC General

The PM3386 integrates standard IEEE 802.3-1998 Gigabit Ethernet Media Access Control interfaces for connection to internal serializer-deserializers (SERDES) or external transceivers using Gigabit Media Independent Interface (GMII) pins on each gigabit Ethernet port. The dual ports of the PM3386 are capable of operation in either SERDES or GMII mode. The ports can be configured to operate independently from each other using the PMD_SEL0 and PMD_SEL1 pins.

The EGMAC is capable of supporting normal Ethernet frame sizes of 1518 bytes, VLAN tagged frame sizes of 1522 bytes, and Jumbo frames sizes up to 9.6k bytes. The **Transmit Max Frame Length** and the **Receive Max Frame Length** registers contain the values associate with maximum accepted Ethernet frame sizes. By default these registers contain a value of 1518 bytes. This allows for normal frame sizes as well as 1522 VLAN tagged frames to be accepted. The EGMAC will base all frame length calculations and statistics off of these registers. The EGMAC takes into account the VLAN tagging of frames to ensure their proper representation in the statistics gathering process. Note that it is possible to program the ingress and egress maximum frame sizes separately.

10.2.2 EGMAC Egress Direction

In the egress direction packet data from the PL3EP is presented to the EGMAC synchronizing transmit FIFO. The EGMAC/PL3EP interface is a push style interface. If packet data is available for transmit the PL3EP will push (transfer) data to the EGMAC. The PL3EP will notify the EGMAC of the start and end of packets by using simple end of packet and start of packet indications. The PL3EP will also present to the EGMAC an error signal that is asserted when an error condition is observed on the POS-PHY bus or if an internal error is encountered in the egress data path.

The EGMAC has an upper bound of 9.6k bytes on the size of egress frames. The egress direction of the EGMAC can accept packets of a minimum size of 14 bytes. Egress packets sent to the EGMAC that are of the minimum 14 bytes but

are less than the minimum 64 byte frame length required by 802.3-1998 have the programmed option to be padded appropriately to 64 bytes (68 bytes for VLAN tagged frames) and optionally have the associated 32 bit CRC appended to the frame prior to transmit. The user may also elect to program the EGMAC to insert the Frame Check Sequence (FCS) field.

In the case that the link device disregards the flow control information provided by DTPA0, DTPA1, STPA, or PTPA and continues to write to the PM3386 in an attempt to overflow the egress FIFO the PM3386 will truncate the current packet when the FIFO becomes full. At this time the PM3386 will wait until a minimum packet can be accepted and then resume data transfer.

In the event that the link device can not deliver the data fast enough to the PM3386, placing the PM3386 in a case of FIFO underrun, the current packet will be truncated sending all bytes currently available and then the PM3386 will re-sync to TSOP. In all error cases the CRC-32 that is kept over the packet will be invalidated and appended to the frame as it is transmitted thereby signaling an error.

Following each frame transmission the EGMAC provides a statistical vector to the MSTAT block that updates statistic collection counters maintained in system visible registers. Please refer to the MSTAT functional description and Register section of this document for a full list of port statistics.

10.2.3 EGMAC Ingress Direction

In the ingress direction the SERDES or GMII presents receive physical packet to the EGMAC. The EGMAC scans the preamble looking for the Start Frame Delimiter (SFD). By default the preamble and SFD are stripped converting the physical packet to a frame. The EGMAC will then compare the destination address in the frame to the address filtering logic for the given port. If enabled the address filtering logic may be programmed to accept or reject incoming frames. The EGMAC is also programmable to accept all frames regardless of validity.

The EGMAC supports ingress frame sizes of up to 9.6k bytes. The EGMAC interfaces to the PL3IP using a simple push style interface. The EGMAC signals start of frame and end of frame while transferring data information to the PL3IP.

There are two decision points at which the frame forwarding and filtering decisions are made. The first decision point is at the beginning of the ingress frame. At this point and once the SA, DA, and the possible VID fields are recognized the frame may be filtered based on the address filter logic described later. If the frame is to be forwarded the incoming data will be written to the

EGMAC ingress FIFO in preparation for frame transfer. If the frame is to be filtered the frame will not be written to the EGMAC FIFO and the EGMAC will re-sync to the next incoming ingress frame.

The second decision point is at the end of the frame. The EGMAC will perform frame integrity checks such as length and CRC. If the frame violates these integrity checks the frame will need to be discarded. Discarding a frame can be done in two possible ways. The cases are described below.

1. If the number of bytes that have been written to the EGMAC ingress FIFO are less than the programmed value within the **EGMAC Receive FIFO Forwarding Threshold** register, the frame in its entirety is stored within the FIFO, and will therefore be dropped within the EGMAC. The EGMAC will flush this frame from the FIFO and resume reception of ingress traffic on the next start of frame indication.

2. If the number of bytes that have been written to the EGMAC ingress FIFO are greater than the programmed value within the **EGMAC Receive FIFO Forwarding Threshold** register the frame will have started draining from the FIFO and therefore can not be dropped within the PM3386. In this case the frame will be marked as bad by assertion of the RX_ERR bit on the EGMAC PL3IP interface. This indication is carried to the POS-PHY Level 3 interface and will cause the assertion of the RERR bit on the last byte transfer of the packet.

As mentioned above ingress frames are held in the receive FIFO within the EGMAC until the byte count exceeds the forwarding threshold programmed in the **EGMAC Receive FIFO Forwarding Threshold** register or until End Of Frame (EOF). Frames that contain errors and are greater than the programmed value within the **EGMAC Receive FIFO Forwarding Threshold** register will be marked as erred by the PM3386 but will not be discarded within the PM3386.

The EGMAC will distinguish between unicast, broadcast, and multicast frames. The EGMAC can be programmed to forwarded or filter frames based on unicast, broadcast, or multicast type frames.

10.2.4 EGMAC Flow Control - MAC Control Sublayer

The PM3386 provides loss-less frame flow control for frame sizes up to 9.6k bytes over 1000BASE TX, 1000BASE SX, and 1000BASE LX implementations.

The EGMAC interface contains the MAC Control Sublayer which adheres to IEEE 802.3-1998 and provides support for Control frames. The EGMAC performs the functions out lined in IEEE 802.3-1998 Clause 31 “MAC Control” and Annexes 31A and 31B. Clause 31 introduces the optional MAC Control

sublayer to the popular layer stack. This sublayer provides for real-time control and manipulation of the MAC operation. The clause defines MAC control frames distinguishable by their unique Length/Type field identifier.

The EGMAC supports Annex 31A opcode PAUSE by implementing Annex31B's frame based flow control scheme which utilizes PAUSE Control frames. The purpose of flow control is to slow down the aggregate rate of frames that the other end of a link is sending. Finite FIFO depths have a tendency to overflow when line-rate frames are being received and the upper layer device cannot keep up. Thus to prevent the overflow of the FIFOs, flow control is used. A MAC Control client wishing to inhibit transmission of data frames from the PM3386 generates a PAUSE Control frame which contains the reserved multicast address (01-80-C2-00-00-01), the Control frame type field 88-08, the PAUSE opcode, 00-01, and the pauseTimer, a 16-bit value expressed in pause quanta of 512 bit times. When the EGMAC receives a PAUSE Control frame, it loads the Pause Timer with the value sent in the pauseTime filed. If pauseTime is non-zero and the **FCRX** bit within the **EGMAC GMACC1-Config Register** is asserted, the EGMAC will pause from transmitting frames and will wait for pauseTime number of slot times before resuming operation. If, however, the pauseTime value is equal to zero, the EGMAC is allowed to resume transmitting data frames. At any time if the EGMAC is receiving PAUSE control frames the EGMAC will assert the PAUSED0 or PAUSED1 status pins. These pins will be held asserted until the EGMAC pauseTime counts down to zero and the EGMAC resumes transmitting data frames. It is possible depending on the system requirements to allow ingress PAUSE Control frames to be processed or not processed at the EGMAC layer (see **FCRX** bit) and PAUSE Control frames to be dropped at the EGMAC layer or passed to the upper layer device(see **PASS_CTRL** bit).

If for any reason the upstream device needs to stop incoming frames, it can accomplish this by four different ways. First, the upper layer device can send 802.3-1998 PAUSE Control frames of its own. Second, the upper layer device can assert the PAUSE0 or PAUSE1 pins on the device to have the EGMAC automatically send PAUSE Control frames. Third, the system processor can initiate PAUSE operation via configuration registers in the EGMAC. Fourth, the link device can de-assert RENB and cause the FIFO fill levels in the PL3IP block to fill and start automatic flow control. Note that even though the EGMAC can be sending egress PAUSE Control frames the ingress channel will still be operational with the exception of normal blocking of the POS-PHY L3 data-path from the link level. Please refer to the Operations section under PAUSE Flow Control for programming options.

At the end of a PAUSE operation the PM3386 will send a PAUSE frame with a null Pause Timer value allowing quick PAUSE off signaling to downstream devices.

10.2.5 EGMAC Auto-Negotiation

The EGMAC implements Clause 37 of the IEEE 802.3-1998 Standard, Auto-Negotiation function, type 1000BASE-X. The Auto-Negotiation for 1000BASE-X function provides the means to exchange information between two devices that share a link segment allowing management the ability to configure both devices in such a way that takes maximum advantage of their capabilities. After a reset occurs the EGMAC senses whether or not Auto-Negotiation is enabled. If so the EGMAC will start Auto-Negotiation exactly following the state diagram as outlined in 802.3-1998 Clause 37. Base page Auto-Negotiation is therefore completely taken care of by the EGMAC.

Above base page Auto-Negotiation, the EGMAC communicates between the host processor and an external MII physical device by means of a two wire interface. The EGMAC block produces the clock (MDC) and the general MII I/O pin MDIO. The host controls the EGMAC MII via the MII management registers.

10.2.6 EGMAC Address Filter Logic

The EGMAC provides a rich set of address filtering options. The host microprocessor has complete programmable access to all filtering features.

The EGMAC can perform 8 separate exact-match MAC/VID unicast filter operations. Each unicast filter will perform an exact match on either the DA or the SA, and an optional exact match on the VID. If enabled, each unicast filter channel can be programmed to indicate ACCEPT or DISCARD upon match. Each unicast filter channel can be enabled separately.

The EGMAC also includes a 64-bin hash-based multicast filter. This hash-based filter utilizes 6-bits of the CRC-32 output taken over the MAC DA to provide the standard imperfect multicast filtering capability. The multicast filter output will be asserted only if the IEEE Group/Functional bit is set in the DA of the frame (Most significant bit of the least significant byte of the MAC DA). If enabled, the filter output will indicate ACCEPT only. If not enabled, it will indicate nothing.

10.3 Management Statistics (MSTAT)

The MSTAT block is used to accumulate Ethernet specific counts used for supporting management agents such RMON, SNMP, and Etherlike interfaces. The MSTAT provides counter width support for compliance with 802.3-1998

rollover requirements of 58 minutes. The MSTAT supports full system probing with counter snapshotting via shadow registers. Incorporated into the MSTAT block is a fully programmable interrupt array enabling per counter rollover monitoring with interrupt reporting.

10.4 POS-PHY Level 3 Physical Layer Interface

10.4.1 POS-PHY Level 3 General

The PM3386 can connect to a single upper level device through a POS-PHY Level 3 Interface. The POS-PHY Level 3 interface is a 32-bits wide interface with a clock rate of 104 MHz. POS-PHY Level 3 was developed with the cooperation of the SATURN Development Group to cover all application bit rates up to and including 3.2 Gbit/s. The POS-PHY Level 3 specification defines the requirements for interoperation between devices such as the multi-PHY PM3386 and a single Link Layer device. Each channel within the PM3386 contains a 64k byte ingress and 16k byte egress POS-PHY latency FIFO.

10.4.2 POS-PHY Level 3 Ingress Physical Layer Interface (PL3IP)

As a POS-PHY slave device, hence in the ingress or receive direction, the PM3386 outputs received packets to the upper layer device whenever data is available. The interface accepts a read clock (RFCLK) and read enable signal (RENB) when data is read from the ingress FIFO (using the rising edge of the RFCLK). The start of packet (RSOP) marks the first byte of received packet data on the RDAT[31:0] bus. The RPRTY signal reports parity on the RDAT[31:0] bus. Parity defaults to odd but may be programmed for even parity. The end of a packet is indicated by the REOP signal. The RERR signal is provided to indicate that an error in a received packet has occurred. The RVAL signal is used to indicate when RSOP, REOP, RERR, and RDAT[31:0] are valid. RSX indicates the start of transfer and marks the clock cycle where the in-band channel address is given on the RDAT[31:0] bus.

In the event that the upper level device cannot accept data it can de-assert RENB. At this point the specific port's POS-PHY interface ingress 64k byte FIFO will start to fill up. When the FIFO exceeds the programmed high water mark flow control threshold the ingress FIFO will assert an indication to the EGMAC to start PAUSE flow control. The ingress POS-PHY FIFO will continue to keep the flow control signal high until the number of entries in the FIFO have decreased to the programmed low water mark flow control threshold level.

In the event that the link layer device does not re-assert RENB to continue the data flow the PM3386 will buffer the incoming frames from the line side interface until all the buffer facilities within the PM3386 are exhausted. At this time the PM3386 will no longer accept data from the line side. All data bits will be dropped at the line interface until resources within the PM3386 become available. At this time the PM3386 will re-sync to physical packet and continue reception. In the event that the PM3386 truncates a frame because of resource exhaustion the frame will be marked as erred by asserting the RERR bit on the last interface transaction for the packet transfer as specified by the PL3 bus protocol.

The POS-PHY ingress FIFO will absorb in-flight frames when the PM3386 is placed into a PAUSE flow control state from the upper level device. The FIFO will accept a number of maximum size 9.6k byte frames without loss.

The scheduling of packets through the ingress POS-PHY interface is controlled via a simple round robin approach that fairly switches between both Gigabit Ethernet channels. The POS-PHY bursts packets across the interface using programmable burst sizes.

10.4.3 POS-PHY Level 3 Egress Physical Layer Interface (PL3EP)

The POS-PHY Level 3 compliant interface consists of a write clock (TFCLK), a write enable signal (TENB), the start of packet (TSOP) indication, the end of packet (TEOP) indication, erred packet (TERR) indication, and the parity bit (TPRTY).

The PM3386 supports all three POS-PHY Level 3 egress status modes. The STPA signal reports the selected egress FIFO's fill status. The PTPA signal shows the FIFO fill status for the polled channel. The DTPA[1:0] signal pins show the direct FIFO fill status on a per-channel basis. The TSX signal indicates when the in-band channel selection is given on the TDAT[7:0] pins. This is done at the beginning of each transfer sequence. If the in-band address does not equal 0 or 1 subsequent data transfers on the TENB bus will be dropped.

The TMOD[1:0] signal is provided to indicate whether 1, 2, 3, or 4 bytes are valid on the final word transfer of the packet(TEOP is asserted). A packet may be aborted by asserting the TERR signal at the end of the packet.

In the egress direction the PM3386 collects packets into the PM3386 egress FIFO and delays data transfer to the PM3386 EGMAC for transmission until the number of bytes gathered are equal to or greater than the **PL3EP Channel Minimum Frame Size** register or until end of packet (via TEOP) is signaled. Each packet must satisfy one of the two forwarding conditions prior to

transmission. This allows for programmable MAC underrun protection depending upon the application.

10.5 Microprocessor Interface

The PM3386 uses a simple 16 bit multiplexed or non-multiplexed microprocessor interface that is commonly found on PMC-Sierra devices.

The PM3386 supports complete accessibility to internal resources from the host microprocessor. This allows the host to read and write all host accessible registers and chip data structures.

10.6 JTAG Test Access Port Interface

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The PM3386 identification code is 033860CD hexadecimal.

11 NORMAL MODE REGISTER DESCRIPTION

This section describes the normal mode registers in the device.

Table 11 - PM3386 General Memory Map

Group	Address Range (Hex)
Top	0x0 to 0x7
PL3IP	0x100 to 0x14F
PL3EP	0x200 to 0x24B
EGMAC 0	0x300 to 0x376
EGMAC 1	0x400 to 0x476
MSTAT 0	0x500 to 0x5E9
MSTAT 1	0x600 to 0x6E9
SERDES	0x700 to 0x71F

Table 12 PM3386 Specific Memory Map

Address (Hex)	Register
Top Level Registers	
0x0	Identification Register
0x1	Product Revision Register
0x2	Reset Control Register
0x3	Interrupt Status Register
0x4	Device Status Register
0x5	Reference Out of Lock Status Register
0x6	Data Out Of Lock Status Register
0x7	Software Resource Register

Address (Hex)		Register
PL3IP Common Configuration Registers		
0x100		Reserved
0x101		PL3IP Interrupt Status
0x102		PL3IP Interrupt Mask
0x103		PL3IP Configuration Register
0x104		PL3IP Equalization Threshold Limit
0x105		PL3IP Equalization Difference Limit
0x106		Reserved
0x107		Reserved
0x108 – 0x11f		Reserved
PL3IP Channel Specific Registers		
Channel 0	**Channel 1**	
0x120	0x140	PL3IP Channel High Watermark
0x121	0x141	PL3IP Channel Low Watermark
0x122	0x142	PL3IP Channel Packet Burst Mask
PL3EP Common Configuration Registers		
0x200		Reserved
0x201		PL3EP Interrupt Status
0x202		PL3EP Interrupt Mask
0x203		PL3EP Configuration Register
0x204		Reserved
0x205		Reserved
0x206		Reserved
0x207 – 0x21f		Reserved
PL3EP Channel Specific Registers		
Channel 0	**Channel 1**	
0x220	0x240	PL3EP Channel FIFO Reserve
0x221	0x241	PL3EP Channel Minimum Frame Size

Address (Hex)		Register
EGMAC Registers		
Channel 0	**Channel 1**	
0x300	0x400	EGMAC - GMACC0: Config Register Low Word
0x301	0x401	EGMAC - GMACC0: Config Register High Word
0x302	0x402	EGMAC - GMACC1: Config Register Low Word
0x303	0x403	EGMAC - GMACC1: Config Register High Word
0x304	0x404	EGMAC - GMACC2: Config Register Low Word
0x305	0x405	EGMAC - GMACC2: Config Register High Word
0x306	0x406	EGMAC - GPCSC: PHY Config Low Word
0x307	0x407	EGMAC - GPCSC: PHY Config High Word
0x308	0x408	EGMAC - SA: Station Address [15:0]
0x309	0x409	EGMAC - SA: Station Address [31:16]
0x30A	0x40A	EGMAC - SA: Station Address [47:32]
0x30C	0x40C	EGMAC - TPID: VLAN Tag ID Register
0x310	0x410	EGMAC - RX_MAXFR: Receive Max Frame Length
0x316	0x416	Reserved
0x318	0x418	EGMAC - ANCTL: Auto-Negotiation Control
0x31A	0x41A	EGMAC - ANSTT: Auto-Negotiation Status
0x31C	0x41C	EGMAC - ANADV: Auto-Negotiation Advert low word
0x31D	0x41D	EGMAC - ANADV: Auto-Negotiation Advert high word
0x31E	0x41E	EGMAC - ANLPA: Auto-Neg Link Part Able low word
0x31F	0x41F	EGMAC - ANLPA: Auto-Neg Link Part Able high word
0x320		EGMAC - MCMD: MII Managment Command
0x322		EGMAC - MADR: MII Management PHY Address
0x324		EGMAC - MWTD: MII Management Write Data
0x326		EGMAC - MRDD: MII Management Read Data
0x328		EGMAC - MIND: MII Management Indicators
0x332	0x432	EGMAC – Transmit Control

Address (Hex)		Register
0x333	0x433	EGMAC: Control register
0x334	0x434	EGMAC: PAUSE Timer register
0x335	0x435	EGMAC: PAUSE Interval register
0x336	0x436	EGMAC: Transmit Max Frame Length
0x337	0x437	EGMAC: Receive FIFO Forwarding Threshold
0x338	0x438	Reserved
0x339	0x439	EGMAC: Exact Match Address 0 A Register
0x33A	0x43A	EGMAC: Exact Match Address 0 B Register
0x33B	0x43B	EGMAC: Exact Match Address 0 C Register
0x33C	0x43C	EGMAC: Exact Match Address 1 A Register
0x33D	0x43D	EGMAC: Exact Match Address 1 B Register
0x33E	0x43E	EGMAC: Exact Match Address 1 C Register
0x33F	0x43F	EGMAC: Exact Match Address 2 A Register
0x340	0x440	EGMAC: Exact Match Address 2 B Register
0x341	0x441	EGMAC: Exact Match Address 2 C Register
0x342	0x442	EGMAC: Exact Match Address 3 A Register
0x343	0x443	EGMAC: Exact Match Address 3 B Register
0x344	0x444	EGMAC: Exact Match Address 3 C Register
0x345	0x445	EGMAC: Exact Match Address 4 A Register
0x346	0x446	EGMAC: Exact Match Address 4 B Register
0x347	0x447	EGMAC: Exact Match Address 4 C Register
0x348	0x448	EGMAC: Exact Match Address 5 A Register
0x349	0x449	EGMAC: Exact Match Address 5 B Register
0x34A	0x44A	EGMAC: Exact Match Address 5 C Register
0x34B	0x44B	EGMAC: Exact Match Address 6 A Register
0x34C	0x44C	EGMAC: Exact Match Address 6 B Register
0x34D	0x44D	EGMAC: Exact Match Address 6 C Register
0x34E	0x44E	EGMAC: Exact Match Address 7 A Register

Address (Hex)		Register
0x34F	0x44F	EGMAC: Exact Match Address 7 B Register
0x350	0x450	EGMAC: Exact Match Address 7 C Register
0x351	0x451	EGMAC: Exact Match VID 0 Register
0x352	0x452	EGMAC: Exact Match VID 1 Register
0x353	0x453	EGMAC: Exact Match VID 2 Register
0x354	0x454	EGMAC: Exact Match VID 3 Register
0x355	0x455	EGMAC: Exact Match VID 4 Register
0x356	0x456	EGMAC: Exact Match VID 5 Register
0x357	0x457	EGMAC: Exact Match VID 6 Register
0x358	0x458	EGMAC: Exact Match VID 7 Register
0x359	0x459	EGMAC: Multicast Hash Low Word Register
0x35A	0x45A	EGMAC: Multicast Hash MidLow Word Register
0x35B	0x45B	EGMAC: Multicast Hash MidHigh Word Register
0x35C	0x45C	EGMAC: Multicast Hash High Word Register
0x35D	0x45D	EGMAC: Address Filter Control 0 Register
0x35E	0x45E	EGMAC: Address Filter Control 1 Register
0x35F	0x45F	EGMAC: Address Filter Control 2 Register
0x360	0x460	EGMAC: Address Filter Control 3 Register
MSTAT Registers		
Channel 0	**Channel 1**	
0x500	0x600	MSTAT: Control
0x501	0x601	MSTAT: Counter Rollover 0
0x502	0x602	MSTAT: Counter Rollover 1
0x503	0x603	MSTAT: Counter Rollover 2
0x504	0x604	MSTAT: Counter Rollover 3
0x505	0x605	MSTAT: Interrupt Mask 0
0x506	0x606	MSTAT: Interrupt Mask 1
0x507	0x607	MSTAT: Interrupt Mask 2

Address (Hex)		Register	
0x508	0x608	MSTAT: Interrupt Mask 3	
0x509	0x609	MSTAT Counter Write Address	
0x50A	0x60A	MSTAT Counter Write Data Low	
0x50B	0x60B	MSTAT Counter Write Data Middle	
0x50C	0x60C	MSTAT Counter Write Data High	
0x50D-0x50F	0x60D-0x60F	Reserved	
MSTAT Counter Registers			
0x510	0x610	Low	FramesReceivedOK
0x511	0x611	Mid	
0x512	0x612	High	
0x514	0x614	Low	OctetsReceivedOK
0x515	0x615	Mid	
0x516	0x616	High	
0x518	0x618	Low	FramesReceived
0x519	0x619	Mid	
0x51A	0x61A	High	
0x51C	0x61C	Low	OctetsReceived
0x51D	0x61D	Mid	
0x51E	0x61E	High	
0x520	0x620	Low	UnicastFramesReceivedOK
0x521	0x621	Mid	
0x522	0x622	High	
0x524	0x624	Low	MulticastFramesReceivedOK
0x525	0x625	Mid	
0x526	0x626	High	

Address (Hex)		Register	
0x528	0x628	Low	BroadcastFramesReceivedOK
0x529	0x629	Mid	
0x52A	0x62A	High	
0x52C	0x62C	Low	TaggedFramesReceivedOK
0x52D	0x62D	Mid	
0x52E	0x62E	High	
0x530	0x630	Low	PAUSEMACControlFrameReceived
0x531	0x631	Mid	
0x532	0x632	High	
0x534	0x634	Low	MACControlFrameReceived
0x535	0x635	Mid	
0x536	0x636	High	
0x538	0x638	Low	FrameCheckSequenceErrors
0x539	0x639	Mid	
0x53A	0x63A	High	
0x53C	0x63C	Low	FramesLostDueToInternalMACError
0x53D	0x63D	Mid	
0x53E	0x63E	High	
0x540	0x640	Low	SymbolError
0x541	0x641	Mid	
0x542	0x642	High	
0x544	0x644	Low	InRangeLengthErrors
0x545	0x645	Mid	
0x546	0x646	High	
0x548	0x648	Low	Reserved
0x549	0x649	Mid	
0x54A	0x64A	High	

Address (Hex)		Register	
0x54C	0x64C	Low	FramesTooLongErrors
0x54D	0x64D	Mid	
0x54E	0x64E	High	
0x550	0x650	Low	Jabbers
0x551	0x651	Mid	
0x552	0x652	High	
0x554	0x654	Low	Fragments
0x555	0x655	Mid	
0x556	0x656	High	
0x558	0x658	Low	UndersizedFrames
0x559	0x659	Mid	
0x55A	0x65A	High	
0x55C	0x65C	Low	ReceiveFrames64Octets
0x55D	0x65D	Mid	
0x55E	0x65E	High	
0x560	0x660	Low	ReceiveFrames65to127Octets
0x561	0x661	Mid	
0x562	0x662	High	
0x564	0x664	Low	ReceiveFrames128to255Octets
0x565	0x665	Mid	
0x566	0x666	High	
0x568	0x668	Low	ReceiveFrames256to511Octets
0x569	0x669	Mid	
0x56A	0x66A	High	
0x56C	0x66C	Low	ReceiveFrames512to1023Octets
0x56D	0x66D	Mid	
0x56E	0x66E	High	

Address (Hex)		Register	
0x570	0x670	Low	ReceiveFrames1024to1518Octets
0x571	0x671	Mid	
0x572	0x672	High	
0x574	0x674	Low	ReceiveFrames1519toMAXOctets
0x575	0x675	Mid	
0x576	0x676	High	
0x578	0x678	Low	JumboOctetsReceivedOK
0x579	0x679	Mid	
0x57A	0x67A	High	
0x57C	0x67C	Low	FilteredOctets
0x57D	0x67D	Mid	
0x57E	0x67E	High	
0x580	0x680	Low	FilteredUnicastFrames
0x581	0x681	Mid	
0x582	0x682	High	
0x584	0x684	Low	FilteredMulticastFrames
0x585	0x685	Mid	
0x586	0x686	High	
0x588	0x688	Low	FilteredBroadcastFrames
0x589	0x689	Mid	
0x58A	0x68A	High	
0x590	0x690	Low	FramesTransmittedOK
0x591	0x691	Mid	
0x592	0x692	High	
0x594	0x694	Low	OctetsTransmittedOK
0x595	0x695	Mid	
0x596	0x696	High	

Address (Hex)		Register	
0x598	0x698	Low	OctetsTransmitted
0x599	0x699	Mid	
0x59A	0x69A	High	
0x59C	0x69C	Low	FramesLostDueToInternalMACTransmissionError
0x59D	0x69D	Mid	
0x59E	0x69E	High	
0x5A0	0x6A0	Low	TransmitSystemError
0x5A1	0x6A1	Mid	
0x5A2	0x6A2	High	
0x5A4	0x6A4	Low	UnicastFramesTransmittedAttempted
0x5A5	0x6A5	Mid	
0x5A6	0x6A6	High	
0x5A8	0x6A8	Low	UnicastFramesTransmittedOK
0x5A9	0x6A9	Mid	
0x5AA	0x6AA	High	
0x5AC	0x6AC	Low	MulticastFramesTransmittedAttempted
0x5AD	0x6AD	Mid	
0x5AE	0x6AE	High	
0x5B0	0x6B0	Low	MulticastFramesTransmittedOK
0x5B1	0x6B1	Mid	
0x5B2	0x6B2	High	
0x5B4	0x6B4	Low	BroadcastFramesTransmittedAttempted
0x5B5	0x6B5	Mid	
0x5B6	0x6B6	High	
0x5B8	0x6B8	Low	BroadcastFramesTransmittedOK
0x5B9	0x6B9	Mid	
0x5BA	0x6BA	High	

Address (Hex)		Register	
0x5BC	0x6BC	Low	PAUSEMACCTRLFramesTransmitted
0x5BD	0x6BD	Mid	
0x5BE	0x6BE	High	
0x5C0	0x6C0	Low	MACCTRLFramesTransmitted
0x5C1	0x6C1	Mid	
0x5C2	0x6C2	High	
0x5C4	0x6C4	Low	TransmittedFrames64Octets
0x5C5	0x6C5	Mid	
0x5C6	0x6C6	High	
0x5C8	0x6C8	Low	TransmittedFrames65to127Octets
0x5C9	0x6C9	Mid	
0x5CA	0x6CA	High	
0x5CC	0x6CC	Low	TransmittedFrames128to255Octets
0x5CD	0x6CD	Mid	
0x5CE	0x6CE	High	
0x5D0	0x6D0	Low	TransmittedFrames256to511Octets
0x5D1	0x6D1	Mid	
0x5D2	0x6D2	High	
0x5D4	0x6D4	Low	TransmittedFrames512to1023Octets
0x5D5	0x6D5	Mid	
0x5D6	0x6D6	High	
0x5D8	0x6D8	Low	TransmittedFrames1024to1518Octets
0x5D9	0x6D9	Mid	
0x5DA	0x6DA	High	
0x5DC	0x6DC	Low	TransmittedFrames1519toMAXOctets
0x5DD	0x6DD	Mid	
0x5DE	0x6DE	High	

Address (Hex)		Register	
0x5E0	0x6E0	Low	JumboOctetsTransmittedOK
0x5E1	0x6E1	Mid	
0x5E2	0x6E2	High	
SERDES			
0x700		SERDES Lock Detect Change	
0x701		SERDES Lock Detect Mask	
0x702		Reserved	
0x703	0x713	SERDES Port Configuration	
0x704	0x714	Reserved	
0x705	0x715	SERDES Port TX Mode	
0x706	0x716	Reserved	
0x707	0x717	Reserved	
0x708	0x718	SERDES Port CRU Mode	

Register 0x0H: Identification Register

Bit	Type	Function	Default
Bit 15	R	ID[15]	0
Bit 14	R	ID[14]	0
Bit 13	R	ID[13]	1
Bit 12	R	ID[12]	1
Bit 11	R	ID[11]	0
Bit 10	R	ID[10]	0
Bit 9	R	ID[9]	1
Bit 8	R	ID[8]	1
Bit 7	R	ID[7]	1
Bit 6	R	ID[6]	0
Bit 5	R	ID[5]	0
Bit 4	R	ID[4]	0
Bit 3	R	ID[3]	0
Bit 2	R	ID[2]	1
Bit 1	R	ID[1]	1
Bit 0	R	ID[0]	0

ID[15:0]:

The Identification register presents a valid PMC product ID number for the device. This register is read only. The default value is 3386.

Register 0x1H: Product Revision Register

Bit	Type	Function	Default
Bit 15:0	R	Revision	X

Revision

This register is read only. This register presents the current device revision

Register 0x2H: Reset Control Register

Bit	Type	Function	Default
Bit 15:7	R	Reserved	0
Bit 6	R/W	RESET_PL3EPB	1
Bit 5	R/W	RESET_PL3IPB	1
Bit 4	R/W	DIS_STRETCH	0
Bit 3:2	R	Reserved	0
Bit 1	R/W	ARESETB	1
Bit 0	R/W	DRESETB	1

The Reset Control Register generates the reset source output used by blocks in the PM3386.

DRESETB:

Master digital device reset. Performing a hardware reset will clear this bit to a 1. Setting this bit to a 0 will cause the digital portion of the device to reset. It is the responsibility of the programmer to de-assert or set this bit to a one in order to perform a proper software reset sequence. Please refer to the operations section of this document for instructions concerning resetting this device using software.

ARESETB:

Master analog device reset. Performing a hardware reset will clear this bit to a 1. Setting this bit to a 0 will cause the analog portion of the device to reset. It is the responsibility of the programmer to de-assert or set this bit to a one in order to perform a proper software reset sequence. Please refer to the operations section of this document for instructions concerning resetting this device using software.

DIS_STRETCH:

By default the internal digital reset is held asserted approximately 10ms after the de-assertion of the RSTB pin. To disable this delay the DIS_STRETCH bit can be set to logic 1. This will terminate the internal digital reset delay. By default this bit is disabled. Please refer to the operations section for further information.

RESET_PL3IPB:

This bit allows for software reset of the PL3IP logic. By default this pin is not asserted or logic 1. To reset the PL3IP the programmer must set this bit to logic 0, wait for a minimum of 100 ns (there is no maximum), and then set this bit back to logic 1.

RESET_PL3EP:

This bit allows for software reset of the PL3EP logic. By default this pin is not asserted or logic 1. To reset the PL3EP the programmer must set this bit to logic 0, wait for a minimum of 100 ns (there is no maximum), and then set this bit back to logic 1.

Register 0x3H: Interrupt Status Register

Bit	Type	Function	Default
Bit 15:6	R	Reserved	0
Bit 7	R	DOOL_INT	0
Bit 6	R	ROOL_INT	0
Bit 5	R	Reserved	0
Bit 4	R	Reserved	0
Bit 3	R	PL3EP_INT	0
Bit 2	R	PL3IP_INT	0
Bit 1	R	MSTAT1_INT	0
Bit 0	R	MSTAT0_INT	0

X_INT:

Interrupt indication bits. Theses bits indicate that the given interrupt is currently active. In general this is a global interrupt status indication. Simply reading this register does not clear the interrupt. Each interrupt source may have its own requirements for clearing the interrupt condition. Further specification on each interrupt bit can be found in the Operation section of this document. A logical NOR of all the X_INT signals produces the active low INTB signal used to notify the external processor of an interrupt condition. The following table provides the block source interrupt and mask registers that make up the top level interrupt bits as listed above.

Table 13 Interrupt Bit Resource Mapping

Top Level Interrupt Bit	Block Level Interrupt Register (Interrupt Source)	Block Level Interrupt Mask Register
DOOL_INT	Register 0x700 Bits[1:0]	Register 0x701 Bits[1:0]
ROOL_INT	Register 0x700 Bits[15],[9:8]	Register 0x701 Bits[15],[9:8]
PL3EP_INT	Register 0x201 Bits[7:0]	Register 0x202 Bits[7:0]
PL3IP_INT	Register 0x101 Bits[15:0]	Register 0x102 Bits[15:0]
MSTAT1_INT	Register 0x601 Bits[15], [13:0]	Register 0x605 Bits[15],[13:0]
	Register 0x602 Bits[14:0]	Register 0x606 Bits[14:0]
	Register 0x603 Bits[15:0]	Register 0x607 Bits[15:0]
	Register 0x604 Bits[5:0]	Register 0x608 Bits[5:0]
MSTAT0_INT	Register 0x501 Bits[15], [13:0]	Register 0x505 Bits[15],[13:0]
	Register 0x502 Bits[14:0]	Register 0x506 Bits[14:0]
	Register 0x503 Bits[15:0]	Register 0x507 Bits[15:0]
	Register 0x504 Bits[5:0]	Register 0x508 Bits[5:0]

Register 0x4H: Device Status Register

Bit	Type	Function	Default
Bit 15	R	Reserved	1
Bit 14	R	Reserved	1
Bit 13:6	R	Reserved	0
Bit 5	R	DLL1_ERR	0
Bit 4	R	DLL1_RUN	0
Bit 3	R	Reserved	0
Bit 2	R	Reserved	0
Bit 1	R	DLL0_ERR	0
Bit 0	R	DLL0_RUN	0

The Device Status Register provides the ability to monitor device operation.

DLL0_RUN:

The DLL0 run status (DLL0_RUN) indicates the DLL0 has locked to the reference clock RFCLK input (Active high).

DLL0_ERR:

The DLL0 error status (DLL0_ERR) indicates the DLL0 has run out of delay line and can not achieve lock (Active High).

DLL1_RUN

The DLL1 run status (DLL1_RUN) indicates the DLL1 has locked to the reference clock (TFCLK_TREE) input (Active High).

DLL1_ERR:

The DLL1 error status (DLL1_ERR) indicates the DLL1 has run out of delay

Register 0x5H: Reference Out Of Lock Status Register

Bit	Type	Function	Default
Bit 15	R	TX_ROOL	1
Bit 14:2	R	Reserved	0
Bit 1	R	RX_ROOL1	1
Bit 0	R	RX_ROOL0	1

The Reference Out Of Lock Status Register provides information from the SERDES blocks of the device.

RX_ROOL0:

Receive Reference Out Of Lock Condition Channel 0 (Active logic 1). The receive clock is not trained to the reference frequency.

RX_ROOL1:

Receive Reference Out Of Lock Condition Channel 1 (Active logic 1). The receive clock is not trained to the reference frequency.

TX_ROOL:

Transmit Reference Out Of Lock Condition (Active logic 1). The transmit clock is not trained to the reference frequency. All ports share a single

Register 0x6H: Data Out of Lock Status Register

Bit	Type	Function	Default
Bit 15:2	R	Reserved	0
Bit 1	R	RX_DOOL1	1
Bit 0	R	RX_DOOL0	1

The Data Out of Lock Status Register provides information for the SERDES block of the device.

RX_DOOL0:

Receive Data Out Of Lock Condition Channel 0 (Active logic 1). The receive clock is not aligned to the selected data steam.

RX DOOL1:

Receive Data Out Of Lock Condition Channel 1 (Active logic 1). The receive

Register 0x7H: Software Resource Register

Bit	Type	Function	Default
Bit 15:0	R/W	User_Defined	X

User_Defined:

The Software Resource register does not control any internal function within the PM3386. This register is not reset. This register is read/writeable for use by software.

Register 0x101H: PL3IP Interrupt Status

Bit	Type	Function	Default
Bit 15	R	IP_IS[15]	0
Bit 14	R	Reserved	0
Bit 13	R	IP_IS[13]	0
Bit 12-8	R	Reserved	0
Bit 7	R	IP_IS[7]	0
Bit 6	R	Reserved	0
Bit 5	R	IP_IS[5]	0
Bit 4-0	R	Reserved	0

The PL3IP Interrupt Status register is used to capture error status bits from both channels. This register is used in conjunction with the PL3IP Interrupt Mask register. This register is read only to the user. A read of this register will clear the register and the interrupt.

IP_IS[5] – Channel 0 Software Programmed Fault

The software programmed fault occurs when the user programs the PL3IP Channel Low Watermark Register 0x121 to a larger value than the PL3IP Channel High Watermark Register 0x120.

IP_IS[7] – Channel 0 Equalization Indication

Indicates that at some time during the operation of the PL3IP that the equalization for this channel was activated.

IP_IS[13] – Channel 1 Software Programmed Fault

A software programmed fault occurs when the user programs the PL3IP Channel Low Watermark Register 0x141 to a larger value then the PL3IP Channel High Watermark Register 0x140.

IP_IS[15] – Channel 1 Equalization Indication

Indicates that at some time during the operation of the PL3IP that the equalization for this channel was activated.

Register 0x102H: PL3IP Interrupt Mask

Bit	Type	Function	Default
Bit 15	R	IP_IM[15]	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	IP_IM[13]	0
Bit 12-8	R/W	Reserved	0
Bit 7	R	IP_IM[7]	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	IP_IM[5]	0
Bit 4-0	R/W	Reserved	0

The PL3IP Interrupt Mask register is used to mask out errors when determining when to send an interrupt. A bit set in any location will enable the corresponding interrupt notification by unmasking the possible pending interrupt. This is a user programmable register.

IP_IM[5] – Channel 0 Software Programmed Fault Mask

Mask bit for error type specified in corresponding bit location in the PI3IP Interrupt Status register.

IP_IM[7] – Channel 0 Equalization Indication Mask

Mask bit for indication type specified in corresponding bit location in the PI3IP Interrupt Status register.

IP_IM[13] – Channel 1 Software Programmed Fault Mask

Mask bit for error type specified in corresponding bit location in the PI3IP Interrupt Status register.

IP_IM[15] – Channel 1 Equalization Indication Mask

Mask bit for indication type specified in corresponding bit location in the PI3IP Interrupt Status register.

Register 0x103H: PL3IP Configuration Register

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	Reserved	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 7	R/W	IP_CR[7]	1
Bit 6	R/W	IP_CR[6]	0
Bit 5	R/W	IP_CR[5]	0
Bit 4	R/W	IP_CR[4]	0
Bit 3	R/W	IP_CR[3]	0
Bit 2	R/W	IP_CR[2]	0
Bit 1	R/W	IP_CR[1]	0
Bit 0	R/W	IP_CR[0]	0

The PL3IP Configuration Register controls the enabling and disabling of features for the PL3IP. Writing a 1 to a non-reserved bit location will cause the feature to be enabled.

IP_CR[0] - Channel 0 Protocol Check Enable

This bit turns on the protocol checking feature and does not allow corrupted packets to be written into the FIFO. Disabling this feature may be useful for system diagnostics. High is on. Low is off.

IP_CR[1] - Channel 1 Protocol Check Enable

This bit turns on the protocol checking feature and does not allow corrupted packets to be written into the FIFO. Disabling this feature may be useful for system diagnostics. High is on. Low is off.

IP_CR[2] - Enable Equalized Transfer Mode

Enable equalized transfer mode. When enabled, the threshold register and the limit register will be used to evaluate the state of both channels.

IP_CR[3] - Parity Odd or Even Generation

Parity Generation mode for the PL3IP. The default is odd mode parity generation (0). If set high (1), even mode parity generation will be used. Once set, the same mode is used on both channels.

IP_CR[5:4] - RFCLK Transfer Gap Selection

Bits [5:4] are used to set the transfer gap selection for the POS-PHY L3 interface. The rate is programmable from 0 to 3 RFCLK cycles. This will allow the user to program the latency between selection of new channel and transmitting of a new packet.

Table 11-14: Transfer Gap Rate

IP_CR[5:4]	Gap Transfer Rate
00(Default)	0 RFCLKs
01	1 RFCLKs
10	2 RFCLKs
11	3 RFCLKs

IP_CR[6] – Pause Mode Selection

Pause Mode Selection controls how the PAUSE0 and PAUSE1 pins are used.
If Pause Mode Selection is low (default) the PAUSE0 and PAUSE1 inputs control the PAUSE frame generation for their respective channels. Setting PAUSE0 or PAUSE1 to high will cause the PM3386 to start sending pause frames on their corresponding channels as described in the Operations section. Setting PAUSE0 or PAUSE1 low, and the PM3386 was previously sending PAUSE frames, the PM3386 will send an xoff PAUSE frame on that channel.
If Pause Mode Selection is high the PAUSE0 and PAUSE1 pins are masked from directly effecting the PAUSE frame generation. In this case when the user asserts the PAUSE0 or PAUSE1 pins the respective channel will finish sending on the PL3 bus the remaining number of bytes in the programmed

minimum burst size or until EOP is detected and then hold off sending data on the channel until the PAUSE0 or PAUSE1 pins are de-asserted. Upon de-assertion, if available, data will continue to be transferred across the PL3 interface for that channel. Please refer to the Operation section for more detail on this feature.

IP_CR[7] – Channel Enable

Channel Enable is used to update configuration values into the PL3IP when required due to configuration change. The differing PL3IP configuration registers (0x104, 0x105, 0x120, 0x121, 0x122, 0x140, 0x141, 0x142) may be written to at any time but will only update when this bit is cleared. The user programs the PL3IP configuration registers and then writes a zero to this bit to update the registers within the PL3IP. This bit will automatically return to one when the update is complete..

Register 0x104H: PL3IP Equalization Threshold Limit

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	Reserved	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	Reserved	0
Bit 4	R	Reserved	0
Bit 3	R	Reserved	0
Bit 2	R/W	IP_ETL[2]	1
Bit 1	R/W	IP_ETL[1]	1
Bit 0	R/W	IP_ETL[0]	0

The PL3IP Equalization Threshold Limit is used when the equalized transfer mode is enabled. This register can be written at any time but is only updated internally by using the **PL3IP Configuration** register.

IP_ETL[2:0]

PL3IP Threshold Limit Register is used to set the upper limit in bytes for equalization support. Please refer to the Operations section for more information on equalization. Table 15 provides the programmable options.

Table 15 Equalization Threshold Limits

IP_ETL[2:0]	Equalization Threshold Limit
000	512
001	1024
010	2048
011	4096
100	8192
101	16384
110 (default)	32768
111	32768

Register 0x105H: PL3IP Equalization Difference Limit

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	Reserved	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	Reserved	0
Bit 4	R	Reserved	0
Bit 3	R	Reserved	0
Bit 2	R/W	IP_EDL[2]	1
Bit 1	R/W	IP_EDL[1]	1
Bit 0	R/W	IP_EDL[0]	0

The PL3IP Equalization Difference Limit Register is used when the equalized transfer mode is enabled. This register can be written at any time but is only updated by using the **PL3IP Configuration** register.

IP_EDL[2:0]

PL3IP Equalization Difference Limit is used to set the maximum difference in bytes between the two channels FIFOs. Default is 32768 bytes, or the 1/2 FIFO storage space. The lower limit supported by the hardware is 512 bytes. Please refer to the Operations section for more information on equalization. Table 16 provides the accepted programmable options.

Table 16 Equalization Difference Limits

IP_EDL[2:0]	Equalization Difference Limit
000	512
001	1024
010	2048
011	4096
100	8192
101	16384
110	32768
111	32768

Register 0x120H, 0x140H: PL3IP Channel High Watermark

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	Reserved	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	Reserved	0
Bit 4	R	Reserved	0
Bit 3	R/W	IP_PHWM[3]	0
Bit 2	R/W	IP_PHWM[2]	1
Bit 1	R/W	IP_PHWM[1]	1
Bit 0	R/W	IP_PHWM[0]	0

The PL3IP High Watermark register can be written at any time but is only updated by using the **PL3IP Configuration** register.

IP_PHWM[3:0]

The high water mark sets point at which the EGMAC begins to transmit a PAUSE frame (if enabled). The minimum high watermark is 128 bytes. The watermark will default to the 8192 bytes.

Table 17 PL3IP Channel High Water Mark

IP_PHWM[3:0]	Channel High Water Mark
0000	128 bytes
0001	256 bytes
0010	512 bytes
0011	1024 bytes
0100	2048 bytes
0101	4096 bytes
0110	8192 bytes
0111	16384 bytes
1000	32768 bytes
1001	65500 bytes
1010	4096 bytes
1011	4096 bytes
1100	4096 bytes
1101	4096 bytes
1110	4096 bytes
1111	4096 bytes

Register 0x121H, 0x141H: PL3IP Channel Low Watermark

Bit	Type	Function	Default
Bit 15-4	R	Reserved	0
Bit 3	R/W	IP_PLWM[3]	0
Bit 2	R/W	IP_PLWM[2]	1
Bit 1	R/W	IP_PLWM[1]	0
Bit 0	R/W	IP_PLWM[0]	1

The PL3IP Channel Low Water Mark register can be written at any time but is only updated by using the **PL3IP Configuration** register.

IP_PLWM[3:0]

The low watermark sets the lower limit that must be reached before EGMAC will cease to send PAUSE frames. The minimum low watermark is 64 bytes. The watermark will default to the 2048 bytes.

Table 18 PL3IP Channel Low Water Mark

IP_PLWM[3:0]	Channel Low Water Mark
0000	64 bytes
0001	128 bytes
0010	256 bytes
0011	512 bytes
0100	1024 bytes
0101	2048 bytes
0110	4096 bytes
0111	8192 bytes
1000	16384 bytes
1001	32768 bytes
1010	2048 bytes
1011	2048 bytes
1100	2048 bytes
1101	2048 bytes
1110	2048 bytes
1111	2048 bytes

Register 0x122H, 0x142H: PL3IP Channel Packet Burst Mask

Bit	Type	Function	Default
Bit 15-4	R	Reserved	0
Bit 3	R/W	IP_CFBM[3]	0
Bit 2	R/W	IP_CFBM[2]	0
Bit 1	R/W	IP_CFBM[1]	0
Bit 0	R/W	IP_CFBM[0]	0

The PL3IP Channel Packet Burst Mask register can be written at any time but is only updated upon channel update using the **PL3IP Configuration** register.

IP_CFBM[3:0]

The packet burst mask determines the amount of data transmitted for one channel on the PL3 bus before switching to the other channel. If an end of packet is detected before the burst limit is reached, the burst will terminate asserting REOP on the PL3 bus. Setting IP_CFBM = 08H enables store-and-forward mode. The PM3386 will store the entire packet into the ingress FIFO before transmission. The entire packet will be sent on the PL3 bus prior to re-arbitration between the two channels.

Table 19 Channel Frame Burst Mask

IP_CFBM[3:0]	Channel Frame Burst Mask
0000	16 bytes or EOP
0001	32 bytes or EOP
0010	64 bytes or EOP
0011	128 bytes or EOP
0100	256 bytes or EOP
0101	512 bytes or EOP
0110	1024 bytes or EOP
0111	2048 bytes or EOP
1XXX	Burst till EOP

Register 0x201H: PL3EP Interrupt Status

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	Reserved	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	EP_IS[7]	0
Bit 6	R	Reserved	0
Bit 5	R	EP_IS[5]	0
Bit 4	R	Reserved	0
Bit 3	R	EP_IS[3]	0
Bit 2	R	Reserved	0
Bit 1	R	EP_IS[1]	0
Bit 0	R	Reserved	0

The PL3EP Interrupt Status register is used to capture error status bits from both PL3EP channels. This register is used in conjunction with the **PL3EP Interrupt Mask** register. The register is read only. A read of this register will clear the register. The status register is written in the same clock domain as the TSB and can only be written by the TSB. Reads to this register are asynchronous.

EP_IS[1] – Channel 0 FIFO Truncate

Truncation occurs when the PL3EP de-asserts DPTA, STPA, or PTPA to the Link Layer and data continues to be sent beyond the programmed limitation, filling all locations in the PL3EP FIFO. The PL3EP will truncate the packet by adding an EOP to the packet internally, assert and internal TERR indication, and ignore all data presented externally until the PL3EP FIFO is capable of accepting data.

EP_IS[3] – Channel 0 PL3 TDAT Parity Error

TPRTY reported from the PL3 bus interface is different than the internally generated parity check for this channel.

EP_IS[5] – Channel 1 FIFO Truncate

Truncation occurs when the PL3EP de-asserts DPTA, STPA, or PTPA to the Link Layer and data continues to be sent beyond the programmed limitation, filling all locations in the PL3EP FIFO. The PL3EP will truncate the packet by adding an EOP to the packet internally, assert and internal TERR indication, and ignore all data presented externally until the PL3EP FIFO is capable of accepting data.

EP_IS[7] – Channel 1 PL3 TDAT Parity Error

TPRTY reported from the PL3 bus interface is different than the internally generated parity check for this channel.

Register 0x202H: PL3EP Interrupt Mask

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	Reserved	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R/W	EP_IM[7]	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	EP_IM[5]	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	EP_IM[3]	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	EP_IM[1]	0
Bit 0	R/W	Reserved	0

The PL3EP Interrupt Mask register is used to mask out errors when determining when to send an interrupt. A bit set in any location other than the reserved locations, will enable that type of error to cause an interrupt. This is a programmable register.

EP_IM[1] – Channel 0 FIFO Truncate Mask

Mask bit for error type specified in corresponding bit location in the PL3EP Interrupt Status register.

EP_IM[3] – Channel 0 PL3 TDAT Parity Error Mask

Mask bit for error type specified in corresponding bit location in the PL3EP Interrupt Status register.

EP_IM[5] – Channel 1 FIFO Truncate Mask

Mask bit for error type specified in corresponding bit location in the PL3EP Interrupt Status register.

EP_IM[7] – Channel 1 PL3 TDAT Parity Error Mask

Mask bit for error type specified in corresponding bit location in the PL3EP Interrupt Status register.

Register 0x203H: PL3EP Configuration Register

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	Reserved	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	Reserved	0
Bit 4	R	Reserved	0
Bit 3	R/W	EP_CR[3]	1
Bit 2	R/W	EP_CR[2]	1
Bit 1	R/W	EP_CR[1]	0
Bit 0	R/W	EP_CR[0]	0

The PL3EP Configuration Register controls the enabling and disabling of features for the TSB. Writing a 1 to a non-reserved bit location will cause the feature to be enabled.

EP_CR[0] Parity Checking Enable on TDAT[31:0]

This feature will enable the checking of parity on the data from the PL3 TDAT[31:0] bus. High is on. Low is off.

EP_CR[1] – Odd or even parity generation and check mode

Parity Check mode is use to determine whether odd or even mode parity check is used across the egress PL3 bus. The default mode is 0 for odd parity. Parity mode applies to both channels.

EP_CR[2] – Channel 0 Update

Channel 0 Update is used to update configuration values into the PL3EP when required due to configuration change. The differing PL3EP configuration registers (0x220, 0x221) may be written to at any time but will only update when this bit is cleared. The user programs the PL3EP configuration registers and then writes a zero to this bit to update the registers within the channel. This bit will automatically return to one when the update is complete.

EP_CR[3] – Channel 1 Update

Channel 1 Update is used to update configuration values into the PL3EP when required due to configuration change. The differing PL3EP configuration registers (0x240, 0x241) may be written to at any time but will only update when this bit is cleared. The user programs the PL3EP configuration registers and then writes a zero to this bit to update the registers within the channel. This bit will automatically return to one when the update is complete.

Register 0x220H, 0x240H: PL3EP Channel FIFO Reserve

Bit	Type	Function	Default
Bit 15-3	R	Reserved	0
Bit 2	R/W	EP_CTR[2]	1
Bit 1	R/W	EP_CTR[1]	0
Bit 0	R/W	EP_CTR[0]	1

The PL3EP Channel FIFO Reserve register is user programmable to establish the amount of reserved FIFO space left once DPTA, STPA, or PTPA have been de-asserted. The default is 2k bytes. This register can be written to at any time but the internal logic will only be updated by a write to the update bits within the PL3EP configuration register.

EP_CTR[2:0]

Table 20 PM3386 FIFO Reserve Programming Options

EP_CTR[2:0]	Reserve Space in bytes
000	64 bytes
001	128 bytes
010	256 bytes
011	512 bytes
100	1024 bytes
101	2048 bytes (default)
110	4096 bytes
111	8192 bytes

Register 0x221H, 0x241H: PL3EP Channel Minimum Frame Size

Bit	Type	Function	Default
Bit 15-3	R	Reserved	0
Bit 2	R/W	EP_CMF[2]	0
Bit 1	R/W	EP_CMF[1]	0
Bit 0	R/W	EP_CMF[0]	0

The Channel Minimum Frame Size register determines the amount of data to gather prior to transmitting the data on the line side via the EGMAC. The logic will compare the frame size to the frame counter and look at the EOP count before pushing data out of the FIFO. If EOP is hit before the minimum frame size is met, the PL3EP will send the completed frame. The default setting is 64 bytes of data. This register can be written to at any time but the internal logic will only be updated by a write to the update bits within the **PL3EP Configuration** register.

EP_CMF[2:0]

Table 21 PM3386 Minimum Frame Size Programming Options

EP_CMF[2:0]	Minimum Frame Size in bytes
000	64 bytes (default)
001	128 bytes
010	256 bytes
011	512 bytes
100	1024 bytes
101	2048 bytes
110	4096 bytes
111	12288 bytes

Register 0x300H,0x400H: EGMAC - GMACC0 – Config Register Low Word

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	Reserved	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R/W	L10B	0
Bit 8	R/W	L32B	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	Reserved	0
Bit 4	R	Reserved	0
Bit 3	R	Reserved	0
Bit 2	R	Reserved	0
Bit 1	R	Reserved	0
Bit 0	R/W	MIIM	PMD_SEL

MIIM:

MII Mode select. On reset MIIM takes the value of the PMD_SELx pin. A value of logic 1 selects the GMII interface for this channel. A logic value of 0 selects the SERDES/TBI interface for this channel.

L32B:

Setting this bit will cause the 32-bit transmit packet data to be looped back to the receive logic in the EGMAC. Clearing this bit results in normal operation, both transmit and receive.

L10B:

Setting this bit will cause the 10-bit encoded transmit data to be looped back to the receive logic in the EGMAC. Clearing this bit results in normal operation, both transmit and receive.

Please note that after updating this register a software reset of the state logic is required using the SRST bit in EGMAC GMACC0 – Config Register High Word Register

Register 0x301H,0x401H: EGMAC - GMACC0 – Config Register High Word

Bit	Type	Function	Default
Bit 15	R/W	SRST	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	Reserved	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	Reserved	0
Bit 4	R	Reserved	0
Bit 3	R	Reserved	0
Bit 2	R	Reserved	0
Bit 1	R	Reserved	0
Bit 0	R	Reserved	0

SRST:

Soft Reset. Setting this bit will reset the internal state of the EGMAC block and load register settings from registers 0x300-0x305 or 0x400-0x405. Note: Registers 0x300-0x305 or 0x400-0x405 will retain their written value. This bit should be set whenever changes are made to the register bits found in register 0x300-0x305 or 0x400-0x405 except for the TXEN0 and RXEN0 bits. To reset / update state first write a 1 to SRST and then write a 0.
Note that the address filter registers 0x339-0x35F or 0x439-0x45F are reset by the use of the SRST bit. The pre-update registers within the PM3386 will always contain the last loaded address filter information so it is possible to write to register 0x360 or 0x460 Update bit to restore the PM3386 address filtering registers to pre-software reset condition.

Register 0x302H,0x402H: EGMAC - GMACC1 – Config Register Low Word

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R/W	LONGP	0
Bit 11	R	Reserved	0
Bit 10	R/W	FCRX	0
Bit 9	R/W	FCTX	0
Bit 8	R/W	PUREP	1
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R/W	FLCHK	0
Bit 4	R/W	CRCEN	0
Bit 3	R	Reserved	0
Bit 2	R	Reserved	0
Bit 1	R/W	PADEN	1
Bit 0	R	FULLD	1

FULLD:

Full-Duplex. This bit is always set to 1 to indicate that the MAC is always in Full-Duplex mode.

PADEN:

Pad Enable. Pad frames including VID field with 0's to 60 bytes (if necessary) and append CRC thereby ensuring minimum frame size of 64 bytes.

CRCEN:

CRC Enable. Set this bit to have the MAC append a CRC on each and every frame it transmits. Clear this bit when frames from the system already have a valid CRC. Note: Frames are always checked for a valid CRC.

FLCHK:

Frame Length Check. Set this bit to allow the MAC to check the length of received frames. The MAC will then check all frames whose length/type field represents a valid length (46-1500 octets) comparing the value in the length/type field to the actual LLC data field length.

PUREP:

Pure Preamble. Set this bit to cause the EGMAC to check the content of the preamble field of the packet, ensuring a data pattern of 0x55. Clear this bit if no preamble checking is desired. The length of the preamble is not checked in either case.

FCTX:

Flow Control: Transmit Capable. Setting this bit allows the MAC Control sub-layer to transmit PAUSE Control frames. Clearing this bit prevents the transmission of internally generated PAUSE frames. Please note that it is illegal to enable the FCTX bit without enabling the PADEN bit. However it is legal to enable the PADEN bit without enabling the FCTX bit.

FCRX:

Flow Control: Receive Capable. Setting this bit allows the MAC Control sub-layer to respond to PAUSE Control frames by pausing the transmitter from transmitting data frames. Transmit pause control frames are still allowed to be transmitted if they are triggered by internal FIFO fill levels or via the PAUSE pin. Clearing this bit prevents any action based on the reception of PAUSE frames. Note that the PM3386 PAUSE counter will always reflect the PAUSE quanta as updated by incoming PAUSE frames. The PM3386 will only act upon (by ceasing transmit traffic) the non zero PAUSE counter if FCRX is high. The PAUSED0 or PAUSED1 will always reflect the status of the corresponding channels PAUSE counter.

LONGP:

Accept Preambles Over 12 Bytes. If LONGP is disabled, packets with preambles > 12 bytes will be dropped.

Please note that after updating this register a software reset of the state logic is required using the SRST bit in EGMAC GMACC0 – Config Register High Word Register

Register 0x303H,0x403H: EGMAC - GMACC1 – Config Register High Word

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R/W	TXEN0	0
Bit 13	R	Reserved	0
Bit 12	R/W	RXEN0	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	Reserved	0
Bit 4	R	Reserved	0
Bit 3	R	Reserved	0
Bit 2	R	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

RXEN0:

Receive Enable. Enables device receive operations. When set low (reset default) the receive or ingress direction of the device will cease to transfer data. Traffic will be dropped at the EGMAC interface until the assertion of RXEN0. When set high the PM3386 will allow frame data to be transferred.

TXEN0:

Transmit Enable. Enables possible transmit operations. Upon device reset this bit will be set low. This will disable all transmit or egress traffic flow for this port. To enable possible egress traffic flow this bit must be set to one. This bit should not be used by the programmer to halt transmit data flow as the TPAUSE bit within the **EGMAC Transmit Control** register is responsible for this function. Please see enabling and disabling data flows in the Operation section for more in formation.

Register 0x304H,0x404H: EGMAC - GMACC2 – Config Register Low Word

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	Reserved	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R/W	IPGT[5]	0
Bit 4	R/W	IPGT[4]	0
Bit 3	R/W	IPGT[3]	1
Bit 2	R/W	IPGT[2]	1
Bit 1	R/W	IPGT[1]	0
Bit 0	R/W	IPGT[0]	0

IPGT[5:0]:

Back-to-Back Transmit IPG. This is a programmable field representing the IPG between back-to-back packets. Set this field to the number of octets of IPG desired. A setting of 12 decimal represents the minimum IPG of 0.096μs.

Table 22 InterPacket Gap Encoding

IPGT[5:0]	IPG in ns	IPGT[5:0]	IPG in ns
00h	reserved	20h	256ns
01h	reserved	21h	264ns
02h	reserved	22h	272ns
03h	reserved	23h	280ns
04h	reserved	24h	288ns
05h	reserved	25h	296ns
06h	reserved	26h	304ns
07h	reserved	27h	312ns
08h	reserved	28h	320ns
09h	reserved	29h	328ns
0ah	reserved	2ah	336ns
0bh	reserved	2bh	344ns
0ch(default)	96ns	2ch	352ns
0dh	104ns	2dh	360ns
0eh	112ns	2eh	368ns
0fh	120ns	2fh	376ns
10h	128ns	30h	384ns
11h	136ns	31h	392ns
12h	144ns	32h	400ns
13h	152ns	33h	408ns
14h	160ns	34h	416ns
15h	168ns	35h	424ns
16h	176ns	36h	432ns
17h	184ns	37h	440ns
18h	192ns	38h	448ns
19h	200ns	39h	456ns
1ah	208ns	3ah	464ns
1bh	216ns	3bh	472ns
1ch	224ns	3ch	480ns
1dh	232ns	3dh	488ns
1eh	240ns	3eh	496ns
1fh	248ns	3fh	504ns

Please note that after updating this register a software reset of the state logic is required using the SRST bit in EGMAC GMACC0 – Config Register High Word Register

Register 0x305H,0x405H: EGMAC - GMACC2 – Config Register High Word

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	Reserved	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	Reserved	0
Bit 4	R/W	SPRE	0
Bit 3	R	Reserved	0
Bit 2	R	Reserved	0
Bit 1	R	Reserved	0
Bit 0	R	Reserved	0

SPRE

Suppress Preamble bit. This bit if set to 1 will suppress the MII Management preamble on the MDIO pin.

Please note that after updating this register a software reset of the state logic is required using the SRST bit in EGMAC GMACC0 – Config Register High Word Register

Register 0x306H,0x406H: EGMAC - GPCSC – PHY Config Low Word

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R/W	AUTOS	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	Reserved	0
Bit 4	R	Reserved	0
Bit 3	R	Reserved	0
Bit 2	R	Reserved	0
Bit 1	R	Reserved	0
Bit 0	R	Reserved	0

AUTOS:

Auto Sense Auto-Neg Status. When asserted this bit will cause the MAC to auto sense if Link Partner is in Link Bypass mode or in Auto-negotiation mode.

Register 0x307H,0x407H: EGMAC - GPCSC – PHY Config High Word

Bit	Type	Function	Default
Bit 15	R/W	JTRDE	0
Bit 14	R/W	JTRPS[2]	0
Bit 13	R/W	JTRPS[1]	0
Bit 12	R/W	JTRPS[0]	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R/W	JTRPT[9]	0
Bit 8	R/W	JTRPT[8]	0
Bit 7	R/W	JTRPT[7]	0
Bit 6	R/W	JTRPT[6]	0
Bit 5	R/W	JTRPT[5]	0
Bit 4	R/W	JTRPT[4]	0
Bit 3	R/W	JTRPT[3]	0
Bit 2	R/W	JTRPT[2]	0
Bit 1	R/W	JTRPT[1]	0
Bit 0	R/W	JTRPT[0]	0

JTRPT[9:0]:

Custom Jitter Pattern. Used in conjunction with JITTERN PATTERN SELECT and JITTER DIAGNOSTIC ENABLE, set this field to the desired custom pattern which will be continuously transmitted.

Table 23 Jitter Pattern Table

JTRPS[2:0]	40 bit Data Transmitted to SERDES	Comments
000b	1111100000111111000001111110000011111100000…	Low Freq.
001b	1111101011000001010011111010110000010100…	Mixed Freq.
010b	1010101010101010101010101010101010101010…	High Freq.
011b	See *Custom Jitter Pattern*, bits [25:16]	User Def'd.
1XXb	Reserved	Reserved

JTRPS[2:0]:

Jitter Pattern Select. Selects the jitter pattern to be transmitted in diagnostics mode. See Jitter Table above.

JTRDE:

Jitter Diagnostic Enable. Set this bit to enable the GMAC to transmit the jitter test patterns defined in IEEE 802.3z 36A. Clear this bit to enable normal transmit operation.

Register 0x308H,0x408H: EGMAC - SA – Station Address [15:0]

Bit	Type	Function	Default
Bit 15	R/W	SA[15]	0
Bit 14	R/W	SA [14]	0
Bit 13	R/W	SA [13]	0
Bit 12	R/W	SA [12]	0
Bit 11	R/W	SA [11]	0
Bit 10	R/W	SA [10]	0
Bit 9	R/W	SA [9]	0
Bit 8	R/W	SA [8]	0
Bit 7	R/W	SA [7]	0
Bit 6	R/W	SA [6]	0
Bit 5	R/W	SA [5]	0
Bit 4	R/W	SA [4]	0
Bit 3	R/W	SA [3]	0
Bit 2	R/W	SA [2]	0
Bit 1	R/W	SA [1]	0
Bit 0	R/W	SA [0]	0

SA[15:0]:

Station Address Low word.

Please note that a station address (SA) of SA[47:0] = 0x1234_5678_9ABC would be seen on the wire and by the MAC with the least significant bit of the least significant byte of SA[7:0] being first. In this case the MAC will receive and transmit data with the above example SA as BC_9A_78_56_34_12. Please refer to Table 32 and Table 33 in this document and IEEE 802.3-1998 Section 3.2.3 for reference.

Register 0x309H,0x409H: EGMAC - SA – Station Address [31:16]

Bit	Type	Function	Default
Bit 15	R/W	SA[31]	0
Bit 14	R/W	SA [30]	0
Bit 13	R/W	SA [29]	0
Bit 12	R/W	SA [28]	0
Bit 11	R/W	SA [27]	0
Bit 10	R/W	SA [26]	0
Bit 9	R/W	SA [25]	0
Bit 8	R/W	SA [24]	0
Bit 7	R/W	SA [23]	0
Bit 6	R/W	SA [22]	0
Bit 5	R/W	SA [21]	0
Bit 4	R/W	SA [20]	0
Bit 3	R/W	SA [19]	0
Bit 2	R/W	SA [18]	0
Bit 1	R/W	SA [17]	0
Bit 0	R/W	SA [16]	0

SA[31:16]:

Station Address Mid word.

Register 0x30aH,0x40aH: EGMAC - SA – Station Address [47:32]

Bit	Type	Function	Default
Bit 15	R/W	SA[47]	0
Bit 14	R/W	SA [46]	0
Bit 13	R/W	SA [45]	0
Bit 12	R/W	SA [44]	0
Bit 11	R/W	SA [43]	0
Bit 10	R/W	SA [42]	0
Bit 9	R/W	SA [41]	0
Bit 8	R/W	SA [40]	0
Bit 7	R/W	SA [39]	0
Bit 6	R/W	SA [38]	0
Bit 5	R/W	SA [37]	0
Bit 4	R/W	SA [36]	0
Bit 3	R/W	SA [35]	0
Bit 2	R/W	SA [34]	0
Bit 1	R/W	SA [33]	0
Bit 0	R/W	SA [32]	0

SA[47:32]:

Station Address High word.

Register 0x30CH,0x40CH: EGMAC - TPID – VLAN Tag ID

Bit	Type	Function	Default
Bit 15	R/W	TPID[15]	1
Bit 14	R/W	TPID[14]	0
Bit 13	R/W	TPID[13]	0
Bit 12	R/W	TPID[12]	0
Bit 11	R/W	TPID[11]	0
Bit 10	R/W	TPID[10]	0
Bit 9	R/W	TPID[9]	0
Bit 8	R/W	TPID[8]	1
Bit 7	R/W	TPID[7]	0
Bit 6	R/W	TPID[6]	0
Bit 5	R/W	TPID[5]	0
Bit 4	R/W	TPID[4]	0
Bit 3	R/W	TPID[3]	0
Bit 2	R/W	TPID[2]	0
Bit 1	R/W	TPID[1]	0
Bit 0	R/W	TPID[0]	0

TPID[15:0]:

Tag Protocol Identifier. Program this field with the 16-bit VLAN TPID. The MAC will detect VLAN tagged frames by comparing the two bytes following the Source Address with this field. The VLAN TPID defined by 802.1Q is 0x8100.

Register 0x310H,0x410H: EGMAC - RX_MAXFR – Receive Max Frame Length

Bit	Type	Function	Default
Bit 15	R/W	RX_MAXFR[15]	0
Bit 14	R/W	RX_MAXFR[14]	0
Bit 13	R/W	RX_MAXFR[13]	0
Bit 12	R/W	RX_MAXFR[12]	0
Bit 11	R/W	RX_MAXFR[11]	0
Bit 10	R/W	RX_MAXFR[10]	1
Bit 9	R/W	RX_MAXFR[9]	0
Bit 8	R/W	RX_MAXFR[8]	1
Bit 7	R/W	RX_MAXFR[7]	1
Bit 6	R/W	RX_MAXFR[6]	1
Bit 5	R/W	RX_MAXFR[5]	1
Bit 4	R/W	RX_MAXFR[4]	0
Bit 3	R/W	RX_MAXFR[3]	1
Bit 2	R/W	RX_MAXFR[2]	1
Bit 1	R/W	RX_MAXFR[1]	1
Bit 0	R/W	RX_MAXFR[0]	0

RX_MAXFR[15:0]:

This field defaults to 0x05EE, which represents a maximum receive frame of 1518 octets. An untagged maximum size Ethernet frame is 1518 octets in length. A tagged frame adds four octets for a total of 1522 octets. The frame will be truncated to match the specified length. Note: This field only affects the reception of frames. Also note the addition of 4 bytes for a VLAN tagged frame.

Table 24 Max frame size conditions

Register Setting	Received Size	CRC indication	VLAN Tagged	Result
1518	1518	Good	N/A	Good frame
1518	1518	Bad	N/A	CRC erred frame
1518	1519	Good	No	Length erred frame
1518	1519	Bad	No	Jabber erred frame
1518	1519	Good	Yes	Good frame
1518	1519	Bad	Yes	CRC erred frame
1518	1522	Good	Yes	Good frame
1518	1522	Bad	Yes	CRC erred frame
1518	1523	Good	Yes	Length erred frame
1518	1523	Bad	Yes	Jabber erred frame

Register 0x318H,0x418H: EGMAC - ANCTL – Auto-Negotiation Control

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	Reserved	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	Reserved	0
Bit 4	R	Reserved	0
Bit 3	R	Reserved	0
Bit 2	R	Reserved	0
Bit 1	R/W	ANEN	0
Bit 0	R/W	RSTAN	0

RSTAN:

Restart Auto-Negotiation. Setting this bit to a 1 then to a 0 will restart the Auto-Negotiation Process..

ANEN:

Auto-Negotiation Enable. Setting this bit enables Auto-Negotiation Process. Clearing it will prevent auto negotiation and puts the EGMAC in LINK BYPASS mode.

Register 0x31AH,0x41AH: EGMAC - ANSTT – Auto-Negotiation Status

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	Reserved	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	Reserved	0
Bit 4	R	RFIND	0
Bit 3	R	ANCPLT	0
Bit 2	R	PGRX	0
Bit 1	R	LINKOK	0
Bit 0	R	SYNCOK	0

SYNCOK:

Synchronization Status. Asserted after receiving three valid Idle ordered sets signaling comma detect lock achieved.

LINKOK:

Link OK. This can be asserted by two different means.
1. The SYNCOK bit is asserted (I.E. comma detect achieved) and the ANEN bit in the **Auto Negotiation Status** register is 1 and auto-negotiation is complete.
2. The SYNCOK bit is asserted (I.E> comma detect achieved) and the ANEN bit in the **Auto Negotiation Status** register is 0. (Auto-negotiation status is ignored).
Please note that the LINKOK bit is implemented with a latch implementation. To get the current status the LINKOK must be read once for past status and twice to get current status.

PGRX:

Page Received. MII Mgmt register 6 bit [1]. When ‘1’ – a new page has been received. When ‘0’ – a new page has not been received. This bit is cleared upon reading this register.

ANCPLT:

Auto-Negotiation Complete. Auto-Negotiation has completed.

RFIND:

Remote Fault indicator

Register 0x31CH,0x41CH: EGMAC - ANADV – Auto-Negotiation Advert Low Word

Bit	Type	Function	Default
MII Mgmt Register 4: Base Page			
Bit 15	R/W	NEXTP	0
Bit 14	R	Reserved	0
Bit 13	R/W	ANERR[1]	0
Bit 12	R/W	ANERR[0]	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R/W	ASMDR/PAUSE[1]	1
Bit 7	R/W	ASMDR/PAUSE[0]	1
Bit 6	R	Reserved	0
Bit 5	R/W	FD	1
Bit 4	R	Reserved	0
Bit 3	R	Reserved	0
Bit 2	R	Reserved	0
Bit 1	R	Reserved	0
Bit 0	R	Reserved	0

FD:

Full-Duplex. Setting this bit means local device is capable of full-duplex operation. This bit should be set to a ‘1’ for normal operation.

ASMDR/PAUSE[1:0]:

Local PAUSE Capabilities. The local device’s PAUSE capability is encoded in bits 8:7, and the decodes are shown in Pause Encoding Table below. For priority resolution between link partner and local pause capabilities, consult Pause Priority Resolution Table.

Table 25 Pause Encoding Table

[7]	[8]	Capability
0	0	No PAUSE
0	1	Asymmetric PAUSE toward link partner
1	0	Symmetric PAUSE
1	1	Both Symmetric PAUSE and Asymmetric PAUSE toward local device

ANERR[1:0]:

Auto-Neg Error. The local device's remote fault condition may be encoded in bits 13:12 of the base page. Values are shown in Remote Fault Encoding Table 26 shown below. The default value is 0b00. Local device may indicate a fault by setting a non-zero Remote Fault encoding and re-negotiating.

Table 26 Remote Fault Encoding Table

[12]	[13]	Description
0	0	No error, link OK
0	1	Offline
1	0	Link_Failure
1	1	Auto-Negotiation_Error

NEXTP:

Next Page Capable. The local device asserts this bit to request next page transmission. Clear this bit when local device has no subsequent next pages.

Register 0x31DH,0x41DH: EGMAC - ANADV – Auto-Negotiation Advert High Word

Bit	Type	Function	Default
MII Mgmt Register 7: Local Next Page			
Bit 15	R/W	ANNP	0
Bit 14	R	Reserved	0
Bit 13	R/W	ANMSG	0
Bit 12	R/W	ANACK2	0
Bit 11	R/W	ANTOG	0
Bit 10	R/W	NPLPCF[10]	0
Bit 9	R/W	NPLPCF[9]	0
Bit 8	R/W	NPLPCF[8]	0
Bit 7	R/W	NPLPCF[7]	0
Bit 6	R/W	NPLPCF[6]	0
Bit 5	R/W	NPLPCF[5]	0
Bit 4	R/W	NPLPCF[4]	0
Bit 3	R/W	NPLPCF[3]	0
Bit 2	R/W	NPLPCF[2]	0
Bit 1	R/W	NPLPCF[1]	0
Bit 0	R/W	NPLPCF[0]	0

NPLPCF[10:0]:

Next Page Local Code Field. This field contains the data that is sent in the next page. Message pages are formatted pages that carry a predefined Message Code, which is enumerated in IEE 802.3u/Annex 28C. Unformatted Code Fields take on an arbitrary value.

ANTOG:

Link Partner Toggle. Used to ensure synchronization with the Link Partner during Next Page exchange. This bit always takes opposite value of the Toggle bit of the previously exchanged Link Code Word. The initial value in the first Next Page transmitted is the inverse of bit 11 in the base Link Code Word.

ANACK2:

Auto-Neg Acknowledge 2. Used by next page function to indicate device has ability to comply with the message. Assert bit if local device will comply with message. Clear bit if local device cannot comply with message.

ANMSG:

Auto-Neg Message Page. Assert bit to indicate Message Page. Clear bit to indicate Unformatted Page.

ANNP:

Auto-Neg Next Page. Assert this bit to indicate additional next pages to follow. Bit is cleared to indicate last page.

Register 0x31EH,0x41EH: EGMAC - ANLPA – Auto-Negotiation Link Part Able Low Word

Bit	Type	Function	Default
MII Mgmt Register 5			
Bit 15	R	LPNEXTP	0
Bit 14	R	ACKNOWLEDGE	0
Bit 13	R	LPANERR[1]	0
Bit 12	R	LPANERR[0]	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	LPASMDR/ LPPAUSE[1]	0
Bit 7	R	LPASMDR/ LPPAUSE[0]	0
Bit 6	R	Reserved	0
Bit 5	R	LPFD	0
Bit 4	R	Reserved	0
Bit 3	R	Reserved	0
Bit 2	R	Reserved	0
Bit 1	R	Reserved	0
Bit 0	R	Reserved	0

LPFD:

LP Full-Duplex. When ‘1’ – link partner is capable of Full-Duplex operation. When ‘0’ – link partner is incapable of Full-Duplex mode.

LPASMDR/LPPAUSE[1:0]:

LP Asymmetric Direction / LP Pause. Encoding of the link partner’s PAUSE capability is shown in Pause Encoding Table. For priority resolution between link partner and local pause capabilities consult Pause Priority Resolution Table.

LPANERR[1:0]:

LP Remote Fault. The link partner’s remote fault condition is encoded in bits 13:12 of the base page. Values are shown in Remote Fault Encoding Table.

ACKNOWLEDGE:

The ACKNOWLEDGE bit in the Link Partner’s base page indicates that a device has successfully received its link partner’s base page.

LPNEXTP:

LP Next Page Capable. The link partner asserts this bit to indicate ability to accept next pages.

Table 27 PAUSE Priority Resolution Table

Local Device		Link Partner		Local Resolution	Link Partner Resolution
PAUSE	**ASM_DIR**	**PAUSE**	**ASM_DIR**		
0	0	X	X	Disable PAUSE TX Disable PAUSE RX	Disable PAUSE TX Disable PAUSE RX
0	1	0	X	Disable PAUSE TX Disable PAUSE RX	Disable PAUSE TX Disable PAUSE RX
0	1	1	0	Disable PAUSE TX Disable PAUSE RX	Disable PAUSE TX Disable PAUSE RX
0	1	1	1	**Enable PAUSE TX** Disable PAUSE RX	Disable PAUSE TX **Enable PAUSE RX**
1	0	0	X	Disable PAUSE TX Disable PAUSE RX	Disable PAUSE TX Disable PAUSE RX
1	0	1	X	**Enable PAUSE TX** **Enable PAUSE RX**	**Enable PAUSE TX** **Enable PAUSE RX**
1	1	0	0	Disable PAUSE TX Disable PAUSE RX	Disable PAUSE TX Disable PAUSE RX
1	1	0	1	Disable PAUSE TX **Enable PAUSE RX**	**Enable PAUSE TX** Disable PAUSE RX
1	1	1	X	**Enable PAUSE TX** **Enable PAUSE RX**	**Enable PAUSE TX** **Enable PAUSE RX**

Register 0x31FH,0x41FH: EGMAC - ANLPA – Auto-Negotiation Link Part Able High Word

Bit	Type	Function	Default
MII Mgmt Register 8			
Bit 15	R	LPNP	0
Bit 14	R	ACKNOWLEDGE	0
Bit 13	R	LPMSG	0
Bit 12	R	LPACK2	0
Bit 11	R	LPTOG	0
Bit 10	R	LPCF[10]	0
Bit 9	R	LPCF[9]	0
Bit 8	R	LPCF[8]	0
Bit 7	R	LPCF[7]	0
Bit 6	R	LPCF[6]	0
Bit 5	R	LPCF[5]	0
Bit 4	R	LPCF[4]	0
Bit 3	R	LPCF[3]	0
Bit 2	R	LPCF[2]	0
Bit 1	R	LPCF[1]	0
Bit 0	R	LPCF[0]	0

LPCF[10:0]:

LP Code Field. Message Pages are formatted pages that carry a predefined Message Code, which is enumerated in IEEE 802.3u/Annex 28C.

LPTOG:

LP Toggle. Used to ensure synchronization with the Link Partner during Next Page exchange. This bit always takes opposite value of the Toggle bit of the previously exchanged Link Code Word. The initial value in the first Next Page transmitted is the inverse of bit 11 in the base Link Code Word.

LPACK2:

LP Acknowledge 2. Indicates link partner’s ability to comply with the message. When ‘1’ – link partner will comply with message. When ‘0’ – link partner cannot comply with message.

LPMSG:

LP Message Page. When ‘1’ – indicates Message Page. When ‘0’ – indicates Unformatted Page.

ACKNOWLEDGE:

The ACKNOWLEDGE bit in the Link Partner's next page register is used to indicate that the device has successfully received its link partner's next page.

LPNP:

LP Next Page. The link partner asserts this bit to request next page transmission. When '0' – link partner has no subsequent next pages.

Register 0x320H: EGMAC - MCMD – MII Management Command

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	Reserved	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	Reserved	0
Bit 4	R	Reserved	0
Bit 3	R	Reserved	0
Bit 2	R	Reserved	0
Bit 1	R	Reserved	0
Bit 0	R/W	RSTAT	0

RSTAT:

MII Management Read Status. Writting this bit to a 1 causes a read operation on the register addressed by EGMAC MADR: MII Management PHY Address. Upon completion of the MII read as outlined within the Operations section MII Read Access instructions the RSTAT bit must be cleared to 0.

Register 0x322H: EGMAC - MADR – MII Management PHY Address

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R/W	FIAD[4]	0
Bit 11	R/W	FIAD[3]	0
Bit 10	R/W	FIAD[2]	0
Bit 9	R/W	FIAD[1]	0
Bit 8	R/W	FIAD[0]	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	Reserved	0
Bit 4	R/W	RGAD[4]	0
Bit 3	R/W	RGAD[3]	0
Bit 2	R/W	RGAD[2]	0
Bit 1	R/W	RGAD[1]	0
Bit 0	R/W	RGAD[0]	0

RGAD[4:0]:

PHY Register Address. 5-bit address accessing a particular register in the above addressed PHY.

FIAD[4:0]:

PHY Address. 5-bit unit selection address indexing external PHY.

Register 0x324H: EGMAC - MWTD – MII Management Write Data

Bit	Type	Function	Default
Bit 15	R/W	CTLD[15]	0
Bit 14	R/W	CTLD[14]	0
Bit 13	R/W	CTLD[13]	0
Bit 12	R/W	CTLD[12]	0
Bit 11	R/W	CTLD[11]	0
Bit 10	R/W	CTLD[10]	0
Bit 9	R/W	CTLD[9]	0
Bit 8	R/W	CTLD[8]	0
Bit 7	R/W	CTLD[7]	0
Bit 6	R/W	CTLD[6]	0
Bit 5	R/W	CTLD[5]	0
Bit 4	R/W	CTLD[4]	0
Bit 3	R/W	CTLD[3]	0
Bit 2	R/W	CTLD[2]	0
Bit 1	R/W	CTLD[1]	0
Bit 0	R/W	CTLD[0]	0

CTLD[15:0]:

Control Data. The 16-bit write data for management writes to above address found in the EGMAC- MADR: MII Management PHY register.

Register 0x326H: EGMAC - MRDD – MII Management Read Data

Bit	Type	Function	Default
Bit 15	R	PRSD[15]	0
Bit 14	R	PRSD [14]	0
Bit 13	R	PRSD [13]	0
Bit 12	R	PRSD [12]	0
Bit 11	R	PRSD [11]	0
Bit 10	R	PRSD [10]	0
Bit 9	R	PRSD [9]	0
Bit 8	R	PRSD [8]	0
Bit 7	R	PRSD [7]	0
Bit 6	R	PRSD [6]	0
Bit 5	R	PRSD [5]	0
Bit 4	R	PRSD [4]	0
Bit 3	R	PRSD [3]	0
Bit 2	R	PRSD [2]	0
Bit 1	R	PRSD [1]	0
Bit 0	R	PRSD [0]	0

PRSD[15:0]:

Read Status Data. The 16-bit results from the read operation of register addressed using the EGMAC – MADR: MII Management PHY register.

Register 0x328H: EGMAC - MIND – MII Management Indicators

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	Reserved	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	Reserved	0
Bit 4	R	Reserved	0
Bit 3	R	Reserved	0
Bit 2	R	Reserved	0
Bit 1	R	Reserved	0
Bit 0	R	MBSY	0

MBSY:

MIIM Busy. Management operation in progress. MBSY goes active when a register is written to, or read from or during a SCAN operation and stays active until the end of the respective operation. The read status data is only valid when MBSY is inactive.

Register 0x332H,0x432H: EGMAC – Transmit Control

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	Reserved	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	Reserved	0
Bit 4	R	Reserved	0
Bit 3	R	Reserved	0
Bit 2	R	Reserved	0
Bit 1	R/W	TPAUSE	0
Bit 0	R/W	SPQCT	0

SPQCT:

Shortcut Pause Quanta Counter. When asserted this bit causes the Pause Quanta time to be changed form 512 byte times to 1 bit time. This bit is for testing purposes only and should be cleared for normal operation.

TPAUSE:

The TPAUSE bit directs the EGMAC to gracefully halt transmit traffic. When set the EGMAC will halt transmit traffic. When cleared the EGMAC will resume egress data transfer. When halted the egress traffic will accumulate in the PM3386 egress FIFO and upon de-assertion of the TPAUSE bit the data will resume transmission.

Register 0x333H,0x433H: EGMAC - CONTROL – EGMAC Control Register

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	Reserved	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R:W	Reserved	0
Bit 4	R/W	PASS_CTRL	0
Bit 3	R/W	PASS_ERRORS	0
Bit 2	R/W	HOSTPAUSE	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

HOSTPAUSE:

HOST PAUSE enable bit. When set to a 1 the EGMAC will send PAUSE Control Frames based on the PAUSE timer and PAUSE interval registers. Setting the bit to a 0 will cause the EGMAC to no longer send PAUSE Control Frames and if currently in a PAUSE state will send a PAUSE control frame with a pause timer value set to zero.

PASS_ERRORS:

PASS_ERRORS enable bit. When set to a 1 the EGMAC will forward all erred frames to the system FIFO interface. Setting the bit to a 0 will cause the EGMAC to filter all erred frames.

PASS_CTRL:

PASS_CTRL enable bit. When set to a 1 the EGMAC will forward all received control frames to the system FIFO interface. Setting the bit to a 0 the EGMAC will filter all control frames.

Register 0x334H,0x434H: EGMAC - PAUSE_TIME – PAUSE Timer Register

Bit	Type	Function	Default
Bit 15	R/W	PAUSE_TIME[15]	1
Bit 14	R/W	PAUSE_TIME[14]	1
Bit 13	R/W	PAUSE_TIME[13]	1
Bit 12	R/W	PAUSE_TIME[12]	1
Bit 11	R/W	PAUSE_TIME[11]	1
Bit 10	R/W	PAUSE_TIME[10]	1
Bit 9	R/W	PAUSE_TIME[9]	1
Bit 8	R/W	PAUSE_TIME[8]	1
Bit 7	R/W	PAUSE_TIME[7]	1
Bit 6	R/W	PAUSE_TIME[6]	1
Bit 5	R/W	PAUSE_TIME[5]	1
Bit 4	R/W	PAUSE_TIME[4]	1
Bit 3	R/W	PAUSE_TIME[3]	1
Bit 2	R/W	PAUSE_TIME[2]	1
Bit 1	R/W	PAUSE_TIME[1]	1
Bit 0	R/W	PAUSE_TIME[0]	1

PAUSE_TIME[15:0]:

Pause Timer value that is used on the PAUSE Control Frames that are sent to the downstream PHY. The default is 0xFFFF for a XON/XOFF type of protocol.

Register 0x335H,0x435H: EGMAC - PAUSE_IVAL – PAUSE Timer Interval Register

Bit	Type	Function	Default
Bit 15	R/W	PAUSE_IVAL[15]	0
Bit 14	R/W	PAUSE_ IVAL[14]	1
Bit 13	R/W	PAUSE_IVAL[13]	1
Bit 12	R/W	PAUSE_IVAL[12]	1
Bit 11	R/W	PAUSE_IVAL[11]	1
Bit 10	R/W	PAUSE_IVAL[10]	1
Bit 9	R/W	PAUSE_IVAL[9]	1
Bit 8	R/W	PAUSE_IVAL[8]	1
Bit 7	R/W	PAUSE_IVAL[7]	0
Bit 6	R/W	PAUSE_IVAL[6]	1
Bit 5	R/W	PAUSE_IVAL[5]	1
Bit 4	R/W	PAUSE_IVAL[4]	0
Bit 3	R/W	PAUSE_IVAL[3]	0
Bit 2	R/W	PAUSE_IVAL[2]	1
Bit 1	R/W	PAUSE_IVAL[1]	1
Bit 0	R/W	PAUSE_IVAL[0]	1

PAUSE_IVAL[15:0]:

Pause Timer Interval value that is used by the PAUSE Generation Logic to

Register 0x336H,0x436H: EGMAC - TX_MAXFR – Transmit Max Frame Length

Bit	Type	Function	Default
Bit 15	R/W	TX_MAXFR[15]	0
Bit 14	R/W	TX_MAXFR[14]	0
Bit 13	R/W	TX_MAXFR[13]	0
Bit 12	R/W	TX_MAXFR[12]	0
Bit 11	R/W	TX_MAXFR[11]	0
Bit 10	R/W	TX_MAXFR[10]	1
Bit 9	R/W	TX_MAXFR [9]	0
Bit 8	R/W	TX_MAXFR [8]	1
Bit 7	R/W	TX_MAXFR [7]	1
Bit 6	R/W	TX_MAXFR [6]	1
Bit 5	R/W	TX_MAXFR [5]	1
Bit 4	R/W	TX_MAXFR [4]	0
Bit 3	R/W	TX_MAXFR [3]	1
Bit 2	R/W	TX_MAXFR [2]	1
Bit 1	R/W	TX_MAXFR [1]	1
Bit 0	R/W	TX_MAXFR [0]	0

TX_MAXFR [15:0]:

Specifies the maximum number of bytes that are allowed to be transmitted before truncation in an outgoing normal Ethernet frame. Default = 1518 bytes > 5EE Hex. Frames that have exceeded the TX_MAXFR setting will be truncated having a 4 byte erred CRC appended to them. Please note that VLAN tagged frames have a 4 byte offset (i.e. 1522 bytes) before being considered as violating the frame length setting and therefore being truncated. The total transmitted frame size for frames violating the maximum transmit frame size will be TX_MAXFR + 4 for non tagged frames and TX_MAXFR + 8 for tagged frames. Please note that supported values for this register are from 1518 to 9600 bytes.

Register 0x337H,0x437H: EGMAC - RXFIFO_FWD – Receive FIFO Forwarding Threshold

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	Reserved	0
Bit 11	R/W	RXFIFO_FWD[11]	0
Bit 10	R/W	RXFIFO_FWD[10]	0
Bit 9	R/W	RXFIFO_FWD[9]	0
Bit 8	R/W	RXFIFO_FWD[8]	1
Bit 7	R/W	RXFIFO_FWD[7]	1
Bit 6	R/W	RXFIFO_FWD[6]	0
Bit 5	R/W	RXFIFO_FWD[5]	0
Bit 4	R/W	RXFIFO_FWD[4]	0
Bit 3	R/W	RXFIFO_FWD[3]	0
Bit 2	R/W	RXFIFO_FWD[2]	0
Bit 1	R/W	RXFIFO_FWD[1]	0
Bit 0	R/W	RXFIFO_FWD[0]	1

RXFIFO_FWD [11:0]:

EGMAC Receive FIFO Forwarding Threshold. Sets the forwarding threshold in the EGMAC Receive FIFO. The value set in this register is units of 32 bits (4 bytes). Default is 0x181 hex double words or 1540 bytes. Please refer to the Operations section for further information on frame forwarding.

Register 0x339H,0x439H: EGMAC - ADR_MATCH0_A – Exact Match Address 0 A Register

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH0[39]	0
Bit 14	R/W	ADR_MATCH0[38]	0
Bit 13	R/W	ADR_MATCH0[37]	0
Bit 12	R/W	ADR_MATCH0[36]	0
Bit 11	R/W	ADR_MATCH0[35]	0
Bit 10	R/W	ADR_MATCH0[34]	0
Bit 9	R/W	ADR_MATCH0[33]	0
Bit 8	R/W	ADR_MATCH0[32]	0
Bit 7	R/W	ADR_MATCH0[47]	0
Bit 6	R/W	ADR_MATCH0[46]	0
Bit 5	R/W	ADR_MATCH0[45]	0
Bit 4	R/W	ADR_MATCH0[44]	0
Bit 3	R/W	ADR_MATCH0[43]	0
Bit 2	R/W	ADR_MATCH0[42]	0
Bit 1	R/W	ADR_MATCH0[41]	0
Bit 0	R/W	ADR_MATCH0[40]	0

ADR_MATCH0 A:

The Address Filter Logic uses the Exact Match Address 0 A Register to do comparisons against the 48-bit MAC source or destination address. This hardware register is one of three concurrent hardware registers that make up this 48 bit address filter.

Register 0x33AH,0x43AH: EGMAC - ADR_MATCH0_B – Exact Match Address 0 B Register

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH0[23]	0
Bit 14	R/W	ADR_MATCH0[22]	0
Bit 13	R/W	ADR_MATCH0[21]	0
Bit 12	R/W	ADR_MATCH0[20]	0
Bit 11	R/W	ADR_MATCH0[19]	0
Bit 10	R/W	ADR_MATCH0[18]	0
Bit 9	R/W	ADR_MATCH0[17]	0
Bit 8	R/W	ADR_MATCH0[16]	0
Bit 7	R/W	ADR_MATCH0[31]	0
Bit 6	R/W	ADR_MATCH0[30]	0
Bit 5	R/W	ADR_MATCH0[39]	0
Bit 4	R/W	ADR_MATCH0[28]	0
Bit 3	R/W	ADR_MATCH0[27]	0
Bit 2	R/W	ADR_MATCH0[26]	0
Bit 1	R/W	ADR_MATCH0[25]	0
Bit 0	R/W	ADR_MATCH0[24]	0

ADR_MATCH0 B:

The Address Filter Logic uses the Exact Match Address 0 B Register to do comparisons against the 48-bit MAC source or destination address. This hardware register is one of three concurrent hardware registers that make up this 48 bit address filter.

Register 0x33BH,0x43BH: EGMAC - ADR_MATCH0_C – Exact Match Address 0 C Register

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH0[7]	0
Bit 14	R/W	ADR_MATCH0[6]	0
Bit 13	R/W	ADR_MATCH0[5]	0
Bit 12	R/W	ADR_MATCH0[4]	0
Bit 11	R/W	ADR_MATCH0[3]	0
Bit 10	R/W	ADR_MATCH0[2]	0
Bit 9	R/W	ADR_MATCH0[1]	0
Bit 8	R/W	ADR_MATCH0[0]	0
Bit 7	R/W	ADR_MATCH0[15]	0
Bit 6	R/W	ADR_MATCH0[14]	0
Bit 5	R/W	ADR_MATCH0[13]	0
Bit 4	R/W	ADR_MATCH0[12]	0
Bit 3	R/W	ADR_MATCH0[11]	0
Bit 2	R/W	ADR_MATCH0[10]	0
Bit 1	R/W	ADR_MATCH0[9]	0
Bit 0	R/W	ADR_MATCH0[8]	0

ADR_MATCH0 C:

The Address Filter Logic uses the Exact Match Address 0 C Register to do comparisons against the 48-bit MAC source or destination address. This hardware register is one of three concurrent hardware registers that make up this 48 bit address filter.

Register 0x33CH,0x43CH: EGMAC - ADR_MATCH1_A – Exact Match Address 1 A Register

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH1[39]	0
Bit 14	R/W	ADR_MATCH1[38]	0
Bit 13	R/W	ADR_MATCH1[37]	0
Bit 12	R/W	ADR_MATCH1[36]	0
Bit 11	R/W	ADR_MATCH1[35]	0
Bit 10	R/W	ADR_MATCH1[34]	0
Bit 9	R/W	ADR_MATCH1[33]	0
Bit 8	R/W	ADR_MATCH1[32]	0
Bit 7	R/W	ADR_MATCH1[47]	0
Bit 6	R/W	ADR_MATCH1[46]	0
Bit 5	R/W	ADR_MATCH1[45]	0
Bit 4	R/W	ADR_MATCH1[44]	0
Bit 3	R/W	ADR_MATCH1[43]	0
Bit 2	R/W	ADR_MATCH1[42]	0
Bit 1	R/W	ADR_MATCH1[41]	0
Bit 0	R/W	ADR_MATCH1[40]	0

ADR_MATCH1_A:

The Address Filter Logic uses the Exact Match Address 1 A Register to do comparisons against the 48-bit MAC source or destination address. This hardware register is one of three concurrent hardware registers that make up this 48 bit address filter.

Register 0x33DH,0x43DH: EGMAC - ADR_MATCH1_B – Exact Match Address 1 B Register

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH1[23]	0
Bit 14	R/W	ADR_MATCH1[22]	0
Bit 13	R/W	ADR_MATCH1[21]	0
Bit 12	R/W	ADR_MATCH1[20]	0
Bit 11	R/W	ADR_MATCH1[19]	0
Bit 10	R/W	ADR_MATCH1[18]	0
Bit 9	R/W	ADR_MATCH1[17]	0
Bit 8	R/W	ADR_MATCH1[16]	0
Bit 7	R/W	ADR_MATCH1[31]	0
Bit 6	R/W	ADR_MATCH1[30]	0
Bit 5	R/W	ADR_MATCH1[29]	0
Bit 4	R/W	ADR_MATCH1[28]	0
Bit 3	R/W	ADR_MATCH1[27]	0
Bit 2	R/W	ADR_MATCH1[26]	0
Bit 1	R/W	ADR_MATCH1[25]	0
Bit 0	R/W	ADR_MATCH1[24]	0

ADR_MATCH1_B:

The Address Filter Logic uses the Exact Match Address 1 B Register to do comparisons against the 48-bit MAC source or destination address. This hardware register is one of three concurrent hardware registers that make up this 48 bit address filter.

Register 0x33EH,0x43EH: EGMAC - ADR_MATCH1_C – Exact Match Address 1 C Register

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH1[7]	0
Bit 14	R/W	ADR_MATCH1[6]	0
Bit 13	R/W	ADR_MATCH1[5]	0
Bit 12	R/W	ADR_MATCH1[4]	0
Bit 11	R/W	ADR_MATCH1[3]	0
Bit 10	R/W	ADR_MATCH1[2]	0
Bit 9	R/W	ADR_MATCH1[1]	0
Bit 8	R/W	ADR_MATCH1[0]	0
Bit 7	R/W	ADR_MATCH1[15]	0
Bit 6	R/W	ADR_MATCH1[14]	0
Bit 5	R/W	ADR_MATCH1[13]	0
Bit 4	R/W	ADR_MATCH1[12]	0
Bit 3	R/W	ADR_MATCH1[11]	0
Bit 2	R/W	ADR_MATCH1[10]	0
Bit 1	R/W	ADR_MATCH1[9]	0
Bit 0	R/W	ADR_MATCH1[8]	0

ADR_MATCH1_C:

The Address Filter Logic uses the Exact Match Address 1 C Register to do comparisons against the 48-bit MAC source or destination address. This hardware register is one of three concurrent hardware registers that make up this 48 bit address filter.

Register 0x33FH,0x43FH: EGMAC - ADR_MATCH2_A – Exact Match Address 2 A Register

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH2[39]	0
Bit 14	R/W	ADR_MATCH2[38]	0
Bit 13	R/W	ADR_MATCH2[37]	0
Bit 12	R/W	ADR_MATCH2[36]	0
Bit 11	R/W	ADR_MATCH2[35]	0
Bit 10	R/W	ADR_MATCH2[34]	0
Bit 9	R/W	ADR_MATCH2[33]	0
Bit 8	R/W	ADR_MATCH2[32]	0
Bit 7	R/W	ADR_MATCH2[47]	0
Bit 6	R/W	ADR_MATCH2[46]	0
Bit 5	R/W	ADR_MATCH2[45]	0
Bit 4	R/W	ADR_MATCH2[44]	0
Bit 3	R/W	ADR_MATCH2[43]	0
Bit 2	R/W	ADR_MATCH2[42]	0
Bit 1	R/W	ADR_MATCH2[41]	0
Bit 0	R/W	ADR_MATCH2[40]	0

ADR_MATCH2 A:

The Address Filter Logic uses the Exact Match Address 2 A Register to do comparisons against the 48-bit MAC source or destination address. This hardware register is one of three concurrent hardware registers that make up this 48 bit address filter.

Register 0x340H,0x440H: EGMAC - ADR_MATCH2_B – Exact Match Address 2 B Register

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH2[23]	0
Bit 14	R/W	ADR_MATCH2[22]	0
Bit 13	R/W	ADR_MATCH2[21]	0
Bit 12	R/W	ADR_MATCH2[20]	0
Bit 11	R/W	ADR_MATCH2[19]	0
Bit 10	R/W	ADR_MATCH2[18]	0
Bit 9	R/W	ADR_MATCH2[17]	0
Bit 8	R/W	ADR_MATCH2[16]	0
Bit 7	R/W	ADR_MATCH2[31]	0
Bit 6	R/W	ADR_MATCH2[30]	0
Bit 5	R/W	ADR_MATCH2[29]	0
Bit 4	R/W	ADR_MATCH2[28]	0
Bit 3	R/W	ADR_MATCH2[27]	0
Bit 2	R/W	ADR_MATCH2[26]	0
Bit 1	R/W	ADR_MATCH2[25]	0
Bit 0	R/W	ADR_MATCH2[24]	0

ADR_MATCH2 B:

The Address Filter Logic uses the Exact Match Address 2 B Register to do comparisons against the 48-bit MAC source or destination address. This hardware register is one of three concurrent hardware registers that make up this 48 bit address filter.

Register 0x341H,0x441H: EGMAC - ADR_MATCH2_C – Exact Match Address 2 C Register

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH2[7]	0
Bit 14	R/W	ADR_MATCH2[6]	0
Bit 13	R/W	ADR_MATCH2[5]	0
Bit 12	R/W	ADR_MATCH2[4]	0
Bit 11	R/W	ADR_MATCH2[3]	0
Bit 10	R/W	ADR_MATCH2[2]	0
Bit 9	R/W	ADR_MATCH2[1]	0
Bit 8	R/W	ADR_MATCH2[0]	0
Bit 7	R/W	ADR_MATCH2[15]	0
Bit 6	R/W	ADR_MATCH2[14]	0
Bit 5	R/W	ADR_MATCH2[13]	0
Bit 4	R/W	ADR_MATCH2[12]	0
Bit 3	R/W	ADR_MATCH2[11]	0
Bit 2	R/W	ADR_MATCH2[10]	0
Bit 1	R/W	ADR_MATCH2[9]	0
Bit 0	R/W	ADR_MATCH2[8]	0

ADR_MATCH2 C:

The Address Filter Logic uses the Exact Match Address 2 C Register to do comparisons against the 48-bit MAC source or destination address. This hardware register is one of three concurrent hardware registers that make up this 48 bit address filter.

Register 0x342H,0x442H: EGMAC - ADR_MATCH3_A – Exact Match Address 3 A Register

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH3[39]	0
Bit 14	R/W	ADR_MATCH3[38]	0
Bit 13	R/W	ADR_MATCH3[37]	0
Bit 12	R/W	ADR_MATCH3[36]	0
Bit 11	R/W	ADR_MATCH3[35]	0
Bit 10	R/W	ADR_MATCH3[34]	0
Bit 9	R/W	ADR_MATCH3[33]	0
Bit 8	R/W	ADR_MATCH3[32	0
Bit 7	R/W	ADR_MATCH3[47]	0
Bit 6	R/W	ADR_MATCH3[46]	0
Bit 5	R/W	ADR_MATCH3[45]	0
Bit 4	R/W	ADR_MATCH3[44]	0
Bit 3	R/W	ADR_MATCH3[43]	0
Bit 2	R/W	ADR_MATCH3[42]	0
Bit 1	R/W	ADR_MATCH3[41]	0
Bit 0	R/W	ADR_MATCH3[40]	0

ADR_MATCH3 A:

The Address Filter Logic uses the Exact Match Address 3 A Register to do comparisons against the 48-bit MAC source or destination address. This hardware register is one of three concurrent hardware registers that make up this 48 bit address filter.

Register 0x343H,0x443H: EGMAC - ADR_MATCH3_B – Exact Match Address 3 B Register

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH3[23]	0
Bit 14	R/W	ADR_MATCH3[22]	0
Bit 13	R/W	ADR_MATCH3[21]	0
Bit 12	R/W	ADR_MATCH3[20]	0
Bit 11	R/W	ADR_MATCH3[19]	0
Bit 10	R/W	ADR_MATCH3[18]	0
Bit 9	R/W	ADR_MATCH3[17]	0
Bit 8	R/W	ADR_MATCH3[16]	0
Bit 7	R/W	ADR_MATCH3[31]	0
Bit 6	R/W	ADR_MATCH3[30]	0
Bit 5	R/W	ADR_MATCH3[29]	0
Bit 4	R/W	ADR_MATCH3[28]	0
Bit 3	R/W	ADR_MATCH3[27]	0
Bit 2	R/W	ADR_MATCH3[26]	0
Bit 1	R/W	ADR_MATCH3[25]	0
Bit 0	R/W	ADR_MATCH3[24]	0

ADR_MATCH3 B:

The Address Filter Logic uses the Exact Match Address 3 B Register to do comparisons against the 48-bit MAC source or destination address. This hardware register is one of three concurrent hardware registers that make up this 48 bit address filter.

Register 0x344H,0x444H: EGMAC - ADR_MATCH3_C – Exact Match Address 3 C Register

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH3[7]	0
Bit 14	R/W	ADR_MATCH3[6]	0
Bit 13	R/W	ADR_MATCH3[5]	0
Bit 12	R/W	ADR_MATCH3[4]	0
Bit 11	R/W	ADR_MATCH3[3]	0
Bit 10	R/W	ADR_MATCH3[2]	0
Bit 9	R/W	ADR_MATCH3[1]	0
Bit 8	R/W	ADR_MATCH3[0]	0
Bit 7	R/W	ADR_MATCH3[15]	0
Bit 6	R/W	ADR_MATCH3[14]	0
Bit 5	R/W	ADR_MATCH3[13]	0
Bit 4	R/W	ADR_MATCH3[12]	0
Bit 3	R/W	ADR_MATCH3[11]	0
Bit 2	R/W	ADR_MATCH3[10]	0
Bit 1	R/W	ADR_MATCH3[9]	0
Bit 0	R/W	ADR_MATCH3[8]	0

ADR_MATCH3 C:

The Address Filter Logic uses the Exact Match Address 3 C Register to do comparisons against the 48-bit MAC source or destination address. This hardware register is one of three concurrent hardware registers that make up this 48 bit address filter.

Register 0x345H,0x445H: EGMAC - ADR_MATCH4_A – Exact Match Address 4 A Register

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH4[39]	0
Bit 14	R/W	ADR_MATCH4[38]	0
Bit 13	R/W	ADR_MATCH4[37]	0
Bit 12	R/W	ADR_MATCH4[36]	0
Bit 11	R/W	ADR_MATCH4[35]	0
Bit 10	R/W	ADR_MATCH4[34]	0
Bit 9	R/W	ADR_MATCH4[33]	0
Bit 8	R/W	ADR_MATCH4[32]	0
Bit 7	R/W	ADR_MATCH4[47]	0
Bit 6	R/W	ADR_MATCH4[46]	0
Bit 5	R/W	ADR_MATCH4[45]	0
Bit 4	R/W	ADR_MATCH4[44]	0
Bit 3	R/W	ADR_MATCH4[43]	0
Bit 2	R/W	ADR_MATCH4[42]	0
Bit 1	R/W	ADR_MATCH4[41]	0
Bit 0	R/W	ADR_MATCH4[40]	0

ADR_MATCH4 A:

The Address Filter Logic uses the Exact Match Address 4 A Register to do comparisons against the 48-bit MAC source or destination address. This hardware register is one of three concurrent hardware registers that make up this 48 bit address filter.

Register 0x346H,0x446H: EGMAC - ADR_MATCH4_B – Exact Match Address 4 B Register

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH4[23]	0
Bit 14	R/W	ADR_MATCH4[22]	0
Bit 13	R/W	ADR_MATCH4[21]	0
Bit 12	R/W	ADR_MATCH4[20]	0
Bit 11	R/W	ADR_MATCH4[19]	0
Bit 10	R/W	ADR_MATCH4[18]	0
Bit 9	R/W	ADR_MATCH4[17]	0
Bit 8	R/W	ADR_MATCH4[16]	0
Bit 7	R/W	ADR_MATCH4[31]	0
Bit 6	R/W	ADR_MATCH4[30]	0
Bit 5	R/W	ADR_MATCH4[29]	0
Bit 4	R/W	ADR_MATCH4[28]	0
Bit 3	R/W	ADR_MATCH4[27]	0
Bit 2	R/W	ADR_MATCH4[26]	0
Bit 1	R/W	ADR_MATCH4[25]	0
Bit 0	R/W	ADR_MATCH4[24]	0

ADR_MATCH4 B:

The Address Filter Logic uses the Exact Match Address 4 B Register to do comparisons against the 48-bit MAC source or destination address. This hardware register is one of three concurrent hardware registers that make up this 48 bit address filter.

Register 0x347H,0x447H: EGMAC - ADR_MATCH4_C – Exact Match Address 4 C Register

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH4[7]	0
Bit 14	R/W	ADR_MATCH4[6]	0
Bit 13	R/W	ADR_MATCH4[5]	0
Bit 12	R/W	ADR_MATCH4[4]	0
Bit 11	R/W	ADR_MATCH4[3]	0
Bit 10	R/W	ADR_MATCH4[2]	0
Bit 9	R/W	ADR_MATCH4[1]	0
Bit 8	R/W	ADR_MATCH4[0]	0
Bit 7	R/W	ADR_MATCH4[15]	0
Bit 6	R/W	ADR_MATCH4[14]	0
Bit 5	R/W	ADR_MATCH4[13]	0
Bit 4	R/W	ADR_MATCH4[12]	0
Bit 3	R/W	ADR_MATCH4[11]	0
Bit 2	R/W	ADR_MATCH4[10]	0
Bit 1	R/W	ADR_MATCH4[9]	0
Bit 0	R/W	ADR_MATCH4[8]	0

ADR_MATCH4 C:

The Address Filter Logic uses the Exact Match Address 4 C Register to do comparisons against the 48-bit MAC source or destination address. This hardware register is one of three concurrent hardware registers that make up this 48 bit address filter.

Register 0x348H,0x448H: EGMAC - ADR_MATCH5_A – Exact Match Address 5 A Register

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH5[39]	0
Bit 14	R/W	ADR_MATCH5[38]	0
Bit 13	R/W	ADR_MATCH5[37]	0
Bit 12	R/W	ADR_MATCH5[36]	0
Bit 11	R/W	ADR_MATCH5[35]	0
Bit 10	R/W	ADR_MATCH5[34]	0
Bit 9	R/W	ADR_MATCH5[33]	0
Bit 8	R/W	ADR_MATCH532]	0
Bit 7	R/W	ADR_MATCH5[47]	0
Bit 6	R/W	ADR_MATCH5[46]	0
Bit 5	R/W	ADR_MATCH5[45]	0
Bit 4	R/W	ADR_MATCH5[44]	0
Bit 3	R/W	ADR_MATCH5[43]	0
Bit 2	R/W	ADR_MATCH5[42]	0
Bit 1	R/W	ADR_MATCH5[41]	0
Bit 0	R/W	ADR_MATCH5[40]	0

ADR_MATCH5 A:

The Address Filter Logic uses the Exact Match Address 5 A Register to do comparisons against the 48-bit MAC source or destination address. This hardware register is one of three concurrent hardware registers that make up this 48 bit address filter.

Register 0x349H,0x449H: EGMAC - ADR_MATCH5_B – Exact Match Address 5 B Register

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH5[23]	0
Bit 14	R/W	ADR_MATCH5[22]	0
Bit 13	R/W	ADR_MATCH5[21]	0
Bit 12	R/W	ADR_MATCH5[20]	0
Bit 11	R/W	ADR_MATCH5[19]	0
Bit 10	R/W	ADR_MATCH5[18]	0
Bit 9	R/W	ADR_MATCH5[17]	0
Bit 8	R/W	ADR_MATCH5[16]	0
Bit 7	R/W	ADR_MATCH5[31]	0
Bit 6	R/W	ADR_MATCH5[30]	0
Bit 5	R/W	ADR_MATCH5[29]	0
Bit 4	R/W	ADR_MATCH5[28]	0
Bit 3	R/W	ADR_MATCH5[27]	0
Bit 2	R/W	ADR_MATCH5[26]	0
Bit 1	R/W	ADR_MATCH5[25]	0
Bit 0	R/W	ADR_MATCH5[24]	0

ADR_MATCH5 B:

The Address Filter Logic uses the Exact Match Address 5 B Register to do comparisons against the 48-bit MAC source or destination address. This hardware register is one of three concurrent hardware registers that make up this 48 bit address filter.

Register 0x34AH,0x44AH: EGMAC - ADR_MATCH5_C – Exact Match Address 5 C Register

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH5[7]	0
Bit 14	R/W	ADR_MATCH5[6]	0
Bit 13	R/W	ADR_MATCH5[5]	0
Bit 12	R/W	ADR_MATCH5[4]	0
Bit 11	R/W	ADR_MATCH5[3]	0
Bit 10	R/W	ADR_MATCH5[2]	0
Bit 9	R/W	ADR_MATCH5[1]	0
Bit 8	R/W	ADR_MATCH5[0]	0
Bit 7	R/W	ADR_MATCH5[15]	0
Bit 6	R/W	ADR_MATCH5[14]	0
Bit 5	R/W	ADR_MATCH5[13]	0
Bit 4	R/W	ADR_MATCH5[12]	0
Bit 3	R/W	ADR_MATCH5[11]	0
Bit 2	R/W	ADR_MATCH5[10]	0
Bit 1	R/W	ADR_MATCH5[9]	0
Bit 0	R/W	ADR_MATCH5[8]	0

ADR_MATCH5 C:

The Address Filter Logic uses the Exact Match Address 5 C Register to do comparisons against the 48-bit MAC source or destination address. This hardware register is one of three concurrent hardware registers that make up this 48 bit address filter.

Register 0x34BH,0x44BH: EGMAC - ADR_MATCH6_A – Exact Match Address 6 A Register

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH6[39]	0
Bit 14	R/W	ADR_MATCH6[38]	0
Bit 13	R/W	ADR_MATCH6[37]	0
Bit 12	R/W	ADR_MATCH6[36]	0
Bit 11	R/W	ADR_MATCH6[35]	0
Bit 10	R/W	ADR_MATCH6[34]	0
Bit 9	R/W	ADR_MATCH6[33]	0
Bit 8	R/W	ADR_MATCH6[32]	0
Bit 7	R/W	ADR_MATCH6[47]	0
Bit 6	R/W	ADR_MATCH6[46]	0
Bit 5	R/W	ADR_MATCH6[45]	0
Bit 4	R/W	ADR_MATCH6[44]	0
Bit 3	R/W	ADR_MATCH6[43]	0
Bit 2	R/W	ADR_MATCH6[42]	0
Bit 1	R/W	ADR_MATCH6[41]	0
Bit 0	R/W	ADR_MATCH6[40]	0

ADR_MATCH6 A:

The Address Filter Logic uses the Exact Match Address 6 A Register to do comparisons against the 48-bit MAC source or destination address. This hardware register is one of three concurrent hardware registers that make up this 48 bit address filter.

Register 0x34CH,0x44CH: EGMAC - ADR_MATCH6_B – Exact Match Address 6 B Register

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH6[23]	0
Bit 14	R/W	ADR_MATCH6[22]	0
Bit 13	R/W	ADR_MATCH6[21]	0
Bit 12	R/W	ADR_MATCH6[20]	0
Bit 11	R/W	ADR_MATCH6[19]	0
Bit 10	R/W	ADR_MATCH6[18]	0
Bit 9	R/W	ADR_MATCH6[17]	0
Bit 8	R/W	ADR_MATCH6[16]	0
Bit 7	R/W	ADR_MATCH6[31]	0
Bit 6	R/W	ADR_MATCH6[30]	0
Bit 5	R/W	ADR_MATCH6[29]	0
Bit 4	R/W	ADR_MATCH6[28]	0
Bit 3	R/W	ADR_MATCH6[27]	0
Bit 2	R/W	ADR_MATCH6[26]	0
Bit 1	R/W	ADR_MATCH6[25]	0
Bit 0	R/W	ADR_MATCH6[24]	0

ADR_MATCH6 B:

The Address Filter Logic uses the Exact Match Address 6 B Register to do comparisons against the 48-bit MAC source or destination address. This hardware register is one of three concurrent hardware registers that make up this 48 bit address filter.

Register 0x34DH,0x44DH: EGMAC - ADR_MATCH6_C – Exact Match Address 6 C Register

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH6[7]	0
Bit 14	R/W	ADR_MATCH6[6]	0
Bit 13	R/W	ADR_MATCH6[5]	0
Bit 12	R/W	ADR_MATCH6[4]	0
Bit 11	R/W	ADR_MATCH6[3]	0
Bit 10	R/W	ADR_MATCH6[2]	0
Bit 9	R/W	ADR_MATCH6[1]	0
Bit 8	R/W	ADR_MATCH6[0]	0
Bit 7	R/W	ADR_MATCH6[15]	0
Bit 6	R/W	ADR_MATCH6[14]	0
Bit 5	R/W	ADR_MATCH6[13]	0
Bit 4	R/W	ADR_MATCH6[12]	0
Bit 3	R/W	ADR_MATCH6[11]	0
Bit 2	R/W	ADR_MATCH6[10]	0
Bit 1	R/W	ADR_MATCH6[9]	0
Bit 0	R/W	ADR_MATCH6[8]	0

ADR_MATCH6 C:

The Address Filter Logic uses the Exact Match Address 6 C Register to do comparisons against the 48-bit MAC source or destination address. This hardware register is one of three concurrent hardware registers that make up this 48 bit address filter.

Register 0x34EH,0x44EH: EGMAC - ADR_MATCH7_A – Exact Match Address 7 A Register

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH7[39]	0
Bit 14	R/W	ADR_MATCH7[38]	0
Bit 13	R/W	ADR_MATCH7[37]	0
Bit 12	R/W	ADR_MATCH7[36]	0
Bit 11	R/W	ADR_MATCH7[35]	0
Bit 10	R/W	ADR_MATCH7[34]	0
Bit 9	R/W	ADR_MATCH7[33]	0
Bit 8	R/W	ADR_MATCH7[32]	0
Bit 7	R/W	ADR_MATCH7[47]	0
Bit 6	R/W	ADR_MATCH7[46]	0
Bit 5	R/W	ADR_MATCH7[45]	0
Bit 4	R/W	ADR_MATCH7[44]	0
Bit 3	R/W	ADR_MATCH7[43]	0
Bit 2	R/W	ADR_MATCH7[42]	0
Bit 1	R/W	ADR_MATCH7[41]	0
Bit 0	R/W	ADR_MATCH7[40]	0

ADR_MATCH7 A:

The Address Filter Logic uses the Exact Match Address 7 A Register to do comparisons against the 48-bit MAC source or destination address. This hardware register is one of three concurrent hardware registers that make up this 48 bit address filter.

Register 0x34FH,0x44FH: EGMAC - ADR_MATCH7_B – Exact Match Address 7 B Register

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH7[23]	0
Bit 14	R/W	ADR_MATCH7[22]	0
Bit 13	R/W	ADR_MATCH7[21]	0
Bit 12	R/W	ADR_MATCH7[20]	0
Bit 11	R/W	ADR_MATCH7[19]	0
Bit 10	R/W	ADR_MATCH7[18]	0
Bit 9	R/W	ADR_MATCH7[17]	0
Bit 8	R/W	ADR_MATCH7[16]	0
Bit 7	R/W	ADR_MATCH7[31]	0
Bit 6	R/W	ADR_MATCH7[30]	0
Bit 5	R/W	ADR_MATCH7[29]	0
Bit 4	R/W	ADR_MATCH7[28]	0
Bit 3	R/W	ADR_MATCH7[27]	0
Bit 2	R/W	ADR_MATCH7[26]	0
Bit 1	R/W	ADR_MATCH7[25]	0
Bit 0	R/W	ADR_MATCH7[24]	0

ADR_MATCH7 B:

The Address Filter Logic uses the Exact Match Address 7 B Register to do comparisons against the 48-bit MAC source or destination address. This hardware register is one of three concurrent hardware registers that make up this 48 bit address filter.

Register 0x350H,0x450H: EGMAC - ADR_MATCH7_C – Exact Match Address 7 C Register

Bit	Type	Function	Default
Bit 15	R/W	ADR_MATCH7[7]	0
Bit 14	R/W	ADR_MATCH7[6]	0
Bit 13	R/W	ADR_MATCH7[5]	0
Bit 12	R/W	ADR_MATCH7[4]	0
Bit 11	R/W	ADR_MATCH7[3]	0
Bit 10	R/W	ADR_MATCH7[2]	0
Bit 9	R/W	ADR_MATCH7[1]	0
Bit 8	R/W	ADR_MATCH7[0]	0
Bit 7	R/W	ADR_MATCH7[15]	0
Bit 6	R/W	ADR_MATCH7[14]	0
Bit 5	R/W	ADR_MATCH7[13]	0
Bit 4	R/W	ADR_MATCH7[12]	0
Bit 3	R/W	ADR_MATCH7[11]	0
Bit 2	R/W	ADR_MATCH7[10]	0
Bit 1	R/W	ADR_MATCH7[9]	0
Bit 0	R/W	ADR_MATCH7[8]	0

ADR_MATCH7 C:

The Address Filter Logic uses the Exact Match Address 7 C Register to do comparisons against the 48-bit MAC source or destination address. This hardware register is one of three concurrent hardware registers that make up this 48 bit address filter.

Register 0x351H,0x451H: EGMAC - VID_MATCH0 – Exact Match VID 0 Register

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	VID_MATCH0[11]	0
Bit 10	R/W	VID_MATCH0[10]	0
Bit 9	R/W	VID_MATCH0[9]	0
Bit 8	R/W	VID_MATCH0[8]	0
Bit 7	R/W	VID_MATCH0[7]	0
Bit 6	R/W	VID_MATCH0[6]	0
Bit 5	R/W	VID_MATCH0[5]	0
Bit 4	R/W	VID_MATCH0[4]	0
Bit 3	R/W	VID_MATCH0[3]	0
Bit 2	R/W	VID_MATCH0[2]	0
Bit 1	R/W	VID_MATCH0[1]	0
Bit 0	R/W	VID_MATCH0[0]	0

VID_MATCH0[11:0]:

The Exact Match VID 0 Register is used by the Address Filter Logic to compare on the 12 bit VID field on VLAN tagged frames. This register is one of eight separate Exact Match VID Registers that the Address Filter Logic can use to compare on.

Register 0x352H,0x452H: EGMAC - VID_MATCH1 – Exact Match VID 1 Register

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	VID_MATCH1[11]	0
Bit 10	R/W	VID_MATCH1[10]	0
Bit 9	R/W	VID_MATCH1[9]	0
Bit 8	R/W	VID_MATCH1[8]	0
Bit 7	R/W	VID_MATCH1[7]	0
Bit 6	R/W	VID_MATCH1[6]	0
Bit 5	R/W	VID_MATCH1[5]	0
Bit 4	R/W	VID_MATCH1[4]	0
Bit 3	R/W	VID_MATCH1[3]	0
Bit 2	R/W	VID_MATCH1[2]	0
Bit 1	R/W	VID_MATCH1[1]	0
Bit 0	R/W	VID_MATCH1[0]	0

VID_MATCH1[11:0]:

The Exact Match VID 1 Register is used by the Address Filter Logic to compare on the 12 bit VID field on VLAN tagged frames. This register is one of eight separate Exact Match VID Registers that the Address Filter Logic can use to compare on.

Register 0x353H,0x453H: EGMAC - VID_MATCH2 – Exact Match VID 2 Register

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	VID_MATCH2[11]	0
Bit 10	R/W	VID_MATCH2[10]	0
Bit 9	R/W	VID_MATCH2[9]	0
Bit 8	R/W	VID_MATCH2[8]	0
Bit 7	R/W	VID_MATCH2[7]	0
Bit 6	R/W	VID_MATCH2[6]	0
Bit 5	R/W	VID_MATCH2[5]	0
Bit 4	R/W	VID_MATCH2[4]	0
Bit 3	R/W	VID_MATCH2[3]	0
Bit 2	R/W	VID_MATCH2[2]	0
Bit 1	R/W	VID_MATCH2[1]	0
Bit 0	R/W	VID_MATCH2[0]	0

VID_MATCH2[11:0]:

The Exact Match VID 2 Register is used by the Address Filter Logic to compare on the 12 bit VID field on VLAN tagged frames. This register is one of eight separate Exact Match VID Registers that the Address Filter Logic can use to compare on.

Register 0x354H,0x454H: EGMAC - VID_MATCH3 – Exact Match VID 3 Register

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	VID_MATCH3[11]	0
Bit 10	R/W	VID_MATCH3[10]	0
Bit 9	R/W	VID_MATCH3[9]	0
Bit 8	R/W	VID_MATCH3[8]	0
Bit 7	R/W	VID_MATCH3[7]	0
Bit 6	R/W	VID_MATCH3[6]	0
Bit 5	R/W	VID_MATCH3[5]	0
Bit 4	R/W	VID_MATCH3[4]	0
Bit 3	R/W	VID_MATCH3[3]	0
Bit 2	R/W	VID_MATCH3[2]	0
Bit 1	R/W	VID_MATCH3[1]	0
Bit 0	R/W	VID_MATCH3[0]	0

VID_MATCH3[11:0]:

The Exact Match VID 3 Register is used by the Address Filter Logic to compare on the 12 bit VID field on VLAN tagged frames. This register is one of eight separate Exact Match VID Registers that the Address Filter Logic can use to compare on.

Register 0x355H,0x455H: EGMAC - VID_MATCH4 – Exact Match VID 4 Register

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	VID_MATCH4[11]	0
Bit 10	R/W	VID_MATCH4[10]	0
Bit 9	R/W	VID_MATCH4[9]	0
Bit 8	R/W	VID_MATCH4[8]	0
Bit 7	R/W	VID_MATCH4[7]	0
Bit 6	R/W	VID_MATCH4[6]	0
Bit 5	R/W	VID_MATCH4[5]	0
Bit 4	R/W	VID_MATCH4[4]	0
Bit 3	R/W	VID_MATCH4[3]	0
Bit 2	R/W	VID_MATCH4[2]	0
Bit 1	R/W	VID_MATCH4[1]	0
Bit 0	R/W	VID_MATCH4[0]	0

VID_MATCH4[11:0]:

The Exact Match VID 4 Register is used by the Address Filter Logic to compare on the 12 bit VID field on VLAN tagged frames. This register is one of eight separate Exact Match VID Registers that the Address Filter Logic can use to compare on.

Register 0x356H,0x456H: EGMAC - VID_MATCH5 – Exact Match VID 5 Register

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	VID_MATCH5[11]	0
Bit 10	R/W	VID_MATCH5[10]	0
Bit 9	R/W	VID_MATCH5[9]	0
Bit 8	R/W	VID_MATCH5[8]	0
Bit 7	R/W	VID_MATCH5[7]	0
Bit 6	R/W	VID_MATCH5[6]	0
Bit 5	R/W	VID_MATCH5[5]	0
Bit 4	R/W	VID_MATCH5[4]	0
Bit 3	R/W	VID_MATCH5[3]	0
Bit 2	R/W	VID_MATCH5[2]	0
Bit 1	R/W	VID_MATCH5[1]	0
Bit 0	R/W	VID_MATCH5[0]	0

VID_MATCH5[11:0]:

The Exact Match VID 5 Register is used by the Address Filter Logic to compare on the 12 bit VID field on VLAN tagged frames. This register is one of eight separate Exact Match VID Registers that the Address Filter Logic can use to compare on.

Register 0x357H,0x457H: EGMAC - VID_MATCH6 – Exact Match VID 6 Register

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	VID_MATCH6[11]	0
Bit 10	R/W	VID_MATCH6[10]	0
Bit 9	R/W	VID_MATCH6[9]	0
Bit 8	R/W	VID_MATCH6[8]	0
Bit 7	R/W	VID_MATCH6[7]	0
Bit 6	R/W	VID_MATCH6[6]	0
Bit 5	R/W	VID_MATCH6[5]	0
Bit 4	R/W	VID_MATCH6[4]	0
Bit 3	R/W	VID_MATCH6[3]	0
Bit 2	R/W	VID_MATCH6[2]	0
Bit 1	R/W	VID_MATCH6[1]	0
Bit 0	R/W	VID_MATCH6[0]	0

VID_MATCH6[11:0]:

The Exact Match VID 6 Register is used by the Address Filter Logic to compare on the 12 bit VID field on VLAN tagged frames. This register is one of eight separate Exact Match VID Registers that the Address Filter Logic can use to compare on.

Register 0x358H,0x458H: EGMAC - VID_MATCH7 – Exact Match VID 7 Register

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	VID_MATCH7[11]	0
Bit 10	R/W	VID_MATCH7[10]	0
Bit 9	R/W	VID_MATCH7[9]	0
Bit 8	R/W	VID_MATCH7[8]	0
Bit 7	R/W	VID_MATCH7[7]	0
Bit 6	R/W	VID_MATCH7[6]	0
Bit 5	R/W	VID_MATCH7[5]	0
Bit 4	R/W	VID_MATCH7[4]	0
Bit 3	R/W	VID_MATCH7[3]	0
Bit 2	R/W	VID_MATCH7[2]	0
Bit 1	R/W	VID_MATCH7[1]	0
Bit 0	R/W	VID_MATCH7[0]	0

VID_MATCH7[11:0]:

The Exact Match VID 7 Register is used by the Address Filter Logic to compare on the 12 bit VID field on VLAN tagged frames. This register is one of eight separate Exact Match VID Registers that the Address Filter Logic can use to compare on.

Register 0x359H,0x459H: EGMAC - MHASH[15:0] – Multicast HASH Low Word Register

Bit	Type	Function	Default
Bit 15	R/W	MHASH[15]	0
Bit 14	R/W	MHASH[14]	0
Bit 13	R/W	MHASH[13]	0
Bit 12	R/W	MHASH[12]	0
Bit 11	R/W	MHASH[11]	0
Bit 10	R/W	MHASH[10]	0
Bit 9	R/W	MHASH[9]	0
Bit 8	R/W	MHASH[8]	0
Bit 7	R/W	MHASH[7]	0
Bit 6	R/W	MHASH[6]	0
Bit 5	R/W	MHASH[5]	0
Bit 4	R/W	MHASH[4]	0
Bit 3	R/W	MHASH[3]	0
Bit 2	R/W	MHASH[2]	0
Bit 1	R/W	MHASH[1]	0
Bit 0	R/W	MHASH[0]	0

MHASH[15:0]:

The MHASH[15:0] is the Low word of the 64-bit Multicast Hash bin. This and the following registers are used with a 6-bit CRC value computed from a 9-bit CRC over the Destination Address. This 6-bit CRC is used to index into the 64-bit Multicast Hash register, index[5:0] = 0 corresponds to bit-0 of the 64-bit Multicast Hash register, index[5:0] = 1 corresponds to bit-1 of the 64-bit register and so on. If the computed index bit in the Multicast Hash register is set to one the multicast addressed frame is forwarded, if the bit is set to a zero then the multicast addressed frame is filtered.

Register 0x35AH,0x45AH: EGMAC - MHASH[31:16] – Multicast HASH MidLow Word Register

Bit	Type	Function	Default
Bit 15	R/W	MHASH[31]	0
Bit 14	R/W	MHASH[30]	0
Bit 13	R/W	MHASH[29]	0
Bit 12	R/W	MHASH[28]	0
Bit 11	R/W	MHASH[27]	0
Bit 10	R/W	MHASH[26]	0
Bit 9	R/W	MHASH[25]	0
Bit 8	R/W	MHASH[24]	0
Bit 7	R/W	MHASH[23]	0
Bit 6	R/W	MHASH[22]	0
Bit 5	R/W	MHASH[21]	0
Bit 4	R/W	MHASH[20]	0
Bit 3	R/W	MHASH[19]	0
Bit 2	R/W	MHASH[18]	0
Bit 1	R/W	MHASH[17]	0
Bit 0	R/W	MHASH[16]	0

MHASH[31:16]:

The MHASH[31:16] is the MidLow word of the 64-bit Multicast Hash bin.

Register 0x35BH,0x45BH: EGMAC - MHASH[47:32] – Multicast HASH MidHigh Word Register

Bit	Type	Function	Default
Bit 15	R/W	MHASH[47]	0
Bit 14	R/W	MHASH[46]	0
Bit 13	R/W	MHASH[45]	0
Bit 12	R/W	MHASH[44]	0
Bit 11	R/W	MHASH[43]	0
Bit 10	R/W	MHASH[42]	0
Bit 9	R/W	MHASH[41]	0
Bit 8	R/W	MHASH[40]	0
Bit 7	R/W	MHASH[39]	0
Bit 6	R/W	MHASH[38]	0
Bit 5	R/W	MHASH[37]	0
Bit 4	R/W	MHASH[36]	0
Bit 3	R/W	MHASH[35]	0
Bit 2	R/W	MHASH[34]	0
Bit 1	R/W	MHASH[33]	0
Bit 0	R/W	MHASH[32]	0

MHASH[47:32]:

The MHASH[47:32] is the MidHigh word of the 64-bit Multicast Hash bin.

Register 0x35CH,0x45CH: EGMAC - MHASH[63:48] – Multicast HASH High Word Register

Bit	Type	Function	Default
Bit 15	R/W	MHASH[63]	0
Bit 14	R/W	MHASH[62]	0
Bit 13	R/W	MHASH[61]	0
Bit 12	R/W	MHASH[60]	0
Bit 11	R/W	MHASH[59]	0
Bit 10	R/W	MHASH[58]	0
Bit 9	R/W	MHASH[57]	0
Bit 8	R/W	MHASH[56]	0
Bit 7	R/W	MHASH[55]	0
Bit 6	R/W	MHASH[54]	0
Bit 5	R/W	MHASH[53]	0
Bit 4	R/W	MHASH[52]	0
Bit 3	R/W	MHASH[51]	0
Bit 2	R/W	MHASH[50]	0
Bit 1	R/W	MHASH[49]	0
Bit 0	R/W	MHASH[48]	0

MHASH[63:48]:

The MHASH[63:48] is the High word of the 64-bit Multicast Hash bin.

Register 0x35DH,0x45DH: EGMAC - Address Filter Control 0 Register

Bit	Type	Function	Default
Bit 15	R/W	ADRFILT_CTRL3[3]	0
Bit 14	R/W	ADRFILT_CTRL3[2]	0
Bit 13	R/W	ADRFILT_CTRL3[1]	0
Bit 12	R/W	ADRFILT_CTRL3[0]	0
Bit 11	R/W	ADRFILT_CTRL2[3]	0
Bit 10	R/W	ADRFILT_CTRL2[2]	0
Bit 9	R/W	ADRFILT_CTRL2[1]	0
Bit 8	R/W	ADRFILT_CTRL2[0]	0
Bit 7	R/W	ADRFILT_CTRL1[3]	0
Bit 6	R/W	ADRFILT_CTRL1[2]	0
Bit 5	R/W	ADRFILT_CTRL1[1]	0
Bit 4	R/W	ADRFILT_CTRL1[0]	0
Bit 3	R/W	ADRFILT_CTRL0[3]	0
Bit 2	R/W	ADRFILT_CTRL0[2]	0
Bit 1	R/W	ADRFILT_CTRL0[1]	0
Bit 0	R/W	ADRFILT_CTRL0[0]	0

ADRFILT_CTRL?[3:0]:

The Address Filter Control 0 Register contains the Control bits for the first 4 filters 0-3. Each filter needs 4 bits of control information.

ADRFILT_CTRL?[0] – Match Enable bit.
If set to a 0 then the Address Filter Logic will not use the corresponding filter to perform any compares, ADRFILT_CTRL?[3:1] have no effect. If set to a 1 then the Address Filter Logic will use the corresponding filter to do compares based on ADRFILT_CTRL[3:1].

ADRFILT_CTRL?[1] – Source Address Enable bit.
If set to a 0 then the Address Filter Logic will use the Destination Address to perform a compare to the corresponding Exact Match Address Register. If set to a 1 then the Address Filter Logic will use the Source Address to perform a compare to the corresponding Exact Match Address Register.

ADRFILT_CTRL?[2] – VLAN Enable bit.
If set to a 1 then the Address Filter Logic will use the corresponding 12-bit VID_MATCH register along with the corresponding Exact Match Address Register to perform the compare. If set to a 0 then the Address Filter Logic will only use the corresponding Exact Match Address Register to perform the compare

ADRFILT_CTRL?[3] – Forward Enable bit.
If set to a 1 then the Address Filter Logic will only **accept** frames that match the corresponding Exact Match Address Register, and if the VLAN enable bit is set the corresponding VID_MATCH register all other frame are filtered. If set to a 0 then the Address Filter Logic will only **discard** frames that match the corresponding Exact Match Address Register, and if the VLAN enable bit is set the corresponding VID_MATCH register all other frames are forwarded.

Register 0x35EH,0x45EH: EGMAC - Address Filter Control 1 Register

Bit	Type	Function	Default
Bit 15	R/W	ADRFILT_CTRL7[3]	0
Bit 14	R/W	ADRFILT_CTRL7[2]	0
Bit 13	R/W	ADRFILT_CTRL7[1]	0
Bit 12	R/W	ADRFILT_CTRL7[0]	0
Bit 11	R/W	ADRFILT_CTRL6[3]	0
Bit 10	R/W	ADRFILT_CTRL6[2]	0
Bit 9	R/W	ADRFILT_CTRL6[1]	0
Bit 8	R/W	ADRFILT_CTRL6[0]	0
Bit 7	R/W	ADRFILT_CTRL5[3]	0
Bit 6	R/W	ADRFILT_CTRL5[2]	0
Bit 5	R/W	ADRFILT_CTRL5[1]	0
Bit 4	R/W	ADRFILT_CTRL5[0]	0
Bit 3	R/W	ADRFILT_CTRL4[3]	0
Bit 2	R/W	ADRFILT_CTRL4[2]	0
Bit 1	R/W	ADRFILT_CTRL4[1]	0
Bit 0	R/W	ADRFILT_CTRL4[0]	0

ADRFILT_CTRL?[3:0]:

The Address Filter Control 0 Register contains the Control bits for the last 4 filters 4-7, each filter needs 4 bits of control information.

ADRFILT_CTRL?[0] – Match Enable bit.
If set to a 0 then the Address Filter Logic will not use the corresponding filter to perform any compares, ADRFILT_CTRL?[3:1] have no effect. If set to a 1 then the Address Filter Logic will use the corresponding filter to do compares based on ADRFILT_CTRL[3:1].

ADRFILT_CTRL?[1] – Source Address Enable bit.
If set to a 0 then the Address Filter Logic will use the Destination Address to perform a compare to the corresponding Exact Match Address Register. If set to a 1 then the Address Filter Logic will use the Source Address to perform a compare to the corresponding Exact Match Address Register.

ADRFILT_CTRL?[2] – VLAN Enable bit.
If set to a 1 then the Address Filter Logic will use the corresponding 12-bit VID_MATCH register along with the corresponding Exact Match Address Register to perform the compare. If set to a 0 then the Address Filter Logic will only use the corresponding Exact Match Address Register to perform the compare

ADRFILT_CTRL?[3] – Forward Enable bit.
If set to a 1 then the Address Filter Logic will only **accept** frames that match the corresponding Exact Match Address Register, and if the VLAN enable bit is set the corresponding VID_MATCH register all other frame are filtered. If set to a 0 then the Address Filter Logic will only **discard** frames that match the corresponding Exact Match Address Register, and if the VLAN enable bit is set the corresponding VID_MATCH register all other frames are forwarded.

Register 0x35FH,0x45FH: EGMAC - Address Filter Control 2 Register

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	Reserved	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	Reserved	0
Bit 4	R	Reserved	0
Bit 3	R	Reserved	0
Bit 2	R	Reserved	0
Bit 1	R/W	PMODE	1
Bit 0	R/W	MHASH_EN	0

MHASH_EN:

Multicast Hash filter enable bit. If set to a 1 the 64-bin Multicast Hash Filter function will look at all Multicast Addressed Frames for filter processing. If set to a 0 no Multicast Hash look-ups are performed.

PMODE:

Promiscuous Mode bit. If set to a 1 the EGMAC performs all filtering based on promiscuous mode. If set to a 0 the EGMAC performs all filtering based on Non-Promiscuous mode.

Register 0x360H,0x460H: EGMAC - Address Filter Control 3 Register

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	Reserved	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	Reserved	0
Bit 4	R	Reserved	0
Bit 3	R	Reserved	0
Bit 2	R	Reserved	0
Bit 1	R	Reserved	0
Bit 0	R/W	UPDATE	0

UPDATE:

Update the Address Filter configuration on the next frame boundary. This bit remains set until the update is complete.

Register 0x500H and 0x600H: MSTAT Control

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	Reserved	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	Reserved	0
Bit 4	R	Reserved	0
Bit 3	R	Reserved	0
Bit 2	R/W	WRITE	0
Bit 1	R/W	CLEAR	0
Bit 0	R/W	SNAP	0

The MSTAT Control Register is provides general control over the MSTAT.

SNAP:

The SNAP bit is used to snap all management statistics counters into their complimentary system probe shadow registers for full static system probes. The SNAP bit will perform the copy operation when set high (logic 1). The SNAP bit will automatically clear itself to low (logic 0) after the operation completes.

CLEAR:

The CLEAR bit is used to clear all management statistic registers. The CLEAR bit clear all registers when set high (logic 1). The CLEAR bit will automatically clear itself to low (logic 0) after the operation completes.

WRITE

The WRITE bit is used to initiate a data update write to the selected counter indicated by the MSTAT Counter Write Address Register. The contents of the MSTAT Counter Write Data Registers will be copied into the associative counter. The write is initiated by setting this bit high (logic 1). The WRITE bit will automatically clear itself to low (logic 0) after the operation completes.

Register 0x501H 0x601H: MSTAT Counter Rollover 0

Bit	Type	Function	Default
Bit 15	R	FramesTooLongErrors	0
Bit 14	R	Reserved	0
Bit 13	R	InRangeLengthErrors	0
Bit 12	R	SymbolError	0
Bit 11	R	FramesLostDueToInternalMACError	0
Bit 10	R	FrameCheckSequenceErrors	0
Bit 9	R	MACControlFrameReceived	0
Bit 8	R	PAUSEMACControlFrameReceived	0
Bit 7	R	TaggedFramesReceivedOK	0
Bit 6	R	BroadcastFramesReceivedOK	0
Bit 5	R	MulticastFramesReceivedOK	0
Bit 4	R	UnicastFramesReceivedOK	0
Bit 3	R	OctetsReceived	0
Bit 2	R	FramesReceived	0
Bit 1	R	OctetsReceivedOK	0
Bit 0	R	FramesReceivedOK	0

The MSTAT Counter Rollover Registers provide indication of counter roll over conditions. The register bit remains set until the register is read. Reading this register clears all bits within this register.

Register 0x502H and 0x602H: MSTAT Counter Rollover 1

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	FilteredBroadcastFrames	0
Bit 13	R	FilteredMulticastFrames	0
Bit 12	R	FilteredUnicastFrames	0
Bit 11	R	FilteredOctets	0
Bit 10	R	JumboOctetsReceivedOK	0
Bit 9	R	ReceiveFrames1519toMAXOctets	0
Bit 8	R	ReceiveFrames1024to1518Octets	0
Bit 7	R	ReceiveFrames512to1023Octets	0
Bit 6	R	ReceiveFrames256to511Octets	0
Bit 5	R	ReceiveFrames128to255Octets	0
Bit 4	R	ReceiveFrames65to127Octets	0
Bit 3	R	ReceiveFrames64Octets	0
Bit 2	R	UndersizedFrames	0
Bit 1	R	Fragments	0
Bit 0	R	Jabbers	0

The MSTAT Counter Rollover Registers provide indication of counter roll over conditions. The register bit remains set until the register is read. Reading this register clears all bits within this register.

Register 0x503H and 0x603H: MSTAT Counter Rollover 2

Bit	Type	Function	Default
Bit 15	R	TransmittedFrames128to255Octets	0
Bit 14	R	TransmittedFrames65to127Octets	0
Bit 13	R	TransmittedFrames64Octets	0
Bit 12	R	MACCTRLFramesTransmitted	0
Bit 11	R	PAUSEMACCTRLFramesTransmitted	0
Bit 10	R	BroadcastFramesTransmittedOK	0
Bit 9	R	BroadcastFramesTranmittedAttempted	0
Bit 8	R	MulticastFramesTransmittedOK	0
Bit 7	R	MulticastFramesTransmittedAttempted	0
Bit 6	R	UnicastFramesTransmittedOK	0
Bit 5	R	UnicastFramesTransmittedAttempted	0
Bit 4	R	TransmitSystemError	0
Bit 3	R	FramesLostDueToInternalMacTransmissionError	0
Bit 2	R	OctetsTransmitted	0
Bit 1	R	OctetsTransmittedOK	0
Bit 0	R	FramesTransmitteOK	0

The MSTAT Counter Rollover Registers provide indication of counter roll over conditions. The register bit remains set until the register is read. Reading this register clears all bits within this register.

Register 0x504H and 0x604H: MSTAT Counter Rollover 3

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	Reserved	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	TaggedFramesTransmittedOK	0
Bit 4	R	JumboOctetsTransmittedOK	0
Bit 3	R	TransmittedFrames1519toMAXOctets	0
Bit 2	R	TransmittedFrames1024to1518Octets	0
Bit 1	R	TransmittedFrames512to1023Octets	0
Bit 0	R	TransmittedFrames256to511Octets	0

The MSTAT Counter Rollover Registers provide indication of counter roll over conditions. The register bit remains set until the register is read. Reading this register clears all bits within this register.

Register 0x505H and 0x605H: MSTAT Interrupt Mask 0

Bit	Type	Function	Default
Bit 15	R/W	MASK0[15]	0
Bit 14	R/W	MASK0[14]	0
Bit 13	R/W	MASK0[13]	0
Bit 12	R/W	MASK0[12]	0
Bit 11	R/W	MASK0[11]	0
Bit 10	R/W	MASK0[10]	0
Bit 9	R/W	MASK0[9]	0
Bit 8	R/W	MASK0[8]	0
Bit 7	R/W	MASK0[7]	0
Bit 6	R/W	MASK0[6]	0
Bit 5	R/W	MASK0[5]	0
Bit 4	R/W	MASK0[4]	0
Bit 3	R/W	MASK0[3]	0
Bit 2	R/W	MASK0[2]	0
Bit 1	R/W	MASK0[1]	0
Bit 0	R/W	MASK0[0]	0

The MSTAT Interrupt Mask Registers provide programmable interrupt masking of the MSTAT Counter Rollover Register bits.

MASK[15:0]:

The MASK[15:0] bits are used as a logical mask for each corresponding bit in the **MSTAT Counter Rollover 0** register. If the MASK bit is high (logic 1) the given counter overflow condition in the **MSTAT Counter Rollover 0** register will cause the MSTAT to assert the INTB pin. If the MASK bit is low (logic 0) the corresponding **MSTAT Counter Rollover 0** register bit state has no effect on the INTB pin.

Register 0x506H and 0x606H: MSTAT Interrupt Mask 1

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R/W	MASK1[14]	0
Bit 13	R/W	MASK1[13]	0
Bit 12	R/W	MASK1[12]	0
Bit 11	R/W	MASK1[11]	0
Bit 10	R/W	MASK1[10]	0
Bit 9	R/W	MASK1[9]	0
Bit 8	R/W	MASK1[8]	0
Bit 7	R/W	MASK1[7]	0
Bit 6	R/W	MASK1[6]	0
Bit 5	R/W	MASK1[5]	0
Bit 4	R/W	MASK1[4]	0
Bit 3	R/W	MASK1[3]	0
Bit 2	R/W	MASK1[2]	0
Bit 1	R/W	MASK1[1]	0
Bit 0	R/W	MASK1[0]	0

The MSTAT Interrupt Mask Registers provide programmable interrupt masking of the MSTAT Counter Rollover Register bits.

MASK[14:0]:

The MASK[14:0] bits are used as a logical mask for each corresponding bit in the **MSTAT Counter Rollover 1** register. If the MASK bit is high (logic 1) the given counter overflow condition in the **MSTAT Counter Rollover 1** register will cause the MSTAT to assert the INTB pin. If the MASK bit is low (logic 0) the corresponding **MSTAT Counter Rollover 1** register bit state has no effect on the INTB pin.

Register 0x507H and 0x607H: MSTAT Interrupt Mask 2

Bit	Type	Function	Default
Bit 15	R/W	MASK2[15]	0
Bit 14	R/W	MASK2[14]	0
Bit 13	R/W	MASK2[13]	0
Bit 12	R/W	MASK2[12]	0
Bit 11	R/W	MASK2[11]	0
Bit 10	R/W	MASK2[10]	0
Bit 9	R/W	MASK2[9]	0
Bit 8	R/W	MASK2[8]	0
Bit 7	R/W	MASK2[7]	0
Bit 6	R/W	MASK2[6]	0
Bit 5	R/W	MASK2[5]	0
Bit 4	R/W	MASK2[4]	0
Bit 3	R/W	MASK2[3]	0
Bit 2	R/W	MASK2[2]	0
Bit 1	R/W	MASK2[1]	0
Bit 0	R/W	MASK2[0]	0

The MSTAT Interrupt Mask Registers provide programmable interrupt masking of the MSTAT Counter Rollover Register bits.

MASK2[15:0]:

The MASK2[15:0] bits are used as a logical mask for each corresponding bit in the **MSTAT Counter Rollover 2** register. If the MASK bit is high (logic 1) the given counter overflow condition in the **MSTAT Counter Rollover 2** register will cause the MSTAT to assert the INTB pin. If the MASK bit is low (logic 0) the corresponding **MSTAT Counter Rollover 2** register bit state has no effect on the INTB pin.

Register 0x508H and 0x608H: MSTAT Interrupt Mask 3

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	Reserved	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R/W	MASK3[5]	0
Bit 4	R/W	MASK3[4]	0
Bit 3	R/W	MASK3[3]	0
Bit 2	R/W	MASK3[2]	0
Bit 1	R/W	MASK3[1]	0
Bit 0	R/W	MASK3[0]	0

The MSTAT Interrupt Mask Registers provide programmable interrupt masking of the MSTAT Counter Rollover Register bits.

MASK3[15:0]:

The MASK3[15:0] bits are used as a logical mask for each corresponding bit in the **MSTAT Counter Rollover 3** register. If the MASK bit is high (logic 1) the given counter overflow condition in the **MSTAT Counter Rollover 3** register will cause the MSTAT to assert the INTB pin. If the MASK bit is low (logic 0) the corresponding **MSTAT Counter Rollover 3** register bit state has no effect on the INTB pin.

Register 0x509H,0x609H: MSTAT Counter Write Address

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	Reserved	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R/W	ADDRESS[5]	0
Bit 4	R/W	ADDRESS[4]	0
Bit 3	R/W	ADDRESS[3]	0
Bit 2	R/W	ADDRESS[2]	0
Bit 1	R/W	ADDRESS[1]	0
Bit 0	R/W	ADDRESS[0]	0

The MSTAT Counter Write Address Register provides the write address used during a write operation to the MSTAT counters.

ADDRESS[5:0]:

The ADDRESS[5:0] bits are used as the write address during a write operation to the MSTAT counters. A proper counter address must be written to the MSTAT Counter Write Address prior to initiating a write operation via the WRITE bit in the **MSTAT Control** register. Please refer to Table 28 for the correct counter write address.

Register 0x50AH, 0x60AH: MSTAT Counter Write Data Low

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

The MSTAT Counter Write Data Registers provide the write data used during a write operation to the MSTAT counters. The MSTAT Counter Write Data Registers are partitioned into low, middle, and high register entities.

DATA[15:0]:

The DATA[15:0] bits are used as the write data during a write operation to the MSTAT counters. The proper counter data must be written to the MSTAT Counter Write Data Register prior to initiating a write operation via the WRITE bit in the **MSTAT Control** register.

Register 0x50BH, 0x60BH: MSTAT Counter Write Data Middle

Bit	Type	Function	Default
Bit 15	R/W	DATA[31]	0
Bit 14	R/W	DATA[30]	0
Bit 13	R/W	DATA[29]	0
Bit 12	R/W	DATA[28]	0
Bit 11	R/W	DATA[27]	0
Bit 10	R/W	DATA[26]	0
Bit 9	R/W	DATA[25]	0
Bit 8	R/W	DATA[24]	0
Bit 7	R/W	DATA[23]	0
Bit 6	R/W	DATA[22]	0
Bit 5	R/W	DATA[21]	0
Bit 4	R/W	DATA[20]	0
Bit 3	R/W	DATA[19]	0
Bit 2	R/W	DATA[18]	0
Bit 1	R/W	DATA[17]	0
Bit 0	R/W	DATA[16]	0

The MSTAT Counter Write Data Registers provide the write data used during a write operation to the MSTAT counters. The MSTAT Counter Write Data Registers are partitioned into low, middle, and high register entities.

DATA[31:16]:

The DATA[15:0] bits are used as the write data during a write operation to the MSTAT counters. The proper counter data must be written to the MSTAT Counter Write Data Register prior to initiating a write operation via the WRITE bit in the **MSTAT Control** register.

Register 0x50CH, 0x60CH: MSTAT Counter Write Data High

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	Reserved	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R/W	DATA[39]	0
Bit 6	R/W	DATA[38]	0
Bit 5	R/W	DATA[37]	0
Bit 4	R/W	DATA[36]	0
Bit 3	R/W	DATA[35]	0
Bit 2	R/W	DATA[34]	0
Bit 1	R/W	DATA[33]	0
Bit 0	R/W	DATA[32]	0

The MSTAT Counter Write Data Registers provide the write data used during a write operation to the MSTAT counters. The MSTAT Counter Write Data Registers are partitioned into low, middle, and high register entities.

DATA[39:32]:

The DATA[39:32] bits are used as the write data during a write operation to the MSTAT counters. The proper counter data must be written to the MSTAT Counter Write Data Register prior to initiating a write operation via the WRITE bit in the **MSTAT Control** register.

Register 0x510H to 0x58AH: MSTAT0 Receive Statistical Counters

Bit	Type	Function	Default
Bit 39:0	R/W	COUNT[39:0]	0

The MSTAT Statistical Counters are defined in Table 12. The MSTAT Statistical Counters are 40 bits. The MSTAT Statistical Counters represent the individual counters split between high, middle, and low registers. The low register contains bits 15:0, the middle register contains bits 31:16, and the high register contains bits 39:32 as well as 8 unused or reserved bits in the MSB of the high register. Please see Table 28 for a description of each counter.

COUNT[39:0]:

The COUNT[39:0] bits are used as the 40 bit counter.

Register 0x590H to 0x5E6H: MSTAT0 Transmit Statistical Counters

Bit	Type	Function	Default
Bit 39:0	R/W	COUNT[39:0]	0

The MSTAT Statistical Counters are defined in Table 12. The MSTAT Statistical Counters are 40 bits. The MSTAT Statistical Counters represent the individual counters split between high, middle, and low registers. The low register contains bits 15:0, the middle register contains bits 31:16, and the high register contains bits 39:32 as well as 8 unused or reserved bits in the MSB of the high register. Please see Table 28 for a description of each counter.

COUNT[39:0]:

The COUNT[39:0] bits are used as the 40 bit counter.

Register 0x610H to 0x68AH: MSTAT1 Receive Statistical Counters

Bit	Type	Function	Default
Bit 39:0	R/W	COUNT[39:0]	0

The MSTAT Statistical Counters are defined in Table 12. The MSTAT Statistical Counters are 40 bits. The MSTAT Statistical Counters represent the individual counters split between high, middle, and low registers. The low register contains bits 15:0, the middle register contains bits 31:16, and the high register contains bits 39:32 as well as 8 unused or reserved bits in the MSB of the high register. Please see Table 28 for a description of each counter.

COUNT[39:0]:

The COUNT[39:0] bits are used as the 40 bit counter.

Register 0x690H to 0x6E6H: MSTAT1 Transmit Statistical Counters

Bit	Type	Function	Default
Bit 39:0	R/W	COUNT[39:0]	0

The MSTAT Statistical Counters are defined in Table 12. The MSTAT Statistical Counters are 40 bits. The MSTAT Statistical Counters represent the individual counters split between high, middle, and low registers. The low register contains bits 15:0, the middle register contains bits 31:16, and the high register contains bits 39:32 as well as 8 unused or reserved bits in the MSB of the high register. Please see Table 28 for a description of each counter.

COUNT[39:0]:

The COUNT[39:0] bits are used as the 40 bit counter.

The following table presents a description of the count contained within the respective receive or transmit statistical counter.

Table 28 MSTAT Counter Description

MSTAT Counter Registers			
Read Address			
Channel 0	Channel 1		
0x510	0x610	Low	FramesReceivedOK Contains a count of frames that are successfully received. This does not include frames received that are classified under: FrameCheckSequenceErrors, FramesLostDueToInternalMACError, SymbolError, InRangeLengthErrors, OutofRangeLengthErrors, FramesTooLongErrors, Jabbers, Fragments, or UndersizedFrames. MSTAT Counter Write Address = 0x0
0x511	0x611	Mid	
0x512	0x612	High	

0x514	0x614	Low	OctetsReceivedOK Contains a count of data and padding octets in frames (not including Preamble, SFD, destination/source address, type/length field, Q-Tag prefix or FCS) that are successfully received. This does not include octets in frames received that are classified under: FrameCheckSequenceErrors, FramesLostDueToInternalMACError, SymbolError, InRangeLengthErrors, OutofRangeLengthErrors, FramesTooLongErrors, Jabbers, Fragments, or UndersizedFrames. ifInOctets (MIB-II) can be computed using the following: ifInOctets = OctetsReceivedOK + (18 * FramesReceivedOK) + (TaggedFramesReceivedOK * 4) ifInOctets includes the count of data, padding, destination/source address, length/type field, Q-Tag prefix, and FCS. (excludes preamble and SFD). MSTAT Counter Write Address = 0x1
0x515	0x615	Mid	
0x516	0x616	High	
0x518	0x618	Low	FramesReceived The total number of frames (including bad frames, unicast frames, broadcast frames, and multicast frames) received. This count includes those frames of Jumbo Size. MSTAT Counter Write Address = 0x2
0x519	0x619	Mid	
0x51A	0x61A	High	
0x51C	0x61C	Low	OctetsReceived The total number of octets of data (including those in bad frames) received (excluding framing bits but including FCS octets). This includes the count of bytes from the first byte of the Destination address to the last byte of the FCS field. MSTAT Counter Write Address = 0x3
0x51D	0x61D	Mid	
0x51E	0x61E	High	

0x520	0x620	Low	UnicastFramesReceivedOK Contains a count of frames that are successfully received and are directed to a unicast group address. This does not include octets in frames received that are classified under: FrameCheckSequenceErrors, FramesLostDueToInternalMACError, SymbolError, InRangeLengthErrors, OutofRangeLengthErrors, FramesTooLongErrors, Jabbers, Fragments, or UndersizedFrames. MSTAT Counter Write Address = 0x4
0x521	0x621	Mid	
0x522	0x622	High	
0x524	0x624	Low	MulticastFramesReceivedOK Contains count of frames that are successfully received and are directed to a multicast group address. This counter will not increment for frames classified as unicast or broadcast. This does not include frames received that are classified under: FrameCheckSequenceErrors, FramesLostDueToInternalMACError, SymbolError, InRangeLengthErrors, OutofRangeLengthErrors, FramesTooLongErrors, Jabbers, Fragments, or UndersizedFrames. MSTAT Counter Write Address = 0x5
0x525	0x625	Mid	
0x526	0x626	High	
0x528	0x628	Low	BroadcastFramesReceivedOK Contains a count of frames that are successfully received and are directed to the broadcast group address. This counter will not increment for frames classified as unicast or multicast. This does not include frames received that are classified under: FrameCheckSequenceErrors, FramesLostDueToInternalMACError, SymbolError, InRangeLengthErrors, OutofRangeLengthErrors, FramesTooLongErrors, Jabbers, Fragments, or UndersizedFrames. MSTAT Counter Write Address = 0x6
0x529	0x629	Mid	
0x52A	0x62A	High	

0x52C	0x62C	Low	TaggedFramesReceivedOK Contains a count of tagged frames that are successfully received. This does not include tagged frames received that are classified under: FrameCheckSequenceErrors, FramesLostDueToInternalMACError, SymbolError, InRangeLengthErrors, OutofRangeLengthErrors, FramesTooLongErrors, Jabbers, Fragments, or UndersizedFrames. MSTAT Counter Write Address = 0x7
0x52D	0x62D	Mid	
0x52E	0x62E	High	
0x530	0x630	Low	PAUSEMACControlFrameReceived Contains a count of MAC Control frames passed by the MAC sublayer to the MAC Control sublayer. This counter is incremented when a ReceiveFrame function call returns a valid frame with: (1) A lengthOrType field value equal to the reserved Type for 802.3_MAC_Control as specified in 802.3-1998 (31.4.1.3), and (2) An opcode indicating the PAUSE operation. This does not include frames received that are classified under: FrameCheckSequenceErrors, FramesLostDueToInternalMACError, SymbolError, InRangeLengthErrors, OutofRangeLengthErrors, FramesTooLongErrors, Jabbers, Fragments, or UndersizedFrames. MSTAT Counter Write Address = 0x8
0x531	0x631	Mid	
0x532	0x632	High	

0x534	0x634	Low	MACControlFrameReceived Contains a count of MAC Control frames passed by the MAC sublayer to the MAC Control sublayer. This counter is incremented when a ReceiveFrame function call returns a valid frame with: (1) a lengthOrType field value equal to the reserved Type for 802.3_MAC_Control as specified in 802.3-1998 (31.4.1.3). This does not include frames received that are classified under: FrameCheckSequenceErrors, FramesLostDueToInternalMACError, SymbolError, InRangeLengthErrors, OutofRangeLengthErrors, FramesTooLongErrors, Jabbers, Fragments, or UndersizedFrames. MSTAT Counter Write Address = 0x9
0x535	0x635	Mid	
0x536	0x636	High	
0x538	0x638	Low	FrameCheckSequenceErrors Contains a count of receive frames that are an integral number of octets in length and do not pass the FCS check. This does not include frames received that are too long(jabbers), or too short (fragments). MSTAT Counter Write Address = 0xA
0x539	0x639	Mid	
0x53A	0x63A	High	
0x53C	0x63C	Low	FramesLostDueToInternalMACError Contains a count of frames that would otherwise be received by the device, but could not be accepted due to an internal MAC sublayer receive error (I.E. FIFO overrun). If this counter is incremented, then none of the other error counters in this section are incremented. MSTAT Counter Write Address = 0xB
0x53D	0x63D	Mid	
0x53E	0x63E	High	
0x540	0x640	Low	SymbolError A count of the number of times when valid length frame was received at the port and during which time there was at least one occurrence of an event that causes the PHY to indicate “Data reception error” or invalid “Data symbol error.” This counter shall be incremented only once per valid CarrierEvent. MSTAT Counter Write Address = 0xC
0x541	0x641	Mid	
0x542	0x642	High	

0x544	0x644	Low	InRangeLengthErrors Contains a count of frames with a length/type field value between 46 and 1500 that does not match the number of MAC client data octets received. The counter also increments for frames whose length/type field value is from 0 to 45 regardless of the number of MAC client data octets received. MSTAT Counter Write Address = 0xD
0x545	0x645	Mid	
0x546	0x646	High	
0x54C	0x64C	Low	FramesTooLongErrors Contains a count of frames received that exceed the maximum permitted frame size and have no other errors. This counter is aware of both tagged and non tagged frames as well as frames of Jumbo size. MSTAT Counter Write Address = 0xF
0x54D	0x64D	Mid	
0x54E	0x64E	High	
0x550	0x650	Low	Jabbers Contains a count of the total number of frames received that were longer than the maximum permitted frame size and had a bad Frame Check Sequence (FCS). MSTAT Counter Write Address = 0x10
0x551	0x651	Mid	
0x552	0x652	High	
0x554	0x654	Low	Fragments The total number of frames received that were less than minimum permitted frame size (64 octets long excluding framing bits, but including FCS octets) and had a bad frame check sequence (FCS). MSTAT Counter Write Address = 0x11
0x555	0x655	Mid	
0x556	0x656	High	
0x558	0x658	Low	UndersizedFrames The total number of frames received that were less than the minimum permitted frame size (64 octets long excluding framing bits, but including FCS octets) and were otherwise well formed. MSTAT Counter Write Address = 0x12
0x559	0x659	Mid	
0x55A	0x65A	High	
0x55C	0x65C	Low	ReceiveFrames64Octets The total number of frames (including bad frames) received that were 64 octets in length (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x13
0x55D	0x65D	Mid	
0x55E	0x65E	High	

0x560	0x660	Low	ReceiveFrames65to127Octets The total number of frames (including bad frames) received that were between 65 and 127 octets in length inclusive (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x14
0x561	0x661	Mid	
0x562	0x662	High	
0x564	0x664	Low	ReceiveFrames128to255Octets The total number of frames (including bad frames) received that were between 128 and 255 octets in length inclusive (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x15
0x565	0x665	Mid	
0x566	0x666	High	
0x568	0x668	Low	ReceiveFrames256to511Octets The total number of frames (including bad frames) received that were between 256 and 511 octets in length inclusive (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x16
0x569	0x669	Mid	
0x56A	0x66A	High	
0x56C	0x66C	Low	ReceiveFrames512to1023Octets The total number of frames (including bad frames) received that were between 512 and 1023 octets in length inclusive (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x17
0x56D	0x66D	Mid	
0x56E	0x66E	High	
0x570	0x670	Low	ReceiveFrames1024to1518Octets The total number of frames (including bad frames) received that were between 1024 and (1518 octets for untagged frames and 1522 octets for VLAN tagged frames) in length inclusive (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x18
0x571	0x671	Mid	
0x572	0x672	High	

0x574	0x674	Low	ReceiveFrames1519toMAXOctets The total number of frames (including bad frames) received that were between the maximum normal frame lengths (1518 octets for untagged frames and 1522 octets for tagged frames) and maximum Jumbo frame lengths (i.e. 9600 octets) (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x19
0x575	0x675	Mid	
0x576	0x676	High	
0x578	0x678	Low	JumboOctetsReceivedOK The total number of octets received in frames (excluding bad frames) received that were between the maximum normal frame lengths (1518 octets for untagged frames and 1522 octets for tagged frames) and maximum Jumbo frame lengths (i.e. up to MaxFrameSize) (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x1A
0x579	0x679	Mid	
0x57A	0x67A	High	
0x57C	0x67C	Low	FilteredOctets The total number of octets that would normally be passed to the link that are dropped because of filtering rules. MSTAT Counter Write Address = 0x1B
0x57D	0x67D	Mid	
0x57E	0x67E	High	
0x580	0x680	Low	FilteredUnicastFrames The total number of Unicast classified fames that would normally be passed to the link that are dropped because of filtering rules. MSTAT Counter Write Address = 0x1C
0x581	0x681	Mid	
0x582	0x682	High	
0x584	0x684	Low	FilteredMulticastFrames The total number of Multicast frames that would normally be passed to the link that are dropped because of filtering rules. MSTAT Counter Write Address = 0x1D
0x585	0x685	Mid	
0x586	0x686	High	
0x588	0x688	Low	FilteredBroadcastFrames The total number of Broadcast frames that would normally be passed to the link that are dropped because of filtering rules. MSTAT Counter Write Address = 0x1E
0x589	0x689	Mid	
0x58A	0x68A	High	

0x590	0x690	Low	FramesTransmittedOK Contains the count of frames that are successfully transmitted over the MAC interface. MSTAT Counter Write Address = 0x20
0x591	0x691	Mid	
0x592	0x692	High	
0x594	0x694	Low	OctetsTransmittedOK Contains a count of data and padding (excluding preamble, SFD, destination/source address, length/type field, Q-Tag prefix, and FCS) octets of frames that are successfully transmitted over the MAC interface. ifOutOctets (MIB-II) can be computed using the following: ifOutOctets = OctetsTransmittedOK + JumboOctetsTransmittedOK + (18 * FramesTransmittedOK) + (TaggedFramesTransmittedOK * 4) ifOutOctets includes the count of data, padding, destination/source address, length/type field, Q-Tag prefix, and FCS. (excludes preamble and SFD). MSTAT Counter Write Address = 0x21
0x595	0x695	Mid	
0x596	0x696	High	
0x598	0x698	Low	OctetsTransmitted Contains a count of data and padding (excluding preamble, SFD, destination/source address, length/type field, Q-Tag prefix, and FCS) octets of frames that are attempted to be transmitted over the MAC interface. MSTAT Counter Write Address = 0x22
0x599	0x699	Mid	
0x59A	0x69A	High	
0x59C	0x69C	Low	FramesLostDueToInternalMACTransmissionError Contains a count of frames that would otherwise be transmitted by the device but could not be sent correctly because of : a) A MAC FIFO underrun. b) A POS-PHY Level 3 TERR signal assertion on the last word of the current frame without any further immediately following frames. If this counter is incremented, then none of the other error counters in this section are incremented. MSTAT Counter Write Address = 0x23
0x59D	0x69D	Mid	
0x59E	0x69E	High	

0x5A0	0x6A0	Low	TransmitSystemError Contains a count of frames that would otherwise be transmitted by the device, but could not be sent due to an indication from the POS-PHY Level 3 TERR signal being asserted(other than that already counted by FramesLostDueToInternalMACTransmissionError), an oversize frame being transmitted, or an internal CRC error discovered that was generated from the upstream device. If this counter is incremented, then none of the other error counters in this section are incremented. MSTAT Counter Write Address = 0x24
0x5A1	0x6A1	Mid	
0x5A2	0x6A2	High	
0x5A4	0x6A4	Low	UnicastFramesTransmittedAttempted Contains a count of frames that are requested to be transmitted to a group unicast destination address. This count includes those frames that were discarded or not sent. MSTAT Counter Write Address = 0x25
0x5A5	0x6A5	Mid	
0x5A6	0x6A6	High	
0x5A8	0x6A8	Low	UnicastFramesTransmittedOK Contains a count of frames that are successfully transmitted via the MAC interface to a group unicast destination address. MSTAT Counter Write Address = 0x26
0x5A9	0x6A9	Mid	
0x5AA	0x6AA	High	
0x5AC	0x6AC	Low	MulticastFramesTransmittedAttempted Contains a count of frames that are requested to be transmitted to a group multicast destination address. This count includes those frames that were discarded or not sent. This count is not updated by broadcast frame transmission. MSTAT Counter Write Address = 0x27
0x5AD	0x6AD	Mid	
0x5AE	0x6AE	High	
0x5B0	0x6B0	Low	MulticastFramesTransmittedOK Contains a count of frames that are successfully transmitted to a group multicast destination. This count is not updated by broadcast frame transmission. MSTAT Counter Write Address = 0x28
0x5B1	0x6B1	Mid	
0x5B2	0x6B2	High	

0x5B4	0x6B4	Low	BroadcastFramesTransmittedAttempted Contains a count of the frames that were requested to be transmitted to a broadcast address. This count includes those frames that were discarded or not sent. This count is not updated by multicast frame transmission. MSTAT Counter Write Address = 0x29
0x5B5	0x6B5	Mid	
0x5B6	0x6B6	High	
0x5B8	0x6B8	Low	BroadcastFramesTransmittedOK Contains a count of the frames that were successfully transmitted to the broadcast address. This count is not updated by multicast frame transmission. MSTAT Counter Write Address = 0x2A
0x5B9	0x6B9	Mid	
0x5BA	0x6BA	High	
0x5BC	0x6BC	Low	PAUSEMACCTRLFramesTransmitted Contains a count of PAUSE frames passed to the MAC sublayer for transmission. This counter is incremented when a request to send the PAUSE control frame is generated. MSTAT Counter Write Address = 0x2B
0x5BD	0x6BD	Mid	
0x5BE	0x6BE	High	
0x5C0	0x6C0	Low	MACCTRLFramesTransmitted Contains a count of frames passed to the MAC sublayer for transmission. This counter is incremented when a control frame is transmitted out of the MAC. MSTAT Counter Write Address = 0x2C
0x5C1	0x6C1	Mid	
0x5C2	0x6C2	High	
0x5C4	0x6C4	Low	TransmittedFrames64Octets The total number of frames (including bad frames) transmitted that were 64 octets in length (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x2D
0x5C5	0x6C5	Mid	
0x5C6	0x6C6	High	
0x5C8	0x6C8	Low	TransmittedFrames65to127Octets The total number of frames (including bad frames) transmitted that were between 65 and 127 octets in length inclusive (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x2E
0x5C9	0x6C9	Mid	
0x5CA	0x6CA	High	

0x5CC	0x6CC	Low	TransmittedFrames128to255Octets The total number of frames (including bad frames) transmitted that were between 128 and 255 octets in length inclusive (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x2F
0x5CD	0x6CD	Mid	
0x5CE	0x6CE	High	
0x5D0	0x6D0	Low	TransmittedFrames256to511Octets The total number of frames (including bad frames) transmitted that were between 256 and 511 octets in length inclusive (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x30
0x5D1	0x6D1	Mid	
0x5D2	0x6D2	High	
0x5D4	0x6D4	Low	TransmittedFrames512to1023Octets The total number of frames (including bad frames) transmitted that were between 512 and 1023 octets in length inclusive (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x31
0x5D5	0x6D5	Mid	
0x5D6	0x6D6	High	
0x5D8	0x6D8	Low	TransmittedFrames1024to1518Octets The total number of frames (including bad frames) transmitted that were between 1024 and (1518 octets for untagged frames and 1522 octets for VLAN tagged frames) in length inclusive (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x32
0x5D9	0x6D9	Mid	
0x5DA	0x6DA	High	
0x5DC	0x6DC	Low	TransmittedFrames1519toMAXOctets The total number of frames (including bad frames) transmitted that were between the normal maximum length (1518 octets for un-tagged frames and 1522 octets for tagged frames) and the max Jumbo frame length (i.e. up to MaxFrameSize) (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x33
0x5DD	0x6DD	Mid	
0x5DE	0x6DE	High	

0x5E0	0x6E0	Low	JumboOctetsTransmittedOK The total number of octets (excluding bad frames) transmitted that were between the normal maximum length (1518 octets for un-tagged frames and 1522 octets for tagged frames) and the max Jumbo frame length (i.e. up to MaxFrameSize) (excluding framing bits but including FCS octets). MSTAT Counter Write Address = 0x34
0x5E1	0x6E1	Mid	
0x5E2	0x6E2	High	

Register 0x700H: SERDES Lock Detect Change

Bit	Type	Function	Default
Bit 15	R	TX_ROOL_INT	0
Bit 14:10	R	Reserved	0
Bit 9	R	RX_ROOL_INT[1]	0
Bit 8	R	RX_ROOL_INT[0]	0
Bit 7:2	R	Reserved	0
Bit 1	R	RX_DOOL_INT[1]	0
Bit 0	R	RX_DOOL_INT[0]	0

Indicates whether the values of the TX_ROOL, RX_ROOL0, RX_ROOL1, RX_DOOL0, or RX_DOOL1 status bits within the **Reference Out of Lock** and **Data Out of Lock Status** registers have changed since the previous read from the SERDES Lock Detect Change register. An interrupt request (ROOL_INT or DOOL_INT) to the top level of the device will be asserted when any pair of corresponding bits in the Lock Detect Change and Lock Detect Mask registers are both set to logic 1. This in turn will assert the device INTB pin.

RX_DOOL_INT[1:0]

The Receive Data Out Of Lock condition has changed. RX_DOOL_INT[1:0] bits are set to logic 1 when the value of the corresponding RX_DOOL0 and/or RX_DOOL1 status bits in the **Data Out of Lock Status** register changes state. RX_DOOL_INT[1:0] is cleared to logic "00" by a read from the SERDES Lock Detect Change register.

RX_ROOL_INT[1:0]

The Receive Reference Out Of Lock condition has changed. RX_ROOL_INT[1:0] bits are set to logic 1 when the value of the corresponding RX_ROOL0 and/or RX_ROOL1 status bits in the **Reference Out of Lock Status** register changes state. RX_ROOL_INT[1:0] is cleared to logic "00" by a read from the SERDES Lock Detect Change register.

TX_ROOL_INT

The Transmit Reference Out Of Lock condition has changed. TX_ROOL_INT is set to logic 1 when the corresponding TX_ROOL status bit in the **Reference Out of Lock Status** register changes state. TX_ROOL_INT is cleared to logic 0 by a read from the SERDES Lock Detect Change register.

Register 0x701H: SERDES Lock Detect Mask

Bit	Type	Function	Default
Bit 15	R/W	TX_ROOL_MASK	0
Bit 14:10	R	Reserved	0
Bit 9	R/W	RX_ROOL_MASK[1]	0
Bit 8	R/W	RX_ROOL_MASK[0]	0
Bit 7:2	R	Reserved	0
Bit 1	R/W	RX_DOOL_MASK[1]	0
Bit 0	R/W	RX_DOOL_MASK[0]	0

Arms the SERDES interrupt requests (ROOL_INT and DOOL_INT) when any pair of corresponding bits in the **SERDES Lock Detect Change** and SERDES Lock Detect Mask registers are both set to logic 1.

RX_DOOL_MASK[1:0]

Enables the triggering of DOOL_INT. The DOOL_INT signal is asserted when any pair of corresponding RX_DOOL_INT[1:0] bits in the **SERDES Lock Detect Change** and SERDES Lock Detect Mask registers are both set to logic 1.

RX_ROOL_MASK[1:0]

Enables the triggering of ROOL_INT. The ROOL_INT signal is asserted when any pair of corresponding RX_ROOL_INT[1:0] bits in the **SERDES Lock Detect Change** and SERDES Lock Detect Mask registers are both set to logic 1.

TX_ROOL_MASK

Enables the triggering of ROOL_INT. The ROOL_INT signal is asserted when the TX_ROOL_INT bits in the **SERDES Lock Detect Change** register and SERDES Lock Detect Mask registers are both set to logic 1.

Register 0x703H, 0x713H: SERDES Port Configuration

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	ENABLE	P
Bit 11:7	R	Reserved	0
Bit 6	R/W	SDSEL	0
Bit 5	R/W	RXSEL	0
Bit 4	R/W	Reserved	0
Bit 3:2	R	Reserved	0
Bit 1	R/W	TXSEL[1]	0
Bit 0	R/W	TXSEL[0]	P

Specifies the requested configuration of the SERDES port. In normal operation the SERDES control logic will sequence the internal SERDES components toward the configuration specified in this register.

TXSEL[1:0]

Selects the source of the 10 bit parallel data stream for the transmit section.

00 None
01 MAC transmit data stream (TDS[9:0])
10 Reserved
11 FIFO read data stream
– enables line-side (remote) loopback

TXSEL[1] is cleared to logic 0 when RESETB is asserted.
TXSEL[0] is loaded from the (inverted) PMD_SEL pin when reset is asserted.

RXSEL

Selects the source of the serial data stream for the receive section.

0 RXD input
1 PISO output
– enables system-side (local) loopback

SDSEL

Selects the source for the Signal Detect (SDET) signal to the MAC.

0 CRU lock detect logic
1 RXSD input or PISO output, depending on RXSEL value.

ENABLE

When ENABLE is set to logic 1 normal operation of the port is enabled.

Register 0x704H, 0x714H: SERDES Port RX Mode

Bit	Type	Function	Default
Bit 15	R/W	FORCE	0
Bit 14	R	Reserved	0
Bit 13	R/W	Reserved	C
Bit 12	R/W	Reserved	C
Bit 11	R/W	RXSD	P
Bit 10:0	R	Reserved	0

Provides the ability to observe and coerce the control interface to the PECL RX. In normal operation there is no need to reference this register. It is provided for diagnostic purposes.

RXSD

When RXSD is cleared to logic 0 processing of the RXD data stream is disabled.

When FORCE is set to logic 1 the RXSD signal is driven from this bit, otherwise it is driven from the RXSD pin.

FORCE

When FORCE is set to logic 1 the IDDQ, ENABLE and RXSD bits are written from the ECBI register write, otherwise writes to these bits are ignored. For normal operation FORCE should be cleared to logic 0.

Register 0x705H, 0x715H: SERDES Port TX Mode

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14:13	R	Reserved	0
Bit 12	R/W	Reserved	C
Bit 11	R/W	TXHIGH	0
Bit 10:3	R	Reserved	0
Bit 2	R/W	Reserved	1
Bit 1	R/W	MODE[1]	0
Bit 0	R/W	MODE[0]	0

Provides the ability to observe and coerce the control interface to the PECL TX. In normal operation there is no need to reference this register. It is provided for diagnostic purposes.

MODE[1:0]

Selects the bias current for the PECL TX.

00 30.5 mA (nominal) PECL
01 16.0 mA (nominal) CML
10 Unsupported
11 Unsupported

TXHIGH

When TXHIGH is set to logic 0 the TX_ENx output pin is active low. When TXHIGH is set to logic 1 the TX_ENx output pin is active high.

Register 0x708H, 0x718H: SERDES Port CRU Mode

Bit	Type	Function	Default
Bit 15	R/W	FORCE	0
Bit 14	R/W	RESET	C
Bit 13	R/W	Reserved	C
Bit 12	R/W	ENABLE	C
Bit 11	R/W	LOCKED	S
Bit 10	R/W	ALIGNED	S
Bit 9	R	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	MODE[7]	C
Bit 6	R/W	MODE[6]	1
Bit 5	R/W	MODE[5]	0
Bit 4	R/W	MODE[4]	0
Bit 3	R/W	MODE[3]	0
Bit 2	R/W	MODE[2]	C
Bit 1	R	MODE[1]	0
Bit 0	R	MODE[0]	1

Provides the ability to observe and coerce the control interface to the CRU. In normal operation there is no need to reference this register. It is provided for diagnostic purposes.

MODE[1:0]

These bits are currently unused.
MODE[1:0] is always read as logic "01".

MODE[2]

Selects the input to the phase / frequency comparator for the CRU.

0 Serial data input selected
1 Reference input
– used for CRU training

When FORCE is set to logic 1 the MODE[2] signal to the PISO is driven from this bit, otherwise it is driven from SERDES control logic.

In normal operation MODE[2] is cleared to logic 0 when:
LOCKED is set to logic 1 and
RXSD is set to logic 1 or RXSEL is set to logic 1,
and it is set to logic 1 otherwise.

The CRU requires up to 200 µs to acquire data alignment after MODE[2] is cleared to logic 0 and a valid 8B/10B encoded input data stream is present.

MODE[2] is set to logic 1 when RESETB is asserted.

MODE[4:3]

Controls the CRU narrowbanding feature. Upon initialization 10 must be written to MODE[4:3].

00	Unsupported
01	Unsupported
10	Enable V2I DC Path Current, Enable Offset Current
11	Unsupported

MODE[4:3] is set to logic "00" when RESETB is asserted. It must be set to 10 via register write prior to normal operation.

MODE[6:5]

Selects the loop filter resistance for the CRU.

00	Unsupported
01	Unsupported
10	2.5 KΩ (nominal)
11	Unsupported

MODE[6:5] is set to logic "10" when reset is asserted.

MODE[7]

Selects the source of the serial data stream for the CRU.

0	PISO output – used for CRU training and system-side (local) loopback
1	RXD input

When FORCE is set to logic 1 the MODE[7] signal to the PISO is driven from this bit, otherwise it is driven from SERDES control logic.

In normal operation MODE[7] is loaded from RXSEL when MODE[2] is cleared to logic 0 and it is cleared to logic 0 otherwise.

ALIGNED

The receive clock is aligned to the incoming data stream.

When FORCE is set to logic 1 the ALIGNED signal is driven from this bit, otherwise it is driven from SERDES control logic.

In normal operation ALIGNED is set to logic 1 when:
MODE[2] is cleared to logic 0 and
the TRAN bit in the SIPO Mode register is set to logic 1 and
the recovered CRU clock is within +/-330 ppm (nominal) of the reference frequency,
and it is cleared to logic 0 otherwise.

LOCKED

The receive clock is locked to the reference frequency.

When FORCE is set to logic 1 the LOCKED signal is driven from this bit, otherwise it is driven from SERDES control logic.

In normal operation LOCKED is set to logic 1 when:
the recovered CRU clock is within +/-60 ppm (nominal) of the reference frequency or MODE[2] is cleared to logic 0 and the recovered CRU clock is within +/-330 ppm (nominal) of the reference frequency,
and it is cleared to logic 0 otherwise.

ENABLE

When ENABLE is set to logic 1 the ENB signal to the CRU is asserted.

When ENB is de-asserted the CRU is forced into low power configuration. While ARSTB is asserted ENB must be asserted to properly initialize the CRU. The CRU requires 1 ms to acquire frequency lock after ENB is asserted with ARSTB de-asserted.

When FORCE is set to logic 1 the ENB signal to the CRU is driven from this bit, otherwise it is driven from SERDES control logic.

RESET

When RESET is set to logic 1 the ARSTB signal to the CRU is asserted.

ARSTB must be asserted for 1 ms with IDDQ de-asserted and ENB asserted to properly reset the CRU. The CRU requires 1 ms to acquire frequency lock after ARSTB is deasserted with ENB asserted.

When FORCE is set to logic 1 the ARSTB signal to the CRU is driven from this bit, otherwise it is driven from the ARSTB input to the SERDES.

FORCE

When FORCE is set to logic 1 the RESET, IDDQ, ENABLE, LOCKED, ALIGNED, MODE[7] and MODE[2] bits are written from the ECBI register write, otherwise writes to these bits are ignored. For normal operation FORCE should be cleared to logic 0.

12 TEST FEATURES DESCRIPTION

Simultaneously asserting (low) the CSB, RDB and WRB inputs causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

In addition, the PM3386 also supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port for use in board testing. All digital device inputs may be read and all digital device outputs may be forced via the JTAG test port.

12.1 JTAG Test Port

The PM3386 JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Table 29 - Instruction Register

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Table 30 - Identification Register

Length	32 bits
Version number	0H
Part Number	3386H
Manufacturer's identification code	0CDH
Device identification	033860CDH

13 OPERATION

In the following discussion general terms are used to describe how the PM3386 may be configured.

13.1 Power on Sequence

The PM3386 uses six separate power sources VDDQ, VDDO, VDDI, AVDQ, AVDH, and AVDL. The PM3386 shares a single ground VSS. Analog power AVDQ, AVDH and AVDL must be connected to properly decoupled independent +3.3V and +1.8V DC supplies respectively. The power-on sequence is as follows.

Power to AVDQ and AVDH must be either applied simultaneously or that AVDQ be applied before AVDH. AVDL must come up before or simultaneously with AVDH.

Power to VDDQ and VDDO must be either applied simultaneously or that VDDQ be applied before VDDO. VDDI must come up after or simultaneously with VDDO.

VDDI and AVDL may have power supplied simultaneously. VDDO and AVDH may have power supplied simultaneously.

13.2 System Reset

System reset for the PM3386 is accomplished via the RSTB pin. RSTB has a minimum reset pulse width of 1 ms. Prior to the de-assertion of RSTB the PMD_SEL pins must be in a stable state(strapped high or low) and all clocks for the device are required to be present for a minimum of 1ms. Internally when the RSTB signal is de-asserted the analog portion of the device will start to lock on to the various reference clocks. The digital portion of the device will be held in reset for 10 ms more by an internal timer. System status of analog training and progress can be viewed via the top level **Device Status** register.

The system programmer may also elect to reset the PM3386 via software commands. This is accomplished by writing to the **Reset Control** register. The programmer is to write both the ARESETB and DRESETB to a 0. This asserts software reset. The programmer must pause no less than 1ms (there is no upper limit) then de-assert ARESETB by writing to the **Reset Control** register ARESETB bit with a 1. The programmer is to wait no less than 10ms (there is no upper limit) then de-assert DRESETB by writing to the **Reset Control** register DRESETB bit with a 1. As with assertion of the RSTB pin the programmer must

also insure that the PMD_SEL pins are in a stable state(strapped high or low) and all clocks for the device are present for a minimum of 1ms prior to initiating a software reset sequence.

The internal digital reset delay may be overwritten using the DIS_STRETCH bit within the Reset Control register. This can be accomplished after a RSTB pin reset sequence and is not necessary when under software reset control.

Note that the internal 10ms digital reset delay timer is only initiated after an appropriate RSTB pin reset sequence. Asserting software reset via ARESETB or DRESETB will not properly sequence the delay timer.

13.3 GMII vs. SERDES Configuration

Each port within the PM3386 can be configured to use either the GMII or SERDES interfaces. The PMD_SEL0 and PMD_SEL1 pins are used for this purpose. Note that each port can be configured independently of the other. By tying the PMD_SELx pin to ground the device port will be placed in SERDES mode. By tying the PMD_SELx pin to 3.3v power the device port will be placed in GMII mode.

13.4 System Clocking

13.4.1 PHY-Link Frequency Selection

The POS-PHY Level 3 bus (RFCLK and TFCLK) may be clocked from 60 to 104MHz. For two channel operation to allow for full bandwidth it is suggested that the bus be clocked at 104MHz. For single channel operation to allow for full bandwidth it is suggested that the bus be clocked at 75 MHz or greater.

RFCLK and TFCLK go to separate clock domains within the PM3386. It is allowable for the system integrator to use the same or separate clock sources for both the RFCLK and TFCLK.

RFCLK and TFCLK must be present during both GMII and SERDES mode of operation.

13.4.2 GMII Mode Clocking

In GMII mode the PM3386 requires 3 separate clock inputs for proper operation. The RX_CLK0 and RX_CLK1 must be present for their respective PHY devices. The CLK125 must be present and valid from the clock generation source. The PM3386 will provide GTX_CLK0 and GTX_CLK1 that is properly aligned to the TXD0[7:0] and TXD1[7:0] data busses respectively. GTX_CLK0 and GTX_CLK1

are derived from the CLK125 input. Please see 13.6 for an example of this configuration.

13.4.3 SERDES Mode Clocking

During SERDES mode the PM3386 requires only one clock source. CLK125 must be supplied from a reliable source. Note that it is possible to have one channel in SERDES mode and one channel in GMII mode. In this case the PM3386 shares the CLK125 input for both channels. The GMII mode port must still receive the RX_CLKx for that specific channel.

13.5 Interfacing to ODL

The PM3386 interfaces to many common Fiber Optic Transceivers by way of a high speed PECL interface. The PECL transmit TXD+/- and the receive RXD+/- signals require AC coupling.

Figure 4 PM3386 SERDES to Fiber-Optic Transmitter

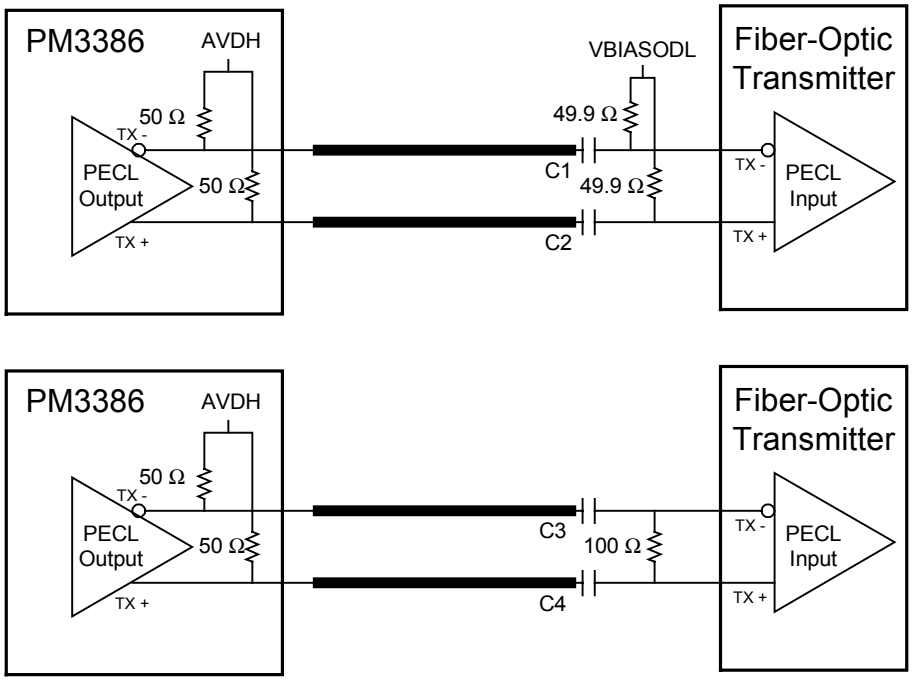


Figure 4 represents a typical application showing the transmit datapath termination. Note that the characteristic impedance for the termination is 50 Ω single ended or 100 Ω differential. Values for C1, C2, C3, and C4 are recommended to be 100nF. Please note that many of the transceivers on the market may contain the needed termination resistors and capacitors. In addition

the TX_EN0 or TX_EN1 signal may be used as the transmit enable while in SERDES mode.

Figure 5 PM3386 SERDES to Fiber-Optic Receiver

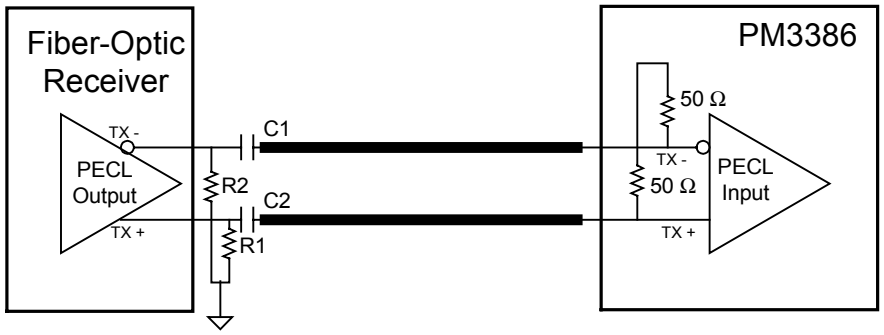


Figure 5 represents a typical application showing the receive datapath termination. Please note the internal 50 Ω single ended termination within the PM3386 receive PECL cells. Please follow the manufactures recommended requirements when interfacing the Fiber-Optic Receiver to the PM3386. Differing Fiber-Optic Receivers require differing values for the R1 and R2 termination resistors. RXSD0 and RXSD1 may be used as the input signal detect for transceivers that support this feature.

In general component placement should be carefully considered. The differential impedance of the line should be kept to 100 Ω. This requires good separation of the board lines to provide for proper impedance matching and reduction of signal reflection. Please refer to the AC timing specification section of this document for clock and data signal specifications.

13.6 GMII Interfacing

The PM3386 may receive the 125MHz CLK125 reference clock input from either a stand alone high precision clock oscillator or via the output from a common 802.3 compliant Gigabit Ethernet transceiver. In either case the PM3386 uses the 125MHz CLK125 input to produce the GTX_CLK0 and GTX_CLK1 outputs to the Gigabit Ethernet transceiver. GTX_CLKx is aligned with the TXD0[7:0] and TXD1[7:0] output pins.

In the case of using the PM3386 with one channel in SERDES mode and one channel in GMII mode the timing requirements for the CLK125 must still be achieved.

13.7 TBI Interfacing

If desired the PM3386 can be configured to use a Ten Bit Interface(TBI) to interface to a given copper PHY or other device. The TBI passes encoded 8B/10B data to and from the PM3386 over the same lines as used for GMII. A pin relationship can be made by referencing the below table.

Table 31 GMII to TBI Pin Mapping

Receive		Transmit	
GMII	**TBI**	**GMII**	**TBI**
TX_ER	TX[9]	RX_ER	RX[9]
TX_EN	TX[8]	RX_DV	RX[8]
TXD[7]	TX[7]	RXD[7]	RX[7]
TXD[6]	TX[6]	RXD[6]	RX[6]
TXD[5]	TX[5]	RXD[5]	RX[5]
TXD[4]	TX[4]	RXD[4]	RX[4]
TXD[3]	TX[3]	RXD[3]	RX[3]
TXD[2]	TX[2]	RXD[2]	RX[2]
TXD[1]	TX[1]	RXD[1]	RX[1]
TXD[0]	TX[0]	RXD[0]	RX[0]
GTX_CLK	GTX_CLK	RX_CLK	RX_CLK

The following process is required to initialize the PM3386 into TBI mode. It is assumed that the given PM3386 port has it's PMD_SELx pin pulled high for GMII mode. This sequence should be executed immediately after power-up or a hardware reset.

1. Write bit 0 (MIIM) of register 0x300 (hex) or 0x400 (hex) for ports 0 and 1 respectfully to a 0.

2. Write bit 6 (SDSEL) of register 0x703 (hex) or 0x713 (hex) for ports 0 and 1 respectfully to a 1.

3. Write bit 11 (RXSD) and bit 15 (FORCE) of register 0x704 (hex) or 0x714 (hex) for ports 0 and 1 respectfully to a 1.

13.8 Enabling and Disabling Data Flows

Data flows within the PM3386 can be halted or enabled via programmable control. The RXEN0 and TXEN0 bits within each **EGMAC GMCC1** register along with the TPAUSE bit in the **EGMAC Transmit Control** register enables and disables the receive and transmit data flows respectively.

13.8.1 Enabling and Disabling Ingress Data Flow

When the RXEN0 bit is low, the given channel will cease data transfer for the receive or ingress direction of the deice. If the device is in the middle of receiving a frame, the frame reception will complete. All further frames on the line side interface will be dropped. All frames that have been received prior to halting will be allowed to be sent to the link via the ingress PL3 bus. By default the PM3386 comes out of reset with the RXEN0 bit low (i.e. traffic halted). To enable the data flow set the RXEN0 bit for the given channel high.

13.8.2 Enabling and Disabling Egress Data Flow

The TXEN0 and TPAUSE bits control data flow in the egress or transmit direction. Upon reset the TXEN0 and TPAUSE bits will be low. To enable data flow after reset the TXEN0 bit must be asserted high. To enable or disable data transfer in cases other than reset the TPAUSE bit must be used. To disable egress or transmit data set the TPAUSE bit to high. If the PM3386 is in the middle of sending a frame, that frame will be finished without error. With the frame transmitted the PM3386 will cease to transmit any more frames. If the link devices continues to write data to the PM3386, that data will be buffered until all egress buffer resources have been used. When the egress buffer resources have been used up, flow control signals will be presented to the link device via the DTPA, STPA, and PTPA signals. To re-enable data flow set the TPAUSE bit low.

13.9 Register Access Procedures

The PM3386 register map allows for direct access to all device register via simple microprocessor reads and writes. Most register do not have side effects when read or written to other that that which is specified within the register description. There are some register within the device that require specific access procedures to allow for proper operation. These special procedures will be noted below and within the corresponding register descriptions. Upon chip

initialization it is recommended that the differing configuration register be written to the appropriate values for the application before traffic transfer is enabled.

13.9.1 PL3IP Register Access Procedure

The differing PL3IP configuration registers (0x104, 0x105, 0x120, 0x121, 0x122, 0x140, 0x141, 0x142) may be written to at any time but will only be updated when the Channel Enable (IP_CR[7]) bit is set to zero.

13.9.2 PL3EP Register Access Procedure

The differing PL3EP configuration register (0x220, 0x221, 0x240, 0x241) may be written to at any time but will only be updated when the Channel 0 Update (EP_CR[2]) or Channel 1 Update Register(EP_CR[3]) bits are set to zero respectively.

13.9.3 EGMAC Register Access Procedure

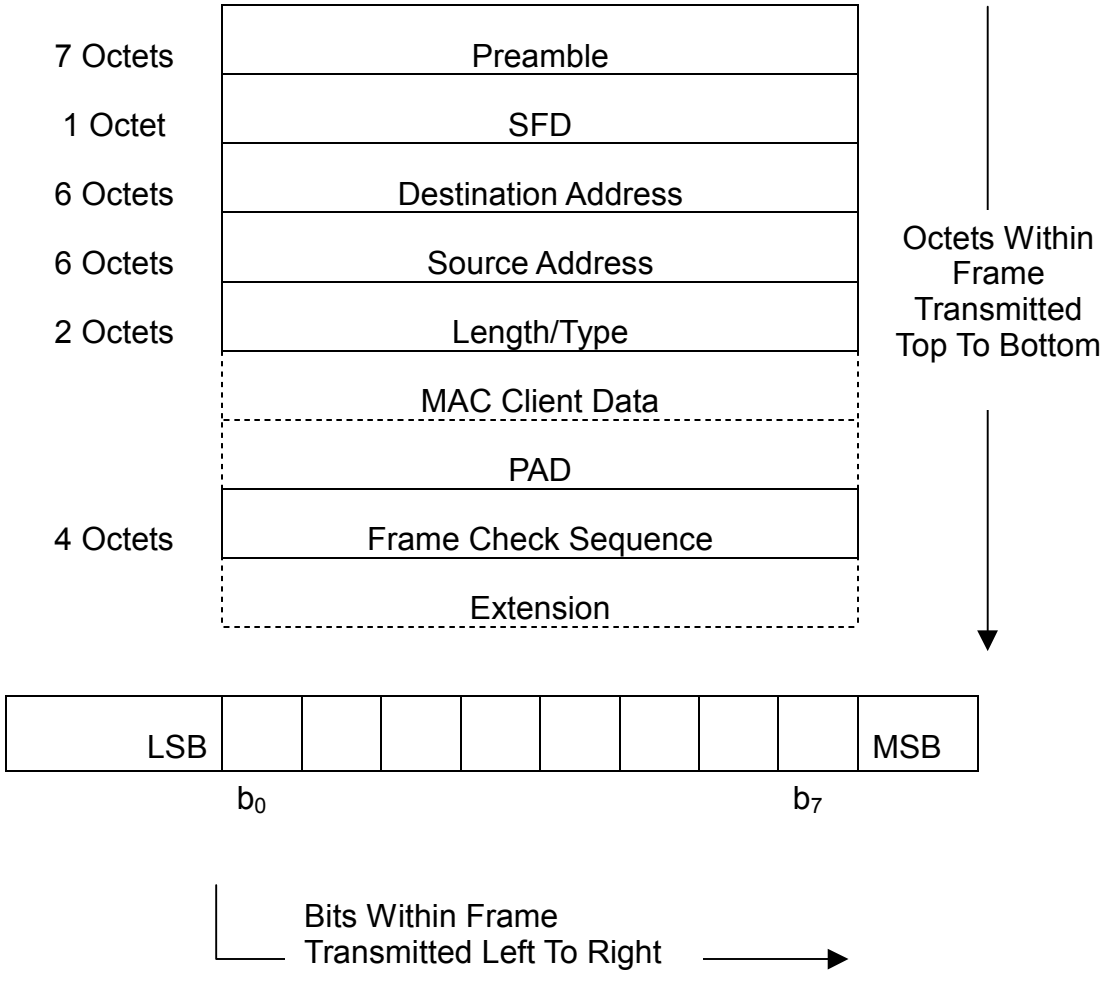
The differing EGMAC configuration registers (0x300, 0x301, 0x302, 0x303, 0x304,0x305, 0x400, 0x401, 0x402, 0x403, 0x404, 0x405) require an EGMAC software reset to enable the state machines within the EGMAC to obtain the new configuration value. The software reset is done with the SRST bit in the EGMAC GMACC0 Config Register High Word Register(0x301, 0x401).

The EGMAC address filter configuration registers can be written to at any time but will only be updated when the Update bit is set within the EGMAC Address Filter Control 3 Register(0x360, 0x460).

13.10 Frame Data and Byte Format

The PM3386 provides support for big endian data transfer on the POS-PHY L3 bus. However, Ethernet data is always transmitted and received via the EGMAC line side in the following format. Bits are transmitted and received from the top to bottom and from left to right. For example, for the destination address (DA[47:0]), bit DA[0] is transmitted first and bit DA[47] is transmitted last.

Table 32 MAC Frame Format



The PM3386 can present or obtain the frame data to or from the system POS-PHY interface in big endian mode. Below is the format for big endian data transfer. Note that both the system side POS-PHY interface and the ingress or egress FIFOs contain the same data mapping.

Table 33 - PM3386 Big Endian POS-PHY L3 Configuration

Bits 31:24	Bits 23:16	Bits 15:8	Bits 7:0
DA[7:0]	DA[15:8]	DA[23:16]	DA[31:24]
DA[39:32]	DA[47:40]	SA[7:0]	SA[15:8]
SA[23:16]	SA[31:24]	SA[39:32]	SA[47:40]
L/T[15:8]	L/T[7:0]	Data[7:0]	Data[15:8]
Data[23:16]	…	…	…
…	…	…	…
FCS[24:31]	FCS[16:23]	FCS[8:15]	FCS[0:7]

13.11 SERDES Loopback

The PM3386 can perform system and line side loop back using differing sections of the SERDES to complete the loop back path. As noted in the **SERDES Port Configuration** register, by setting bits TXSEL[1:0] to 11 the PM3386 will be enabled in a line side loop back configuration. Note that to use this feature the external reference clock (CLK125) and the recovered data clock must be externally locked to the same frequency source. The use of different reference frequencies will ultimately cause the internal SERDES FIFO to underflow or overflow. Upon detection of the underflow or overflow the SERDES FIFO will automatically re-center itself, however, the re-centering action will cause a discontinuity in the repeated data stream. When the reference clock (CLK125) and the receive data stream are derived for the same frequency source (synchronous operation) and meet all other SERDES input timing requirements, and their peak relative jitter is less than +/-8ns, no FIFO slips should occur.

By setting bit RXSEL to 1 in the PM3386 **SERDES Port Configuration** register the device will be enabled into a system side loop back mode. This feature will exercise the entire datapath through the PM3386.

13.12 GMII Loopback

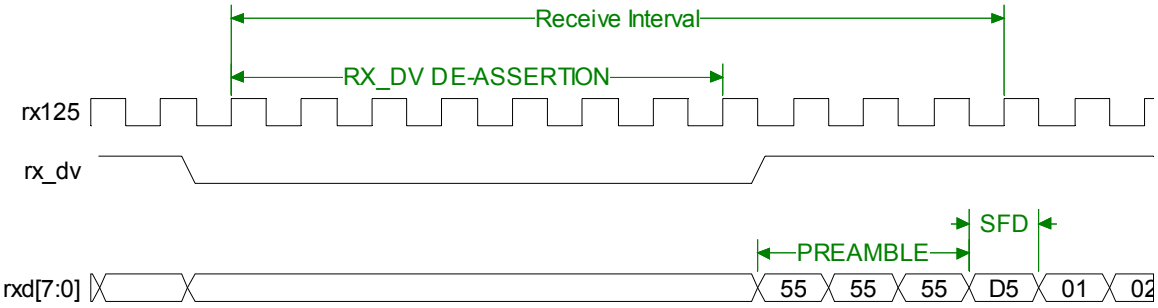
The PM3386 can perform system side loop back using the differing sections of the EGMAC to complete the loop back path. As noted in the **EGMAC GMACC0**

register by setting either bits L32B or L10B the EGMAC will loop back the egress data coming from the PL3 bus to the ingress data going out of the PM3386 via the PL3 bus. The L32B bit causes the 32 bit data bus prior to the GMII or 8B/10B encoder/decoder to be looped back. The L10B bit causes the 10 bit data in the GMII or 8B10B encoder/decoder to be looped back. If both L32B and L10B bits are set the 32 bit path will be used. From the system level perspective there is no difference between the L10B and L32B looped back data

13.13 IFG Manipulation

The PM3386 can receive frames continuously at the normal receive interval of equal to or greater than 96 ns. The normal receive interval is specified as the time between the last byte of the previous frames CRC and the sampling of the Start of Frame Delimiter (SFD) as shown in Figure 6

Figure 6 GMII minimum receive interval



For transmit or egress traffic the PM3386 will insert the appropriate IFG of 96ns by default. The transmit IFG is also programmable allowing frame traffic shaping on back-to-back frames. The IPGT[5:0] field in the **EGMAC GMACC2** register defines the programmable back-to-back IFG between frames. This field is programmed to the number of octets of IFG desired. A setting of 12 decimal represents the minimum IFG of 96 ns. Note that this register is expressed in byte times.

13.14 Frame Length Support

The PM3386 supports jumbo frames up to 9.6k bytes. The **EGMAC Max Receive Frame Length** register controls the maximum size of the ingress frame. If the frame is greater than the programmed size the frame will be treated as a long or jabber frame. The minimum frame size on the ingress channel is 64 bytes. The **EGMAC Transmit Max Frame Length** register controls the

maximum size of the egress frame. If the frame is greater than the programmed size the frame will be treated as long and thus truncated. The minimum frame size on the egress channel is 64 bytes.

The **EGMAC Receive FIFO Forwarding Threshold** register sets the forwarding threshold used for ingress frame gathering and error reporting. Frames are passed from the EGMAC to the PL3 ingress FIFO if an end of frame indication has been received by the EGMAC or the number of bytes received by the EGMAC is greater than the **EGMAC Receive FIFO Forwarding Threshold** register.

This mechanism provides for two different frame error handling capabilities. First if the forwarding threshold is set higher than the received frame size the EGMAC will drop and not forward the erred frame. Second if the forwarding threshold is set lower than the received frame size the EGMAC will immediately start passing the incoming frame as soon as the threshold is reached. When the EGMAC determines the end of frame and an error is detected the EGMAC marks the frame as erred and the PM3386 will assert RERR on the data transfer of the packet on the PL3 bus.

The **PL3EP Channel Minimum Frame Size** register sets the forwarding threshold used for egress frame gathering. Packets passed to the PM3386 on the PL3 bus will be gathered in the egress FIFO until an end of packet indication or until the number bytes transferred to the PM3386 are greater than or equal to the **PL3EP Channel Minimum Frame Size** register. This allows a slow link device to ensure that an entire packet is prepared within the PM3386 before the transmitting the packet on the line. For faster link devices the threshold can be set to the minimum 64 bytes to remove system latency penalties.

13.15 Transmit Padding and CRC Generation

The PM3386 can pad transmit or egress frames to minimum legal frame lengths and append a proper FCS to the frame prior to transmit. This is accomplished only if the PADEN bit is set in the **EGMAC GMACC1** register. Note that in this mode that all frames less than the minimum frame size of 64 bytes will be considered to not have a valid CRC and will have a FCS appended after padding.

The PM3386 can append a proper FCS to each and every frame prior to transmission if the CRCEN bit within the **EGMAC GMACC1** register is set.

The resulting minimum egress frames transmitted by the PM3386 can be understood through the following table.

Table 34 PM3386 Minimum Transmit Frame Size Padding

Input Frame Length	Frame Type	PADEN State	CRCEN State	Pad Action	CRC Action
<60 bytes	Normal	0	0	No Pad	No CRC Append
<60 bytes	Normal	0	1	No Pad	Append 4 byte CRC
<60 bytes	Normal	1	0	Pad with 0's to 60 bytes	Append 4 byte CRC
<60 bytes	Normal	1	1	Pad with 0's to 60 bytes	Append 4 byte CRC
60,61,62,63 bytes	Normal	0	0	No Pad	No CRC Append
60,61,62,63 bytes	Normal	0	1	No Pad	Append 4 byte CRC
60,61,62,63 bytes	Normal	1	0	No Pad	Append 4 byte CRC
60,61,62,63 bytes	Normal	1	1	No Pad	Append 4 byte CRC
>=64 bytes	Normal	0	0	No Pad	No CRC Append
>=64 bytes	Normal	0	1	No Pad	Append 4 byte CRC
>=64 bytes	Normal	1	0	No Pad	No CRC Append
>=64 bytes	Normal	1	1	No Pad	Append 4 byte CRC
<64 bytes	Tagged	0	0	No Pad	No CRC Append
<64 bytes	Tagged	0	1	No Pad	Append 4 byte CRC
<64 bytes	Tagged	1	0	Pad with 0's to 64 bytes	Append 4 byte CRC
<64 bytes	Tagged	1	1	Pad with 0's to 64 bytes	Append 4 byte CRC
>=64 bytes	Tagged	0	0	No Pad	No CRC Append
>=64 bytes	Tagged	0	1	No Pad	Append 4 byte CRC
>=64 bytes	Tagged	1	0	No Pad	No CRC Append
>=64 bytes	Tagged	1	1	No Pad	Append 4 byte CRC

13.16 MII Operations

This section describes how the host can use on-chip registers to access the external gigabit PHY's. There are five registers that are used to read and write to the external gigabit PHY's. These are **EGMAC MCMD**, **EGMAC MADR**, **EGMAC MWTD**, **EGMAC MRDD** and **EGMAC MIND**. The bit definitions and details of these registers are defined in the Normal Mode Register Description. The access to the PHY's are separated into Read Access and Write Access. These Accesses are described below:

13.16.1 MII Read Access

1) Write the PHY Address and PHY Register Address to the **EGMAC MADR** register.

2) Write the RSTAT bit (bit – 0) in the **EGMAC MCDM** register with a 1. This will start the read process and set the MBSY bit in the **EGMAC MIND** register.

3) Wait for or poll the MBSY bit in the **EGMAC MIND** register until the MBSY bit is low.

4) Once the MBSY bit is low then the data in **EGMAC MRDD** is valid. Read the **EGMAC MRDD** register for the data.

5) Write the RSTAT bit (bit – 0) in the **EGMAC MCDM** register with a 0.

13.16.2 MII Write Access

1) Write the PHY Address and PHY Register Address to the **EGMAC MADR** register.

2) Write the data to be written to the **EGMAC MWTD** register. The MBSY bit in the **EGMAC MIND** register will be asserted until the write access is complete.

13.17 Auto-Negotiation

The PM3386 implements Clause 37 of IEEE 802.3-1998 Auto-Negotiation function type 1000BASE-X. The Auto Negotiation for the 1000BASE-X function provides the means to exchange information between two devices that share a link segment allowing management the ability to configure both devices in such a way that takes maximum advantage of their capabilities. Auto-Negotiation is performed using special 10-bit ordered sets defined within Clause 36 of the IEEE

802.3 Standard. The EGMAC module takes care of all Auto-Negotiation functions inside of the PM3386. After reset the PM3386 senses Auto-Negotiation Enable bit (ANEN) from the **EGMAC Auto-Negotiation Control** register to determine whether or not the Auto-Negotiation is enabled. If not enabled, the PM3386 transmits frames normally interspersed with idles. If, however, the ANEN control signal is active, the PM3386 starts the Auto-Negotiation State Machine. The Auto-Negotiation State Machine follows the state diagram exactly as outlined in 802.3-1998 Clause 37. The configuration word to be transmitted is set to 0x0000h. The “all zero” configuration word is transmitted to the Link Partner as a /C/ (Configuration) ordered set to the link partner for a duration of 10ms as governed by the Link Timer in the EGMAC module. After 10ms is complete, the PM3386 transmits /C/ ordered sets containing the **EGMAC Base Page** register, with ACK not set. This is done continuously until the PM3386 detects Ability Match Received (ABMRX) which indicates that three consecutive matching /C/ ordered sets have been received ignoring the ACK bit.

The PM3386 then continuously transmits /C/ ordered sets containing the **EGMAC Base Page** register, with ACK set. This is done until the PM3386 detects Acknowledge Match Received (ACMRX) which indicates that three consecutive matching /C/ ordered sets have been received with the ACK bit set. The PM3386 then determines if there has been consistency in the /C/ ordered sets received. If so, it proceeds to start the Link Timer once more. When the Link Timer finishes and if either device does not advertise an ability to exchange Next Pages, the PM3386 transmits idles /I/. The Link Timer is then stared once more.

When the Link Timer is done, the PM3386 verifies that IDMRX is active (receiving idles), which verifies that the link partner has gone through its Auto-Negotiation process and is ready to start sending and receiving frame data. IDMRX active prompts the Auto-Negotiation State Machine to transition into its final state and to assert the Auto-Negotiation Complete (ANCPLT) signal. This informs the system that packet data can be sent across the link.

The Auto-Negotiation state machine will stay in this final state until any of these following events occur:

1. The Auto-Negotiation is restarted by the **EGMAC Management** register (RSTAN) bit being asserted.

2. The EGMAC or PM3386 is reset.

3. The synchronization state machine in the EGMAC flags a loss of code synchronicity.

4. The Link Partner remotely re-initiates the Auto-Negotiation process by sending /C/ order sets containing the “all zero” configuration codeword.

When any of the above events occur, the EGMAC Auto-Negotiation state machine will transition from its final state to its starting state and the process will start from the beginning.

13.17.1 Monitoring Auto-negotiation

To monitor Auto-negotiation the host reads the **EGMAC ANSTT** register for status and can also read the **EGMAC ANLPA** register to get information on the link partner. The register and bit definitions for these registers are defined in the Normal Mode Register Description section.

13.17.2 Modifying Auto-negotiation

To modify Auto-negotiation the host reads and writes the **EGMAC ANNPG/ANADV** register for Advertisement on this device. The register and bit definitions for these registers are defined in the Normal Mode Register Description section.

13.17.3 Control of Auto-negotiation

To control Auto-negotiation the host reads and writes the **EGMAC ANCTL** register for control of enabling/disabling or re-starting auto-negotiation on this device. The other control is the AUTOS bit (bit – 8) in the **EGMAC GPCSC** register, when asserted this bit will cause the MAC to auto sense if the Link Partner is in Link Bypass or Auto-neg is disabled. The register and bit definitions for these registers are defined in the Normal Mode Register Description section.

13.18 TX_ER Assertion Criteria

TX_ER on the PM3386 line side will be asserted if any of the following conditions are present:

1. If the link asserts TX_ERR on the last word of a PL3 egress data transfer.

2. If parity checking is enabled in the **PL3EP Configuration** register and invalid parity is determined on any PL3 egress data transfer word.

3. If parity checking is enabled in the **PL3EP Configuration** register and invalid parity is determined on a valid TSX address cycle.

4. If the egress frame to be transmitted is considered short, long, without a valid CRC, or any type of internal transmit MAC error.

13.19 Frame Filtering

The PM3386 has simple programmable options to filter or forward ingress frames to the upstream link device. The PM3386 EGMAC Receive Address Filtering Logic consists of eight exact-match MAC/VID filters, one 64-bin hash based multicast filter and four address filtering control registers that control the state of the forwarding for each filter. Each exact match filter includes one 48-bit MAC Address register and one 12-bit VID register that can be programmed through the microprocessor interface to the appropriate values. The filter logic is controlled by the four EGMAC Address Filter Control registers. The host microprocessor has complete programmable access to all filtering features.

13.19.1 Group Multicast Address Filtering

In parallel with the exact address match, the PM3386 performs multicast filter lookups. Within the PM3386 there resides a 64-bin hash based multicast filter per channel consisting of one 64-bit mask register that is programmable from the Microprocessor interface (**EGMAC Multicast Hash** register). This register is used in conjunction with a 6-bit value which is derived from bits [28:23] of the 32-bit CRC computed over the Destination Address. This 6-bit value is used to index into the 64-bit mask register. The 64-bit mask register is used to determine if a multicast address that hashes to a given bin will be accepted for forwarding The 64-bin hash based multicast filtering is enabled by the MHASH_EN bit in the **EGMAC Address Control 2** register. If the MHASH_EN bit is 0 then there is no hash based multicast filtering, however if MHASH_EN is 1 then hash based multicast filtering is enabled.

The multicast hash filter operation operates only on multicast-type frames: those with the IEEE Group/Functional bit set in the DA of the frame (most significant bit of the least significant byte of the MAC DA). The 48-bit destination address of the received frame is passed through the standard 802.3 CRC function in the same order in which the destination address octets are received. Making reference to the 802.3 specification, section 3.2.8 Frame Check Sequence field, the CRC function generating polynomial and function is:

$$G(x) = x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^{8}+x^{7}+x^{5}+x^{4}+x^{2}+x^{1}+1$$

1. The first 32-bits of the frame (which is the first 32-bits of the destination address received) are complemented.

2. The 48 bits of the destination address are then considered to be the coefficients of a polynomial M(x) of degree 47

3. M(x) is multiplied by x^{32} and divided by G(x), producing a remainder R(x) of degree <= 31.

4. The coefficients of R(x) are considered to be a 32-bit sequence.

Bits [28:23] of the resultant 32-bit CRC remainder (call this crc_rem[28:23]) are used as the index into the MHASH[63:0] register. The result of the Group Multicast address filter is logically represented by the variable MHASH_ACCEPT:

MHASH_ACCEPT = (MHASH_EN == 1) & (MHASH[crc_rem[28:23]] ==1);

13.19.2 Exact Match Filter Program Options

Each of the eight exact match filters on each EGMAC has four bits of associated configuration. These are found in the Address Filter Control 0 and Address Filter Control 1 registers:

1. ADRFILT_CTRLx[0] enables the exact match operation. If this bit is a logic 0 then the EXACT_MATCH operation returns a logic 0.

2. ADRFILT_CTRLx[1] enables the match function to also compare the VLAN Tag VID[11:0] field of the receive frame if the two bytes following the receive frame source address are equal to the VLAN Tag ID register

3. ADRFILT_CTRLx[2] selects whether the source address or destination address of the received frame is used as the address for matching.

4. ADRFILT_CTLRx[3] is a configuration bit that determines whether an exact match will affect the variable ACCEPT or DISCARD.

13.19.3 Exact Match Filter Operation

The exact match filter operation is a two step process. The first step is to determine whether the address match criteria is logically true:

EXACT_MATCH is logic 1 if the exact match filter is enabled and the selected frame address (and optional VID field of a VLAN tagged frame) are equal; otherwise, EXACT_MATCH is logic 0.

The second step is to set the EXACT_MATCH_ACCEPT or EXACT_MATCH_DISCARD variable for the given (one of eight) exact match filters based on the setting of ADRFILT_CTRLx[3] register bit:

EXACT_MATCH_ACCEPT = EXACT_MATCH & (ADRFILT_CTRLx[3] == 1);

EXACT_MATCH_DISCARD = EXACT_MATCH & (ADRFILT_CTRLx[3] == 0);

13.19.4 Address Filter ACCEPT / DISCARD Evaluation

The final result of the address filter function is a single filter versus forward decision. This again is a two step process. First the result of the Group Multicast Address filter is combined with the result of the eight possible exact match filter operations to determine a final filter versus forward decision. Let EXACT_MATCH_ACCEPT[7:0] and EXACT_MATCH_DISCARD[7:0] represent the ACCEPT and DISCARD variables for the eight independent exact match filters respectively. The final combined value of ACCEPT and DISCARD for all address filters is logically:

ACCEPT = (EXACT_MATCH_ACCEPT[7:0] != 0) | MHASH_ACCEPT;

DISCARD = (EXACT_MATCH_DISCARD[7:0] != 0);

Secondly the address filter logic can be configured so that a frame has a higher priority for being forwarded or filtered: this decision is based on the configuration bit PMODE in the Address Filter Control 2 register.

13.19.4.1 Address Filtering in Non-Promiscuous Mode (PMODE = 0)

DISCARD has priority over ACCEPT in non-Promiscuous mode (PMODE a logic 0). A frame will be filtered only if ACCEPT is true and DISCARD is false. This is shown in the following table. It should be noted that if all filters are disabled, then all frames are filtered.

Table 35 Address Filter Result in Non-Promiscuous Mode

PMODE	DISCARD	ACCEPT	Result of Address Filter Function
0	0	0	Filter frame
0	0	1	Forward frame
0	1	0	Filter frame
0	1	1	Filter frame

13.19.4.2 Address Filtering in Promiscuous Mode (PMODE = 1)

ACCEPT has priority over DISCARD in Promiscuous mode (PMODE a logic 1). A frame will be filtered only if DISCARD is true and ACCEPT is false. This is shown in the following table. It should be noted that if all filters are disabled, then all frames are accepted.

Table 36 Address Filter Result in Promiscuous Mode

PMODE	DISCARD	ACCEPT	Result of Address Filter Function
1	0	0	Forward frame
1	0	1	Forward frame
1	1	0	Filter frame
1	1	1	Forward frame

13.19.5 Address Filter Programming

The EGMAC frame filtering is programmed in the following manner.

1. Program all desired filters with the desired contents.

    a. Program the **EGMAC Exact Match Address** and **EXACT Match VID** registers and respective **EGMAC Address Control 0** or **EGMAC Address Control 1** registers for the desired Exact match options.

    b. Program the **EGMAC Multicast Hash** register with the desired bit mask and enable by programming the **EGMAC Address Filter Control 2** register.

2. Enable the programmed values to take effect by writing to the UPDATE bit within the **EGMAC Address Filter Control 3** register. Upon a write to this register the EGMAC updates all of the filter information for the device upon the end of the reception of the current frame. If not currently receiving frames the filter logic will be updated immediately. When the update has happened the UPDATE bit will be self-cleared by the EGMAC.

13.20 PAUSE Flow Control

The PM3386 allows 802.3 PAUSE frames to be transmitted out the egress MAC port based on three separate PAUSE frame catalysts aside from client based PAUSE frame injection. These conditions are discussed further in this section but first a general description of the PM3386 PAUSE frame generation is desired.

The Transmit PAUSE Control Frame logic responds to a Transmit PAUSE Control Request caused from either:

1. Internal FIFO Flow Control.
2. External side-band PAUSE Request.
3. External host based PAUSE Request.

In each case the PM3386 responds by initiating a Transmit PAUSE Frame State. The logic, if need be, waits for the current frame transmission to end before attempting to send a PAUSE control frame. The PAUSE control frame is formatted as follows:

Table 37 - PAUSE Control Frame Format

Octets	Frame Field	Source of Information
7 Octets	Preamble	Auto-generated
1 Octet	SFD	Auto-generated
6 Octets	Destination Address	Auto-generated (01-80-c2-00-00-01) Note that DA[7:0] = 01, DA[15:8] = 80…etc.
6 Octets	Source Address	**EGMAC Station Address** register. User defined
2 Octets	Length/Type Field	Auto-generated (88-08)
2 Octets	Opcode Field	Auto-generated (00-01)
2 Octets	PAUSETimer Field	**EGMAC PAUSE Timer** register: By default FF-FF
42 Octets	PAD	Auto-generated
4 Octets	FCS	Auto-generated

The PAUSE frame is stitched together using register based information and a series of auto-generated fields. As long as the PM3386 is in the Transmit PAUSE Frame State the EGMAC will continually send a PAUSE control frame each time the internal **EGMAC PAUSE Timer Interval** register counts down to zero. In this fashion the egress data-pipe will not be blocked for normal egress data traffic. The **EGMAC PAUSE Timer** and **EGMAC PAUSE Timer Interval** registers are both programmable. By default the **EGMAC PAUSE Timer** register defaults to 0xFFFF and the **EGMAC PAUSE Timer Interval** register defaults to 0x7F67. Both are representative of the number of PAUSE Quanta used in the system. Note that PAUSE Quanta is defined as 512 bits. The **EGMAC PAUSE Timer Interval** will reload to the programmed state when it reaches zero. It is the responsibility of the PAUSE catalyst to hold the input to the EGMAC until normal ingress traffic can be resumed. When the catalyst removes the request for PAUSE the EGMAC will send out a PAUSE Control frame with the PAUSE timer value of zero.

Aside from the POS-PHY Level 3 client sending PAUSE Control frames there are three different PAUSE frame catalysts. These are discussed below.

13.20.1 Internal FIFO Flow Control

The ingress FIFO logic is programmable via the **PL3IP Channel High Watermark** register to the FIFO fill level that will trigger a PAUSE flow control signal. When the POS-PHY ingress FIFO exceeds this level the PL3IP module asserts an internal signal to the EGMAC requesting PAUSE flow control. The EGMAC can be programmed to accept POS-PHY FIFO PAUSE flow control requests for egress traffic if the **FCTX** bit is set in the **EGMAC GMACC1** register. When enabled and the internal signal is asserted the EGMAC will commence sending 802.3 PAUSE frames. The PL3IP logic will continue to hold the pause request signal to the EGMAC until the separate **PL3IP Channel Low Watermark** register threshold has been achieved. At this time the pause request signal will be de-asserted informing the EGMAC to cease PAUSE frame flow control by sending a PAUSE Control frame with the PAUSE timer value of zero.

13.20.2 External Side-Band PAUSE Request

The PAUSE0 and PAUSE1 signals are sideband PAUSE request signals synchronous to RFCLK.

When the **IP_CR[6] PAUSE Mode Selection** bit in the **PL3IP Configuration Register** is set to zero the PAUSE0 and PAUSE1 signals, when asserted, will activate the same PAUSE mechanism in the EGMAC that the internal FIFO fill levels would have accomplish. These signals are useful when lack of resources in the upper level device becomes critical and the upper level device would like to send PAUSE frames on the egress data-path while continuing to receive frame data on the ingress datapath without blockage. These signals are asserted and held as long as PAUSE frames are required to be sent out the egress interface. When normal frame reception is desired the PAUSE0 or PAUSE1 signals can be de-asserted. Upon de-assertion the given channel will transmit a PAUSE Control frame with the PAUSE timer value of zero.

When the **IP_CR[6] PAUSE Mode Selection** bit in the **PL3IP Configuration Register** is set to one the PAUSE0 and PAUSE1 signals, when asserted, will allow the given programmed data burst on the corresponding channel to complete and then halt data traffic on that channel until the PAUSE0 or PAUSE1 for the corresponding channel is de-asserted. Uner this mode the PAUSE Control frame generation defaults to Internal FIFO Flow Control as described above. This mode allows the upper layer POS-PHY Level 3 device to bypass RENB (always assert RENB). This removes a possible head-of-line block problem that might be inherint in the system design. In this mode PAUSE0 and PAUSE1 become the individule RENB signals for the PM3386.

13.20.3 External Host Based PAUSE Request

The PM3386 allows and external microprocessor to initiate transmission of PAUSE frames by programming the internal **HOSTPAUSE** bit in the **EGMAC Control** register. When the **HOSTPAUSE** bit is set the EGMAC is placed in a Transmit PAUSE Frame State. When cleared no PAUSE frames will be transmitted. Again when transitioning from a Transmit PAUSE Frame State to no PAUSE a PAUSE Control frame will be sent with a PAUSE timer value of zero.

13.20.4 Reception of 802.3 PAUSE frames.

The PM3386 can be programmed to handle ingress PAUSE control frames in the manner as outlined below. This programming is done via the PASS_CTRL bit in the **EGMAC Control** register and the **FCRX** bit in the **EGMAC GMACC1** register. The PASS_CTRL bit programs whether or not control frames are passed to the upper layer device. The **FCRX** bit programs whether or not the PM3386 follows 802.3 PAUSE flow control.

Table 38 PAUSE Frame Programmable Control

PASS_CTRL	FCRX	PM3386 Action
0	0	PAUSE Frames are ignored and dropped at the PM3386 level.
0	1	PAUSE Frames are executed but are no passed to the upper layer.
1	0	PAUSE Frames are ignored and forwarded to the upper layer device.
1	1	PAUSE Frames are executed and forwarded to the upper layer device.

Please note as per 802.3-1998 that if the PM3386 is currently executing reception of a PAUSE frame and is currently blocking the egress data-path from transmission of normal data traffic that it is still possible to send PAUSE control frames by following the prescribed flow control methods in 13.20.

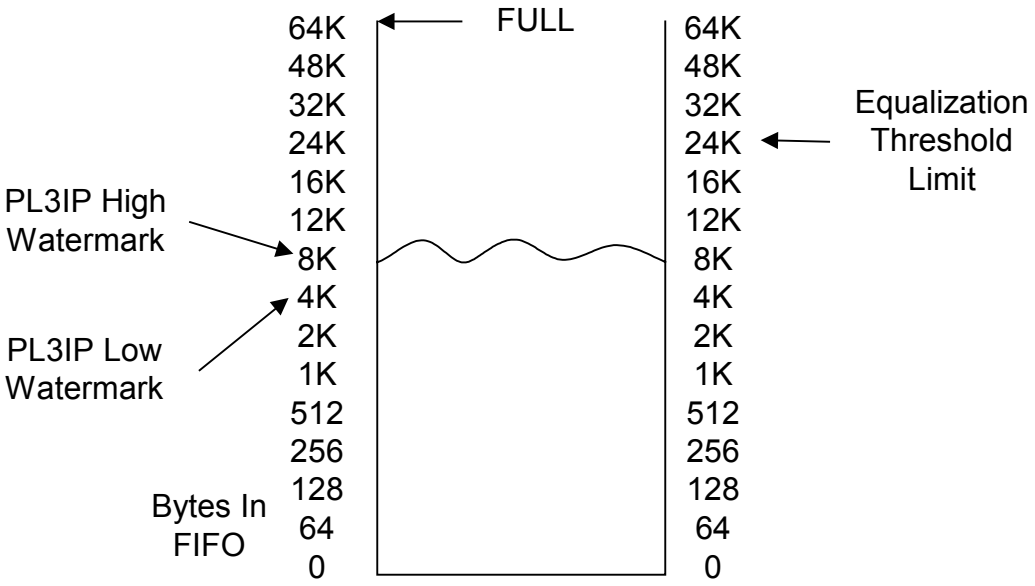
13.21 Ingress POS-PHY Buffer Thresholds

The PM3386 contains 64k bytes per channel ingress buffers. Each buffer is organized in standard FIFO format. The FIFO's are filled with data from the

ingress EGMAC interface and are drained on the PL3 side by the link device. Each FIFO has programmable threshold to provide for system ingress flow control and hysteresis. Figure 7 represents the PM3386 ingress FIFO structure as a simple bucket for easier explanation. The pm3386 will fill the FIFO with data coming in from the EGMAC line side interface. When the number of bytes in the FIFO are greater than the programmed threshold in the PL3IP **PL3IP High Watermark** register a signal is sent to the EGMAC from the FIFO to start flow control. If enabled the EGMAC will start sending PAUSE frames out on the media. When the ingress FIFO is drained past the threshold programmed in the PL3IP **PL3IP Low Watermark** register the signal to the EGMAC telling it to flow control will become de-asserted. The EGMAC will cease to send PAUSE frames with the transmission of a final PAUSE Control frame with the PAUSE timer value set to zero.

If the FIFO fills to the programmable level as contained within the **PL3IP Equalization Threshold Limit** register the PM3386, if enabled, will start monitoring for channel starvation. This feature allows the PM3386 to compensate for lack luster channel performance caused by a slow link draining devices or radically unmatched data sizes between channels. Channel equalization allows for a more fair data flow across the PL3 bus promoting greater bandwidth optimization. Once the **Equalization Threshold Limit** is reached the PM3386 monitors the difference in bytes between the two internal ingress FIFOs. If this byte difference becomes greater than or equal to the **PL3IP Equalization Difference Limit** register the PM3386 will initiate channel equalization. During channel equalization all know rules of burst size and packet handling will still be observed but the arbitration will take into account the differential fill levels of the FIFOs favoring the FIFO that has the fullest level. This mode of operation is transparent to the link device. All PL3 bus protocols are still observed.

Figure 7 Ingress FIFO Representation



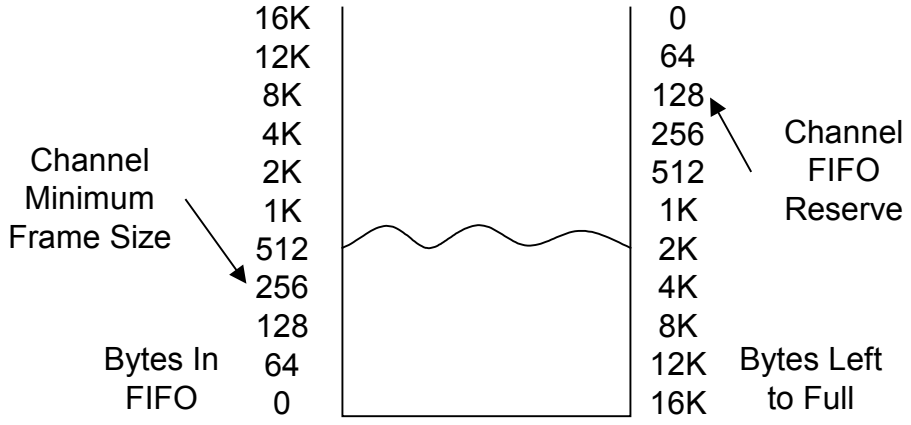
13.22 Egress POS-PHY Buffer Thresholds

The PM3386 contains 16k byte per channel egress buffers. Each buffer is organized in standard FIFO format. The FIFO's are filled with data from the egress PL3 interface and are drained at the internal chip side by the EGMAC. Each FIFO has programmable thresholds to provide frame gathering and PL3 bus flow control. Figure 8 represents the PM3386 egress FIFO structure as a simple bucket for easier explanation. The **PL3EP Channel Minimum Frame Size** register is used to promote the gathering mechanism of the egress FIFO. As the FIFO is filling with a packet, the FIFO will not start draining packet data until either the fill level is greater than or equal to the threshold programmed in the **PL3EP Channel Minimum Frame Size** register or until an End of Packet (via TEOP) has been written to the FIFO. This allows the down stream link device to deposit the entire packet into the EGRESS channel prior to transmission by the PM3386 on to the wire. The programmer may prefer, depending on the application, to set the gathering threshold low in order to promote lower system latencies. In this case of a small gather threshold programmed in the **PL3EP Channel Minimum Frame Size** register the link device must keep the egress PL3 FIFO full in order to not under-run the PM3386 transmission datapath. In the event that an under-run condition does happen the PM3386 will recover gracefully incrementing all appropriate counters and marking the outgoing frame as being in error. When the PM3386 egress FIFO

receives an EOP from the link device the given frame will be sent regardless of the programmed gathering threshold. The next frame after the EOP will have to satisfy either the Channel Minimum Frame Size or EOP requirements prior to transmit. It is therefore possible to set the gathering threshold to only send packets when all of the per packet contents they have been gathered into the egress FIFO. This ensures non under-run conditions caused by link devices that may be slower to insert data into the egress FIFO via the PL3 interface.

The PM3386 provides a rich set of egress flow control signals generated toward the link device. These signals include DTPA, STPA, and PTPA. In each case the flow control signals all originate from a single source. As the egress FIFO fills the number of bytes left in the FIFO is monitored and compared to the threshold set in the **PL3EP Channel FIFO Reserve** register. When the fill limit meets or exceeds the programmed fill limit the PM3386 de-asserts the status signals DTPA, STPA, and PTPA. This mechanism allows the device user to select at which point they would like to start the flow control measures. If the link device ignores the TPA signals and attempts to overflow the egress FIFO the PM3386 will truncate the offending packet. The PM3386 will wait until a small amount of egress FIFO has been recovered then resume accepting data from the link device.

Figure 8 Egress FIFO Representation



13.23 POS-PHY Parity Selection

By default the PM3386 supports odd parity as specified in the PL3 specification. If desired the PM3386 can be programmed to use even parity. Please see the **PL3IP Configuration** and **PL3EP Configuration** registers for selection options.

13.24 POS-PHY Frame Burst Sizes

The ingress datapath of the PM3386 has a programmable PHY-to-Link byte burst capability. The PM3386 can be programmed to send ingress data transfers in multiple byte bursts as programmed by the **PL3IP Channel Packet Burst Mask registers** within the PL3IP block.

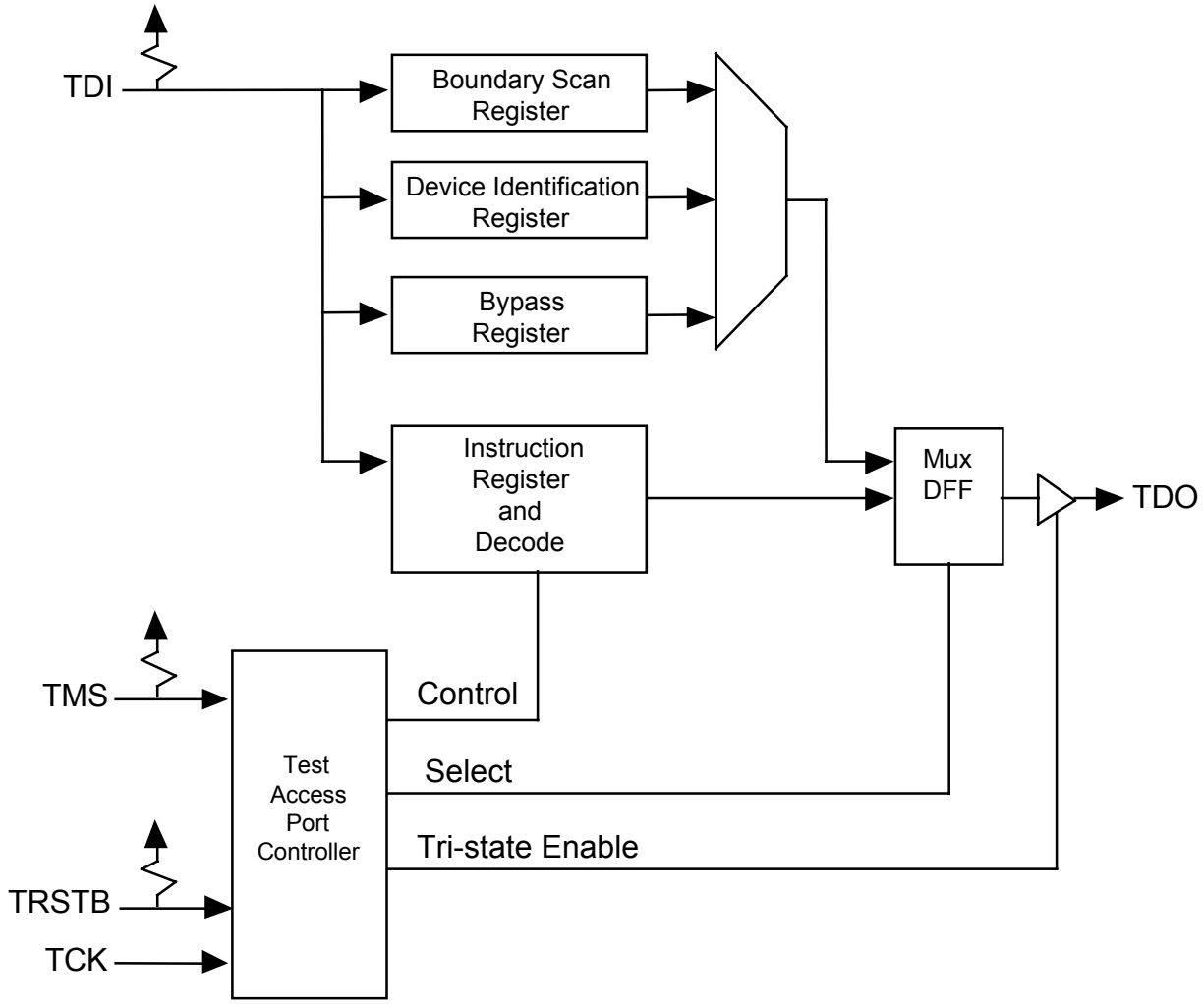
13.25 Interrupt Handling

The PM3386 signals the host processor via the use of the INTB active low signal. When INTB is asserted the host processor can interrogate the PM3386 for the source of the interrupt by reading the **Interrupt Status** register. The resulting information will provide the programmer with the block from which the interrupt originated. To clear the interrupt the host processor reads the block interrupt as decoded by Table 13. A read from this block register will clear the block level interrupt. Note that there may be more than one block level interrupt. To clear the device level interrupt all block level interrupts must be cleared or masked off.

13.26 JTAG Support

The PM3386 supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

Figure 9 - Boundary Scan Architecture



The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

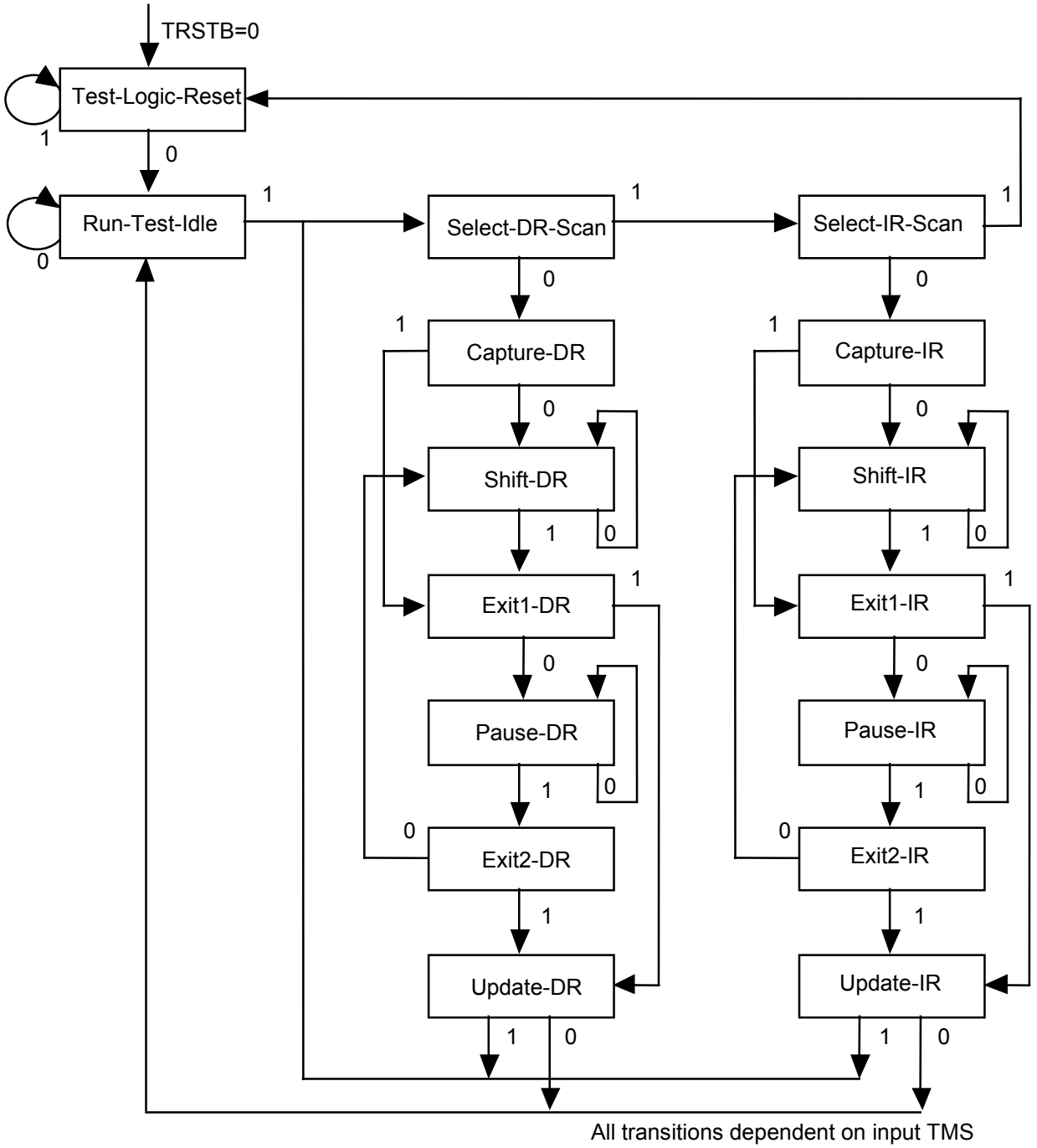
The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be

sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

13.26.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

Figure 10 - TAP Controller Finite State Machine



Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is an description of the standard instructions. Each instruction selects an serial test data register path between input, TDI and output, TDO.

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

13.27 Field guide to first packet

The following steps are suggested to successfully bring up the PM3386.

1. Ensure proper connections to test equipment have been made.

2. Insure proper power and ground supplies as per specification. Also insure that the required pins have pull-ups or pull-downs as described by this specification. Please also note to tie the PMD_SEL0 and PMD_SEL1 pins to either power or ground.

3. Insure proper clocks are being supplied to the PM3386.

4. Follow the Operation section System Reset procedure.

5. Check Register 0x4H Device Status Register. This register should show the DLL0_RUN and DLL1_RUN signals high. If these signals are not present the most likely issue will be lack of the proper RFCLK or TFCLK respectively. Ensure bits [14] and [15] are set to 1. If not the most likely problem will be that TDI or TMS do not have pull up resistors installed.

6. Check Register 0x5H Reference Out of Lock Status Register. This register should read 0x0. Issues that might cause other values to be read are typically the lack of the CLK125 being present to the device.

7. Check Register 0x6H Data Out of Lock Status Register. This register should read 0x0 if in SERDES mode. If in SERDES mode and this register is not 0x0 the link to the test equipment for the Gigabit Ethernet may not be connected.

8. Prior to enabling the PM3386 set all optional registers to conform to the target application. Please note that there are no registers that need to be set if the user is just trying to get data through the device for debug purposes.

8. Enable the desired channel that data is to be passed on. This is done as described above in the Enabling and Disabling Data Flows sections.

10. Send data into the device.

12. The PM3386 statistic register can be used to check for data flow.

14 FUNCTIONAL TIMING

14.1 POS-PHY Level 3 Interface

Figure 11 is a typical example of the PM3386 POS PHY Level 3 interface ingress timing. The link device throughout this example holds the RENB asserted signaling to the PM3386 that it can accept data. In cycle 2 the PM3386 asserts RSX to qualify the in-band address presented on the RDAT bus. In cycle 3 RVAL is asserted qualifying both the valid data on RDAT as well as the RSOP signal indicating the start of a frame. The PM3386 bursts 16 bytes over cycles 3,4,5, and 6. In cycle 7 the PM3386 re-arbitrates to channel 0. The PM3386 signals the link device of the change by asserting the RSX signal qualifying the in-band address on the RDAT bus. In cycle 8 and 9 bytes are transferred to the link device. However in cycle 9 the PM3386 ceases the transfer and asserts the REOP, RMOD, and RERR signals. In this case the RERR signal indicates that an error has occurred on this transfer. In cycles 10 and 11 the PM3386 pauses transfer. This can be noted by the de-assertion of the RVAL signal. In cycle 12 the PM3386 resumes transfer for channel 1. It should be noted that RPRTY will indicate the parity across the RDAT bus when RVAL or RSX are asserted.

Figure 11 - PM3386 POS-PHY L3 Receive Logical Timing

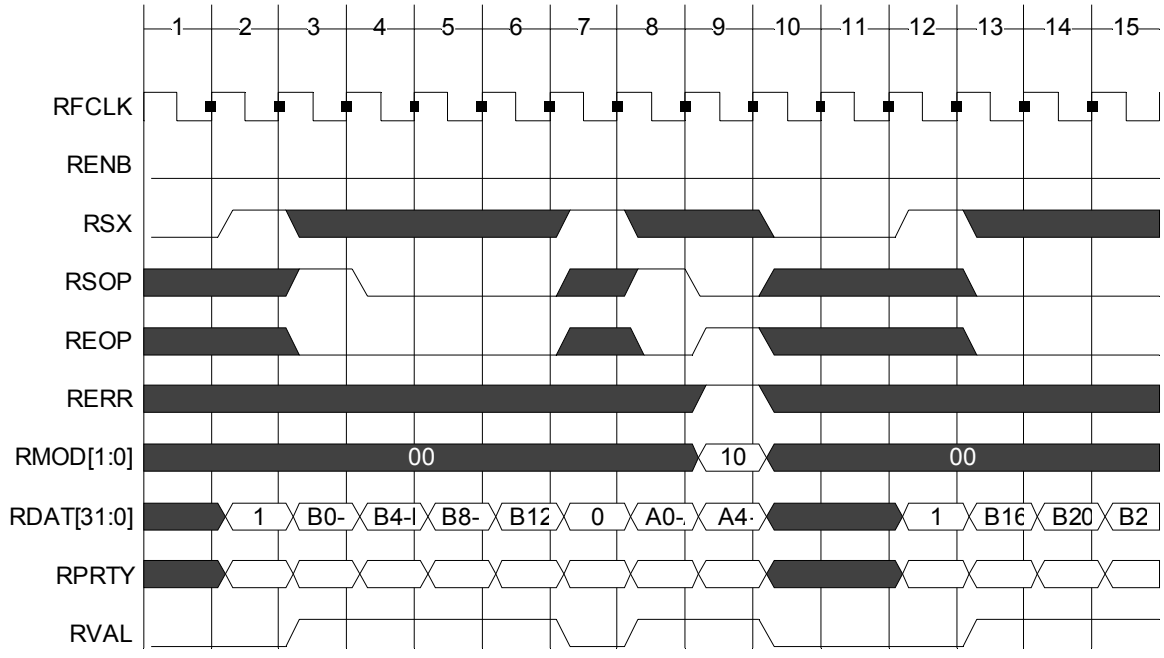


Figure 12 is an example of the PM3386 being paused by the upper level link device. In cycle 1 the PM3386 concludes a transfer to channel 1. In cycle 2 the PM3386

pauses. In this case no data was available for transfer. In cycle 3 the PM3386 indicates to the link device the in-band address for the upcoming data transfer. Note that even though RENB is asserted in cycle 3 that the PM3386 will not hold RSX asserted as RENB was not de-asserted (logic high) during cycle 2. RENB does however have an effect on RVAL in cycle 4. Since the link device indicates that it requires a pause in cycles 3 and 4 the PM3386 will hold the RVAL signal high and will not advance the valid data until one cycle (pos-edge of cycle 6) after the assertion of RENB. RENB is asserted in cycle 5 therefore data can be considered valid on the positive edge of cycle 6. Data transfer continues in cycle 7 and 8. In cycle 9 the PM3386 pauses. This is indicated by the de-assertion of RVAL. In cycle 10 the PM3386 concludes the transfer of this frame. In this case the frame is in error and is indicated such by the assertion of RERR and REOP. In cycle 11 the PM3386 indicates the in-band address to the link device. Since the link device indicated a pause in cycle 10 by de-asserting RENB the PM3386 will hold the RSX signal high and will not change the value of the RDAT bus until one cycle (pos-edge of 14) after the assertion of RENB. The PM3386 resumes sending data on RDAT in cycle 15.

Figure 12 - PM3386 POS-PHY L3 Receive Logical Timing with Pausing

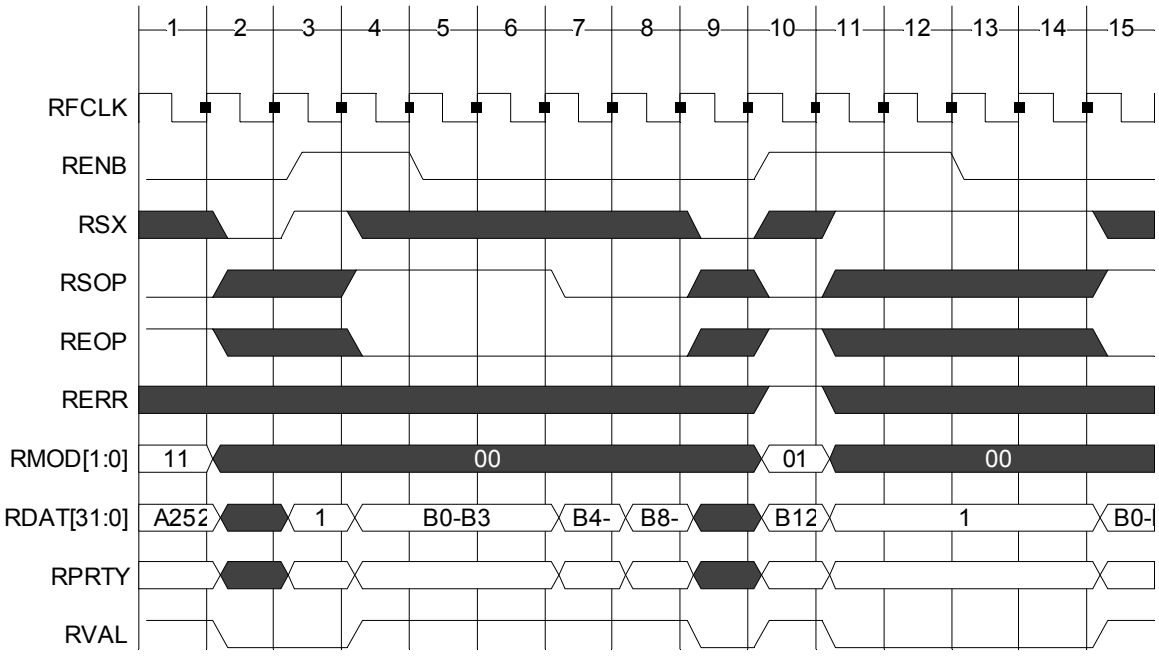


Figure 13 provides a look at a few cases for when the RENB signal is asserted. It is acceptable for the point of view of the PM3386 that the link layer device de-assert RENB at any time and for any length of time. In the first case RENB is de-asserted in cycle 3. The PM3386 captures the de-assertion on the rising edge of RFCLK on the beginning of cycle 4. Because of the RENB induced pause in cycle 5 the data on the RDAT bus will remain unchanged . In the second case the RENB signal is de-asserted in cycle 8. Again note that the data in cycle 10 will be held as the RENB de-assertion causes a pause on the data transfer on the RDAT bus. In the third case RENB is de-asserted in cycle 12. Note that in cycle 14 both the RVAL and RSOP as well as the data on RDAT are held unchanged because of the paused induced by the de-assertion of RENB.

Figure 13 - PM3386 POS-PHY L3 Receive Logical Timing Cases A

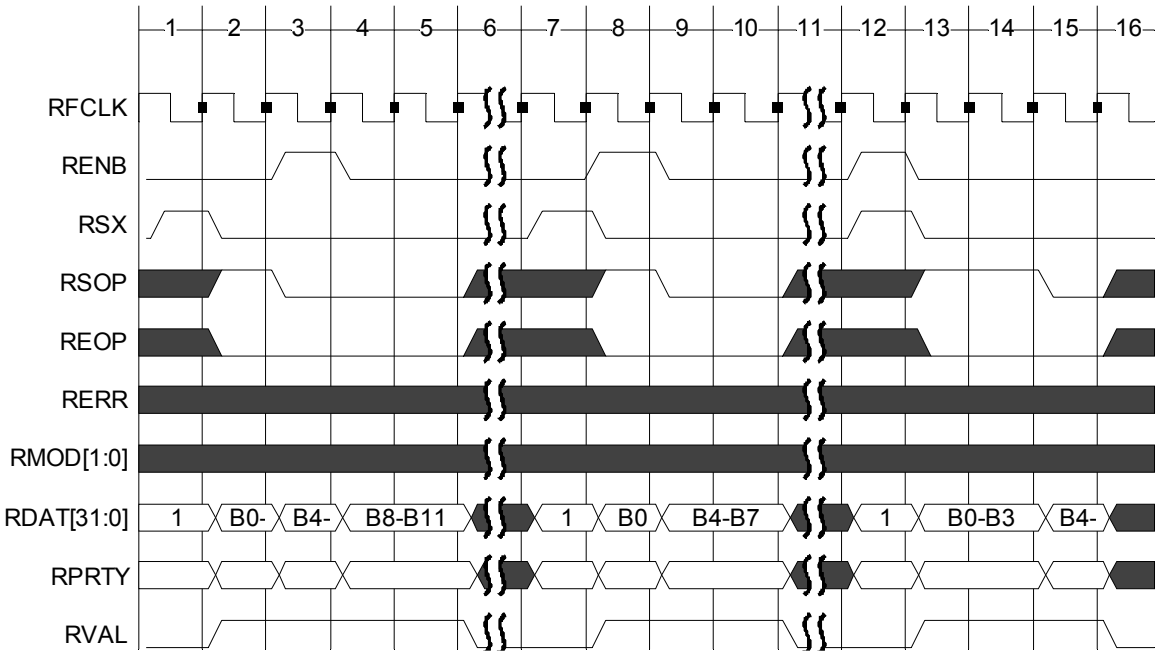


Figure 14 continues to look at the POS-PHY Level 3 receive interface as it is paused by the RENB signal. In case 1 the RENB is de-asserted in cycle 1 and 2. This causes the PM3386 to hold the RSX value as well as the in band address on the RDAT bus until assertion of RENB. In case 2 the RENB signal is de-asserted toward the end of a packet. In cycle 8 this has no effect on the previously finished frame. The same holds true in case 3 as is shown by cycle 11 RENB de-assertion to have no effect. However in case 4 we see that RENB

de-assertion in cycle 14 and 15 cause the RDAT, REOP, RERR, RMOD, RPRTY, and RVAL signals to hold value until the sampled assertion of RENB.

Figure 14 -PM3386 POS-PHY L3 Receive Logical Timing Cases B

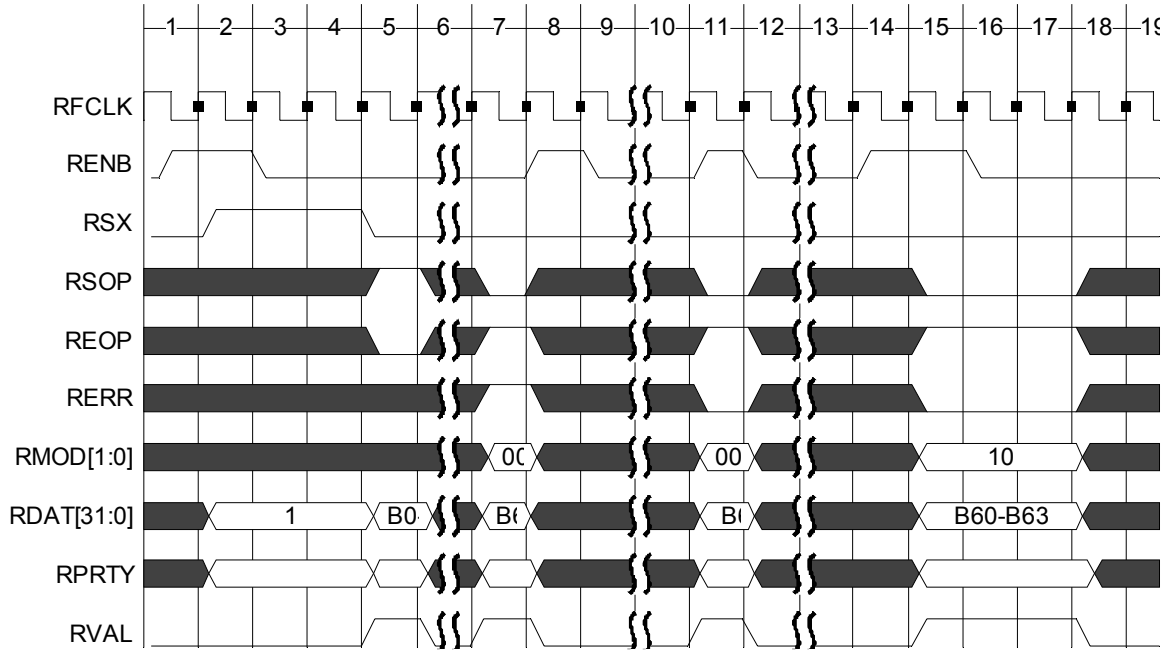
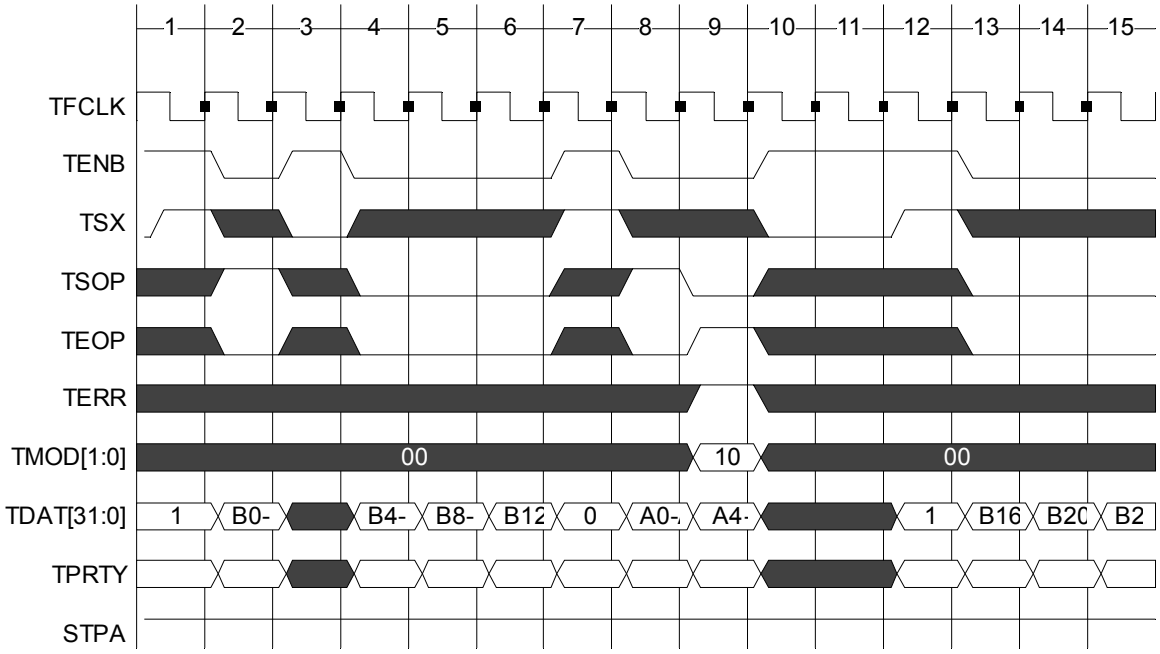


Figure 15 is an example of the PM3386 POS PHY Level 3 egress functional timing. Throughout the below transfer the STPA signal from the PM3386 stays asserted signaling the link device that there is room in the PM3386 FIFOs for the incoming frame. On cycle 1 the link device asserts TSX indicating the validity of the in-band address on the TDAT[7:0] bus pins. On cycle 2 the link starts the data transfer. The data transfers are qualified by TENB and the beginning of the frame is indicated by the TSOP being asserted. On cycle 3 the link device pauses the data transfer by de-asserting TENB. On cycles 4, 5, and 6 the link finishes the first burst of the frame and re-arbitrates channels to channel zero on cycle 7. Note that the link device does not assert TEOP in cycle 6 as it is not the end of a frame. On cycle 7 the link address channel zero and initiates data transfer on cycles 8 and 9. On cycle 9 the link ends the transfer with the TEOP. In this case the frame also contains an error so the TERR signal is asserted. TMOD qualifies the number of valid bytes on TDAT during cycle 9. Cycle 10 and 11 are optional link induced pause cycles. On cycle 12 the link arbitrates back to channel 1 and starts data transmission for that channel over the TDAT bus. Note that TSOP is not asserted in cycle 13 as it is not the start of frame.

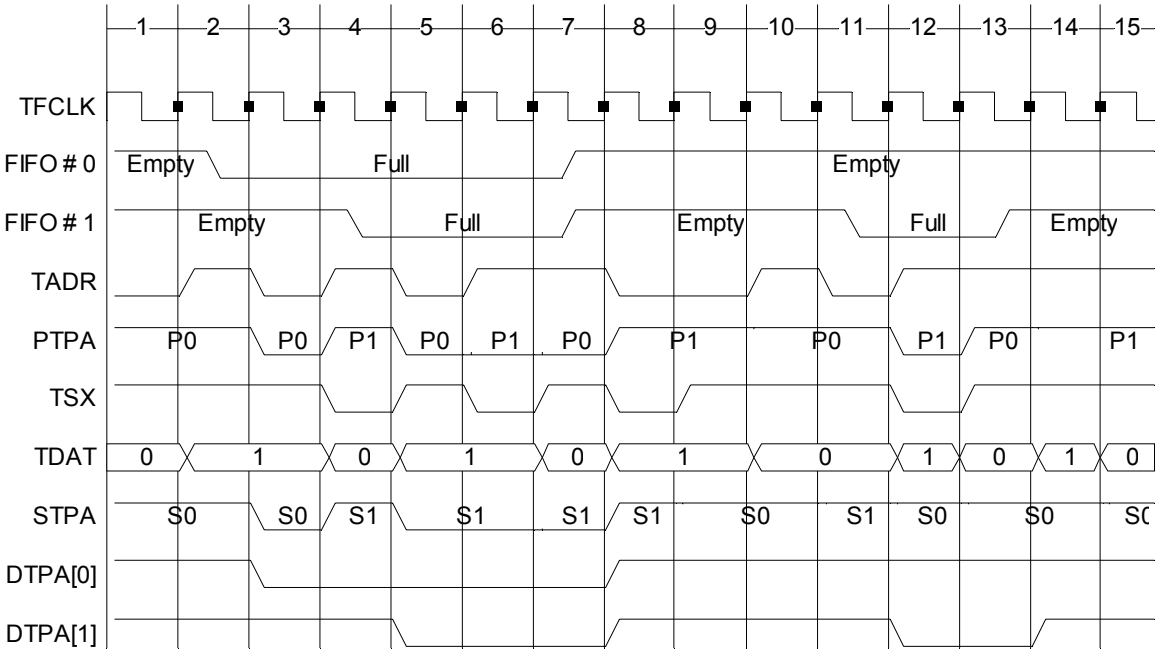
Figure 15 - PM3386 POS-PHY L3 Transmit Logical Timing



The PM3386 allows for three separate egress flow control signals that the link device may utilize during egress traffic generation. DTPA[1:0] is a direct indication from the PM3386 egress FIFO fill levels. STPA will indicate the PM3386 FIFO fill levels associated with the generated in-band address. PTPA will indicate the PM3386 FIFO fill levels for the polled channel via the TADR input. In all three cases all three indications are derived directly from the FIFO fill levels. Using all three indication methods are not a prerequisite for a given design. It is up to the implementer to choose which methods work for the given design implementation.

Figure 16 is an example PM3386 POS PHY Level 3 egress flow control signals. Included in the diagram is a representation of the egress FIFO fill levels. The signals are labeled FIFO # 0 and FIFO # 1. These states are used to help illustrate the relationship between the DTPA[1:0], STPA, and PTPA signals.

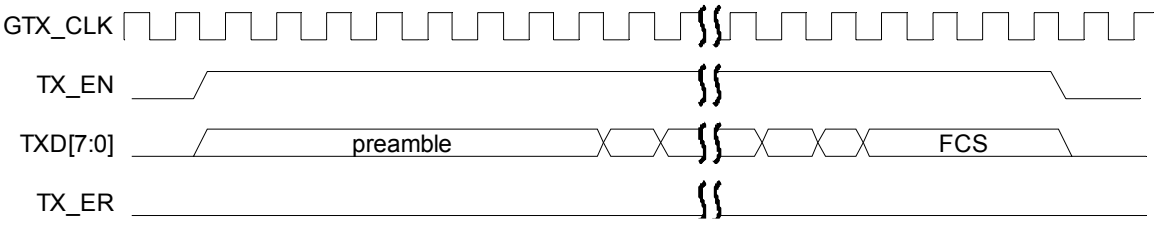
Figure 16 - PM3386 Packet-Level Transmit Polling Logical Timing



14.2 GMII Interface

Figure 17 depicts a common frame transmission on the GMII. The TX_EN in combination with TX_ER indicates that the PM3386 is presenting data on the GMII for transmission. TX_EN shall be asserted by the PM3386 synchronously with the first octet of the preamble and shall remain asserted while all octets to be transmitted are presented to the GMII. TX_EN shall be negated prior to the first rising edge of GTX_CLK following the final data octet of a frame. TX_EN is driven by the PM3386 and shall transition synchronously with respect to the GTX_CLK. TXD is a bundle of eight data signals (TXD[7:0]) that are driven by the PM3386. TXD shall transition synchronously with respect to the GTX_CLK. For each GTX_CLK period in which TX_EN is asserted and TX_ER is de-asserted, data are presented on the TXD to the PHY for transmission. TXD[0] is the least significant bit. While TX_EN and TX_ER are both de-asserted, TXD shall have no effect upon the PHY.

Figure 17 - GMII Basic Frame Transmission



TX_ER is driven by the PM3386 and shall transition synchronously with respect to the GTX_CLK. When TX_ER is asserted for one or more TX_CLK periods while TX_EN is also asserted, the PM3386 shall emit one or more non-valid data bytes. These bytes are not valid but do not represent the end of the packet. End of packet is only demonstrated by the de-assertion of TX_EN. Figure 18 represents a common transmission of a frame with errors.

Figure 18 - GMII Frame Transmission Error

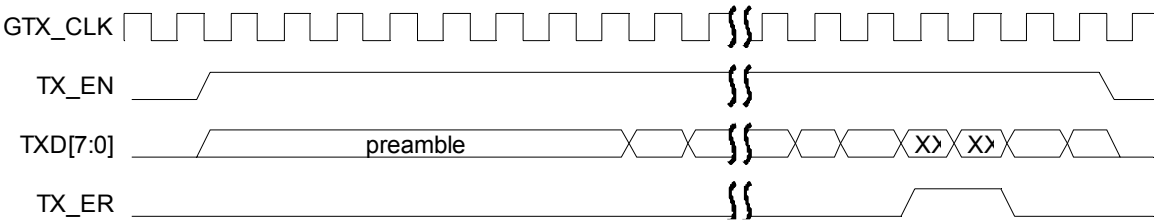
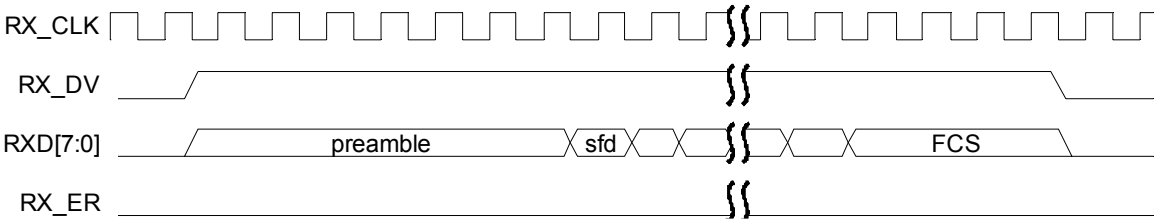


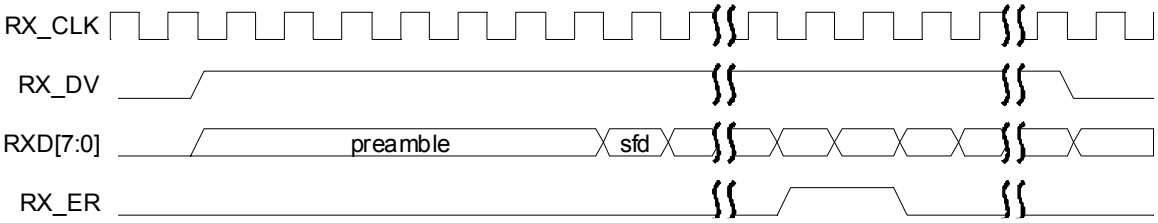
Figure 19 depicts a common received frame on the GMII interface. RX_DV is driven by the PHY to indicate that the PHY is presenting recovered and decoded data on the RXD[7:0] bundle. RX_DV shall transition synchronously with respect to the RX_CLK. RX_DV shall be asserted continuously from the first recovered octet of the frame through the final recovered octet and shall be negated prior to the first rising edge of RX_CLK that follows the final octet. In order for a received frame to be correctly interpreted by the PM3386, RX_DV must encompass the frame, starting no later than the Start Frame Delimiter (SFD) and excluding any End of Frame delimiter. RXD is a bundle of eight data signals (RXD[7:0]) that are driven by the PHY. RXD shall transition synchronously with respect to RX_CLK. For each RX_CLK period in which RX_DV is asserted, RXD transfers eight bits of recovered data from the PHY to the PM3386. RXD[0] is the least significant bit. In order for a frame to be correctly interpreted by the PM3386, a completely formed SFD must be passed across the GMII.

Figure 19 - GMII Basic Frame Reception



RX_ER is driven by the PHY and shall transition synchronously with respect to RX_CLK. When RX_DV is asserted, RX_ER shall be asserted for one or more RX_CLK periods to indicate to the PM3386 that an error (e.g. a coding error, or another error that the PHY is capable of detecting that may otherwise be undetectable at the MAC sub-layer) was detected somewhere in the frame presently being transferred from the PHY to the PM3386. Figure 20 depicts a common reception of a frame with errors.

Figure 20 - GMII Frame Reception With Error



14.3 Microprocessor Interface

The PM3386 supports a standard 16-bit microprocessor interface. The microprocessor bus can be used in a multiplexed fashion with both address and data being present on the board system bus or in a de-multiplexed fashion with the address and data on separate busses upon the system board.

Figure 21 represents the PM3386 microprocessor interface during a de-multiplexed read access. At point A the host drives the A bus with a valid read address. It is important to note that the host must drive a valid address on the A bus prior to assertion of the RDB signal. At point B the PM3386 is instructed to take ownership of the D bus by the assertion (active low) of CSB and RDB. Both CSB and RDB need to be asserted if accessing the PM3386. At point C the PM3386 drives the D bus with invalid data. At point D the PM3386 will present valid data to the host. The delay between point C and D is the internal access

time for reading the register. The PM3386 will continue to present valid data to the host until RDB or CSB are de-asserted. At point E the PM3386 is instructed by the host to relinquish control of the D bus by the de-assertion of RDB. At point F the PM3386 releases control over the D bus. The address on the A bus must be held for the entire read cycle. In this case at point G the host releases the valid address on the A bus. Please refer to the A.C. timing section for setup and hold time requirements.

Figure 21 - Microprocessor De-multiplexed Read Functional Timing

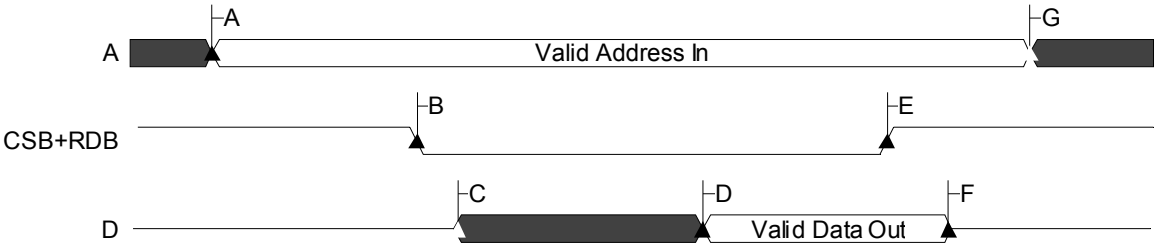


Figure 22 represents the PM3386 microprocessor interface during a de-multiplexed write access. At point A the host drives the A bus with a valid write address. It is important to note that the host must drive a valid address on the A bus prior to assertion of the WRB signal. At point B the host asserts (active low) both the CSB and WRB signals. At point C the host drives the D bus with valid write data. It is important to note that the host must drive valid data on the D bus prior to de-assertion of the WRB or CSB signals. At point D the host de-asserts WRB causing the PM3386 to internally write the data into the destined register. At point E the host removes the valid write data from the D bus. At point F the host removes the valid write address from the A bus.

Figure 22 - Microprocessor De-multiplexed Write Functional Timing

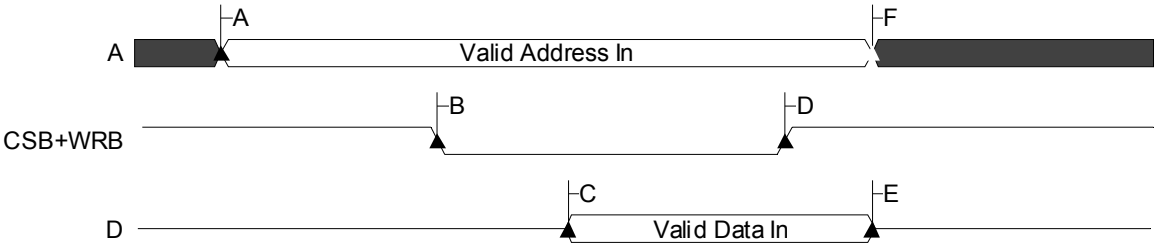


Figure 23 represents the PM3386 microprocessor interface during a multiplexed read access. The signal System Bus is used to illustrate the use of a shared system bus that might be implemented on the system board. The host presents a valid read address at points A and F. This address is latched into the PM3386 on the falling edge of ALE at point G. The host then turns the bus control over to the PM3386 by asserting RDB at point I. At point J the PM3386 starts to drive the bus with invalid data. At point K valid data is presented to the D bus and the System Bus. Valid data will continue to be present on the D bus until the host removes the D bus control from the PM3386 by de-assertion of the RDB signal at point L. At point M the PM3386 no longer drives the D or System Bus.

Figure 23 - Microprocessor Multiplexed Read Functional Timing

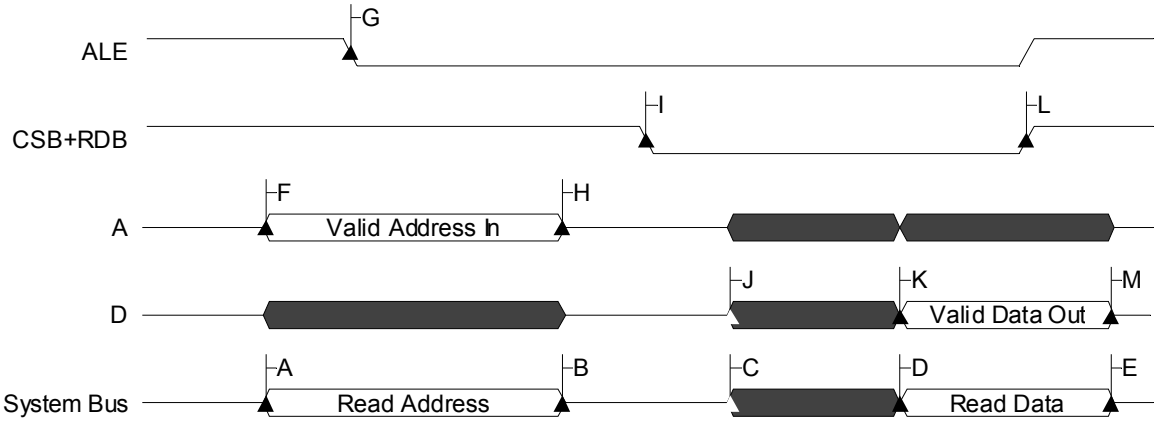
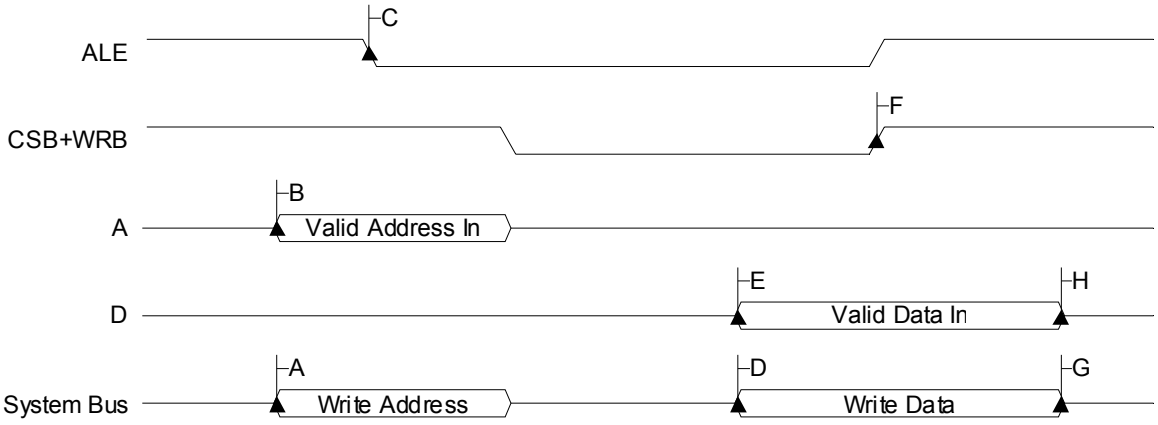


Figure 24 represents the PM3386 microprocessor interface during a multiplexed write access. The signal System Bus is used to illustrate the use of a shared system bus that might be implemented on the system board. The host presents a valid write address at points A and B. This address is latched into the PM3386 on the falling edge of ALE at point C. The host then drives valid write data on the System Bus and D bus at point E. Upon the de-assertion of WRB at point F the PM3386 will write the valid data in to the destined register. The host can then start another read or write cycle after point H.

Figure 24 - Microprocessor Multiplexed Write Functional Timing



15 ABSOLUTE MAXIMUM RATINGS

Maximum rating are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

Table 39 - Absolute Maximum Ratings

Storage Temperature	-40°C to +125°C
Core Supply Voltage	-0.3V to +1.89V
Supply Voltage	-0.3V to +3.46V
Voltage on Any Pin (except D[15:0], A[10:0], CSB, RDB, WRB and ALE)	-0.3V to VDDO+0.3V
Voltage on D[15:0], A[10:0], CSB, RDB, WRB and ALE	-0.3V t0 5.5V
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead Temperature	+230°C
Absolute Maximum Junction Temperature	+150°C

16 D.C. CHARACTERISTICS

T_A = -40°C to +85°C, V_{VDDI}= $VDDI_{typ}$± 5%, V_{VDDO} = $VDDO_{typical}$ ± 5%, V_{AVDH}= $AVDH_{typ}$± 5%, V_{AVDL}= $AVDL_{typ}$± 5%,

(Typical Conditions: T_A = 25°C, V_{VDDI} = 1.8V, V_{VDDO} = 3.3V, V_{AVDH} = 3.3V, V_{AVDL} = 1.8V)

Table 40: D.C. Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{VDDI}	Power Supply	1.71	1.8	1.89	Volts	Core Voltage
V_{VDDO}	Power Supply	3.14	3.3	3.46	Volts	I/O Voltage
V_{AVDH}	Power Supply	3.14	3.3	3.46	Volts	Analogy Voltage High
V_{AVDL}	Power Supply	1.71	1.8	1.89	Volts	Analogy Voltage Low
V_{IL}	Input Low Voltage	0		0.8	Volts	Guaranteed Input Low voltage.
V_{IH}	Input High Voltage	2.0			Volts	Guaranteed Input High voltage.
V_{IHC}	Input High Voltage	2.2			Volts	Guaranteed Input High voltage. For tfclk,rfclk,clk125,rx_clk0 and rx_clk1 only.
V_{OL}	Output or Bi-directional Low Voltage			0.4	Volts	Guaranteed output Low voltage at VDDO=3.0V and I_{OL}=maximum rated for pad.
V_{OH}	Output or Bi-directional High Voltage	2.4			Volts	Guaranteed output High voltage at VDDO=3.0V and I_{OH}=maximum rated current for pad.
V_{ODV}	PECL Output Differential Voltage	1.37	1.55	1.64	Vppd	100 Ω differential AC termination (30.5mA PECL)

V_{IDV}	PECL Input Differential Voltage	0.4		2.00	Vppd	100 Ω differential AC termination
V_{T+}	Reset Input High Voltage	2.4			Volts	Applies to RSTB and TRSTB only.
V_{T-}	Reset Input Low Voltage			0.8	Volts	Applies to RSTB and TRSTB only.
V_{TH}	Reset Input Hysteresis Voltage		0.53		Volts	Applies to RSTB and TRSTB only.
I_{ILPU}	Input Low Current	-300	-120	-10	µA	V_{IL} = GND. Notes 1 and 3.
I_{IHPU}	Input High Current	10	0	10	µA	V_{IH} = V_{DD}. Notes 1 and 3.
I_{ILPD}	Input Low Current	-10		10	µA	V_{IL} = GND. Notes 1 and 3.
I_{IHPD}	Input High Current	-350		-50	µA	V_{IH} = V_{DD}. Notes 1 and 3.
I_{IL}	Input Low Current	-10	0	+10	µA	V_{IL} = GND. Notes 2 and 3.
I_{IH}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DD}. Notes 2 and 3.
C_{IN}	Input Capacitance		5		pF	t_A=25°C, f = 1 MHz
C_{OUT}	Output Capacitance		5		pF	t_A=25°C, f = 1 MHz
C_{IO}	Bi-directional Capacitance		5		pF	t_A=25°C, f = 1 MHz
SERDES MODE						
P_{DDOP}	Operating Power		1.90		W	V_{DD} = typ, Outputs loaded @ 30 pf
I_{VDDO}	Operating Current		124		mA	V_{DD} = typ, Outputs loaded @ 30 pf
I_{VDDI}	Operating Current		320		mA	V_{DD} = typ, Outputs loaded @ 30 pf
I_{AVDH}	Operating Current		140		mA	V_{DD} = typ, Outputs loaded @ 30 pf
I_{AVDL}	Operating Current		250		mA	V_{DD} = typ, Outputs loaded @ 30 pf

GMII/TBI MODE						
P_{DDOP}	Operating Power		1.30		W	V_{DD} = typ, Outputs loaded @ 30 pf
I_{VDDO}	Operating Current		185		mA	V_{DD} = typ, Outputs loaded @ 30 pf
I_{VDDI}	Operating Current		320		mA	V_{DD} = typ, Outputs loaded @ 30 pf
I_{AVDH}	Operating Current		6		mA	V_{DD} = typ, Outputs loaded @ 30 pf
I_{AVDL}	Operating Current		50		mA	V_{DD} = typ, Outputs loaded @ 30 pf

Notes on D.C. Characteristics:

1. Input pin or bi-directional pin with internal pull-up resistor.
2. Input pin or bi-directional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

17 INTERFACE TIMING CHARACTERISTICS

T_A = -40°C to +85°C, VDDI = 1.8V±5% VDDO = 3.3V±5% AVDH = 3.3±5% AVDL = 1.8V±5%

Table 41 - Microprocessor Interface Multiplexed Read Access

Symbol	Parameter	Min	Typ	Max	Units
tSALR	Address to Latch Setup Time	10			ns
tHALR	Address to Latch Hold Time	10			ns
tVL	Valid Latch Pulse Width	20			ns
tSLR	Latch to Read Setup		0		ns
tHLR	Latch to Read Hold		5		ns
tDRD	Read to Data Bus Drive		0		ns
tPRD	Valid Read to Valid Data Propagation Delay			70	ns
tZRD	Valid Read Negated to Output Tri-state	0		20	ns

Figure 25 Microprocessor Interface Multiplexed Read Access

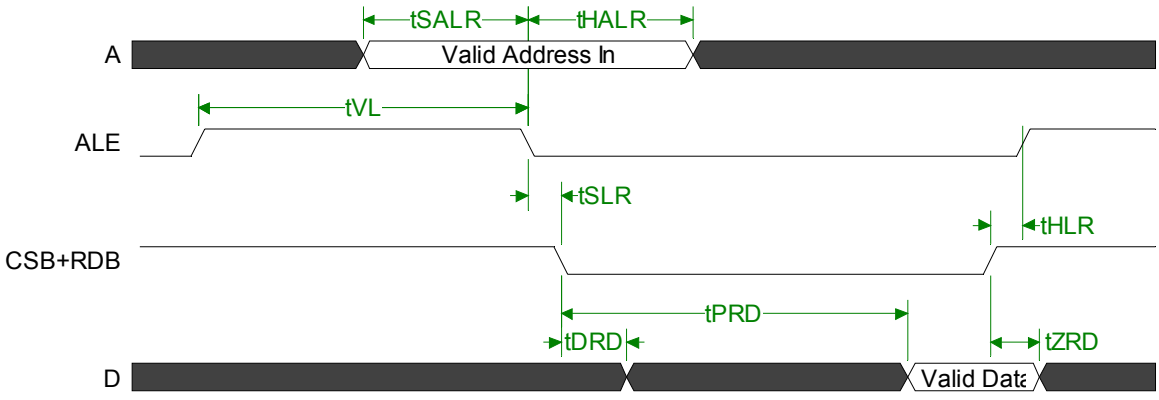
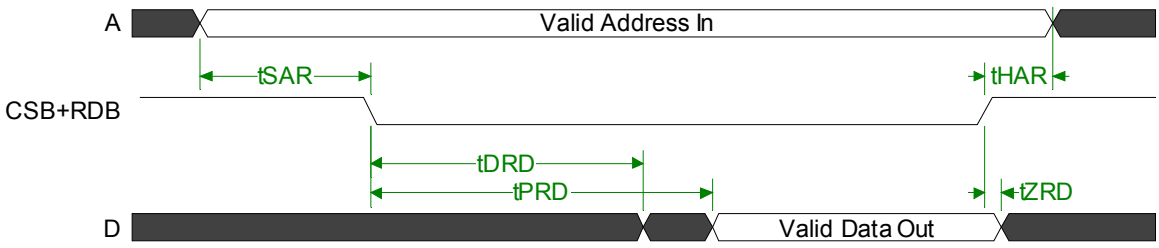


Table 42 - Microprocessor Interface De-multiplexed Read Access

Symbol	Parameter	Min	Typ	Max	Units
tSAR	Address to Valid Read Setup Time	10			ns
tHAR	Address to Valid Read Hold Time	5			ns
tDRD	Read to Data Bus Drive		0		ns
tPRD	Valid Read to Valid Data Propagation Delay			70	ns
tZRD	Valid Read Negated to Output Tri-state	0		20	ns

Figure 26 Microprocessor Interface De-Multiplexed Read Access



Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point to the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[15:0]).

3. A valid read cycle is defined as a logical AND of the CSB and the RDB signals.

4. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tVL and tSLR are not applicable.

5. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

6. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Table 43 - Microprocessor Interface Interrupt Timing

Symbol	Parameter	Min	Max	Units
tPintb	Valid Read Negated to INTB Negation		50	ns

Figure 27 Microprocessor Interface Interrupt Timing

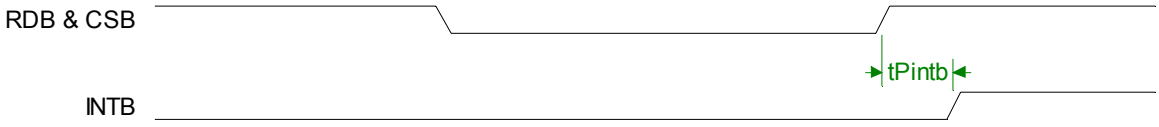


Table 44 - Microprocessor Interface Multiplexed Write Access

Symbol	Parameter	Min	Typ	Max	Units
tSALW	Address to Latch Setup Time	10			ns
tHALW	Address to Latch Hold Time	10			ns
tVL	Valid Latch Pulse Width	20			ns
tSLW	Latch to Write Setup	0			ns
tVWR	Valid Write Pulse Width	40			ns
tHLW	Latch to Write Hold	5			
tSDW	Data to Valid Write Setup Time	20			ns
tHDW	Data to Valid Write Hold Time	5			ns

Figure 28 Microprocessor Interface Multiplexed Write Access

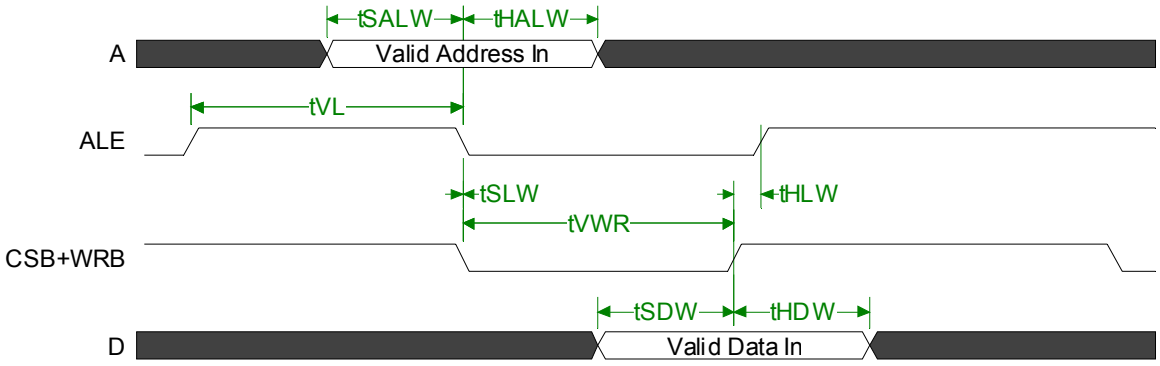
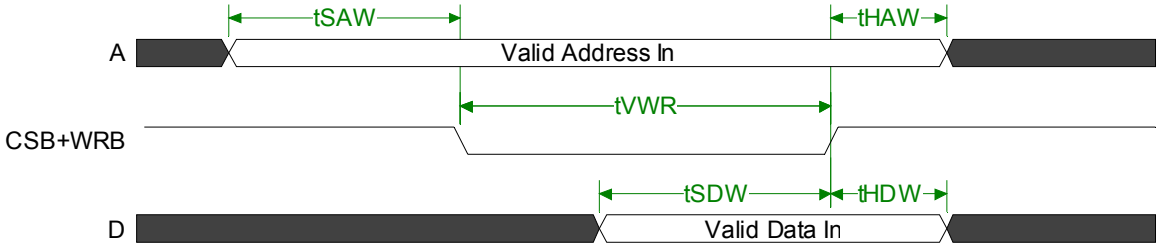


Table 45 - Microprocessor Interface De-Multiplexed Write Access

Symbol	Parameter	Min	Typ	Max	Units
tSAW	Address to Valid Write Setup Time		10		ns
tHAW	Address to Valid Write Hold Time	5			ns
tVWR	Valid Write Pulse Width	40			ns
tSDW	Data to Valid Write Setup Time	20			ns
tHDW	Data to Valid Write Hold Time	5			ns

Figure 29 Microprocessor Interface De-Multiplexed Write Access



Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical AND of the CSB and the WRB signals.
2. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tVL and tSLW are not applicable.
3. Parameter thaw is not applicable if address latching is used.
4. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
5. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Table 46 - RSTB Timing

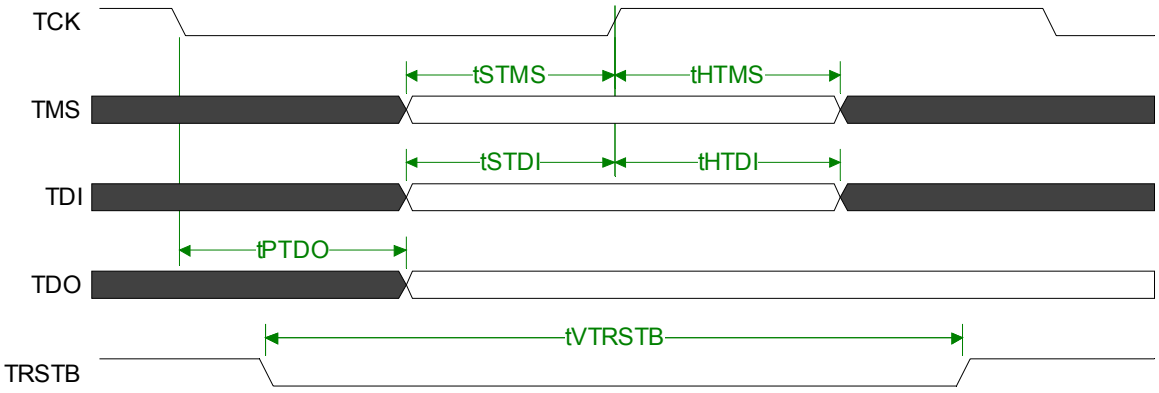
Symbol	Description	Min	Max	Units
tVRSTB	RSTB Pulse Width	1		ms

Figure 30 - RSTB Timing

Table 47 - JTAG Port Interface

Symbol	Description	Min	Max	Units
	TCK Frequency		1	MHz
	TCK Duty Cycle	40	60	%
tSTMS	TMS Set-up time to TCK	50		ns
tHTMS	TMS Hold time to TCK	50		ns
tSTDI	TDI Set-up time to TCK	50		ns
tHTDI	TDI Hold time to TCK	50		ns
tPTDO	TCK Low to TDO Valid	2	50	ns
tVTRSTB	TRSTB Pulse Width	100		ns

Figure 31 - JTAG Port Interface Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on JTAG Output Timing:

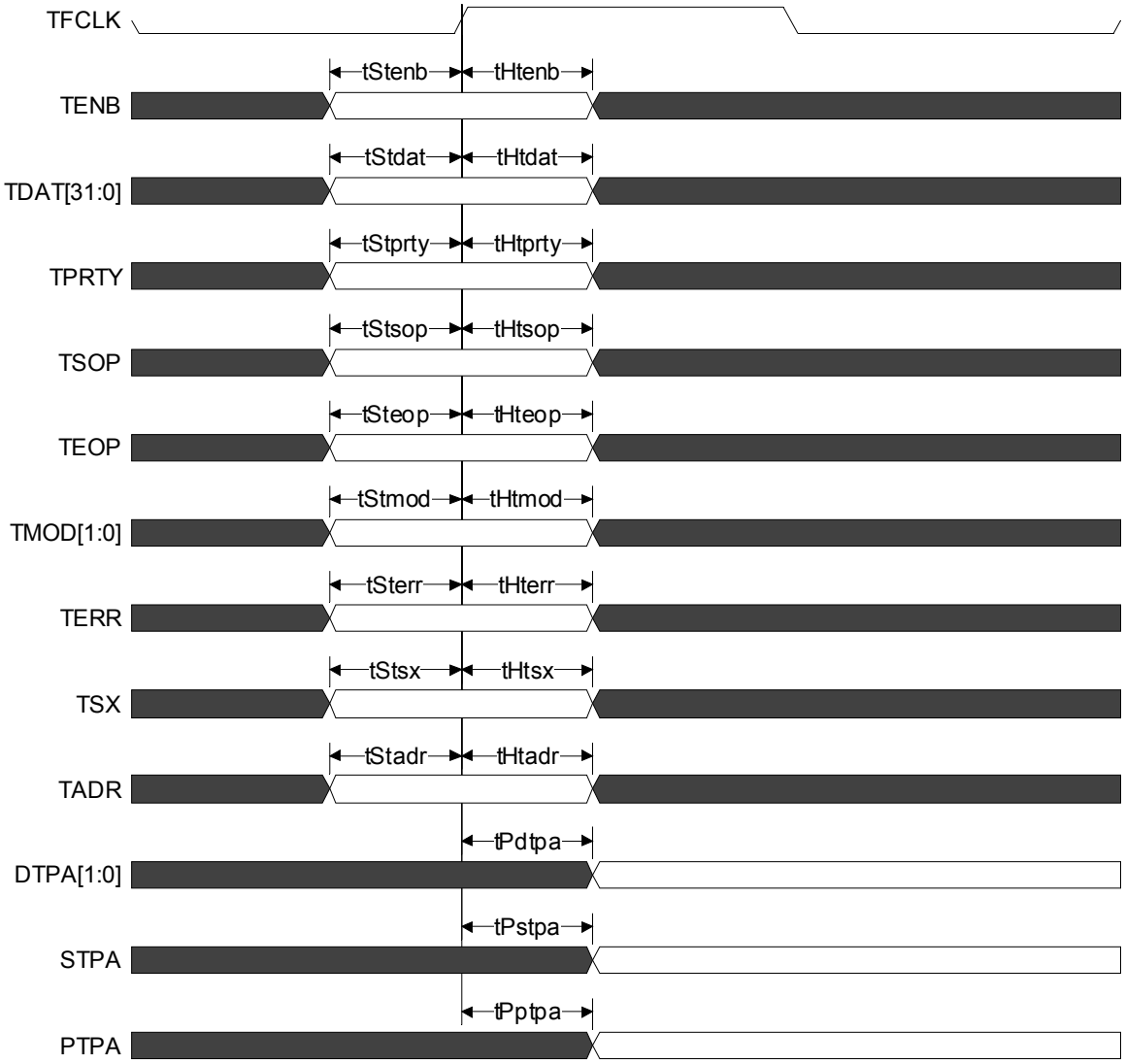
1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 30 pF load on the outputs.

Table 48 POS-PHY Transmit Interface Timing

Symbol	Description	Min	Max	Units
	TFCLK Frequency	60	104	MHz
	TFCLK Duty Cycle	40	60	%
tS_{tenb}	TENB Set-up time to TFCLK	2		ns
tH_{tenb}	TENB Hold time to TFCLK	1.25		ns
tS_{tdat}	TDAT[31:0] Set-up time to TFCLK	2		ns
tH_{tdat}	TDAT[31:0] Hold time to TFCLK	1.25		ns
tS_{tprty}	TPRTY Set-up time to TFCLK	2		ns
tH_{tprty}	TPRTY Hold time to TFCLK	1.25		ns
tS_{tsop}	TSOP Set-up time to TFCLK	2		ns
tH_{tsop}	TSOP Hold time to TFCLK	1.25		ns
tS_{teop}	TEOP Set-up time to TFCLK	2		ns
tH_{teop}	TEOP Hold time to TFCLK	1.25		ns
tS_{tmod}	TMOD[1:0] Set-up time to TFCLK	2		ns
tH_{tmod}	TMOD[1:0] Hold time to TFCLK	1.25		ns
tS_{terr}	TERR Set-up time to TFCLK	2		ns
tH_{terr}	TERR Hold time to TFCLK	1.25		ns
tS_{tsx}	TSX Set-up time to TFCLK	2		ns
tH_{tsx}	TSX Hold time to TFCLK	1.25		ns
tS_{tadr}	TADR Set-up time to TFCLK	2		ns
tH_{tadr}	TADR Hold time to TFCLK	1.25		ns
tP_{dtpa}	TFCLK High to DTPA[1:0] Valid	1.5	6.35	ns
tP_{stpa}	TFCLK High to STPA Valid	1.5	6.35	ns
tP_{ptpa}	TFCLK High to PTPA Valid	1.5	6.35	ns

Figure 32 - POS-PHY Level 3 Transmit Physical Timing



Notes on POS-PHY Transmit I/O Timing:

Note 1: When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Note 2: When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Note 3: Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

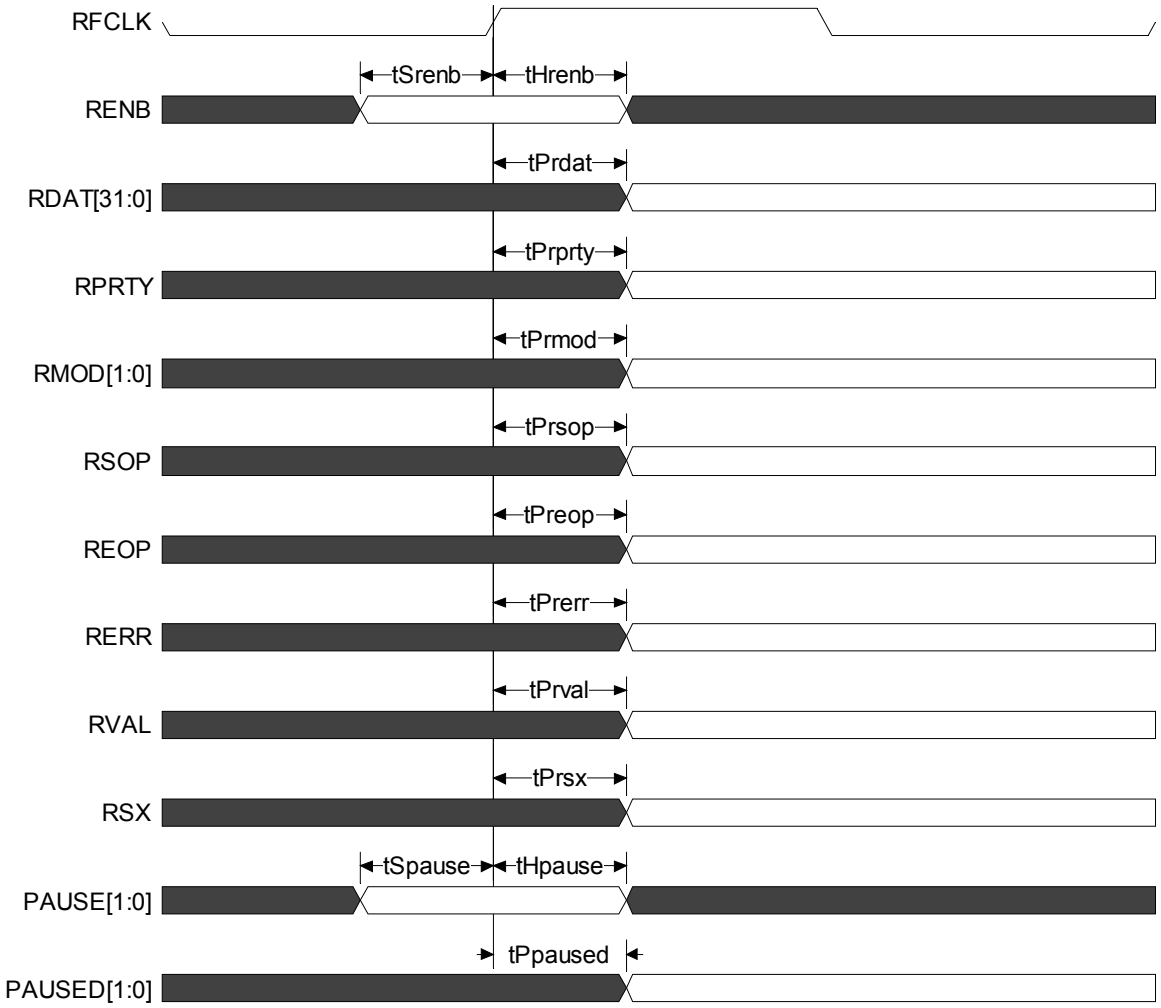
Note 4: Maximum output propagation delays are measured with a 30 pF load on the outputs.

Note 5: Minimum output propagation delays are measured with a 10 pF load on the outputs.

Table 49 POS-PHY Receive Interface Timing

Symbol	Description	Min	Max	Units
	RFCLK Frequency	60	104	MHz
	RFCLK Duty Cycle	40	60	%
tS_{renb}	RENB Set-up time to RFCLK	2		ns
tH_{renb}	RENB Hold time to RFCLK	1.25		ns
tP_{rdat}	RFCLK High to RDAT[31:0] Valid	1.5	6.35	ns
tP_{rprty}	RFCLK High to RPRTY Valid	1.5	6.35	ns
tP_{rsop}	RFCLK High to RSOP Valid	1.5	6.35	ns
tP_{reop}	RFCLK High to REOP Valid	1.5	6.35	ns
tP_{rmod}	RFCLK High to RMOD[1:0] Valid	1.5	6.35	ns
tP_{rerr}	RFCLK High to RERR Valid	1.5	6.35	ns
tP_{rval}	RFCLK High to RVAL Valid	1.5	6.35	ns
tP_{rsx}	RFCLK High to RSX Valid	1.5	6.35	ns
tS_{pause}	PAUSE[1:0] Set-up time to RFCLK	2		ns
tH_{pause}	PAUSE[1:0] Hold time to RFCLK	1.25		ns
tP_{paused}	RFCLK High to PAUSED[1:0] Valid	1.5	6.35	ns

Figure 33 - POS-PHY Receive Physical Timing



Notes on POS-PHY Receive I/O Timing:

Note 1: When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Note 2: When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Note 3: Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

Note 4: Maximum output propagation delays are measured with a 30 pF load on the outputs.

Note 5: Minimum output propagation delays are measured with a 10 pF load on the outputs.

Table 50. CLK125 Reference Clock Timing

Symbol	Parameter	Min	Typ	Max	Units
Fref	Nominal CLK_125 Reference Frequency	125		125	MHz
Fdev	Frequency Deviation from Nominal	-100		+100	ppm
DCref	CLK125 Reference Clock Duty Cycle	40		60	%
DJref	CLK_125 Reference Clock Deterministic Jitter (peak to peak above 200 KHz)			0.00756	UI ps
TJref	CLK_125 Reference Clock Total Jitter (peak to peak above 200 KHz)			0.020160	UI ps
tRFref	CLK_125 Reference Clock Rise / Fall Time		1		ns

Notes on Reference Clock Timing:

1. Rise time is measured from the 0.8 Volt threshold of the reference signal to the 2.0 Volt threshold of the reference signal.

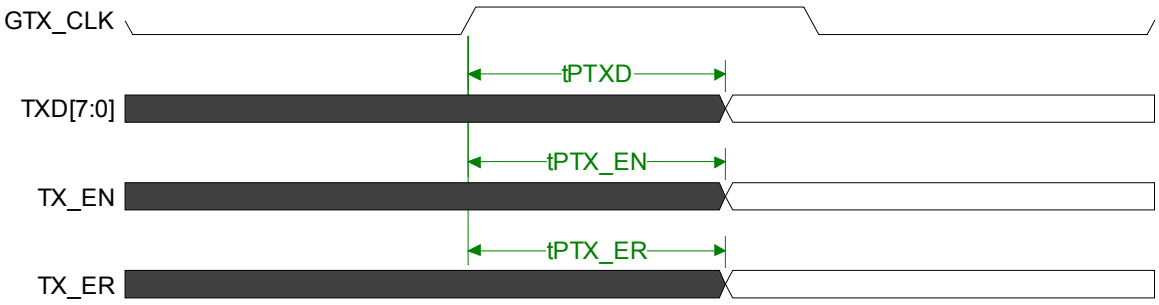
2. Fall time is measured from the 2.0 Volt threshold of the reference signal to the 0.8 Volt threshold of the reference signal.

3. Duty cycle and jitter are specified between crossings of the 1.4 Volt threshold of the reference signal.

Table 51 - GMII Transmit Interface Timing

Symbol	Description	Min	Max	Units
Fref	Nominal GTX_CLK Frequency	125	125	MHz
Fdev	Frequency Deviation from Nominal	- 100	+ 100	ppm
DCref	GX_CLK Duty Cycle	40	60	%
tPTXD	GTX_CLK high to TXD[7:0] valid	.5	4.5	ns
tPTX_EN	GTX_CLK high to TX_EN valid	.5	4.5	ns
tPTX_ER	GTX_CLK high to TX_ER valid	.5	4.5	ns

Figure 34 GMII Transmit Physical Timing



Notes on GMII Transmit I/O Timing:

Note 1: Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

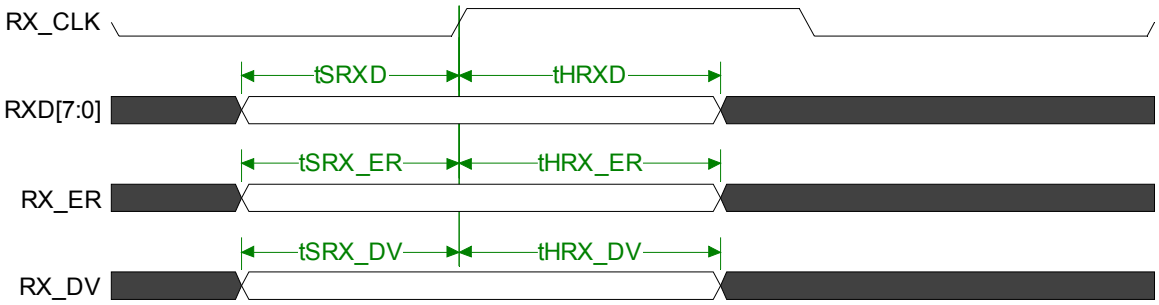
Note 2: Maximum output propagation delays are measured with a 30 pF load on the outputs.

Note 3: Minimum output propagation delays are measured with a 10 pF load on the outputs.

Table 52 - GMII Receive Interface Timing

Symbol	Description	Min	Max	Units
Fref	RX_CLK Frequency	125	125	MHz
Fdev	Frequency Deviation from Nominal	- 100	+ 100	ppm
Dcref	RX_CLK Duty Cycle	40	60	%
tSRXD	RXD[7:0] set-up time to RX_CLK	2		ns
tHRXD	RXD[7:0] hold time to RX_CLK	.25		ns
tSRX_ER	RX_ER set-up time to RX_CLK	2		ns
tHRX_ER	RX_ER hold time to RX_CLK	.25		ns
tSRX_DV	RX_DV set-up time to RX_CLK	2		ns
tHRX_DV	RX_DV hold time to RX_CLK	.25		ns

Figure 35 GMII Receive Physical Timing



Notes on GMII Receive I/O Timing:

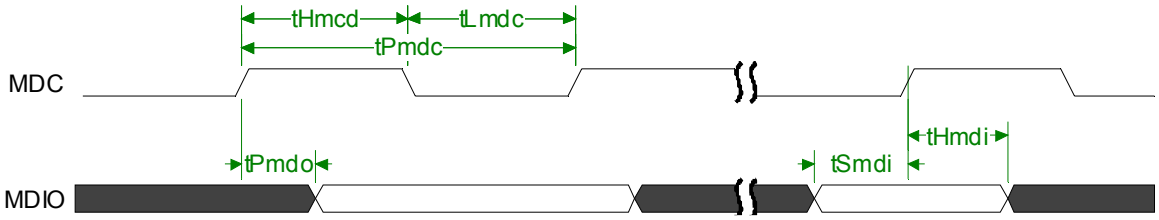
Note 1: When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Note 2: When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Table 53 - MDC / MDIO Interface Timing

Symbol	Description	Min	Typ	Max	Units
tPmcd	MDC Period	2.0		2.5	MHz
tHmcd	Time High MDC	160			ns
tLmcd	Time Low MDC	160			ns
tPmdo	MDC High to Valid MDIO Data	10		100	ns
tSmdi	MDIO Setup Time to MDC	15			ns
tHmdi	MDIO Hold Time to MDC		0		ns

Figure 36 - MDC / MDIO Physical Timing



Notes on MDC/MDIO I/O Timing:

Note 1: When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Note 2: When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Note 3: Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

Table 54. SERDES Transmit Data Timing

Symbol	Parameter	Min	Typ	Max	Units
Ftx	Nominal Transmit Frequency	1.25		1.25	GHz
Fdev	Frequency Deviation from Nominal	-100		+100	ppm
DJtx	Transmit Data Deterministic Jitter (peak to peak above 637 KHz)			0.10080	UI ps
TJtx	Transmit Data Total Jitter (peak to peak above 637 KHz)			0.265212	UI ps

Notes on Transmit Data Timing:

1. Total jitter includes both deterministic jitter and random jitter.
2. Values are measured with each PECL output AC coupled into a 50 Ohm impedance (100 Ohms differential impedance).
3. Rise time is measured from the 20% threshold of the reference signal to the 80% threshold of the reference signal.
4. Fall time is measured from the 80% threshold of the reference signal to the 20% threshold of the reference signal.
5. Jitter and skew are specified between crossings of the 50% threshold of the reference signal.

Table 55. SERDES Receive Data Timing

Symbol	Parameter	Min	Typ	Max	Units
Frx	Nominal Receive Frequency	1.25		1.25	GHz
Fdev	Frequency Deviation from Nominal	-100		+100	ppm
PJrxl	Receive Data Periodic Jitter (peak to peak from 750kHz to 20MHz)			0.400 360	UI ps
PJrxh	Receive Data Periodic Jitter (peak to peak above 20 MHz)		0.600 480		UI ps
DJrx	Receive Data Deterministic Jitter (peak to peak above 750 KHz)			0.462 370	UI ps
TJrx	Receive Data Total Jitter (peak to peak above 750 KHz)			0.749 599	UI ps

Notes on Receive Data Timing:

1. Periodic jitter is measured separately from total jitter.
2. Total jitter includes both deterministic jitter and random jitter. Total jitter excludes periodic jitter in excess of the specified maximum deterministic jitter.
3. Values are measured with each PECL input AC coupled into a 50 Ohm impedance (100 Ohms differential impedance).
4. Rise time is measured from the 20% threshold of the reference signal to the 80% threshold of the reference signal.
5. Fall time is measured from the 80% threshold of the reference signal to the 20% threshold of the reference signal.
6. Jitter and skew are specified between crossings of the 50% threshold of the reference signal.

18 ORDERING AND THERMAL INFORMATION

Table 56: Ordering Information

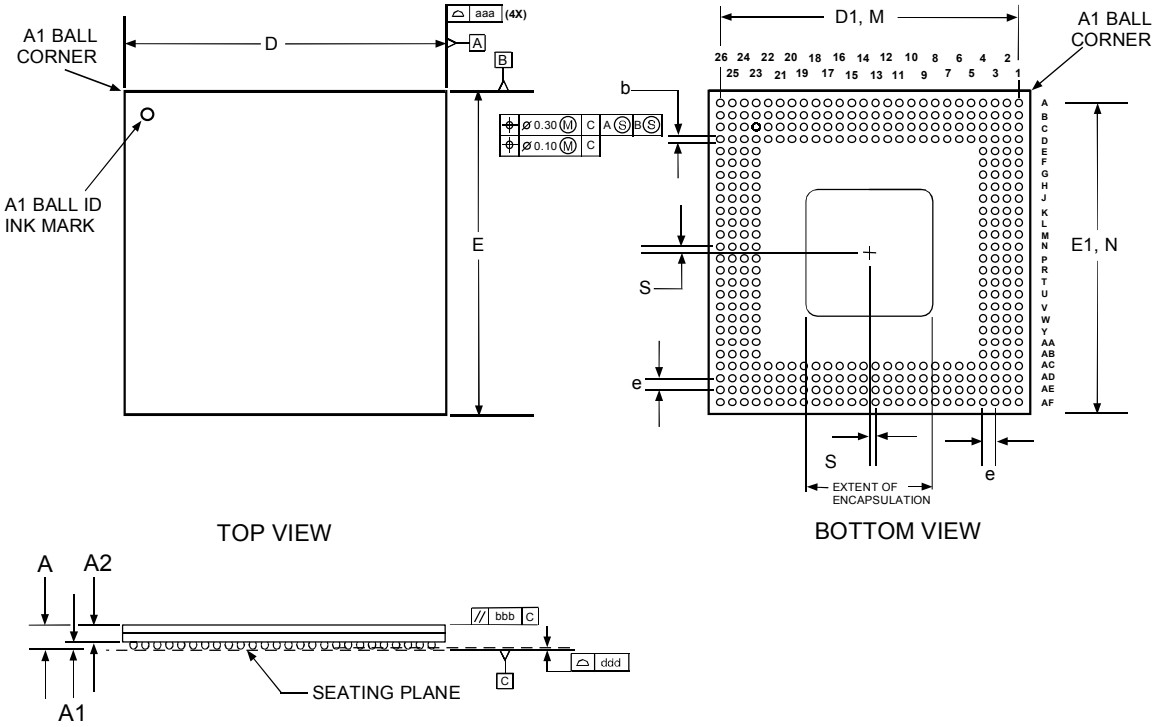
PART NO.	DESCRIPTION
PM3386-BI	352-pin Ultra Ball Grid Array (UBGA)

Table 57: Thermal Information

PART NO.	AMBIENT TEMPERATURE	Theta Ja	Theta Jc
PM3386-BI	-40°C to 85°C	18 °C/W	1 °C/W

19 MECHANICAL INFORMATION

Figure 37 -Mechanical 352 pin Thermally Enhanced Ball Grid Array (UBGA)



NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES PACKAGE BODY PROFILE.
3) DIMENSION bbb DENOTES PARALLEL.
4) DIMENSION ddd DENOTES COPLANARITY.

PACKAGE TYPE : 352 THERMALLY ENHANCED BALL GRID ARRAY - UBGA															
BODY SIZE : 27 x 27 x 1.47 MM															
Dim.	A	A_1	A_2	D	D_1	E	E_1	M,N	b	e	aaa	bbb	ddd	S	
Min.	1.32	0.40	0.92	26.90	-	26.90	-	-	0.50	-	-	-	-	0.45	
Nom.	1.47	0.50	0.97	27.00	25.00	27.00	25.00	26x26	0.63	1.00	-	-	-	0.50	
Max.	1.62	0.60	1.02	27.10	-	27.10	-	-	0.70	-	0.20	0.25	0.20	0.55	

NOTES:

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Contacting PMC-Sierra, Inc.
PMC-Sierra, Inc.
105-8555 Baxter Place Burnaby, BC
Canada V5A 4V7

Tel: (604) 415-6000

Fax: (604) 415-6200

Document Information: document@pmc-sierra.com
Corporate Information: info@pmc-sierra.com
Application Information: apps@pmc-sierra.com
(604) 415-4533
Web Site: http://www.pmc-sierra.com

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