# PM6681A

## Dual step-down controller with adjustable LDO

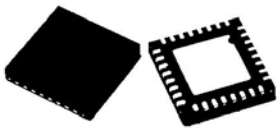
**Target Specification**

## Features

- 6V to 36V input voltage range
- Adjustable output voltages
- 0.9-3.3V LDO adjustable delivers 100mA peak current
- 5V LDO delivers 100mA peak current
- 1.237V ±1% reference voltage available
- NO $R_{SENSE}$ current sensing using low side MOSFETs' $R_{DS(on)}$
- Negative current limit
- Soft start internally fixed at 2ms
- Soft output discharge
- Latched UVP
- Not-latched OVP
- Selectable pulse skipping at light loads
- Selectable minimum frequency(33kHz) in pulse skip mode
- 5mW maximum quiescent power
- Indipendent power good signals
- Output voltage ripple compensation

## Applications

- Embedded computer system
- FPGA system power
- Industrial applications on 24V
- High performance and high density DC/DC modules



**VFQFPN-32 (5mm x 5mm)**

## Description

PM6681A is a dual step-down controller specifically designed to provide extremely high efficiency conversion, with lossless current sensing technique. The constant on-time architecture assures fast load transient response and the embedded voltage feed-forward provides nearly constant switching frequency operation. An embedded integrator control loop compensates the DC voltage error due to the output ripple. Pulse skipping technique increases efficiency at very light load. Moreover a minimum switching frequency of 33kHz is selectable to avoid audio noise issues. The PM6681A provides a selectable switching frequency, allowing three different values of switching frequencies for the two switching sections. The output voltages OUT1 and OUT2 can be adjusted from 0.9V to 5V and from 0.9V to 3.3V respectively. The device provides also 2 LDOs, 5V fixed and 0.9V-3.3V adjustable.

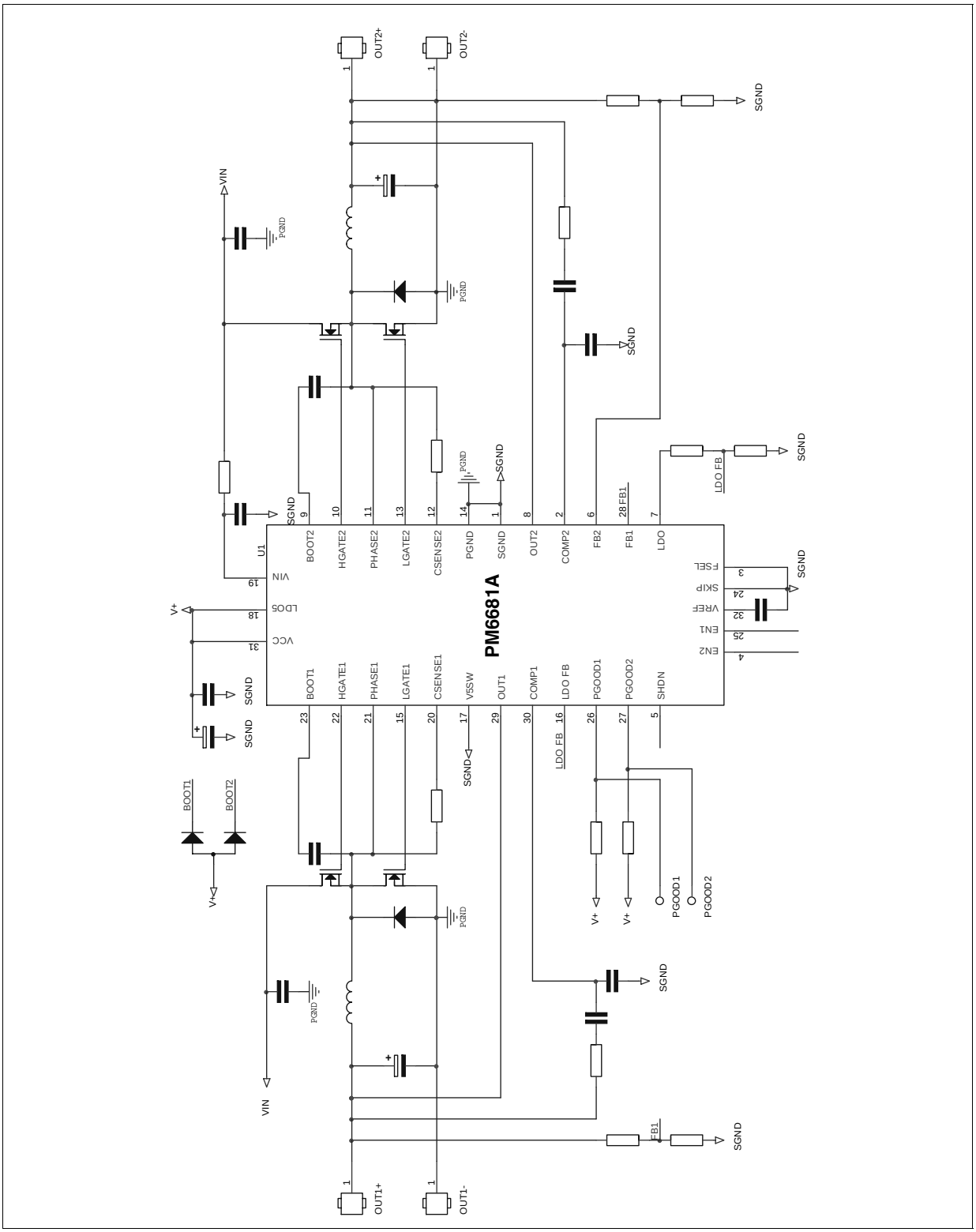
## Order codes

| Part number | Package | Packaging |
|---|---|---|
| PM6681A | VFQFPN-32 (5mm x 5mm) | Tube |
| PM6681ATR | VFQFPN-32 (5mm x 5mm) | Tape and Reel |

# Contents

# 1 Simplified application schematic

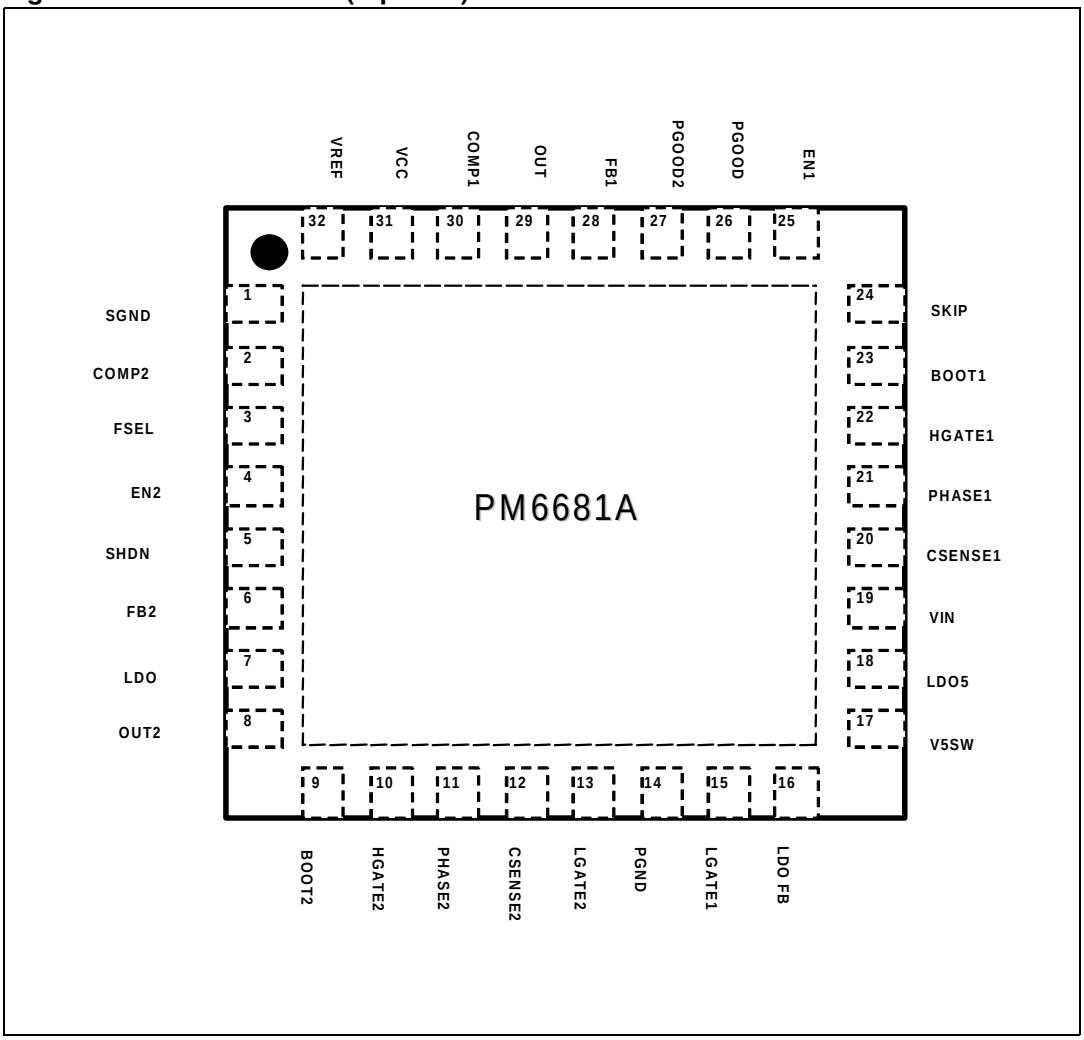
**Figure 1. Simplified application schematic**



# 2 Pin settings

## 2.1 Connections

**Figure 2. Pin connection (top view)**



## 2.2 Functions

**Table 1. Pin functions**

| N° | Pin | Function |
|---|---|---|
| 1 | SGND1 | Signal ground. Reference for internal logic circuitry. It must be connected to the signal ground plan of the power supply. The signal ground plan and the power ground plan must be connected together in one point near the PGND pin. |
| 2 | COMP2 | DC voltage error compensation pin for the switching section 2 |
| 3 | FSEL | Frequency selection pin. It provides a selectable switching frequency, allowing three different values of switching frequencies for the switching sections. |
| 4 | EN2 | Enable input for the switching section 2.<br>– The section 2 is enabled applying a voltage greater than 2.4V to this pin.<br>– The section 2 is disabled applying a voltage lower than 0.8V.<br>When the section is disabled the High Side gate driver goes low and Low Side gate driver goes high. If both EN1 and EN2 pins are low and SHDN pin is high the device enters in standby mode. |
| 5 | SHDN | Shutdown control input.<br>– The device switch off if the SHDN voltage is lower than the device off thershold (Shutdown mode)<br>– The device switch on if the SHDN voltage is greater than the device on threshold.<br>The SHDN pin can be connected to the battery through a voltage divider to program an undervoltage lockout. In shutdown mode, the gate drivers of the two switching sections are in high impedance (high-Z). |
| 6 | FB2 | Feedback input for the switching section 2 This pin is connected to a resistive voltage-divider from OUT2 to PGND to adjust the output voltage from 0.9V to 3.3V. |
| 7 | LDO | Adjustable internal regulator output. It can be set from 0.9V to 3.3V. LDO pin can provide a 100mA peak current. |
| 8 | OUT2 | Output voltage sense for the switching section 2.This pin must be directly connected to the output votage of the switching section. |
| 9 | BOOT2 | Bootstrap capacitor connection for the switching section 2. It supplies the high-side gate driver. |
| 10 | HGATE2 | High-side gate driver ouput for section 2. This is the floating gate driver output. |
| 11 | PHASE2 | Switch node connection and return path for the high side driver for the section 2. It is also used as negative current sense input. |
| 12 | CSENSE2 | Positive current sense input for the switching section 2. This pin must be connected through a resistor to the drain of the synchronous rectifier to obtain a positive current limit threshold for the power supply controller. |
| 13 | LGATE2 | Low-side gate driver output for the section 2. |
| 14 | PGND | Power ground. This pin must be connected to the power ground plan of the power supply. |
| 15 | LGATE1 | Low-side gate driver output for the section 1. |

**Table 1. Pin functions (continued)**

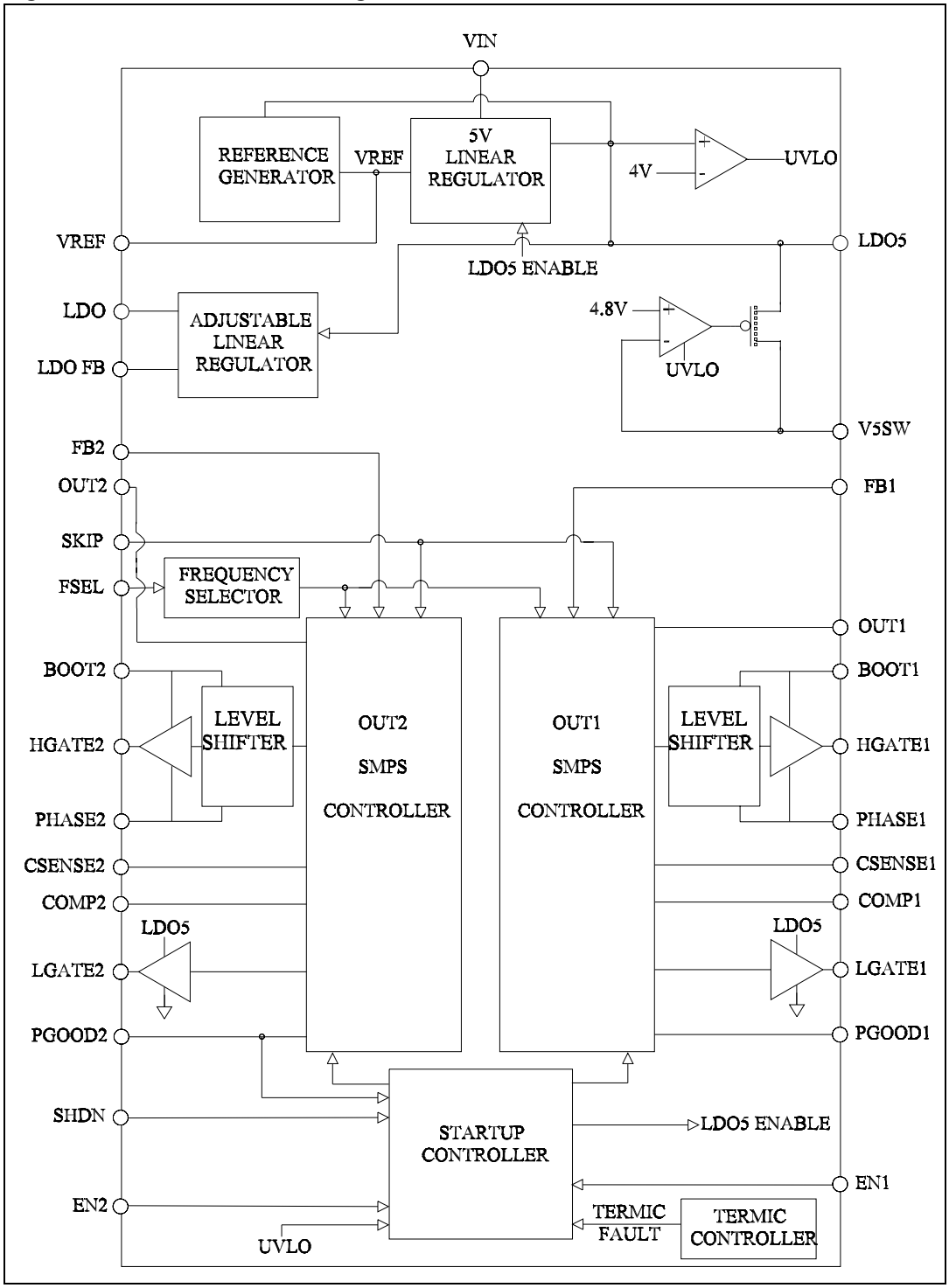
| N° | Pin | Function |
|---|---|---|
| 16 | LDO FB | Feedback input for the adjustable internal linear regulator. This pin is connected to a resistive voltage-divider from LDO to SGND to adjust the output voltage from 0.9V to 3.3V. |
| 17 | V5SW | Internal 5V regulator bypass connection.<br>– If V5SW is connected to OUT5 (or to an external 5V supply) and V5SW is greater than 4.9V, the LDO5 regulator shuts down and the LDO5 pin is directly connected to OUT5 through a 3W (max) switch.<br>If V5SW is connected to GND, the LDO5 linear regulator is always on. |
| 18 | LDO5 | 5V internal regulator output. It can provide up to 100mA peak current. LDO5 pin supplies embedded low side gate drivers and an external load. |
| 19 | VIN | Device supply voltage input and battery voltage sense. A bypass filter (4Ω and 4.7mF) between the battery and this pin is recommended. |
| 20 | CSENSE1 | Positive current sense input for the switching section 1. This pin must be connected through a resistor to the drain of the synchronous rectifier to obtain a positive current limit threshold for the power supply controller. |
| 21 | PHASE1 | Switch node connection and return path for the high side driver for the section 1.It is also used as negative current sense input. |
| 22 | HGATE1 | High-side gate driver ouput for section 1. This is the floating gate driver output. |
| 23 | BOOT1 | Bootstrap capacitor connection for the switching section 1. It supplies the high-side gate driver. |
| 24 | SKIP | Pulse skipping mode control input.<br>– If the pin is connected to LDO5 the PWM mode is enabled.<br>– If the pin is connected to GND, the pulse skip mode is enabled.<br>– If the pin is connected to VREF the pulse skip mode is enabled but the switching frequency is kept higher than 33KHz (No-audible puse skip mode). |
| 25 | EN1 | Enable input for the switching section 1.<br>– The section 1 is enabled applying a voltage greater than 2.4V to this pin.<br>– The section 1 is disabled applying a voltage lower than 0.8V.<br>When the section is disabled the High Side gate driver goes low and Low Side gate driver goes high. |
| 26 | PGOOD1 | Power Good ouput signal for the section 1. This pin is an open drain ouput and when the ouput of the switching section 1 is out of +/- 10% of its nominal value.It is pulled down. |
| 27 | PGOOD2 | Power Good ouput signal for the section 2. This pin is an open drain ouput and when the ouput of the switching section 2 is out of +/- 10% of its nominal value.It is pulled down. |
| 28 | FB1 | Feedback input for the switching section 1. This pin is connected to a resistive voltage-divider from OUT1 to PGND to adjust the output voltage from 0.9V to 5.5V. |
| 29 | OUT1 | Output voltage sense for the switching section 1.This pin must be directly connected to the output votage of the switching section. |

**Table 1. Pin functions (continued)**

| N° | Pin | Function |
|---|---|---|
| 30 | COMP1 | DC voltage error compensation pin for the switching section 1. |
| 31 | VCC | Device Supply Voltage pin. It supplies all the internal analog circuitry except the gate drivers (see LDO5). Connect this pin to LDO5. |
| 32 | VREF | Internal 1.237V high accuracy voltage reference. It can deliver 50uA. Bypass to SGND with a 100nF capacitor to reduce noise. |

# 3 Functional block diagram

**Figure 3. Functional block diagram**



# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

**Table 2. VFQFPN 5x5x1.0 32L Pitch 0.50**

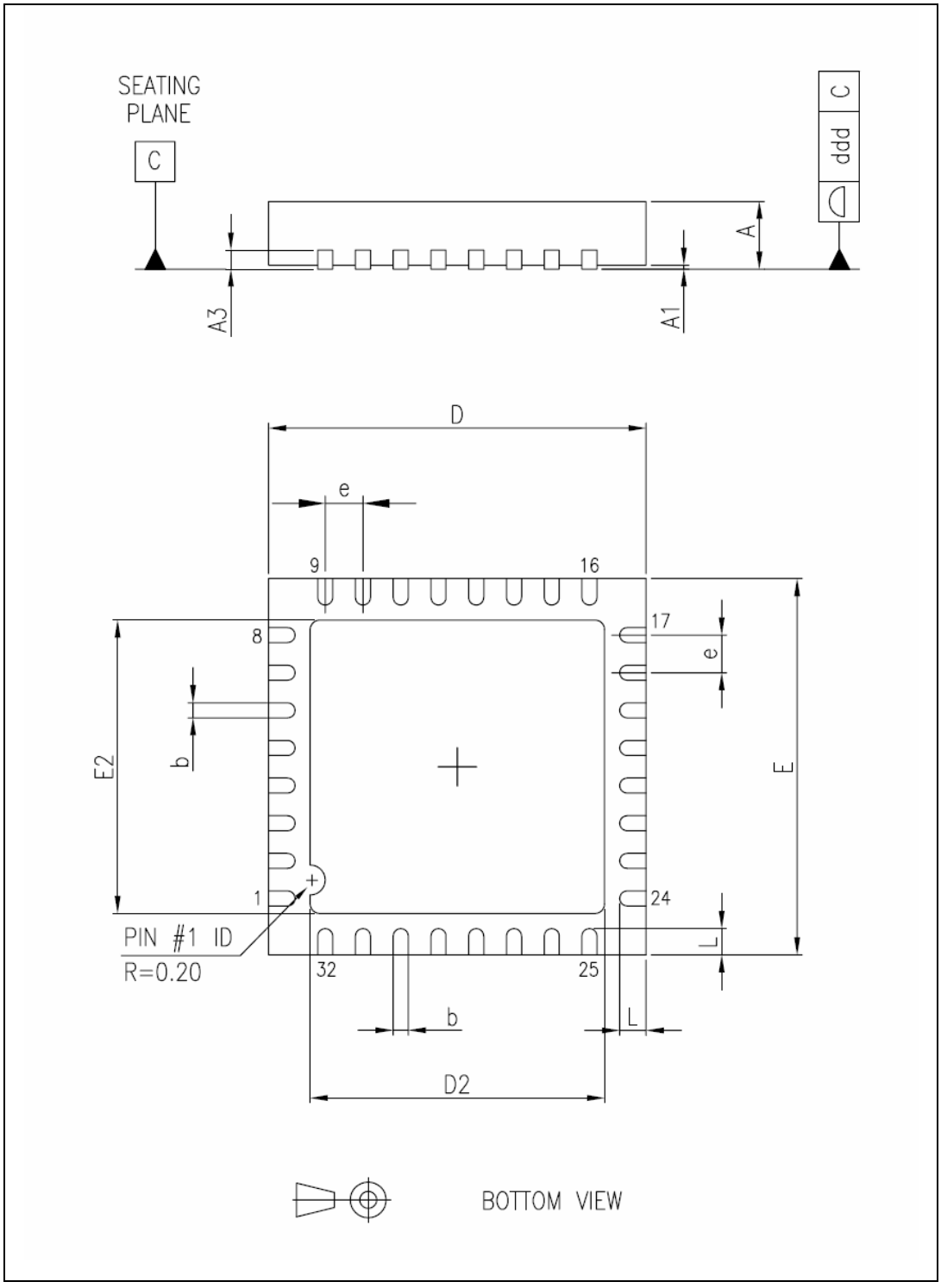
| Dim. | Databook (mm) | | |
|---|---|---|---|
| | Min | Typ | Max |
| A | 0.8 | 0.9 | 1 |
| A1 | 0 | 0.02 | 0.05 |
| A3 | | 0.2 | |
| b | 0.18 | 0.25 | 0.3 |
| D | 4.85 | 5 | 5.15 |
| D2 | See exposed pad variations (2) | | |
| E | 4.85 | 5 | 5.15 |
| E2 | See exposed pad variations (2) | | |
| e | | 0.5 | |
| L | 0.3 | 0.4 | 0.5 |
| ddd | | | 0.05 |

**Table 3. Exposed pad variations**

| D2 | | | E2 | | |
|---|---|---|---|---|---|
| Min | Typ | Max | Min | Typ | Max |
| 2.90 | 3.10 | 3.20 | 2.90 | 3.10 | 3.20 |

1. VFQFPN stands for Thermally Enhanced Very thin Fine pitch Quad Flat Package No lead. Very thin: A = 1.00mm Max.
2. Dimensions D2 & E2 are not in accordance with JEDEC.

**Figure 4. Package dimensions**



# 5 Revision history

**Table 4. Revision history**

| Date | Revision | Changes |
|---|---|---|
| 02-Nov-2006 | 1 | Initial release |

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