

PMK27XP

P-channel extremely low level FET

Rev. 01 — 15 January 2004

Product data

1. Product profile

1.1 Description

Extremely low level P-channel enhancement mode field-effect transistor in a plastic package using TrenchDMOS technology.

1.2 Features

- Low threshold
- Low on-state resistance.

1.3 Applications

- Load switching
- Battery packs
- Laptop computers
- Battery powered portable equipment.

1.4 Quick reference data

- $V_{DS} \leq -20$ V
- $I_D \leq -6.5$ A
- $P_{tot} \leq 2.5$ W
- $R_{DSon} = 27$ m Ω (typ).

2. Pinning information

Table 1: Pinning - SOT96-1 (SO-8), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)	<p>Top view MBK187</p>	<p>MBB075</p>
4	gate (g)		
5,6,7,8	drain (d)		

SOT 96-1 (SO-8)

3. Ordering information

Table 2: Ordering information

Type number	Package		Version
	Name	Description	
PMK27XP	S08	Plastic surface mounted package; 8 leads	SOT96-1



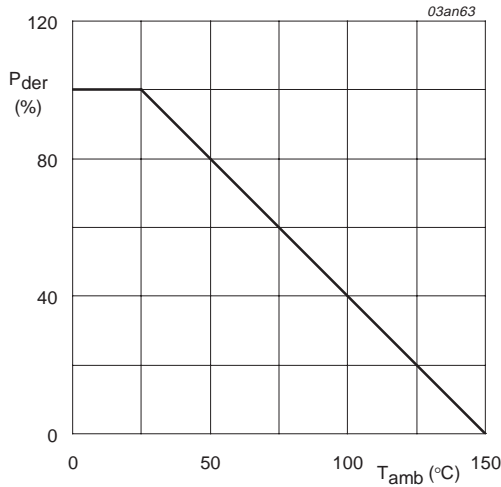
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4. Limiting values

Table 3: Limiting values

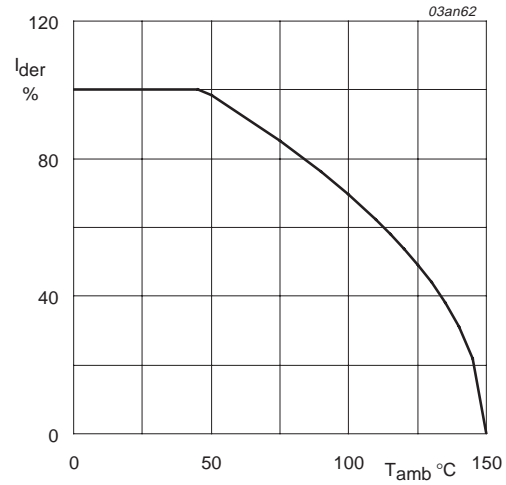
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$T_{amb} = 25\text{ °C}$	-	-20	V
I_D	drain current	$V_{GS} = -4.5\text{ V}; t_p < 10\text{ s}$			
		$T_{amb} = 25\text{ °C}; \text{Figure 2}$	-	-6.5	A
		$T_{amb} = 70\text{ °C}; \text{Figure 2}$	-	-5.2	A
		$V_{GS} = -4.5\text{ V}; t_p > 10\text{ s}$			
		$T_{amb} = 25\text{ °C}; \text{Figure 2}$	-	-4.6	A
		$T_{amb} = 70\text{ °C}; \text{Figure 2}$	-	-3.7	A
V_{GS}	gate-source voltage (DC)		-	-12	V
I_{DM}	peak drain current	$T_{amb} = 25\text{ °C}; \text{pulsed}; t_p \leq 300\text{ }\mu\text{s}; \text{Figure 3}$	-	-32	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}; t_p < 10\text{ s}; \text{Figure 1}$	-	2.5	W
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}; t_p > 10\text{ s}; \text{Figure 1}$	-	1.25	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	$T_{amb} = 25\text{ °C}$	-	-1.7	A



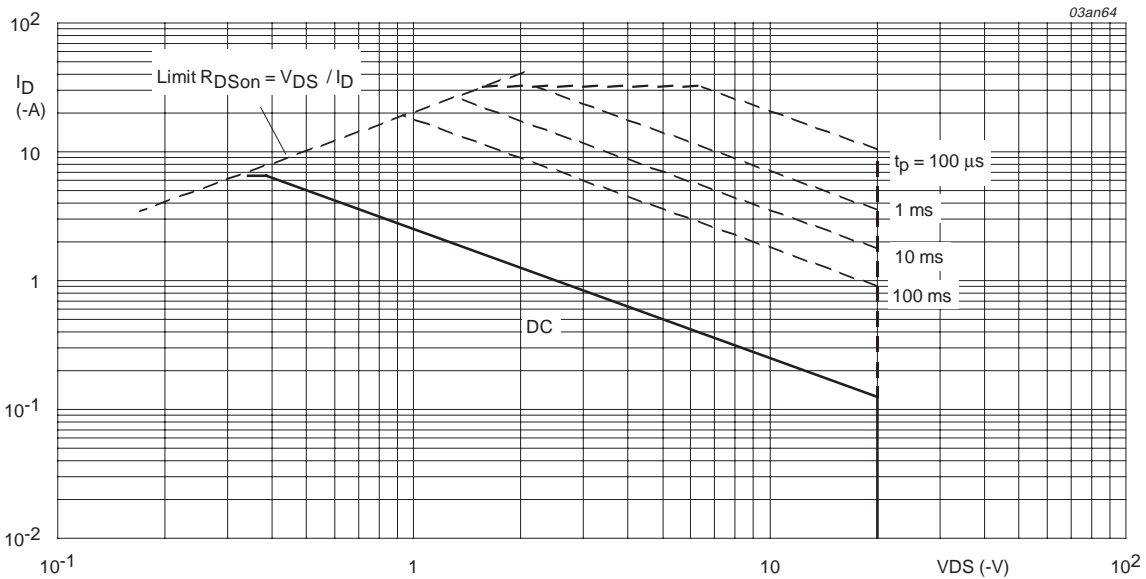
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



T_{amb} = 25 °C; I_{DM} is single pulse

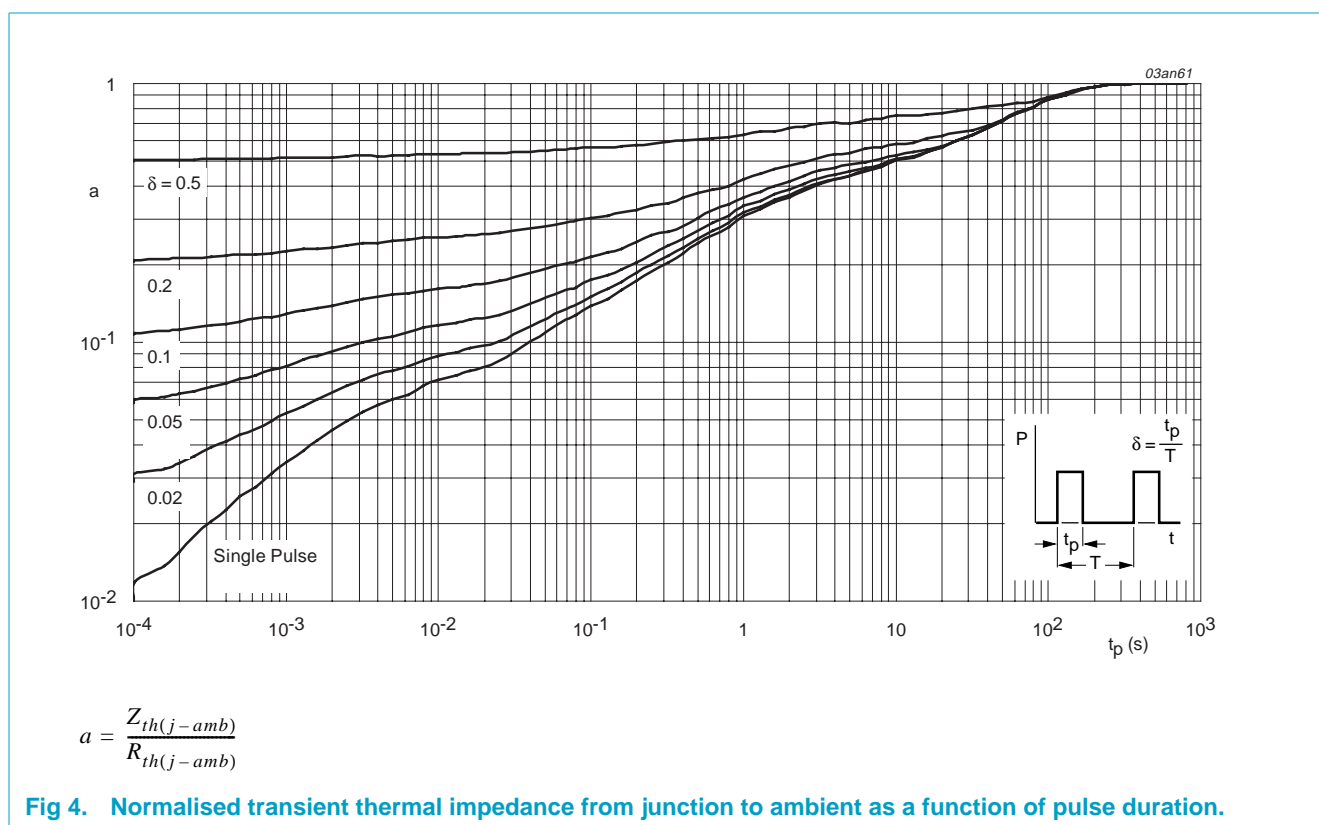
Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Figure 4	-	-	27	K/W
$R_{th(j-amb)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a printed-circuit board				
		steady state	-	-	100	K/W
		$t_p < 10$ s	-	-	50	K/W

5.1 Transient thermal impedance

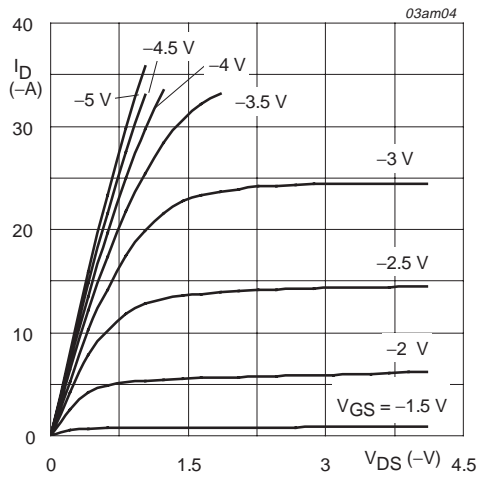


6. Characteristics

Table 5: Characteristics

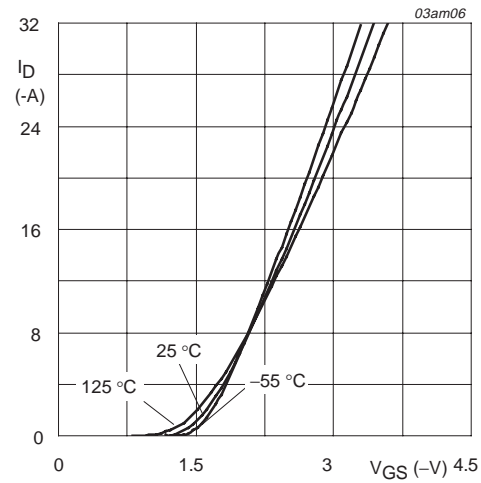
$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$	-20	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = -250\ \mu\text{A}$; $V_{DS} = V_{GS}$; Figure 9	-0.6	-	-	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0\ \text{V}$; $V_{DS} = -20\ \text{V}$	-	-	-1	μA
		$V_{GS} = 0\ \text{V}$; $V_{DS} = -16\ \text{V}$; $T_j = 70\text{ }^\circ\text{C}$	-	-	-5	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 12\ \text{V}$; $V_{DS} = 0\ \text{V}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -4.5\ \text{V}$; $I_D = -6.5\ \text{A}$; Figure 7 and 8	-	27	35	m Ω
		$V_{GS} = -2.5\ \text{V}$; $I_D = -5\ \text{A}$; Figure 7 and 8	-	46	60	m Ω
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$I_D = -6.5\ \text{A}$; $V_{DD} = -15\ \text{V}$; $V_{GS} = -4.5\ \text{V}$; Figure 12	-	13.6	-	nC
Q_{gs}	gate-source charge		-	2.3	-	nC
Q_{gd}	gate-drain (Miller) charge		-	5.5	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\ \text{V}$; $V_{DS} = -10\ \text{V}$; $f = 1\ \text{MHz}$; Figure 10	-	1044	-	pF
C_{oss}	output capacitance		-	273	-	pF
C_{rss}	reverse transfer capacitance		-	211	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = -15\ \text{V}$; $I_D = -6.5\ \text{A}$; $V_{GS} = -4.5\ \text{V}$; $R_G = 6\ \Omega$	-	10	-	ns
t_r	rise time		-	35	-	ns
$t_{d(off)}$	turn-off delay time		-	38	-	ns
t_f	fall time		-	50	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = -6.5\ \text{A}$; $V_{GS} = 0\ \text{V}$; Figure 11	-	-	-1.5	V



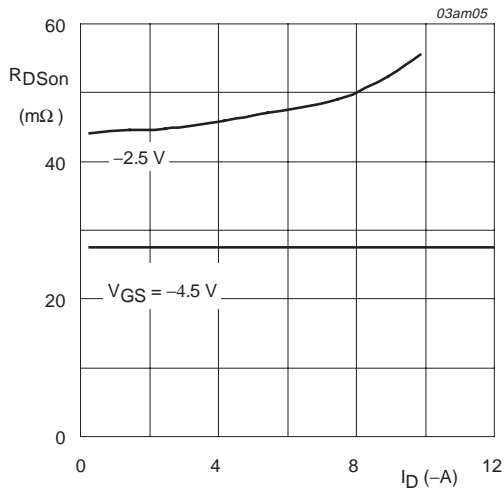
$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



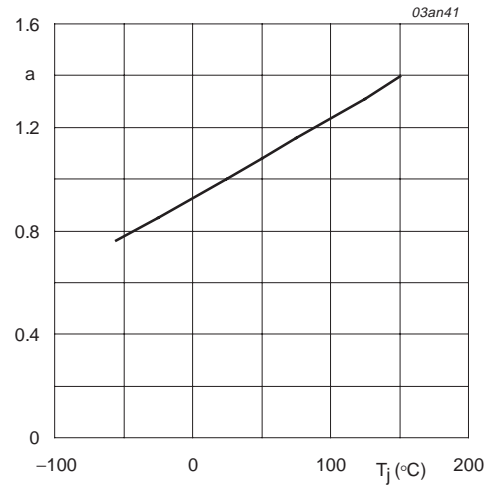
$T_j = -55^\circ\text{C}, 25^\circ\text{C}$ and $125^\circ\text{C}; V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



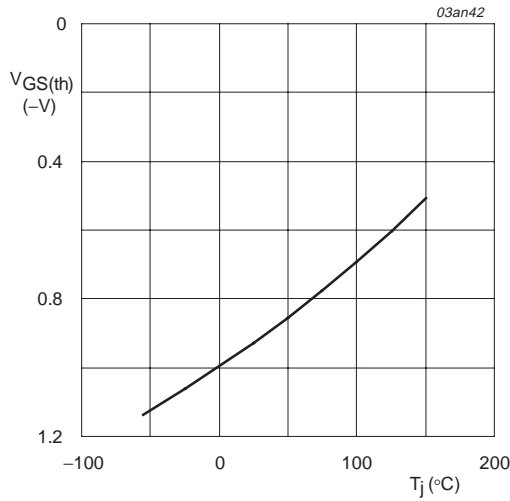
$T_j = 25^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



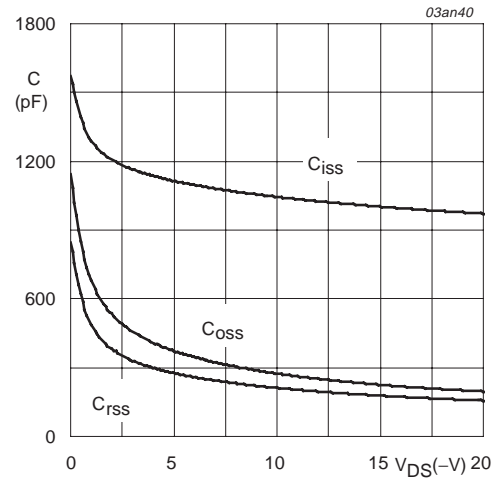
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



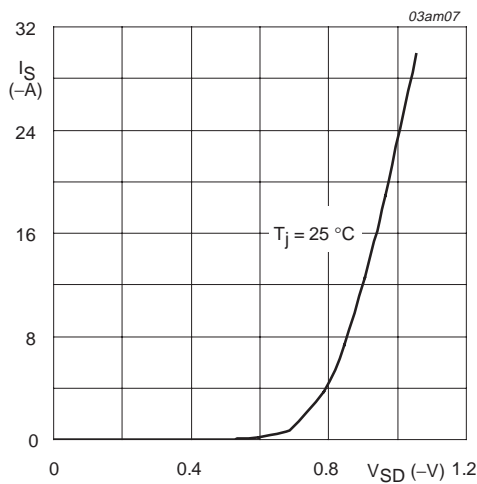
$I_D = -250 \mu A$; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature; typical values.



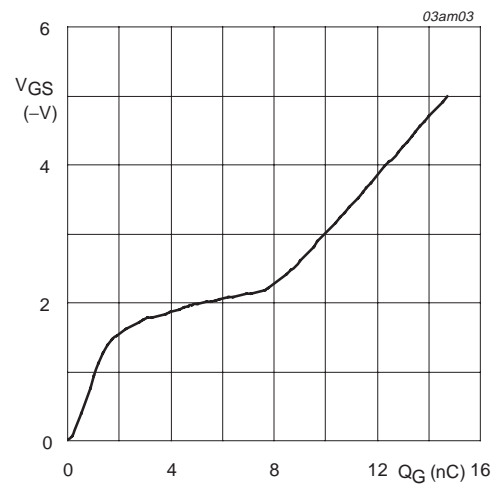
$V_{GS} = 0 V$; $f = 1 MHz$

Fig 10. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$V_{GS} = 0 V$

Fig 11. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = -6.5 A$; $V_{DD} = -15 V$

Fig 12. Gate-source voltage as a function of gate charge; typical values.

7. Package outline

S08: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

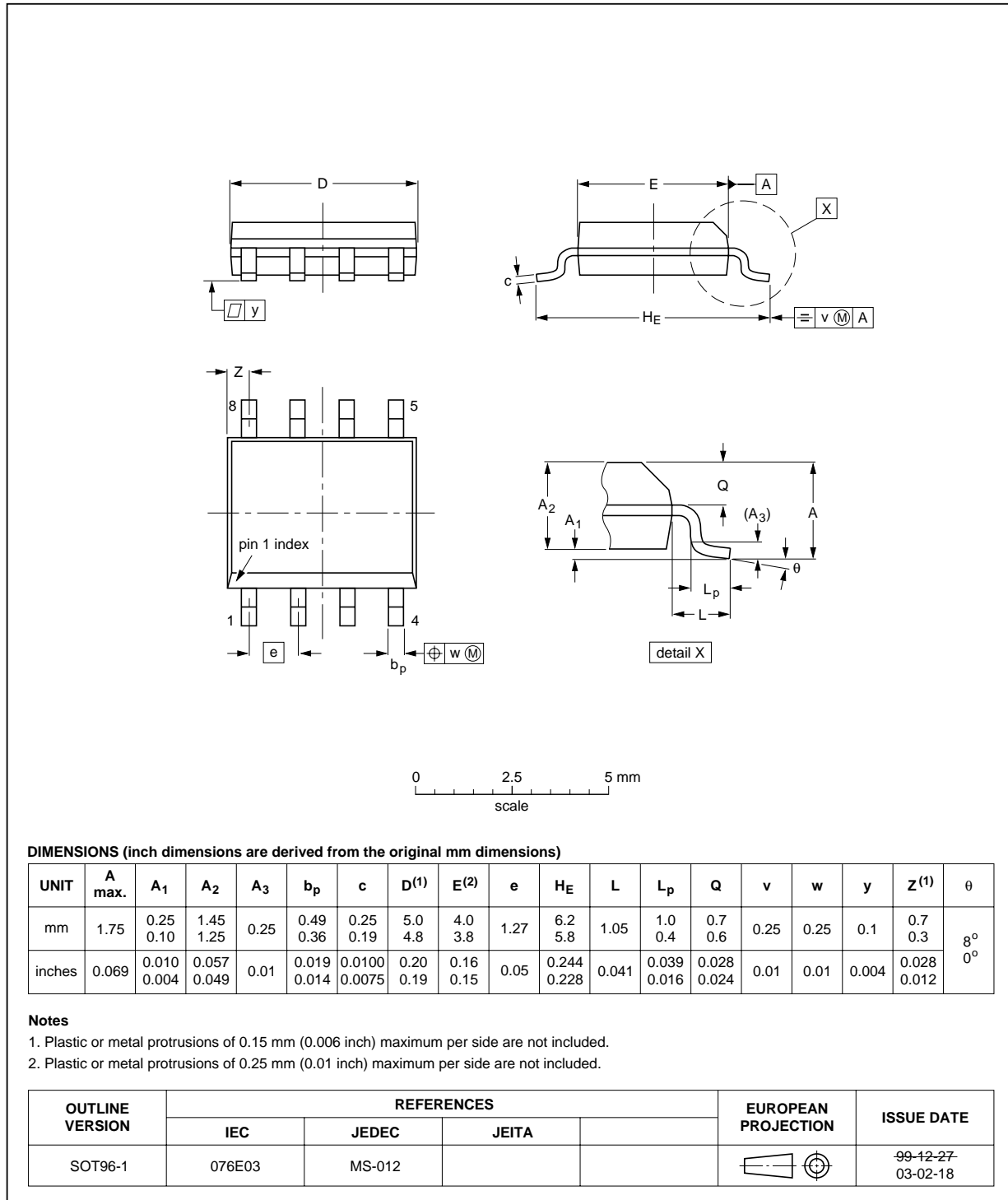


Fig 13. SOT96-1 (S08).

8. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20040115	-	Product data (9397 750 11549).

9. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Contact information

For additional information, please visit <http://www.semiconductors.philips.com>.

For sales office addresses, send e-mail to: sales.addresses@www.semiconductors.philips.com.

Fax: +31 40 27 24825

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