

Features

- Low On-Resistance (60-ohm typ.) Minimizes Distortion and Error Voltages
- Low Glitching Reduces Step Errors and Improves Settling Times. Charge Injection: <5pC
- Split-Supply Operation (+3V to +8V)
- Improved Second Sources for MAX398/MAX399
- On-Resistance Matching Between Channels: <6Ohm
- On-Resistance Flatness: <11-ohm
- Low Off-Channel Leakage,
 $I_{NO(OFF)} < 1\text{nA @ } +85^{\circ}\text{C}$, $I_{COM(ON)} < 2.5\text{nA @ } +85^{\circ}\text{C}$
- TTL/CMOS Logic Compatible
- Fast Switching Speed, $t_{TRANS} < 250\text{ns}$
- Break-Before-Make action eliminates momentary crosstalk
- Rail-to-Rail Analog Signal Range
- Low Power Consumption, <300μW
- Packaging (Pb-free & Green available):
- 16-pin SOIC (W)

Applications

- Data Acquisition Systems
- Audio Switching and Routing
- Test Equipment
- PBX, PABX
- Telecommunication Systems
- Battery-Powered Systems

Description

The PS398/PS399 are improved high precision analog multiplexers. The PS398, an 8-channel single-ended mux, selects one of eight inputs to a common output as determined by a 3-bit address A0-A2. An EN (enable) pin when low disables all switches, useful when stacking several devices. The PS399 is a 4-channel differential multiplexer. It selects one of four differential inputs to a common differential output as determined by a 2-bit address A0, A1. An EN pin may be driven low to disable all switches.

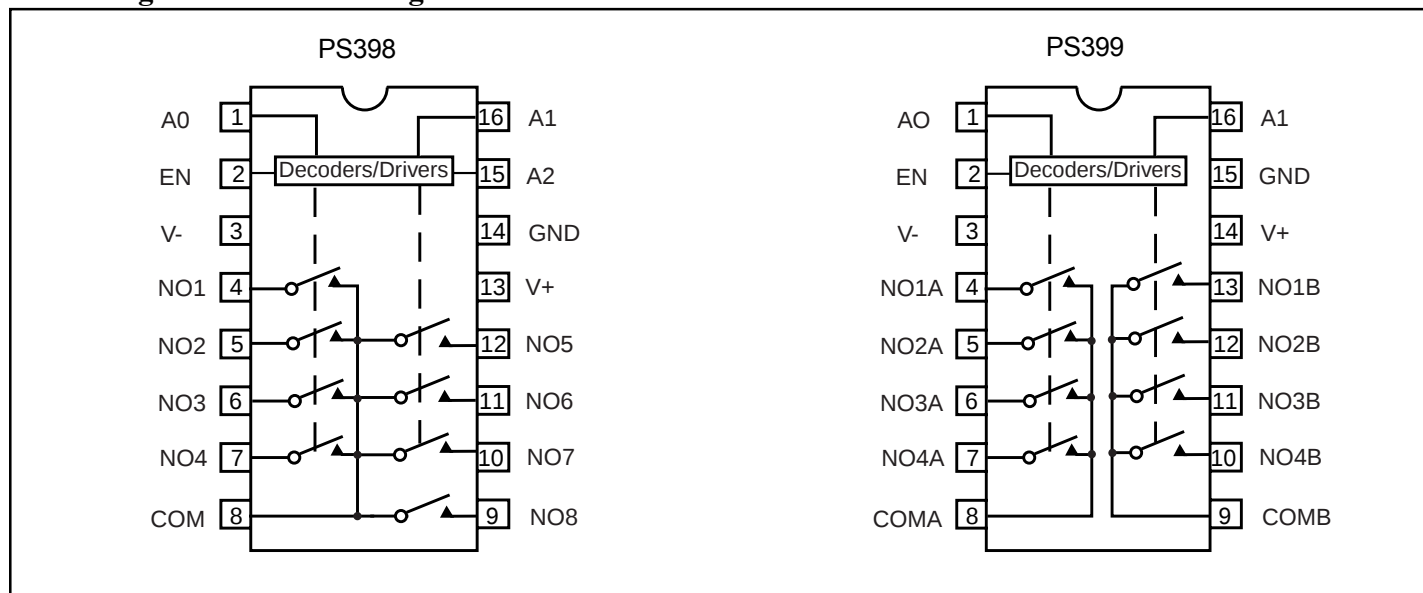
These multiplexers operate with dual supplies from +3V to +8V. Single-supply operation is possible from +3V to +15V.

With +5V power supplies, the PS398/PS399 guarantee <100-ohm on-resistance. On-Resistance matching between channels is within 6-ohm. On-Resistance flatness is less than 11-ohm over the specified signal range.

Each switch conducts current equally well in either direction when on. In the off state each switch blocks voltages up to the power-supply rails.

Both devices guarantee low leakage currents (<2.5nA at +85°C) and fast switching speeds ($t_{TRANS} < 250\text{ns}$). Break-before-make switching action protects against momentary crosstalk between channels.

Block Diagrams and Pin Configurations



Truth Tables

PS398				
A2	A1	A0	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

PS399			
A1	A0	EN	ON Switch
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Logic "0", $V_{AL} \leq 0.8V$

Logic "1", $V_{AH} \geq 2.4V$

Absolute Maximum Ratings

Voltages Referenced to V-

V+ -0.3V to +17V

GND -0.3V to +17V

GND -0.3V to (V+)+0.3V

V_{IN} , V_{COM} , V_{NO} (Note 1) (V-)-2V to (V+) +2V

or 30mA, whichever occurs first

Current (any terminal) 30mA

Peak Current, COM, NO, NC

(pulsed at 1ms, 10% duty cycle) 100mA

ESD per method 3015.7 >2000V

Thermal Information

Continuous Power Dissipation

SOIC (derate 8.7mW/°C above +70°C) 650mW

Storage Temperature -65°C to +150°C

Lead Temperature (soldering, 10s) +300°C

Note 1: Signals on NO, COM, or logic inputs exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to 30mA.

Caution: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.

Electrical Specifications - Dual Supplies ($V_{\pm} = \pm 5V \pm 10\%$, $GND = 0V$, $V_{AH} = V_{ENH} = 2.4V$, $V_{AL} = V_{ENL} = 0.8V$)

Parameter	Symbol	Conditions		Temp. (°C)	Min. ⁽²⁾	Typ. ⁽¹⁾	Max. ⁽²⁾	Units	
Analog Switch									
Analog Signal Range ⁽³⁾	V _{ANALOG}			Full	V-		V+	V	
On Resistance	R _{ON}	V+ = 4.5V, V- = -4.5V, V _{COM} = ±3.5V I _{NO} = 1mA,		25		60	100	Ohm	
				Full			125		
On-Resistance Match Between Channels ⁽⁴⁾	ΔR _{ON}	V _{COM} or V _{NC} = ±3.5V, I _{NO} = 1mA, V+ = 5V, V- = -5V		25			6		
				Full			8		
On-Resistance Flatness ⁽⁵⁾	R _{FLAT(ON)}	V+ = 5V, V- = -5V, I _{NO} = 1mA, V _{COM} = ±3V, 0V		25			11		
				Full			14		
NO Off Leakage Current ⁽⁶⁾	I _{NO(OFF)}	V+ = 5.5V, V- = -5.5V, V _{COM} = ±4.5V, V _{NO} = ±4.5V		25	-0.1		0.1	nA	
				Full	-1.0		1.0		
COM-Off Leakage Current ⁽⁶⁾	I _{COM(OFF)}	V+ = 5.5V, V- = -5.5V V _{COM} = ± 4.5V, V _{NO} = -/+4.5V		PS398	25	-0.2			50
					Full	-2.5			100
				PS399	25	-0.1			50
					Full	-1.5			100
COM On Leakage Current ⁽⁷⁾	I _{COM(ON)}	V+ = 5.5V, V- = -5.5V V _{COM} = ±4.5V V _{NO} = 4.5V		PS398	25	-0.4			0.4
					Full	-5			5
				PS399	25	-0.2		0.2	
					Full	-2.5		2.5	
Logic Input									
Logic High Input Voltage	V _{AH} , V _{ENH}			Full	2.4			V	
Logic Low Input Voltage	V _{AL} , V _{ENL}						0.8		
Input Current with Input Voltage High	I _{AH} , I _{ENH}	V _A = V _{EN} = 2.4V			-0.1		0.1	μA	
Input Current with Input Voltage Low	I _{AL} , I _{ENL}	V _A = V _{EN} = 0.8V			-0.1		0.1		

Electrical Specifications - Dual Supplies ($V_{\pm} = \pm 5V \pm 10\%$, $GND = 0V$, $V_{AH} = V_{ENH} = 2.4V$, $V_{AL} = V_{ENL} = 0.8V$)
(continued)

Parameter	Symbol	Conditions		Temp(°C)	Min. ⁽¹⁾	Typ. ⁽²⁾	Max. ⁽¹⁾	Units
Dynamic								
Transition Time	tTRANS	Figure 1					150	ns
Break-Before-Make Time Delay	tOPEN	Figure 3			0	40		
Enable Turn-OnTime	tON(EN)	Figure 2		25		72	150	
				Full			250	
Enable Turn-Off Time	tOFF(EN)	Figure 2		25		55	150	
				Full			200	
Charge Injection ⁽³⁾	Q	CL= 1nF, VS = 0V, RS = 0Ohm,		25		2.8	5	pC
Off Isolation ⁽⁷⁾	OIRR	VEN = 0V, RL= 1kOhm, f= 100kHz				-101		dB
Crosstalk	XTALK	RL = 1kOhm, f= 100kHz, Figure 6				-92		
Logic Input Capacitance	CIN	f=1MHz				2.5		pF
NO Off Capacitance	CNO(OFF)	f=1MHz, VEN = VNO = 0V				3.6		
COM Off Capacitance	CCOM(OFF)	f=1MHz, VEN = VCOM =0V	PS398			31		
			PS399			14		
COM On Capacitance	CCOM(ON)	f=1MHz, VCOM = 0V	PS398			35		
			PS399			20		
Supply								
Power-Supply Range				Full	±3		±8	V
Positive Supply Current	I+	VEN = VA = 0V or V+, V+ =5.5V, V- = -5.5V			-1		1	µA
NegativeSupply Current	I-				-1		1	
Ground Current	IGND				-1		1	

Notes:

- Algebraic convention, where the most negative value is a minimum and the most positive is a maximum, is used in this data sheet.
- Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
- Guaranteed by design.
- $\Delta R_{ON} = R_{ON \max} - R_{ON \min}$.
- Flatness is defined as the difference between the maximum and minimum values of on-resistance measured.
- Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25°C.
- Off Isolation = $20 \log_{10} V_{COM} / V_{NO}$. See Figure 5.

Electrical Characteristics - Single 5V Supply

(V+ = +5V ± 10%, V- = 0V, GND = 0V, V_{AH} = V_{ENH} = +2.4, V_{AL} = V_{ENL} = +0.8V)

Parameter	Symbol	Conditions		Temp(°C)	Min. ⁽¹⁾	Typ. ⁽²⁾	Max. ⁽¹⁾	Units
Switch								
Analog Signal Range ⁽³⁾	V _{COM} , V _{NO}			Full	0		V+	V
On Resistance	R _{ON}	I _{NO} = 1mA, V _{COM} = 3.5V, V+ = 4.5V		25		100	225	Ohm
				Full			280	
R _{ON} Matching Between Channels ⁽⁴⁾	ΔR _{ON}	I _{NO} = 1mA, V _{COM} = 3.5V, V+ = 4.5V		25			11	
				Full			13	
On -Resistance Flatness	R _{FLAT}	I _{NO} = 1mA, V _{COM} = 1.5V, 2.5V, 3.5V, V+ = 5V		25			18	
				Full			22	
NO-Off Leakage Current ⁽⁸⁾	I _{NO(OFF)}	V _{NO} = 4.5V, V _{COM} = 0V, V+ = 5.5V		25	-0.1		0.1	nA
				Full	-1.0		1.0	
COM-Off Leakage Current ⁽⁸⁾	I _{COM(OFF)}	V _{COM} = 4.5V, V _{NO} =0V, V+ = 5.5V	PS398	25	-0.2		50	
				Full	-2.5		100	
			PS399	25	-0.2		50	
				Full	-1.5		100	
COM-On Leakage Current ⁽⁸⁾	I _{COM(ON)}	V _{COM} = 4.5V, V _{NO} =4.5V, V+ = 5.5V	PS398	25	-0.4		0.4	
				Full	-5		5	
			PS399	25	-0.2		0.2	
				Full	-2.5		2.5	
Digital Logic Input								
Logic High Input Voltage	V _{AH} , V _{ENH}			Full	2.4			V
Logic Low Input Voltage	V _{AH} , V _{ENL}						0.8	
Input Current with Input Voltage High	I _{AH} , I _{ENH}	V _A = V _{EN} = 2.4V			-0.1		0.1	μA
Input Current with Input Voltage Low	I _{AH} , I _{ENL}	V _A = V _{EN} = 0.8V			-0.1		0.1	
Supply								
Power-Supply Range	V+			Full	3		15	V
Positive-Supply Current	I+	V _{EN} = V+ or 0V, V _A = 0V, V+ = 5.5V, V- = 0V			-1.0		1.0	μA
Negative-Supply Current	I-				-1.0		1.0	
Ground Current	I _{GND}				-1.0		1.0	

Electrical Characteristics - Single 5V

(V+ = +5V ± 10%, V- = 0V, GND = 0V, V_{AH} = V_{ENH} = +2.4, V_{AL} = V_{ENL} = +0.8V (continued))

Parameter	Symbol	Conditions	Temp(°C)	Min. ⁽¹⁾	Typ. ⁽²⁾	Max. ⁽¹⁾	Units
Dynamic							
Transition Time	t _{TRANS}	V _{NO} = 3V	25		72	245	ns
Break-Before-Make Interval	t _{OPEN}			10	36		
Enable Turn-On Time	t _{ON(EN)}				110	200	
			Full			275	
Enable Turn-Off Time	t _{OFF(EN)}		25		65	125	
			Full			200	
Charge Injection ⁽³⁾	Q	C _L = 1nF, V _S = 0V, R _S = 00hm	25		2.8	5	pC

Electrical Characteristics - Single 3V Supply

(V+ = +3V ± 10%, V- = 0V, GND = 0V, V_{AH} = V_{ENH} = +2.4, V_{AL} = V_{ENL} = +0.8V)

Parameter	Symbol	Conditions	Temp.(°C)	Min. ⁽¹⁾	Typ. ⁽²⁾	Max. ⁽¹⁾	Units
Switch							
Analog Signal Range ⁽³⁾	V _{ANALOG}		Full	0		V+	V
On-Resistance	R _{ON}	I _{NO} = 1mA, V _{COM} = 1.5V, V+ = 3V	25		160	375	Ohm
			Full			425	
Dynamic							
Transition Time ⁽³⁾	t _{TRANS}	Figure 1, V _{IN} = 2.4V V _{NO1} = 1.5V, V _{NO8} = 0V	25		200	575	ns
Enable Turn-OnTime ⁽³⁾	t _{ON(EN)}	Figure 2, V _{INH} = 2.4V V _{INL} = 0V, V _{NO1} = 1.5V			200	500	
Enable Turn-Off Time ⁽³⁾	t _{OFF(EN)}	Figure 2, V _{INH} = 2.4V V _{INL} = 0V, V _{NO1} = 1.5V			92	400	
Charge Injection ⁽³⁾	Q	C _L = 10nF, V _S = 0V, R _S = 0Ohm			2	5	pC

Notes:

1. The algebraic convention, where the most negative value is a minimum and the most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design
4. ΔR_{ON} = R_{ON} max - R_{ON} min
5. Flatness is defined as the difference between the maximum and minimum value of on-resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25°C.
7. Worst-case isolation is on channel 4 because of its proximity to the COM pin.
Off isolation = 20log V_{COM}/V_{NO}, V_{COM} = output, V_{NO} = input to off switch
8. Leakage testing at single supply is guaranteed by testing with dual supplies.

Test Circuits/Timing Diagrams

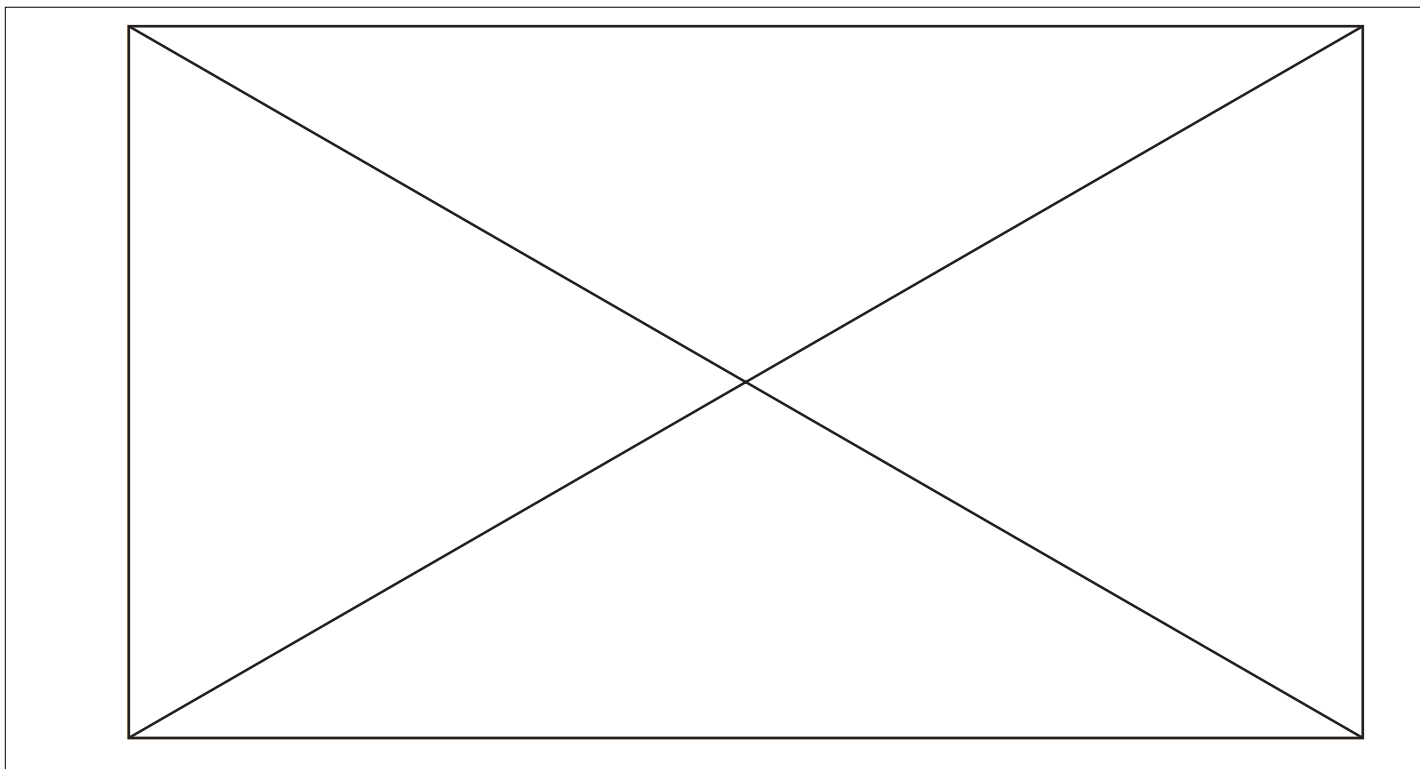


Figure 1. Transition Time

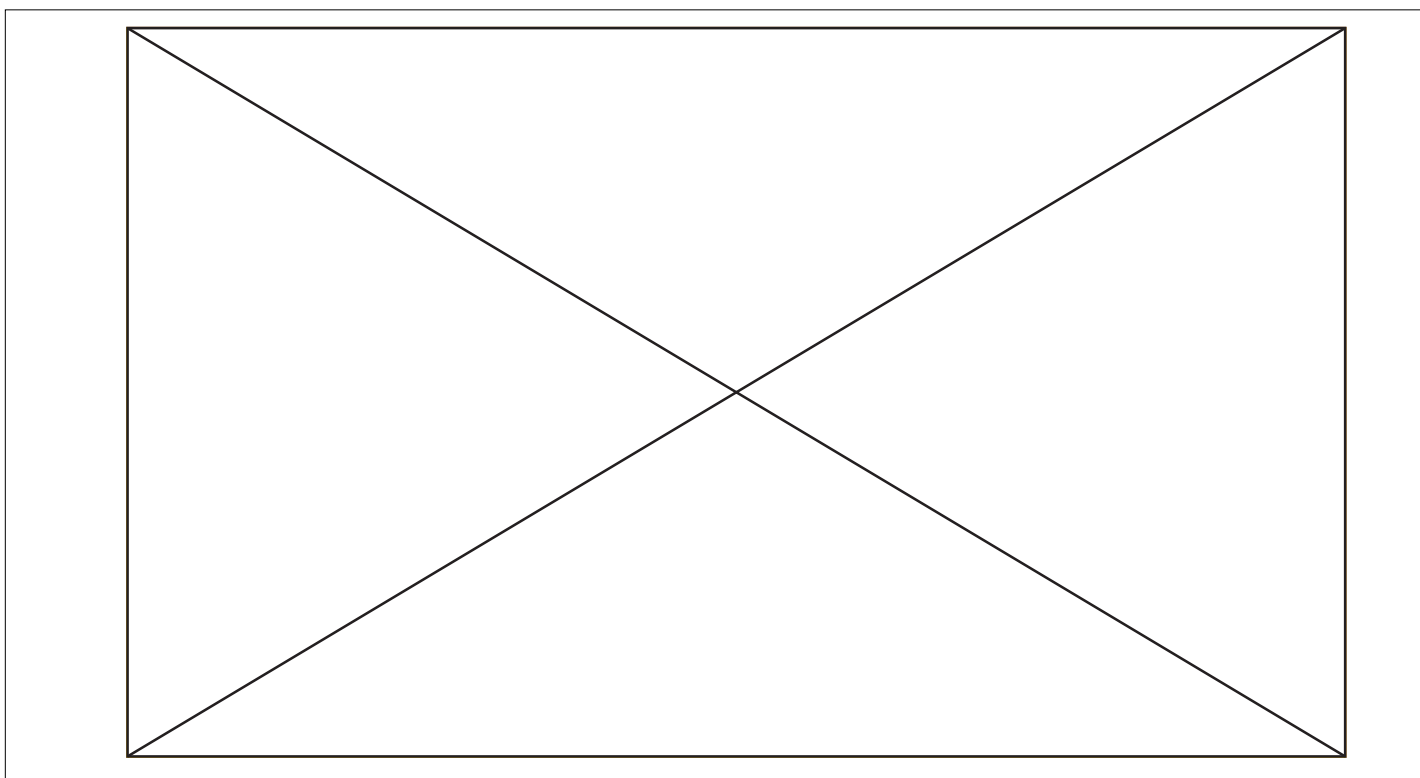


Figure 2. Enable Switching Time

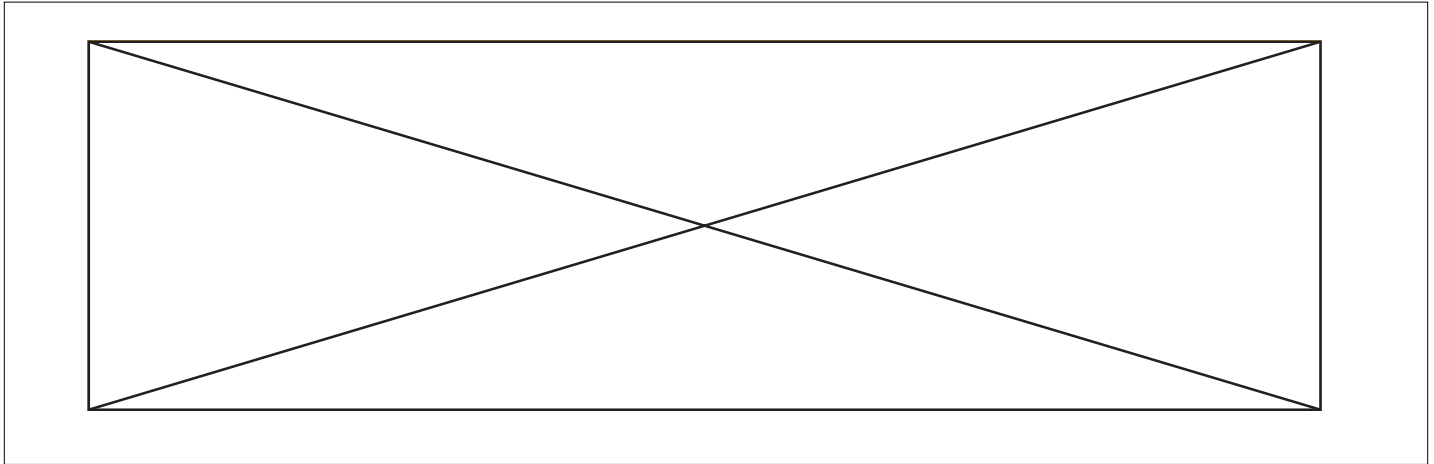


Figure 3. Break-Before-Make Interval

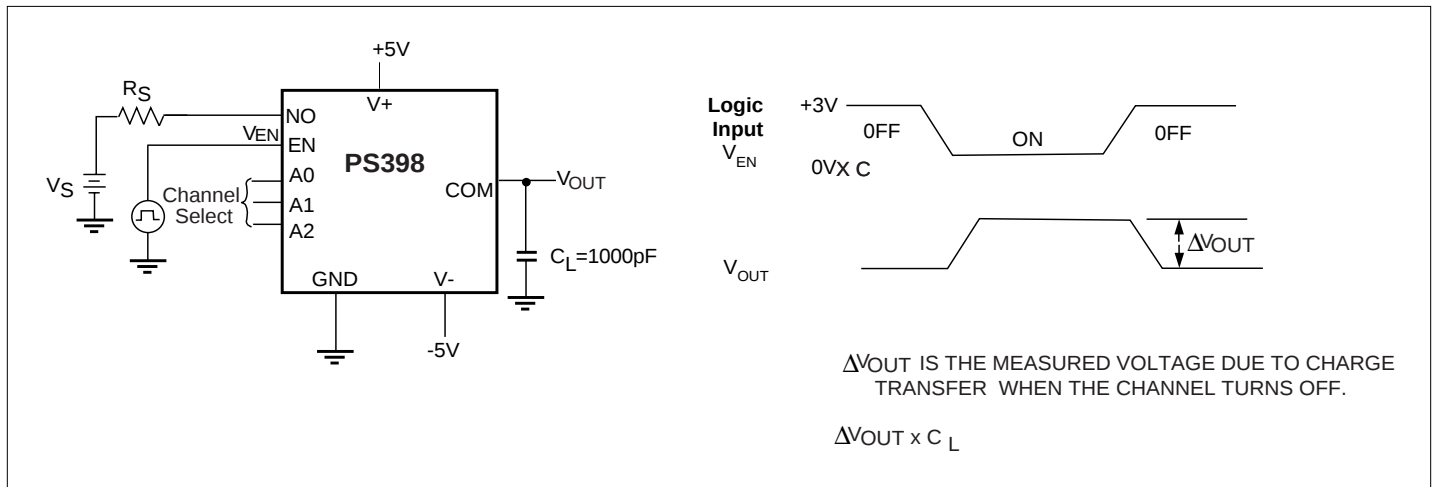


Figure 4. Charge Injection

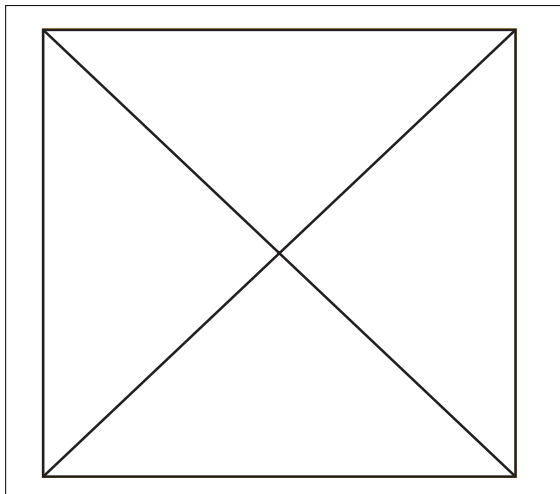


Figure 5. Off Isolation

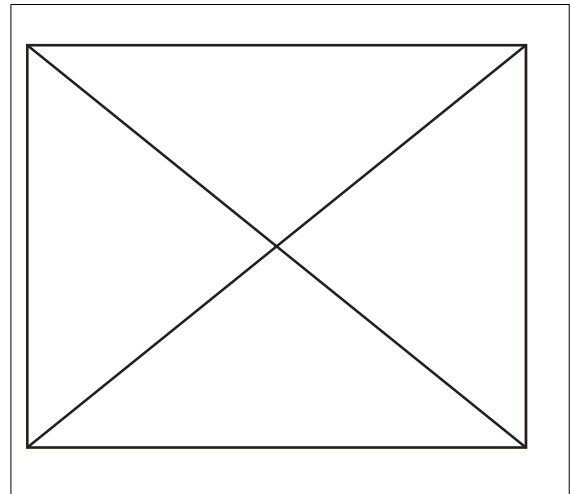


Figure 6. CrossTalk

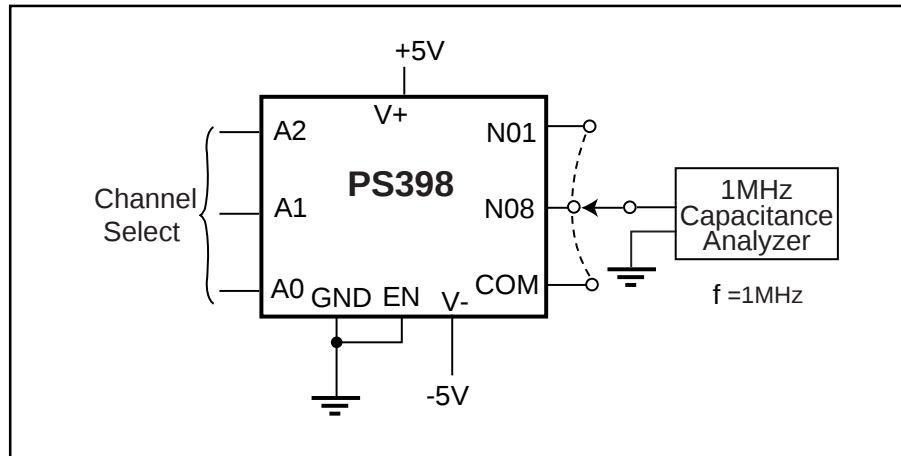


Figure 8. NO/COM Capacitance

Applications

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, followed by V-, and then logic inputs. If power-supply sequencing is not possible, add two small signal diodes or two current limiting resistors in series with the supply pins for overvoltage protection (Figure 9). Adding diodes reduces the analog signal range, but low switch resistance and low leakage characteristics are unaffected.

Maximum Sampling Rate

From the sampling theorem, the sampling frequency needed to properly recover the original signal should be more than twice its maximum component frequency. In real applications, sampling at three or four times the maximum signal frequency is customary.

The maximum sampling rate of a multiplexer is determined by its transition time (t_{TRANS}), the number of channels being multiplexed, and the settling time (t_{SETTLING}) of the sampled signal at the output. The maximum sampling rate is:

$$f_s = \frac{1}{n(t_{\text{TRANS}} + t_{\text{SETTLING}})} \quad (1)$$

Where n = number of channels scanned: 8 for PS398, 4 for PS399. t_{TRANS} is given on the specification table: 150 ns max.

Settling time is the time needed for the output to stabilize within the desired accuracy band of +1 LSB (least significant bit).

Other factors determining settling time are: signal source impedance, capacitive load at the output. Figure 10 illustrates the steady state model. To figure out what the settling time due to the multiplexer is, we can assume that $R_S = 0\Omega$, and $C_L = 0$. In real life, the effects of R_S and C_L should be taken into account when performing these calculations.

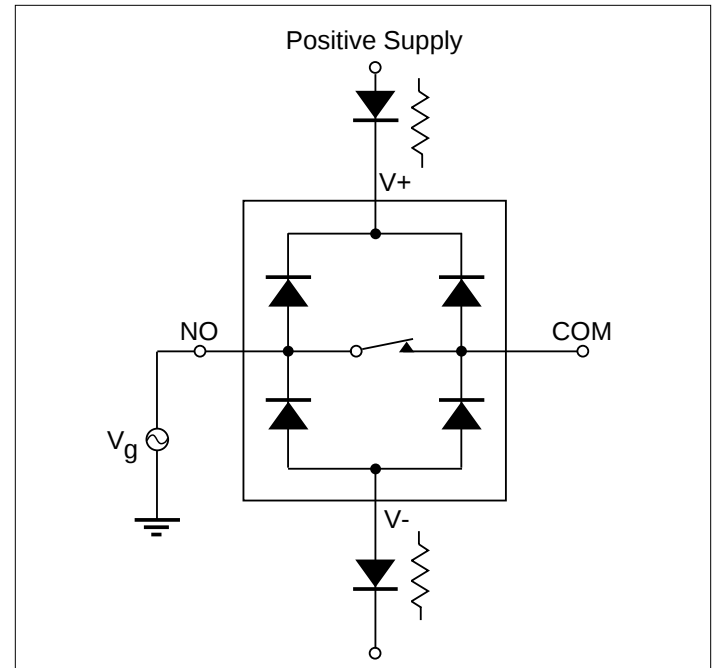


Figure 9. Overvoltage protection is accomplished using two external blocking diodes or two current limiting resistors.

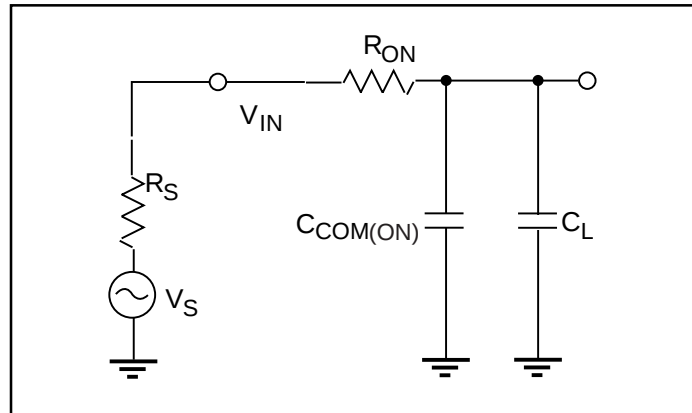


Figure 10. Equivalent model of one multiplexer channel

The table below shows how many time constants ($m\tau$) are needed to reach an accuracy of one LSB. $\tau = R_{ON} \times C_{COM(ON)}$

Bits	Accuracy (%)	m
8	0.25	6
12	0.012	9
15	0.0017	11

Now, let's calculate what the maximum sampling rate for the PS398. Assume a 12-bit accuracy and room temperature operation.

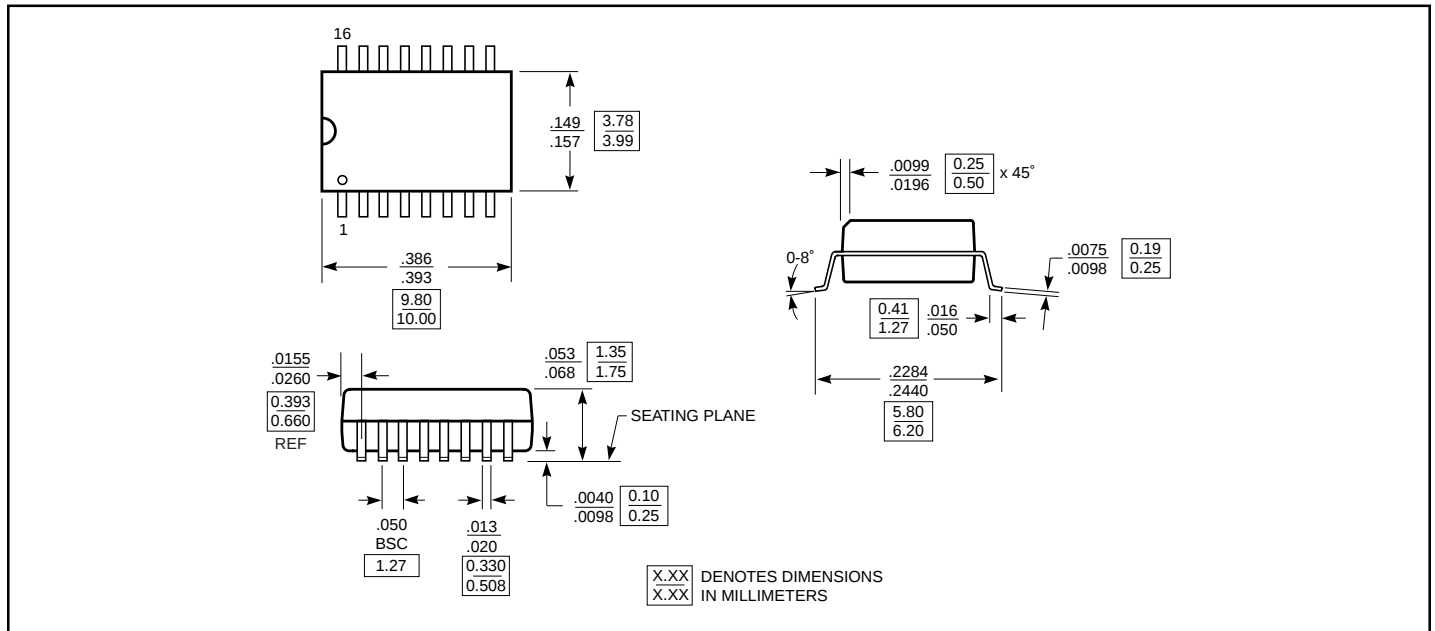
In equation (1) above, $n = 8$, $t_{TRANS} = 150\text{ns}$, $t_{SETTLING} = 9\tau$,
 $\tau = 100\text{ohm} \times 54\text{pF}$

$$f_s = \frac{1}{8 [150\text{ns} + 9(100\text{ohm} \times 54\text{pF})]},$$

or $f_s = 630\text{kHz}$.

Assuming a x4 oversampling rate, the maximum sampling speed for the PS398 would be $630 \div 4 = 157\text{kHz}$.

Packaging Mechanical: 16-pin SOIC (W)



Ordering Information

Ordering Code	Package Code	Package Type
PS398CSE	W	16-pin SOIC
PS398CSEE	W	Pb-free & Green, 16-pin SOIC
PS398ESE	W	16-pin SOIC
PS398ESEE	W	Pb-free & Green, 16-pin SOIC
PS399CSE	W	16-pin SOIC
PS399CSEE	W	Pb-free & Green, 16-pin SOIC
PS399ESE	W	16-pin SOIC
PS399ESEE	W	Pb-free & Green, 16-pin SOIC

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/