

**Features**

- Dual Outputs  
(Independently Regulated)
- Input Voltage Range:  
36 V to 75 V
- Power-up/Down Sequencing
- 1500 VDC Isolation
- Over-Current Protection
- Over-Temperature Shutdown
- Under-Voltage Lockout
- Fixed Frequency Operation
- Temp Range: -40 to 100 °C
- Industry Standard Outline
- Operates with PTB4851x for Complete AC7 Power Solution
- Powers up to 64 DSL Ports
- Safety Approvals:  
UL/cUL 60950  
EN 60950

**Description**

The PTB4850x power modules are a dual-output isolated DC/DC converter, designed to provide the logic supply voltages for AC-7 based xDSL applications. The PTB48500 is rated for 13 A of total output current, making it suitable for 32-channel xDSL applications. The PTB48501 and PTB48502 provide output current for powering up to 64 xDSL channels. The PTB48501 is rated for 16.5 A total output current, and the PTB48502, 21 A. The PTB48502 incorporates 10 W of additional capacity for powering peripheral circuitry. Any of these converters can be used for other applications with similar power requirements.

The modules operate from a standard telecom (-48 V) central office (CO) supply and include an “on/off” enable control,

output current limit, over-temperature protection, input under-voltage lockout (UVLO). The PTB48500 and PTB48501 also incorporates a power-up reset (POR) output.

The modules are designed to operate with one of the PTB4851x DC/DC converter modules. The combination of a PTB4850x and PTB4851x converter provides the complete the power supply for an AC7 chipset. The “EN Out” and “Sync Out” pins provide compatible output signals for controlling both the power up sequence and switching frequency of the PTB48510.

The PTB4850x modules employ double-sided surface mount construction, and are an industry standard size.

**Pin Configuration**

Pin	Function
1	+V <sub>I</sub>
2	Sync Out
3	Enable #
4	EN Out
5	-V <sub>I</sub>
6	+V <sub>O2</sub>
7	COM
8	POR* / COM †
9	Vo <sub>2</sub> Adjust
10	+V <sub>O1</sub>

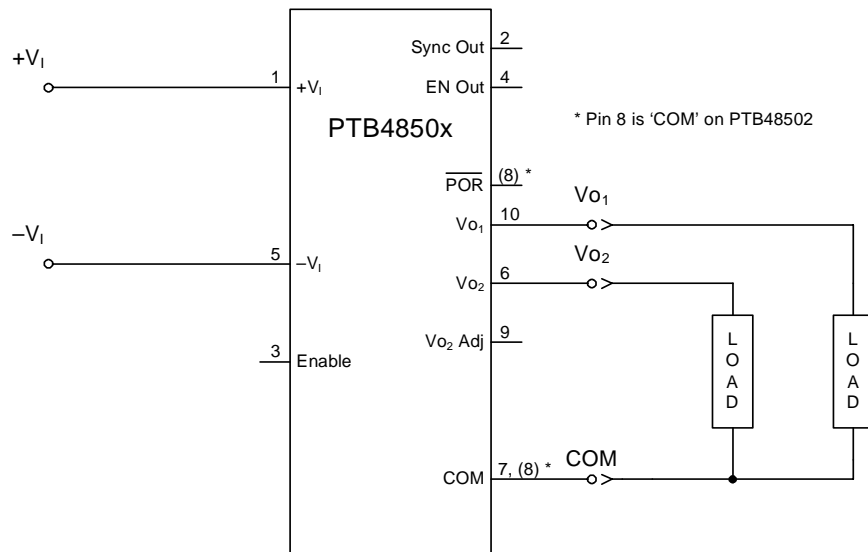
*Shaded functions indicate signals that are referenced to -V<sub>I</sub>.*

# Denotes positive logic:  
Open = Normal operation  
-V<sub>I</sub> = Outputs Off

\* Denotes negative logic:  
High = Normal operation  
Low = Reset

† This pin is COM on the PTB48502

**Stand-Alone Application**



## Ordering Information

Base Part No. (PTB4850□xxx)			Output Voltage (PTB4850x□xx)		Package Options (PT4850xx□□)		
Order Prefix	Description		Code	Voltage	Code	Description	Pkg Ref. (1)
PTB48500xxx	13 A (32-Ports)		A	3.3 V / 1.2 V	AH	Horiz. T/H	(ERH)
PTB48501xxx	16.5 A (48/64-Ports)				AS	SMD, Standard (2)	(ERJ)
PTB48502xx	21 A (64-Ports + 10 W)						

**Notes:** (1) Reference the applicable package reference drawing for the dimensions and PC board layout  
(2) "Standard" option specifies 63/37, Sn/Pb pin solder material.

## Pin Descriptions

**+V<sub>I</sub>:** The positive input supply for the module with respect to  $-V_{in}$ . When powering the module from a -48 V telecom central office supply, this input is connected to the primary system ground.

**-V<sub>I</sub>:** The negative input supply for the module, and the 0 VDC reference for the 'Enable', 'EN Out', and 'Sync Out' signals. When the module is powered from a +48-V supply, this input is connected to the 48-V Return.

**V<sub>0</sub> 1:** The higher regulated power output voltage, which is referenced to the COM node.

**V<sub>0</sub> 2:** The lower regulated power output voltage, which is referenced to the COM node.

**COM:** The secondary return reference for the module's two regulated output voltages. It is dc isolated from the input supply pins.

**V<sub>0</sub> 2 Adjust:** Using a single resistor, this pin allows V<sub>0</sub> 2 to be adjusted higher or lower than the preset value. If not used, this pin should be left open circuit.

**Enable:** This is an open-collector (open-drain) positive logic input that enables the module output. This pin is referenced to  $-V_{in}$ . A logic '0' at this pin disables the module's outputs, and a high impedance enables the outputs. If not used the pin should be left unconnected.

**EN Out:** This open-collector output may be used to enable the output of other DC/DC converters in applications where the power-up sequence of the related voltages must be precisely controlled. The output is used principally to control the startup up of a PTB4851xx module when powering ADSL circuits based on the AC7 chipset. The signal is referenced to  $-V_{in}$ , and is active low. It is initially 'off' (high impedance), and turns 'on' when the output voltage, V<sub>0</sub> 1, has risen to its nominal set-point voltage.

**Sync Out:** The signal generated by this pin is designed to be used exclusively with the PTB48510 in AC7 ADSL applications. When the 'Sync Out' of this converter is connected directly to the 'Sync In' pin of the PTB48510, both modules will operate at the same switch conversion frequency.

**POR\*:** (Available to PTB48500 and PTB48501 only!)

This pin produces an active-low power-on reset signal that may be used to reset logic circuitry. The output is set low during power up just as the output voltage from V<sub>0</sub> 1 starts to rise. It remains low for 10 ms after the voltage at V<sub>0</sub> 1 has reached its nominal set-point voltage. This signal is referenced to the COM node, and has a 3.3-kΩ internal pull-up resistor to V<sub>0</sub> 1.

Environmental and General Specifications (Unless otherwise stated, all voltages are with respect to  $-V_{in}$ )

Characteristics	Symbols	Conditions	Min	Typ	Max	Units
Input Voltage Range	V <sub>in</sub>	Over output load range	36	48	75	VDC
Isolation Voltage		Input-output/input-case	1500	—	—	V
Capacitance		Input to output	—	1500	—	pF
Resistance		Input to output	10	—	—	MΩ
Operating Temperature Range	T <sub>a</sub>	Over V <sub>in</sub> Range	-40	—	+85	°C
Over-Temperature Protection	OTP	Shutdown threshold Hysteresis	—	115 10	—	°C
Solder Reflow Temperature	T <sub>reflow</sub>	Surface temperature of module body or pins	—	—	235 (i)	°C
Storage Temperature	T <sub>s</sub>	—	-40	—	125	°C
Mechanical Shock		Per Mil-STD-883D, Method 2002.3 1 msec, ½ Sine, mounted	—	500	—	G's
Mechanical Vibration		Mil-STD-883D, Method 2007.2 20-2000 Hz	—	20 5	—	G's
Weight	—		—	20	—	grams
Flammability	—	Meets UL 94V-O	—	—	—	

**Notes:** (i) During reflow of SMD package version do not elevate peak temperature of the module, pins or internal components above the stated maximum.

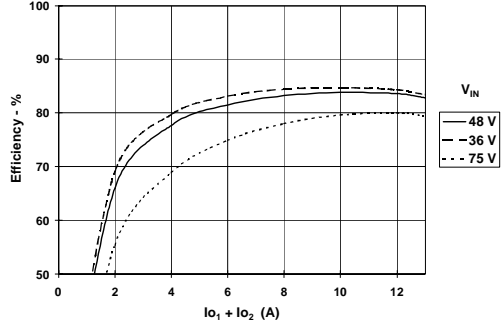
**Specifications** (Unless otherwise stated,  $T_A = 25^\circ\text{C}$ ,  $V_I = 48\text{ V}$ ,  $C_I = 0\mu\text{F}$ ,  $C_O = 0\mu\text{F}$ , and  $I_O = 50\% I_{O,max}$ )

Characteristic	Symbol	Conditions	PTB48500A			Units	
			Min	Typ	Max		
Output Power	$P_{O1}, P_{O2}$		$V_{O1}$ (3.3 V) $V_{O2}$ (1.2 V)	—	—	19.8 8.4	W
	$P_{O\text{ total}}$	Both outputs		—	—	28	W
Output Current	$I_{O1}, I_{O2}$	Over $V_I$ range	$V_{O1}$ (3.3 V) $V_{O2}$ (1.2 V)	0 0	—	6 <sup>(1)</sup> 7 <sup>(1)</sup>	A
	$I_{O1} + I_{O2}$	Total (both outputs)		0	—	13	A
Output Voltage	$V_{O1}$ $V_{O2}$	Includes set point, line, load, $-40 \leq T_A \leq +85^\circ\text{C}$		3.2 1.16	3.3 1.2	3.4 1.24	V
Temperature Variation	$\Delta\text{Reg}_{\text{temp}}$	$-40^\circ \leq T_A \leq +85^\circ\text{C}$ , $I_O = I_{O,\text{min}}$	$V_{O1}$ $V_{O2}$	— —	$\pm 0.5$ $\pm 0.8$	—	$\%V_o$
Line Regulation	$\Delta\text{Reg}_{\text{line}}$	Over $V_I$ range	$V_{O1}, V_{O2}$	—	$\pm 1$	$\pm 10$	mV
Load Regulation	$\Delta\text{Reg}_{\text{load}}$	Over $I_O$ range	$V_{O1}, V_{O2}$	—	$\pm 3$	$\pm 12$	mV
Cross Regulation	$\Delta\text{Reg}_{\text{cross}}$	$I_{O,\text{min}} \leq I_{O2} \leq I_{O,\text{max}}$ , $I_{O1} = 1\text{ A}$ $I_{O,\text{min}} \leq I_{O1} \leq I_{O,\text{max}}$ , $I_{O2} = 1\text{ A}$	$\Delta V_{O1}$ $\Delta V_{O2}$	— —	—	10 10	mV
Efficiency	$\eta$	$I_{O1}, I_{O2} = I_{O,\text{max}}$		—	82	—	%
$V_o$ Ripple (pk-pk)	$V_r$	20 MHz bandwidth	$V_{O1}$ $V_{O2}$	— —	20 20	50 50	mV <sub>pp</sub>
Transient Response	$t_{\text{tr}}$ $\Delta V_{\text{tr}}$	1 A/ $\mu\text{s}$ load step, 50% to 100% $I_{O,\text{max}}$ $V_{O1}, V_{O2}$ over/undershoot		— —	30 $\pm 2.0$	—	$\mu\text{s}$ $\%V_o$
Over Current Threshold	$I_{O,\text{trip}}$	$V_I = 36\text{ V}$ , reset followed by auto-recovery	$I_{O1} + I_{O2}$	13.5	16	—	A
Output Voltage Adjust Range	$V_{\text{adj}}$	$V_{O2}$ only		-10	—	+20	$\%V_o$
Switching Frequency	$f_s$	Over $V_I$ and $I_O$ ranges		500	550	600	kHz
Under-Voltage Lockout	$V_I$ on $V_I$ off	$V_I$ increasing $V_I$ decreasing		— —	34 32	—	V
On/Off Enable (pin 3) Input High Voltage Input Low Voltage Input Low Current	$V_{\text{IH}}$ $V_{\text{IL}}$ $I_{\text{IL}}$	Referenced to $-V_I$ (pin 5)		+3.6 -0.2	— —	+75 <sup>(2)</sup> +0.8	V
Standby Input Current	$I_I$ standby	pins 3 & 5 connected		—	2	—	mA
Internal Input Capacitance	$C_I$			—	2	—	$\mu\text{F}$
External Output Capacitance	$C_{O1}$ $C_{O2}$			0 <sup>(3)</sup> 0 <sup>(3)</sup>	— —	5,000 5,000	$\mu\text{F}$
Reliability	MTBF	Per Telcordia SR-332 50% stress, $T_A = 40^\circ\text{C}$ , ground benign		1.5	—	—	$10^6$ Hrs

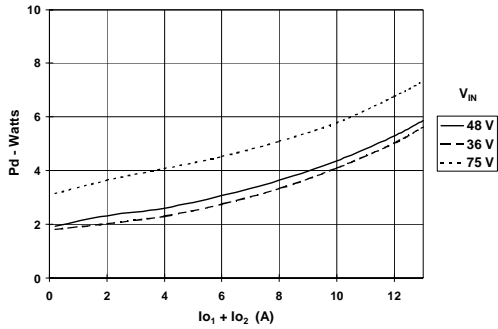
- Notes:**
- (1) See Safe Operating Area curves or contact the factory for the appropriate derating.
  - (2) The On/Off Enable (pin 3) has an internal pull-up and may be controlled with an open-collector (or open-drain) transistor. The input is diode protected and may be connected to  $+V_I$ . The maximum open-circuit voltage is 7 V. If it is left open circuit the converter will operate when input power is applied.
  - (3) An output capacitor is not required.

**PTB48500A Characteristic Data** (See Note A)

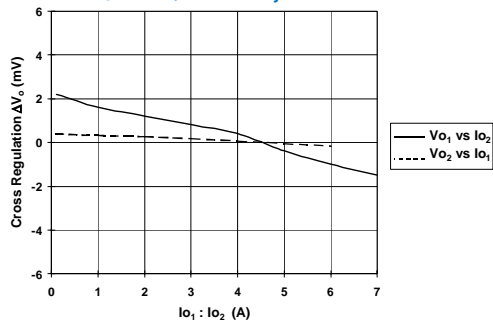
**Efficiency vs Load Current** (See Note B)



**Power Dissipation vs Load Current** (See Note B)

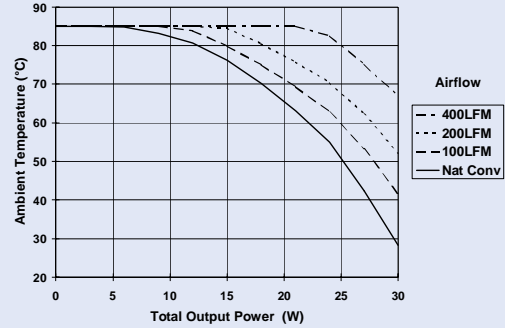


**Cross Regulation,  $\Delta V_o$  vs  $I_{o_y}$  @  $I_{o_x} = 1$  A &  $V_{IN} = 48$  V**



**Safe Operating Area PTB48500A** (See Note C)

**$V_{IN} = 48$  VDC** (See Note B)



**Note A:** Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the converter.

**Note B:** Load current is increased proportionally from both outputs, up to the respective maximum value of each output.

**Note C:** SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in. × 4 in. double-sided PCB with 1 oz. copper.

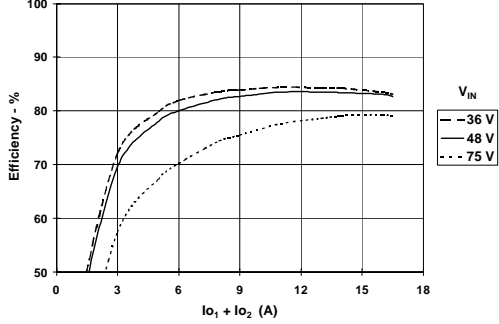
**Specifications** (Unless otherwise stated,  $T_A = 25^\circ\text{C}$ ,  $V_I = 48\text{ V}$ ,  $C_I = 0\ \mu\text{F}$ ,  $C_O = 0\ \mu\text{F}$ , and  $I_O = 50\% I_{O\text{ max}}$ )

Characteristic	Symbol	Conditions	PTB48501A			Units	
			Min	Typ	Max		
Output Power	$P_{O1}, P_{O2}$		$V_{O1}$ (3.3 V)	—	—	19.8	W
			$V_{O2}$ (1.2 V)	—	—	12.6	
	$P_{O\text{ total}}$	Both outputs		—	—	32.4	W
Output Current	$I_{O1}, I_{O2}$	Over $V_I$ range	$V_{O1}$ (3.3 V)	0	—	6 <sup>(1)</sup>	A
			$V_{O2}$ (1.2 V)	0	—	10.5 <sup>(1)</sup>	
	$I_{O1} + I_{O2}$	Total (both outputs)		0	—	16.5	A
Output Voltage	$V_{O1}$ $V_{O2}$	Includes set point, line, load, $-40 \leq T_A \leq +85^\circ\text{C}$		3.2	3.3	3.4	V
				1.16	1.2	1.24	
Temperature Variation	$\Delta\text{Reg}_{\text{temp}}$	$-40^\circ \leq T_A \leq +85^\circ\text{C}$ , $I_O = I_{O\text{ min}}$	$V_{O1}$ $V_{O2}$	— —	$\pm 0.5$ $\pm 0.8$	— —	$\%V_O$
Line Regulation	$\Delta\text{Reg}_{\text{line}}$	Over $V_I$ range	$V_{O1}, V_{O2}$	—	$\pm 1$	$\pm 10$	mV
Load Regulation	$\Delta\text{Reg}_{\text{load}}$	Over $I_O$ range	$V_{O1}, V_{O2}$	—	$\pm 3$	$\pm 12$	mV
Cross Regulation	$\Delta\text{Reg}_{\text{cross}}$	$I_{O\text{ min}} \leq I_{O2} \leq I_{O\text{ max}}$ , $I_{O1} = 1\text{ A}$ $I_{O\text{ min}} \leq I_{O1} \leq I_{O\text{ max}}$ , $I_{O2} = 1\text{ A}$	$\Delta V_{O1}$	—	—	10	mV
			$\Delta V_{O2}$	—	—	10	
Efficiency	$\eta$	$I_{O1}, I_{O2} = I_{O\text{ max}}$		—	81	—	%
$V_O$ Ripple (pk-pk)	$V_r$	20 MHz bandwidth	$V_{O1}$	—	20	50	mV <sub>pp</sub>
			$V_{O2}$	—	20	50	
Transient Response	$t_{\text{tr}}$ $\Delta V_{\text{tr}}$	1 A/ $\mu\text{s}$ load step, 50% to 100% $I_{O\text{ max}}$		—	30	—	$\mu\text{s}$
				—	$\pm 2.0$	—	
Over Current Threshold	$I_{O\text{ trip}}$	$V_I = 36\text{ V}$ , reset followed by auto-recovery	$I_{O1} + I_{O2}$	—	24	—	A
Output Voltage Adjust Range	$V_{\text{adj}}$	$V_{O2}$ only		-20	—	+10	$\%V_O$
Switching Frequency	$f_s$	Over $V_I$ and $I_O$ ranges		500	550	600	kHz
Under-Voltage Lockout	$V_I$ on $V_I$ off	$V_I$ increasing $V_I$ decreasing		—	34	—	V
				—	32	—	
On/Off Enable (pin 3) Input High Voltage Input Low Voltage Input Low Current	$V_{\text{IH}}$ $V_{\text{IL}}$ $I_{\text{IL}}$	Referenced to $-V_I$ (pin 5)		+3.6	—	+75 <sup>(2)</sup>	V
				-0.2	—	+0.8	
				—	-1	—	
Standby Input Current	$I_I$ standby	pins 3 & 5 connected		—	2	—	mA
Internal Input Capacitance	$C_I$			—	2	—	$\mu\text{F}$
External Output Capacitance	$C_{O1}$ $C_{O2}$			0 <sup>(3)</sup>	—	5,000	$\mu\text{F}$
				0 <sup>(3)</sup>	—	5,000	
Reliability	MTBF	Per Telcordia SR-332 50% stress, $T_A = 40^\circ\text{C}$ , ground benign		1.5	—	—	$10^6$ Hrs

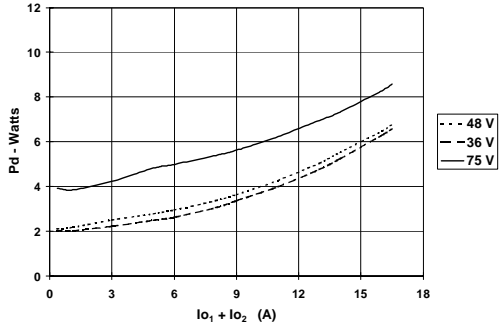
- Notes:**
- (1) See Safe Operating Area curves or contact the factory for the appropriate derating.
  - (2) The On/Off Enable (pin 3) has an internal pull-up and may be controlled with an open-collector (or open-drain) transistor. The input is diode protected and may be connected to  $+V_I$ . The maximum open-circuit voltage is 7 V. If it is left open circuit the converter will operate when input power is applied.
  - (3) An output capacitor is not required.

**PTB48501A Characteristic Data** (See Note A)

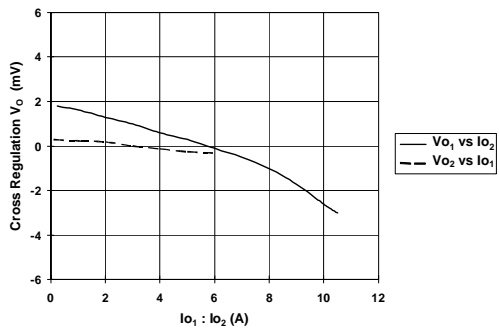
**Efficiency vs Load Current** (See Note B)



**Power Dissipation vs Load Current** (See Note B)

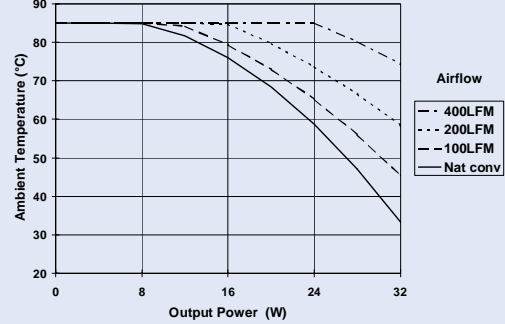


**Cross Regulation,  $\Delta V_{o_x}$  vs  $I_{o_y}$  @  $I_{o_x} = 1$  A &  $V_{IN} = 48$  V**



**Safe Operating Area PTB48501A** (See Note C)

**$V_{IN} = 48$  VDC** (See Note B)



**Note A:** Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the converter.

**Note B:** Load current is increased proportionally from both outputs, up to the respective maximum value of each output.

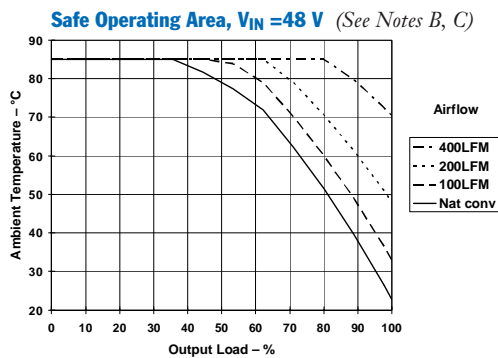
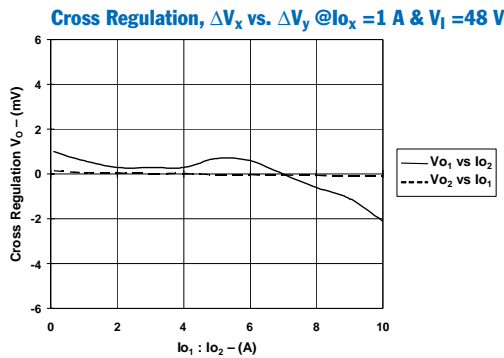
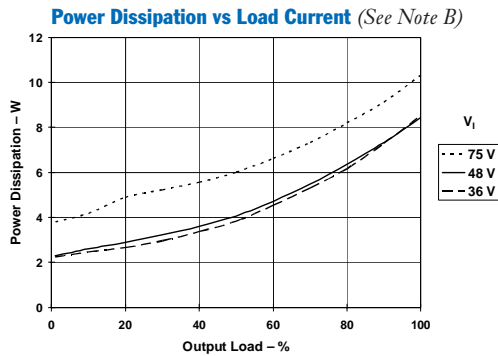
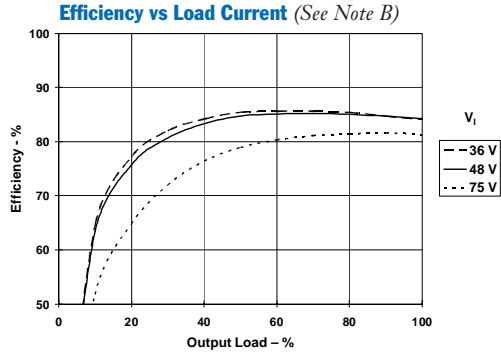
**Note C:** SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in.  $\times$  4 in. double-sided PCB with 1 oz. copper.

**Specifications** (Unless otherwise stated,  $T_A = 25^\circ\text{C}$ ,  $V_I = 48\text{ V}$ ,  $C_I = 0\ \mu\text{F}$ ,  $C_O = 0\ \mu\text{F}$ , and  $I_O = 50\% I_{O\text{ max}}$ )

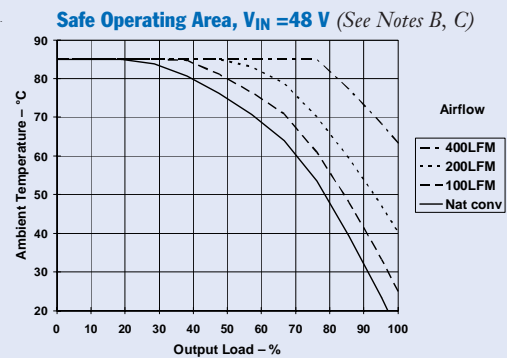
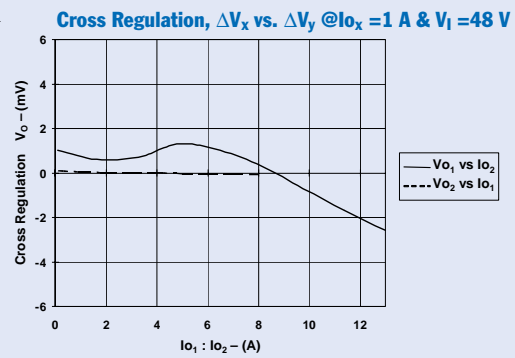
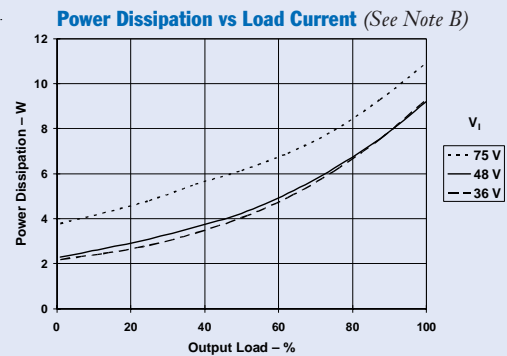
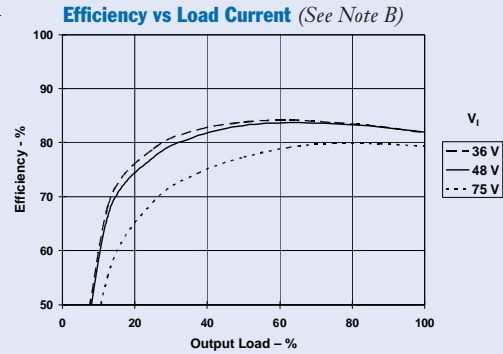
Characteristic	Symbol	Conditions	PTB48502A			Units	
			Min	Typ	Max		
Output Power	$P_{O1}, P_{O2}$		$V_{O1} (3.3\text{ V})$ $V_{O2} (1.2\text{ V})$	—	—	33 15.6	W
	$P_{O\text{ total}}$	Both outputs		—	—	45	W
Output Current	$I_{O1}, I_{O2}$	Over $V_{I\text{ in}}$ range	$V_{O1} (3.3\text{ V})$ $V_{O2} (1.2\text{ V})$	0 0	—	10 (1) 13 (1)	A
	$I_{O1} + I_{O2}$	Total (both outputs)		0	—	21	A
Output Voltage	$V_{O1}$ $V_{O2}$	Includes set point, line, load, $-40 \leq T_A \leq +85^\circ\text{C}$		3.2 1.16	3.3 1.2	3.4 1.24	V
Temperature Variation	$\Delta\text{Reg}_{\text{temp}}$	$-40^\circ \leq T_A \leq +85^\circ\text{C}$ , $I_O = I_{O\text{ min}}$	$V_{O1}$ $V_{O2}$	— —	$\pm 0.5$ $\pm 0.8$	— —	$\%V_O$
Line Regulation	$\Delta\text{Reg}_{\text{line}}$	Over $V_I$ range	$V_{O1}, V_{O2}$	—	$\pm 1$	$\pm 10$	mV
Load Regulation	$\Delta\text{Reg}_{\text{load}}$	Over $I_O$ range	$V_{O1}, V_{O2}$	—	$\pm 3$	$\pm 12$	mV
Cross Regulation	$\Delta\text{Reg}_{\text{cross}}$	$I_{O\text{ min}} \leq I_{O2} \leq I_{O\text{ max}}$ , $I_{O1} = 1\text{ A}$ $I_{O\text{ min}} \leq I_{O1} \leq I_{O\text{ max}}$ , $I_{O2} = 1\text{ A}$	$\Delta V_{O1}$ $\Delta V_{O2}$	— —	— —	10 10	mV
Efficiency	$\eta$	$I_{O1}, I_{O2} = I_{O\text{ max}}$		—	82	—	%
$V_O$ Ripple (pk-pk)	$V_r$	20 MHz bandwidth	$V_{O1}$ $V_{O2}$	— —	20 20	50 50	mV <sub>pp</sub>
Transient Response	$t_{\text{tr}}$	1 A/ $\mu\text{s}$ load step, 50% to 100% $I_{O\text{ max}}$		—	30	—	$\mu\text{s}$
	$\Delta V_{\text{tr}}$	$V_{O1}, V_{O2}$ over/undershoot		—	$\pm 2.0$	—	$\%V_O$
Over Current Threshold	$I_{O\text{ trip}}$	$V_I = 36\text{ V}$ , reset followed by auto-recovery	$I_{O1} + I_{O2}$	—	24	—	A
Output Voltage Adjust Range	$V_{\text{adj}}$	$V_{O2}$ only		-20	—	+10	$\%V_O$
Switching Frequency	$f_s$	Over $V_I$ and $I_O$ ranges		500	550	600	kHz
Under-Voltage Lockout	$V_I$ on	$V_I$ increasing		—	34	—	V
	$V_I$ off	$V_I$ decreasing		—	32	—	V
On/Off Enable (pin 3) Input High Voltage Input Low Voltage Input Low Current	$V_{IH}$	Referenced to $-V_I$ (pin 5)		+3.6	—	+75 (2)	V
	$V_{IL}$		-0.2	—	+0.8		
	$I_{IL}$		—	-1	—		mA
Standby Input Current	$I_I$ standby	pins 3 & 5 connected		—	2	—	mA
Internal Input Capacitance	$C_I$			—	2	—	$\mu\text{F}$
External Output Capacitance	$C_{O1}$			0 (3)	—	5,000	$\mu\text{F}$
	$C_{O2}$			0 (3)	—	5,000	$\mu\text{F}$
Reliability	MTBF	Per Telcordia SR-332 50% stress, $T_A = 40^\circ\text{C}$ , ground benign		1.5	—	—	$10^6$ Hrs

- Notes:**
- (1) See Safe Operating Area curves or contact the factory for the appropriate derating.
  - (2) The On/Off Enable (pin 3) has an internal pull-up and may be controlled with an open-collector (or open-drain) transistor. The input is diode protected and may be connected to  $+V_I$ . The maximum open-circuit voltage is 7 V. If it is left open circuit the converter will operate when input power is applied.
  - (3) An output capacitor is not required.

**PTB48502A Characteristic Data** (See Note A)  
*[ $I_{o1} = 10\text{ A}$ ,  $I_{o2} = 10\text{ A}$  represents 100% load]*



**PTB48502A Characteristic Data** (See Note A)  
*[ $I_{o1} = 8\text{ A}$ ,  $I_{o2} = 13\text{ A}$  represents 100% load]*



**Note A:** Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the converter.

**Note B:** Load current is increased proportionally from both outputs, up to the indicated maximum value of each respective output.

**Note C:** SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in. × 4 in. double-sided PCB with 1 oz. copper.

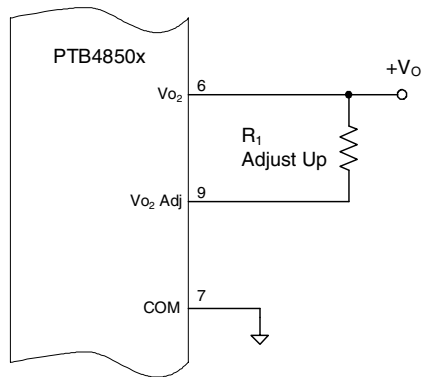


### Adjusting the Lower Output Voltage of the PTB4850x Series of DC/DC Converters

The PTB4850x series of DC/DC converters are designed to produce two logic-level supply voltages for use with the AC-7 ADSL chipset. The magnitude of lowest output voltage ( $V_{O2}$ ) can be adjusted higher or lower by up to +10% or -20% of the nominal. The adjustment method uses a single external resistor.<sup>1</sup> The value of the resistor determines the amount of adjustment, and its placement determines whether the voltage is increased or decreased. The resistor values can be calculated using the appropriate formula (see below), or simply selected from the range of values given in Table 1-2. The placement of each resistor is as follows.

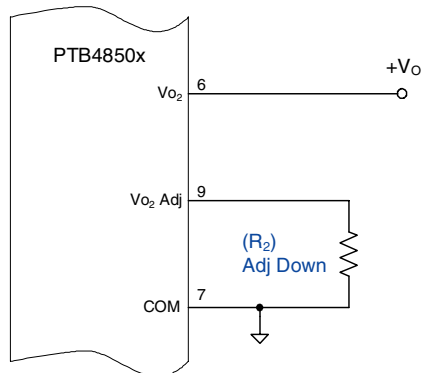
**Adjust Up:** To increase the magnitude of both output voltages, place a resistor  $R_1$  between  $V_{O2} Adj$  (pin 9) and the  $V_{O2}$  (pin 6) voltage rail; see Figure 1-1(a).

Figure 1-1a



**Adjust Down:** To decrease the magnitude of both output voltages, add a resistor ( $R_2$ ), between  $V_{O2} Adj$  (pin 9) and the  $COM$  (pin 7) voltage rail; see Figure 1-1(b).

Figure 1-1b



### Calculation of Resistor Adjust Values

The value of the adjust resistor is calculated using one of the following equations. Use the equation for  $R_1$  to adjust up, or ( $R_2$ ) to adjust down.

$$R_1 \text{ [Adjust Up]} = R_p \cdot \frac{V_a}{(V_a - V_o)} - R_s \quad \text{k}\Omega$$

$$(R_2) \text{ [Adj Down]} = R_n \cdot \frac{V_a}{(V_o - V_a)} - R_s \quad \text{k}\Omega$$

Where:  $V_o$  = Magnitude of the original output voltage  
 $V_a$  = Magnitude of the adjusted voltage  
 $R_p$  = Adjust-up constant from Table 1-1  
 $R_n$  = Adjust-down constant from Table 1-1  
 $R_s$  = Internal series resistor from Table 1-1

Table 1-1

#### ADJUSTMENT RANGE AND FORMULA PARAMETERS

Part No.	PTB48500(1)A	PTB48502A
$V_o(\text{nom})$	1.2 V	1.2 V
$V_a(\text{min})$	0.96 V	0.84 V
$V_a(\text{max})$	1.32 V	1.32 V
$R_p$ (k $\Omega$ )	1.648	1.196
$R_n$ (k $\Omega$ )	4.624	3.598
$R_s$ (k $\Omega$ )	18.2	13.0

#### Notes:

1. A 0.05 W rated resistor may be used. The tolerance should be 1%, with a temperature stability of 100 ppm/°C or better. Place the resistor in either the  $R_1$  or ( $R_2$ ) location, as close to the converter as possible.
2. Never connect capacitors to the  $V_{O2} Adj$  pin. Capacitance added to this pin can affect the stability of the regulated output.

PTB48500, PTB48501, & PTB48502

**Table 1-2**

**ADJUST RESISTOR VALUES**

Part No.		PTB4850xA	PTB48502A
% Adjust	V <sub>a</sub> (V)	R <sub>1</sub> / (R <sub>2</sub> )	R <sub>1</sub> / (R <sub>2</sub> )
-21	0.848	N/A	(0.5) kΩ
-20	0.960	(0.3) kΩ	(1.4) kΩ
-19	0.972	(1.5) kΩ	(2.3) kΩ
-18	0.984	(2.9) kΩ	(3.4) kΩ
-17	0.996	(4.4) kΩ	(4.6) kΩ
-16	1.008	(6.1) kΩ	(5.9) kΩ
-15	1.020	(8.0) kΩ	(7.4) kΩ
-14	1.032	(10.2) kΩ	(9.1) kΩ
-13	1.044	(12.7) kΩ	(11.1) kΩ
-12	1.056	(15.7) kΩ	(13.4) kΩ
-11	1.068	(19.2) kΩ	(16.1) kΩ
-10	1.080	(23.4) kΩ	(19.4) kΩ
- 9	1.092	(28.6) kΩ	(23.4) kΩ
- 8	1.104	(35) kΩ	(28.4) kΩ
- 7	1.116	(43.2) kΩ	(34.8) kΩ
- 6	1.128	(54.2) kΩ	(43.4) kΩ
- 5	1.140	(69.7) kΩ	(55.4) kΩ
- 4	1.152	(92.8) kΩ	(73.4) kΩ
- 3	1.164	(131) kΩ	(103.0) kΩ
- 2	1.176	(208) kΩ	(163.0) kΩ
- 1	1.188	(440) kΩ	(343.0) kΩ
0	1.200		
+ 1	1.212	148 kΩ	108.0 kΩ
+ 2	1.224	65.8 kΩ	48.0 kΩ
+ 3	1.236	38.4 kΩ	28.1 kΩ
+ 4	1.248	24.6 kΩ	18.1 kΩ
+ 5	1.260	16.4 kΩ	12.1 kΩ
+ 6	1.272	10.9 kΩ	8.1 kΩ
+ 7	1.284	7 kΩ	5.3 kΩ
+ 8	1.296	4.1 kΩ	3.2 kΩ
+ 9	1.308	1.8 kΩ	1.5 kΩ
+10	1.320	0 kΩ	0.2 kΩ

R<sub>1</sub> =Adjust up, (R<sub>2</sub>) =Adjust down

### Configuring the PTB4850x & PTB4851x DC/DC Converters for DSL Applications

When operated as a pair, the PTB4850x and PTB4851x converters are specifically designed to provide all the required supply voltages for powering xDSL chipsets. The PTB4850x produces two logic voltages. They include a 3.3-V source for logic and I/O, and a low-voltage for powering a digital signal processor core. The PTB4851x produces a balanced pair of complementary supply voltages that is required for the xDSL transceiver ICs. When used together in these types of applications, the PTB4850x and PTB4851x may be configured for power-up sequencing, and also synchronized to a common switch conversion frequency. Figure 2-1 shows the required cross-connects between the two converters to enable these two features.

#### Switching Frequency Synchronization

Unsynchronized, the difference in switch frequency introduces a beat frequency into the input and output AC ripple components from the converters. The beat frequency can vary considerably with any slight variation in either converter's switch frequency. This results in a variable and undefined frequency spectrum for the ripple waveforms, which would normally require separate filters at the input of each converter. When the switch frequency of the converters are synchronized, the ripple components are constrained to the fundamental and higher. This simplifies the design of the output filters, and allows a common filter to be specified for the treatment of input ripple.

#### Power-Up Sequencing

The desired power-up sequence for the AC7 supply voltages requires that the two logic-level voltages from the PTB4850x converter rise to regulation prior to the two complementary voltages that power the transceiver ICs. This sequence cannot be guaranteed if the PTB4850x and PTB4851x are allowed to power up independently, especially if the 48-V input voltage rises relatively slowly. To ensure the desired power-up sequence, the "EN Out" pin of the PTB4850x is directly connected to the active-low "Enable" input of the PTB4851x (see Figure 2-1). This allows the PTB4850x to momentarily hold off the outputs from the PTB4851x until the logic-level voltages have risen first. Figure 2-2 shows the power-up waveforms of all four supply voltages from the schematic of Figure 2-1.

Figure 2-2; Power-Up Sequencing Waveforms

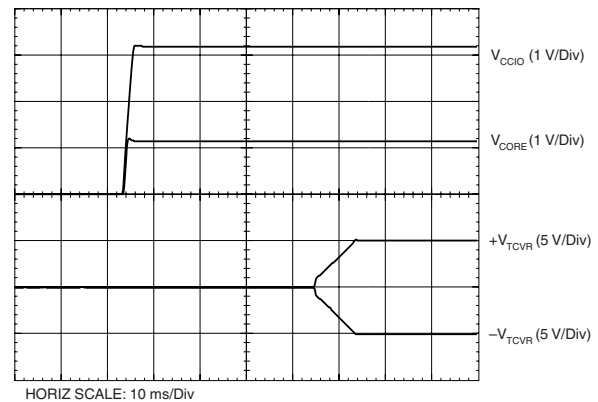
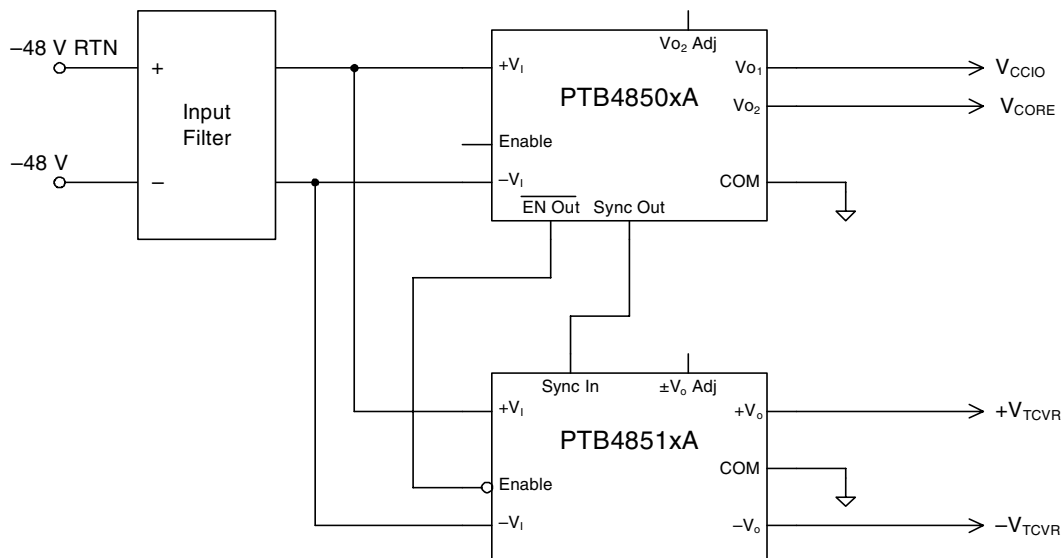
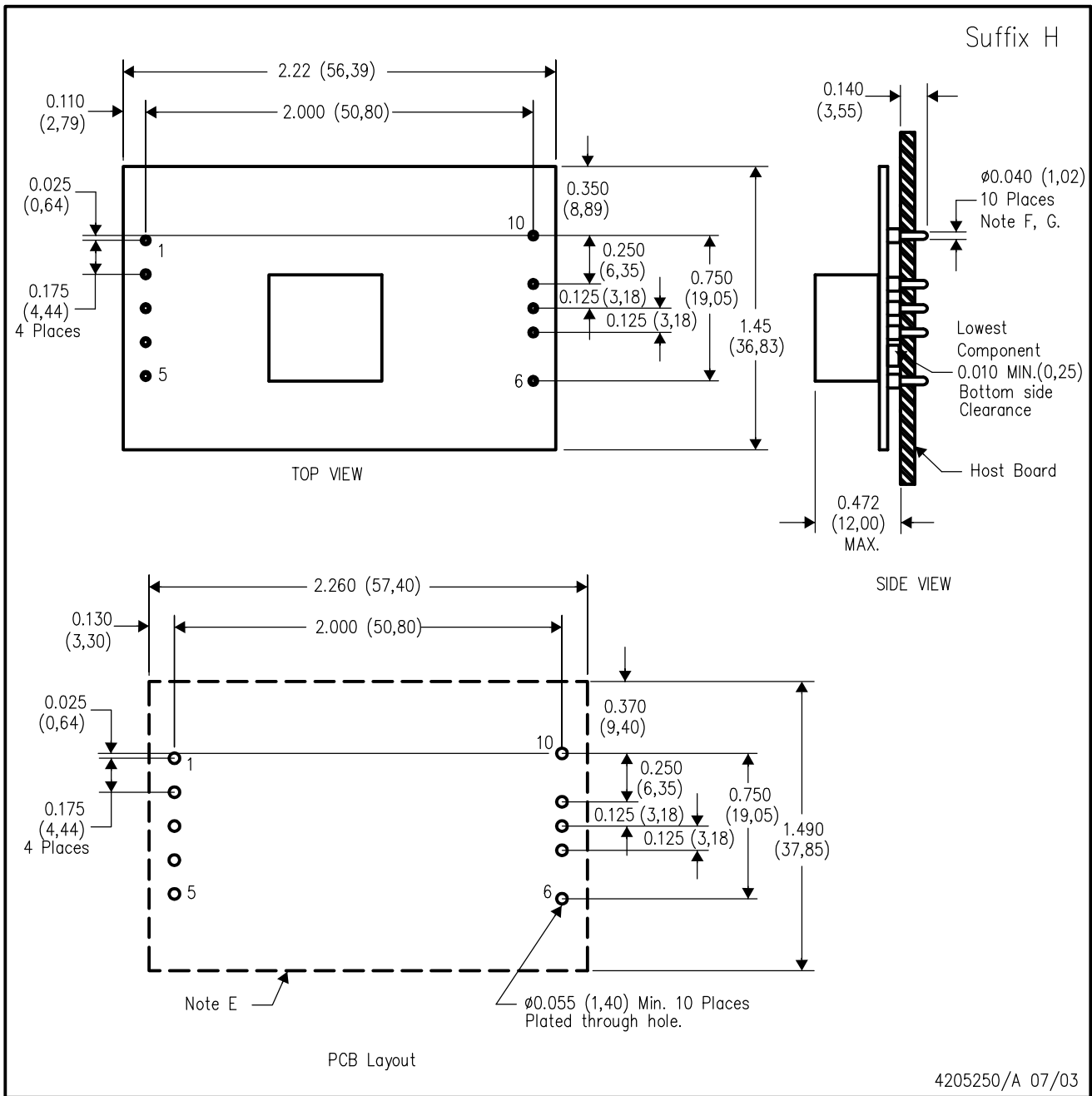


Figure 2-1; Example of PTB4850x & PTB4851x Modules Configured for DSL Applications



**ERH (R-PDSS-T10)**

**DOUBLE SIDED MODULE**



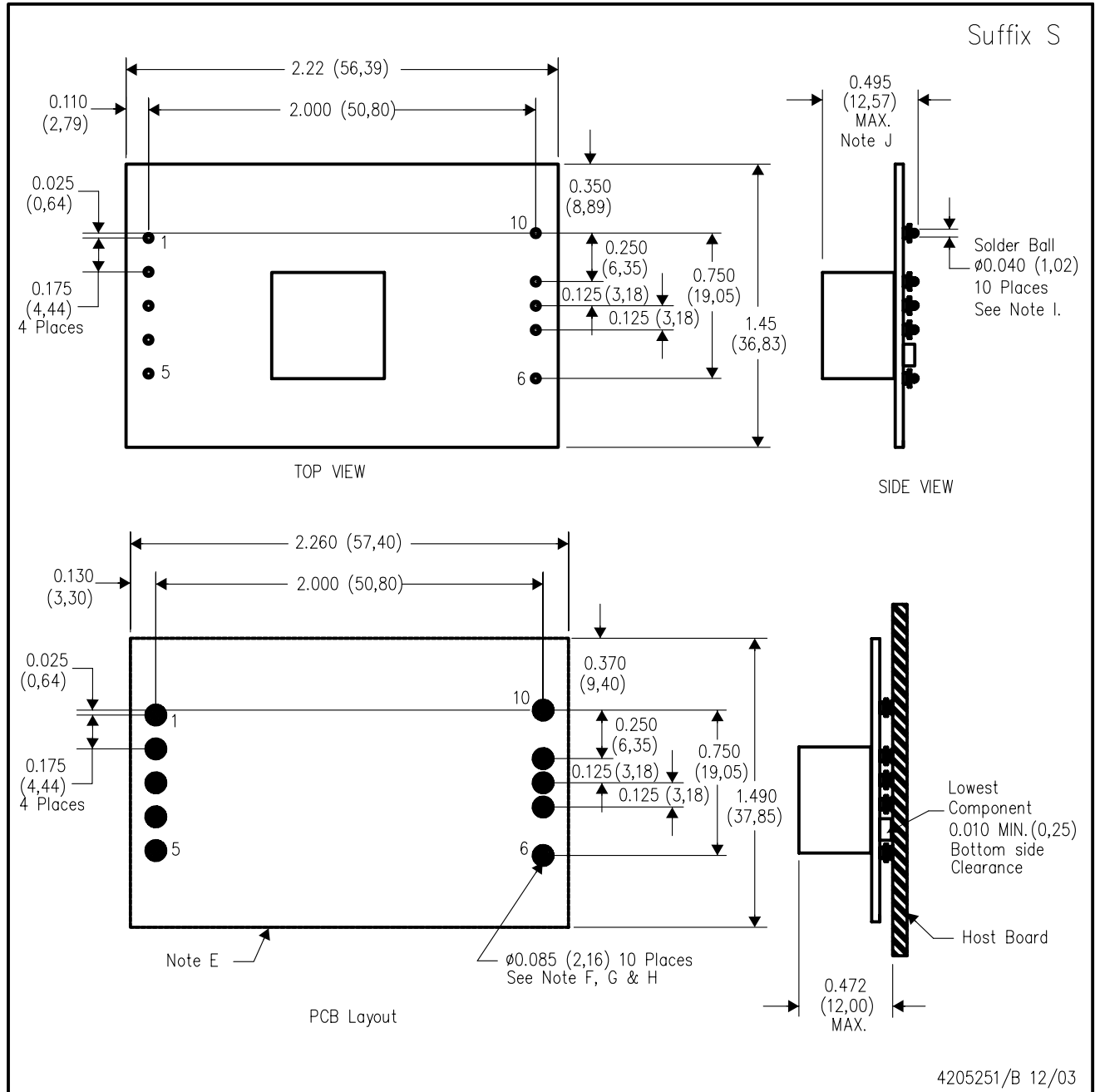
4205250/A 07/03

- NOTES:
- A. All linear dimensions are in inches (mm).
  - B. This drawing is subject to change without notice.
  - C. 2 place decimals are  $\pm 0.020$  ( $\pm 0,51$ mm).
  - D. 3 place decimals are  $\pm 0.010$  ( $\pm 0,25$ mm).
  - E. Recommended keep out area for user components.

- F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
- G. All pins: Material - Copper Alloy  
Finish - Tin (100%) over Nickel plate

ERJ (R-PDSS-B10)

DOUBLE SIDED MODULE



- NOTES:
- A. All linear dimensions are in inches (mm).
  - B. This drawing is subject to change without notice.
  - C. 2 place decimals are  $\pm 0.020$  ( $\pm 0,51$ mm).
  - D. 3 place decimals are  $\pm 0.010$  ( $\pm 0,25$ mm).
  - E. Recommended keep out area for user components.
  - F. Power pin connection should utilize four or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
  - G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
  - H. Pad type: Solder mask defined.
  - I. All pins: Material – Copper Alloy  
Finish – Tin (100%) over Nickel plate  
Solder Ball – See product data sheet.
  - J. Dimension prior to reflow solder.

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Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265