CoolMOS™ Power Transistor

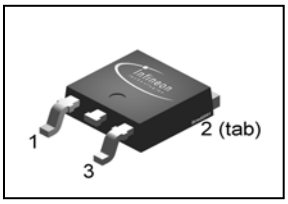
Features

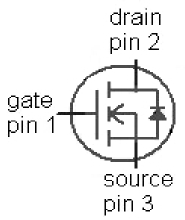
- New revolutionary high voltage technology
- Ultra low gate charge
- Periodic avalanche rated
- High peak current capability
- Ultra low effective capacitances
- Extreme d*v*/d*t* rated
- Improved transconductance
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC[0)] for target applications

Product Summary

V_{DS} @ $T_{j,max}$	650	V
$R_{DS(on),max}$	0.75	Ω
I_D	6.2	A

PG-TO252





Type	Package	Ordering Code	Marking
SPD06N60C3	PG-TO252	Q67040-S4630	06N60C3

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C	6.2	A
		T_C=100 °C	3.9	
Pulsed drain current[1)]	$I_{D,pulse}$	T_C=25 °C	18.6	
Avalanche energy, single pulse	E_{AS}	I_D=3.1 A, V_{DD}=50 V	200	mJ
Avalanche energy, repetitive t_{AR}[1),2)]	E_{AR}	I_D=6.2 A, V_{DD}=50 V	0.5	
Avalanche current, repetitive t_{AR}[1)]	I_{AR}		6.2	A
Drain source voltage slope	d*v*/d*t*	I_D=6.2 A, V_{DS}=480 V, T_j=125 °C	50	V/ns
Gate source voltage	V_{GS}	static	±20	V
	V_{GS}	AC (*f*>1 Hz)	±30	
Power dissipation	P_{tot}	T_C=25 °C	74	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C
Reverse diode dv/dt [7)]	dv/dt		15	V/ns

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	1.7	K/W
Thermal resistance, junction - ambient	R_{thJA}	SMD version, device on PCB, minimal footprint	-	-	75	
		SMD version, device on PCB, 6 cm^2 cooling area[3)]	-	50	-	
Soldering temperature *)	T_{sold}	1.6 mm (0.063 in.) from case for 10 s	-	-	260	°C

Electrical characteristics, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=250 µA	600	-	-	V
Avalanche breakdown voltage	$V_{(BR)DS}$	V_{GS}=0 V, I_D=6.2 A	-	700	-	
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=0.26 mA	2.1	3	3.9	
Zero gate voltage drain current	I_{DSS}	V_{DS}=600 V, V_{GS}=0 V, T_j=25 °C	-	0.1	1	µA
		V_{DS}=600 V, V_{GS}=0 V, T_j=150 °C	-	-	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=3.9 A, T_j=25 °C	-	0.68	0.75	Ω
		V_{GS}=10 V, I_D=3.9 A, T_j=150 °C	-	1.82	-	
Gate resistance	R_G	f=1 MHz, open drain	-	1	-	
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=3.9 A	-	5.6	-	S

*) reflow soldering, MSL3

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=25 V, f=1 MHz	-	620	-	pF
Output capacitance	C_{oss}		-	200	-	
Reverse transfer capacitance	C_{rss}		-	17	-	
Effective output capacitance, energy related[4)]	$C_{o(er)}$	V_{GS}=0 V, V_{DS}=0 V to 480 V	-	28	-	
Effective output capacitance, time related[5)]	$C_{o(tr)}$		-	47	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=480 V, V_{GS}=10 V, I_D=6.2 A, R_G=12 Ω	-	7	-	ns
Rise time	t_r		-	12	-	
Turn-off delay time	$t_{d(off)}$		-	52	-	
Fall time	t_f		-	10	-	
Gate Charge Characteristics						
Gate to source charge	Q_{gs}	V_{DD}=480 V, I_D=6.2 A, V_{GS}=0 to 10 V	-	3.3	-	nC
Gate to drain charge	Q_{gd}		-	12	-	
Gate charge total	Q_g		-	24	31	
Gate plateau voltage	$V_{plateau}$		-	5.5	-	V

1) Pulse width limited by maximum temperature $T_{j,max}$ only

2) Repetitive avalanche causes additional power losses that can be calculated as $P_{AV}=E_{AR}*f$.

3) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

4) $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{DSS.}$

5) $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{DSS.}$

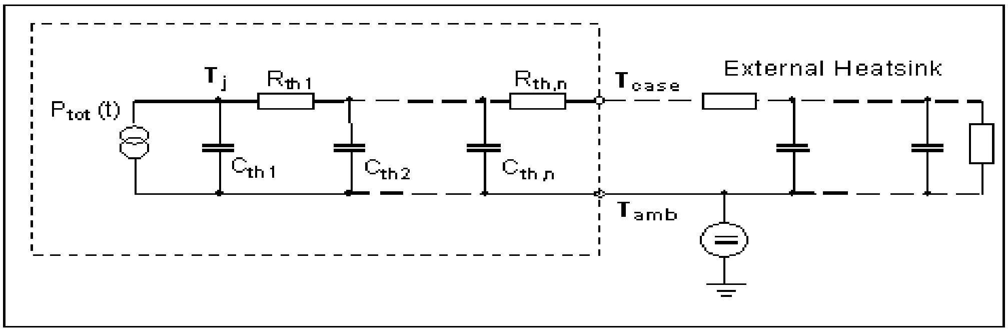
7) I_{SD}<=I_D, di/dt<=400A/us, V_{DClink}=400V, V_{peak}<$V_{BR, DSS}$, T_j<$T_{j,max}$.
Identical low-side and high-side switch.

0) J-STD20 and JESD22

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Reverse Diode						
Diode continuous forward current	I_S	T_C=25 °C	-	-	6.2	A
Diode pulse current	$I_{S,pulse}$		-	-	18.6	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=6.2 A, T_j=25 °C	-	0.97	1.2	V
Reverse recovery time	t_{rr}	V_R=480 V, I_F=I_S, di_F/dt=100 A/µs	-	400	-	ns
Reverse recovery charge	Q_{rr}		-	3.5	-	µC
Peak reverse recovery current	I_{rrm}		-	25	-	A

Typical Transient Thermal Characteristics

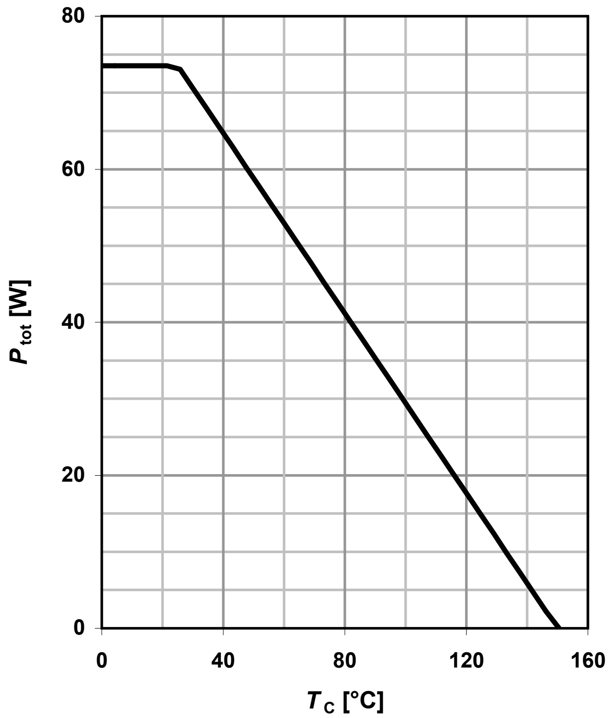
Symbol	Value	Unit	Symbol	Value	Unit
	typ.			typ.	
R_{th1}	0.0325	K/W	C_{th1}	0.0000502	Ws/K
R_{th2}	0.0448		C_{th2}	0.000303	
R_{th3}	0.251		C_{th3}	0.000428	
R_{th4}	0.31		C_{th4}	0.00243	
R_{th5}	0.231		C_{th5}	0.00344	
			C_{th6}	0.198[6)]	



6) C_{th6} models the additional heat capacitance of the package in case of non-ideal cooling. It is not needed if R_{thCA}=0 K/W.

1 Power dissipation

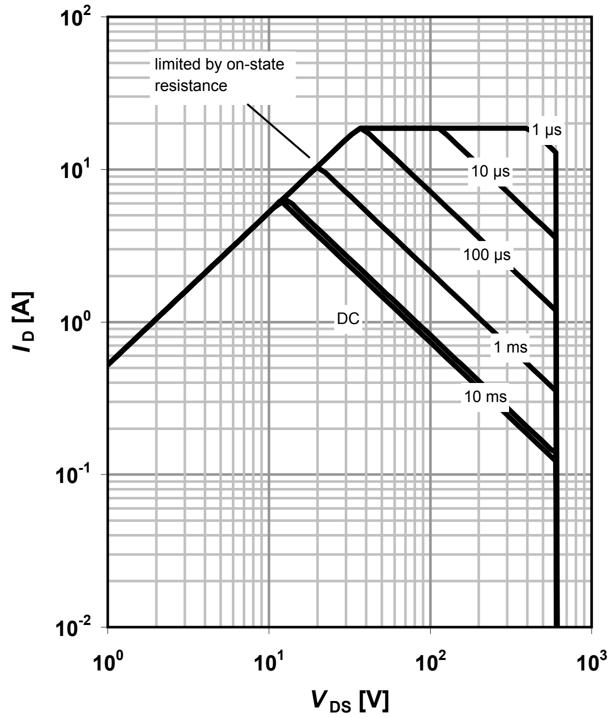
P_{tot}=f(T_C)



2 Safe operating area

I_D=f(V_{DS}); T_C=25 °C; D=0

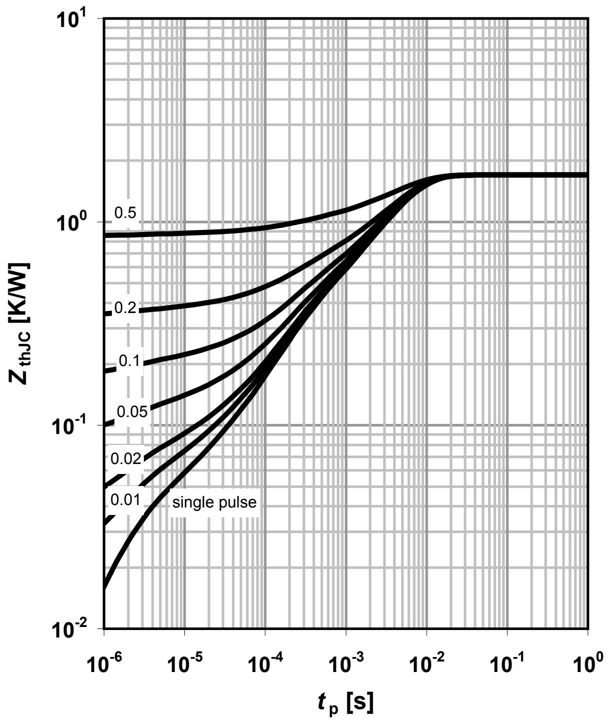
parameter: t_p



3 Max. transient thermal impedance

I_D=f(V_{DS}); T_j=25 °C

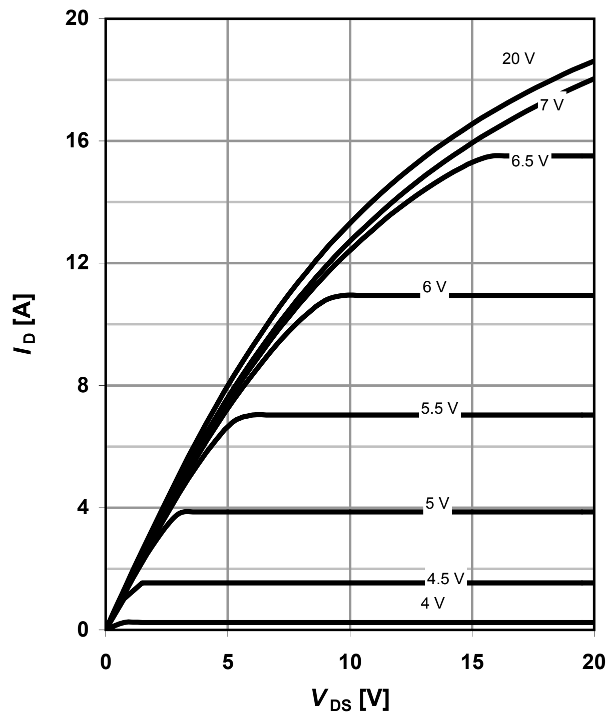
parameter: D=t_p/T



4 Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C

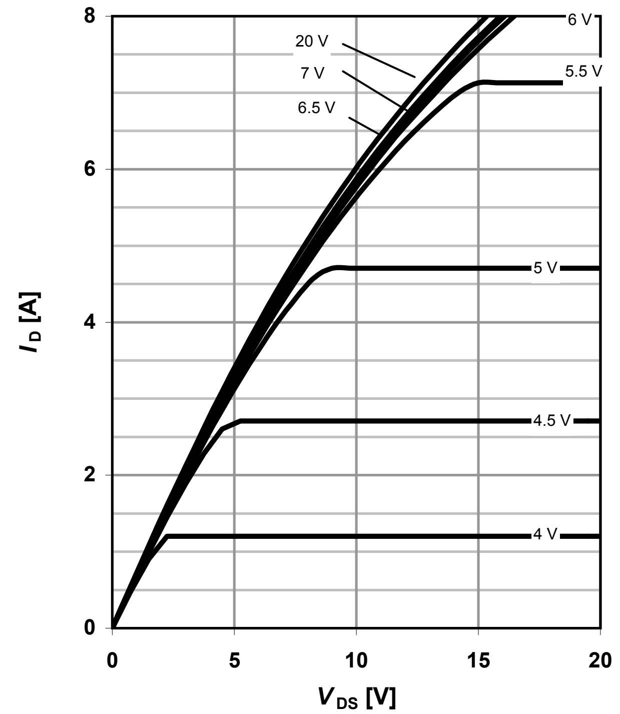
parameter: V_{GS}



5 Typ. output characteristics

I_D=f(V_{DS}); T_j=150 °C

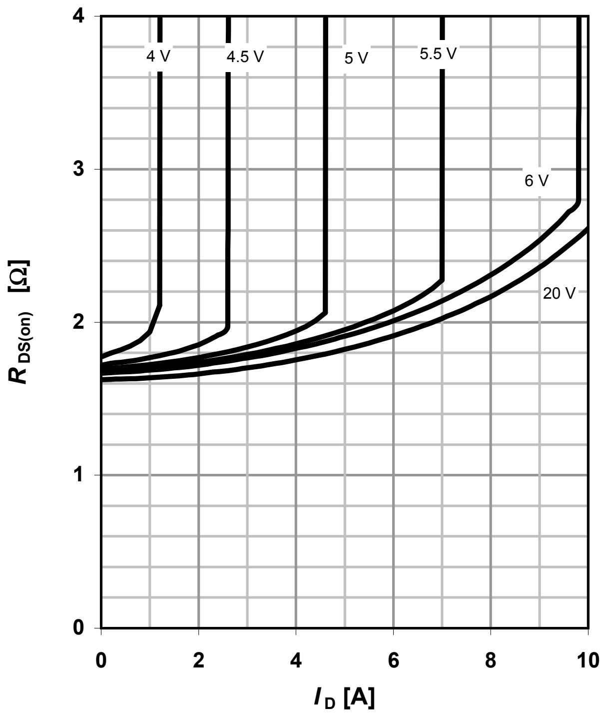
parameter: V_{GS}



6 Typ. drain-source on-state resistance

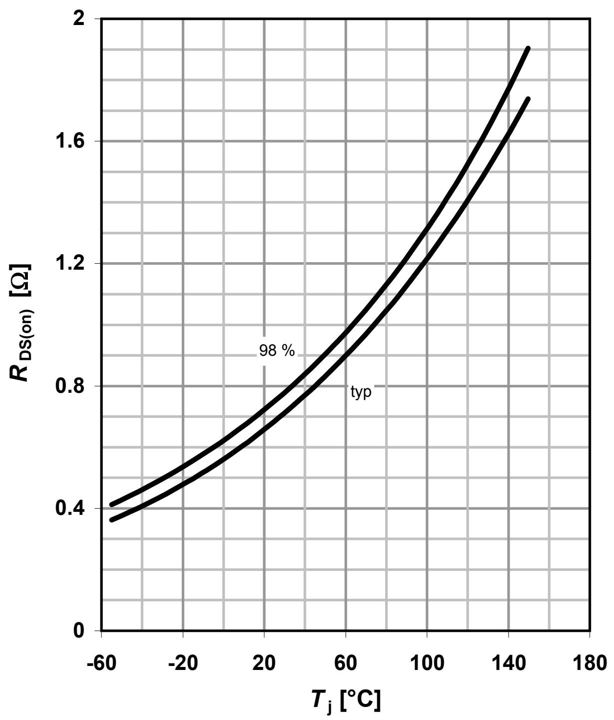
$R_{DS(on)}$=f(I_D); T_j=150 °C

parameter: V_{GS}



7 Drain-source on-state resistance

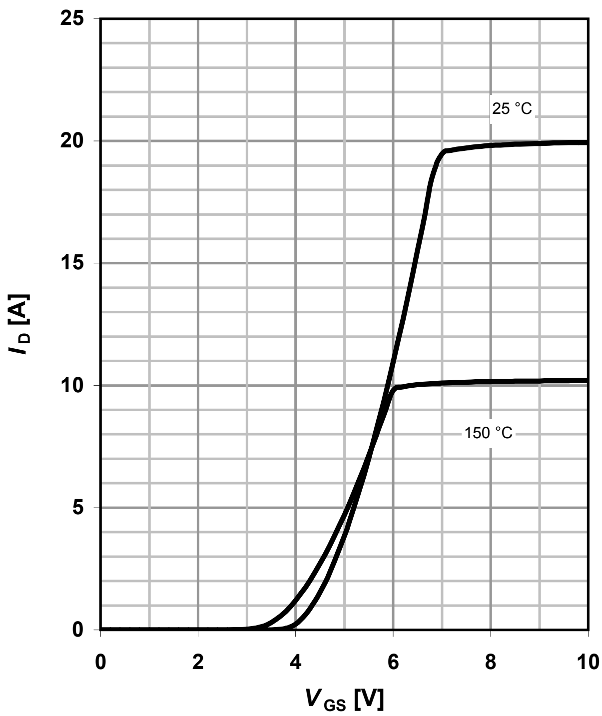
$R_{DS(on)}$=f(T_j); I_D=3.9 A; V_{GS}=10 V



8 Typ. transfer characteristics

I_D=f(V_{GS}); $|V_{DS}|$>2$|I_D|R_{DS(on)max}$

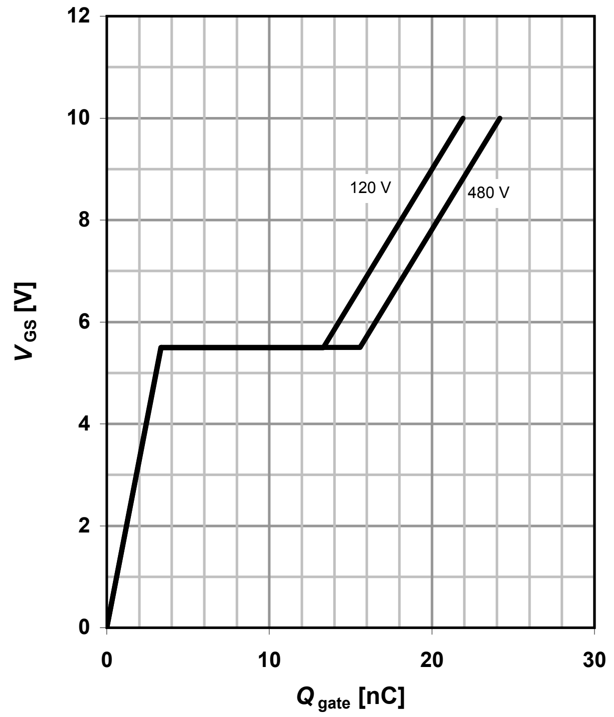
parameter: T_j



9 Typ. gate charge

V_{GS}=f(Q_{gate}); I_D=6.2 A pulsed

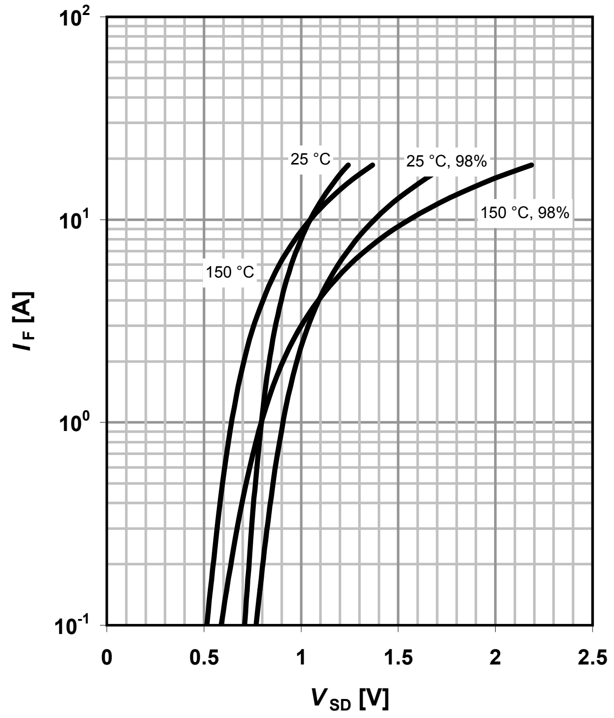
parameter: V_{DD}



10 Forward characteristics of reverse diode

I_F=f(V_{SD})

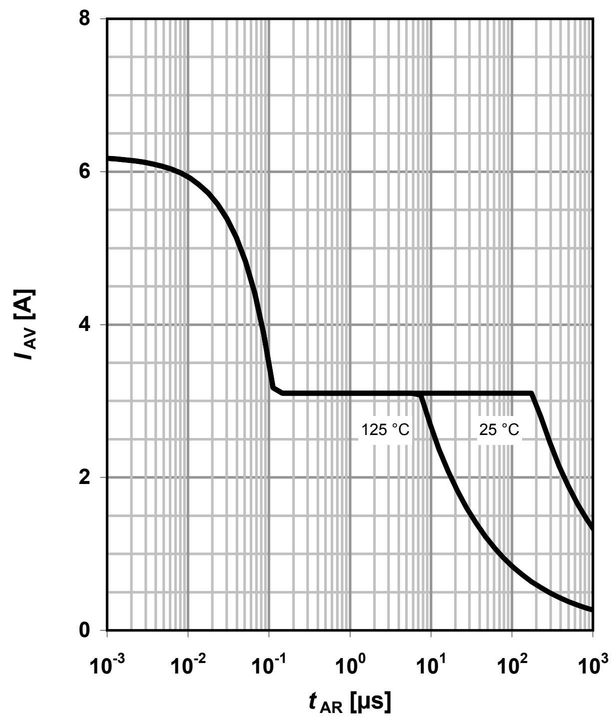
parameter: T_j



11 Avalanche SOA

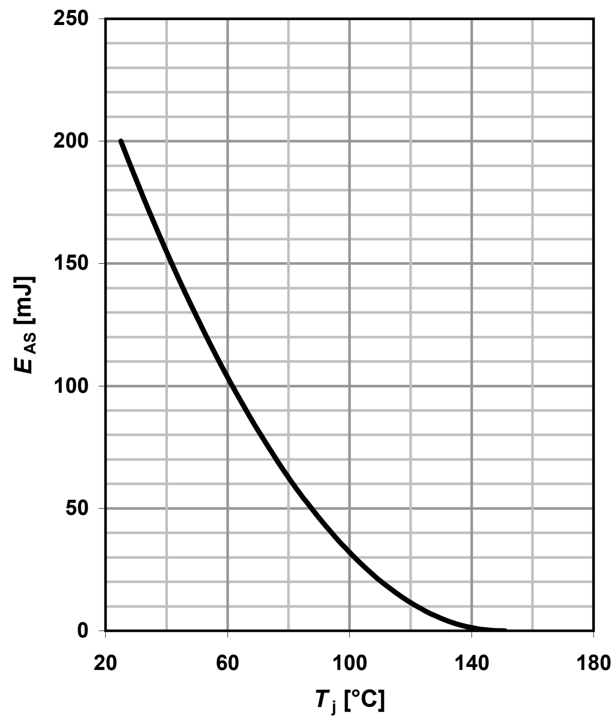
I_{AR}=f(t_{AR})

parameter: $T_{j(start)}$



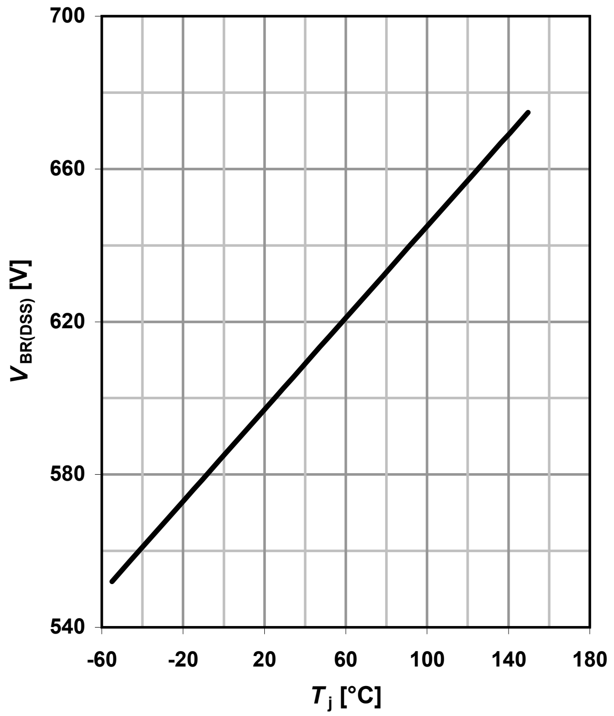
12 Avalanche energy

E_{AS}=f(T_j); I_D=3.1 A; V_{DD}=50 V



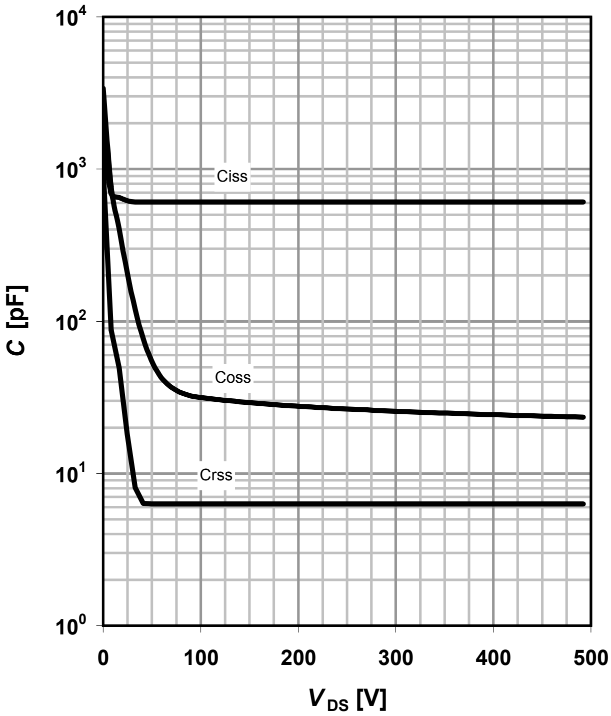
13 Drain-source breakdown voltage

$V_{BR(DSS)}$=f(T_j); I_D=0.25 mA



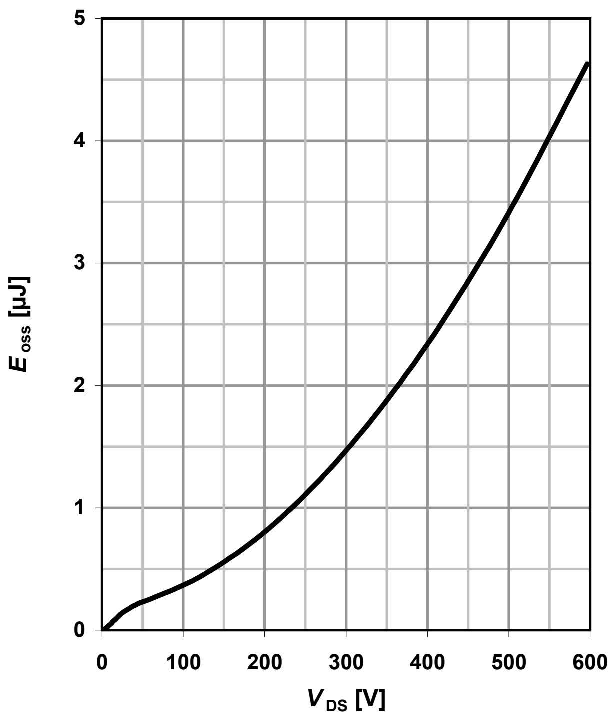
14 Typ. capacitances

C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

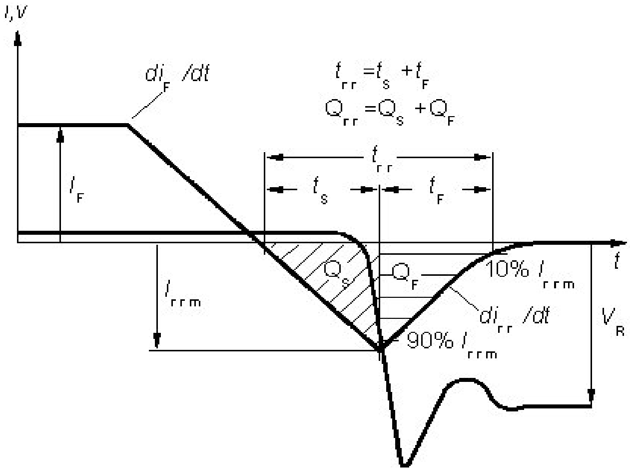


15 Typ. C_{oss} stored energy

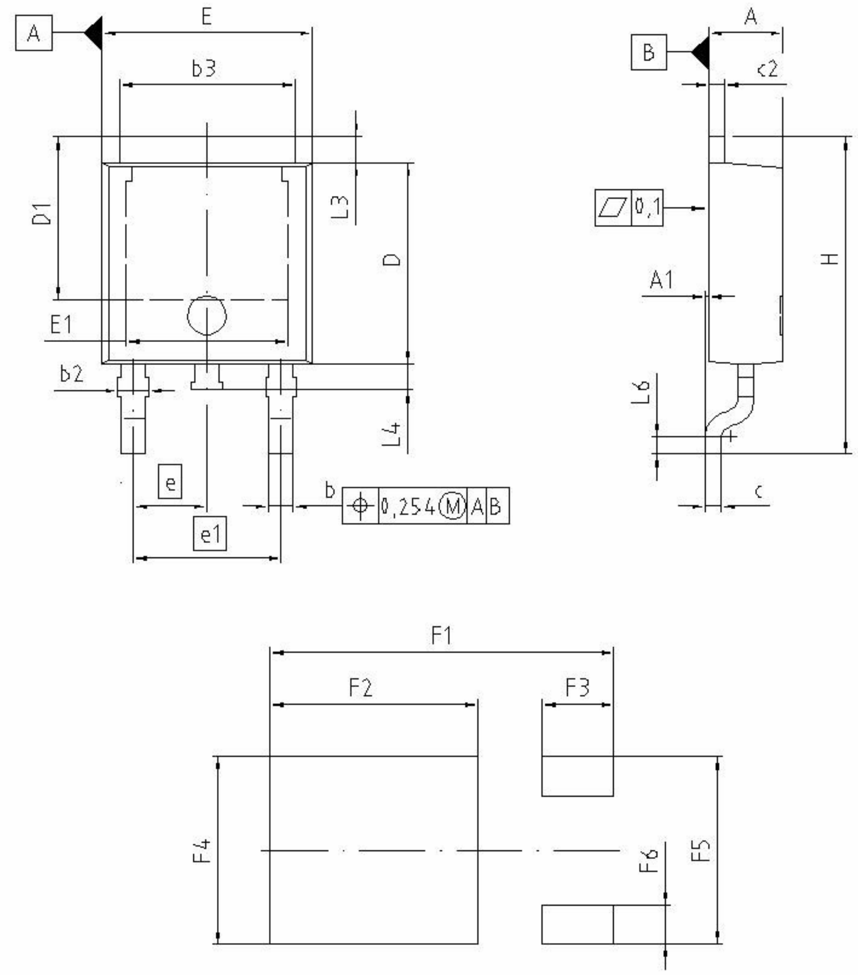
E_{oss}=f(V_{DS})



Definition of diode switching characteristics



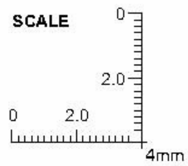
PG-TO252-3-1: Outline , PG-TO-252-3-11 (D-PAK), PG-TO-252-3-21 (D-PAK)



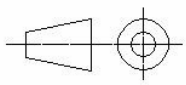
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.159	2.413	0.085	0.095
A1	0.000	0.150	0.000	0.006
b	0.635	0.889	0.025	0.035
b2	0.650	1.150	0.026	0.045
b3	5.004	5.500	0.197	0.217
c	0.457	0.580	0.018	0.023
c2	0.460	0.980	0.018	0.039
D	5.969	6.223	0.235	0.245
D1	5.020	5.842	0.198	0.230
E	6.400	6.731	0.252	0.265
E1	4.850	5.207	0.191	0.205
e	2.286		0.090	
e1	4.572		0.180	
N	3		3	
H	9.400	10.480	0.370	0.413
L3	0.900	1.143	0.035	0.045
L4	0.584	0.950	0.023	0.037
L6	0.510	0.686	0.020	0.027
F1	10.500	10.700	0.413	0.421
F2	6.300	6.500	0.248	0.256
F3	2.100	2.300	0.083	0.091
F4	5.700	5.900	0.224	0.232
F5	5.660	5.860	0.222	0.231
F6	1.100	1.300	0.043	0.051

REFERENCE
JEDEC TO252

SCALE



EUROPEAN PROJECTION



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