SIEMENS

ICs for Communications

Primary Rate Access Clock Generator and Transceiver
PRACT

PEB 22320

Version 2.1

Data Sheet 04.95

PEB 22320 Revision History	Current Version: 04.95
Previous Version:	05.93
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Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

Operating Range

In the operating range the functions given in the circuit description are fulfilled.

For detailed technical information about **“Processing Guidelines”** and **“Quality Assurance”** for ICs, see our Product Overview **“ICs for Communications”**

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SIEMENS

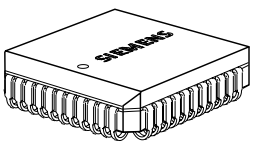
Primary Rate Access Clock Generator and Transceiver PRACT

PEB 22320

Preliminary Data

CMOS

1 Features



P-LCC-44

- ISDN line interface for 1544 and 2048 kbit/s (T1 and CEPT)
- Data and clock recovery
- Transparent to ternary codes
- Low transmitter output impedance for a high return loss with reasonable protection resistors (CCITT G.703 requirements for the line input return loss fulfilled)
- Adaptively controlled receiver threshold
- Programmable pulse shape for T1 applications
- Jitter specifications of CCITT I.431 and BELLCORE TR-NWT-000499 publications met
- Wander and jitter attenuation
- Jitter tolerance of receiver: 0.5 UI s
- Implements local and remote loops for diagnostic purposes
- Monolithic line driver for a minimum of external components
- Low power, reliable CMOS technology
- Loss of signal indication for receiver
- Clock generator for system clocks

Type	Ordering Code	Package
PEB 22320 N	Q67100-A6059	P-LCC-44 (SMD)

The Primary Rate Access Clock Generator and Transceiver PRACT (PEB 22320) is a monolithic CMOS device which implements the analog receive and transmit line interface functions to primary rate PCM carriers. It may be programmed or hard wired to operate in 1.544-Mbit/s (T1) or 2.048-Mbit/s (CEPT) carrier systems.

The PRACT recovers clock and data using an adaptively controlled receiver threshold. It will meet the requirement of CCITT I.431 and Bellcore TR-NWT-000499 Issue 5, December 1993 (Transport System Generic Requirements) in case of pulse shape, jitter tolerance and jitter transfer characteristic.

Features

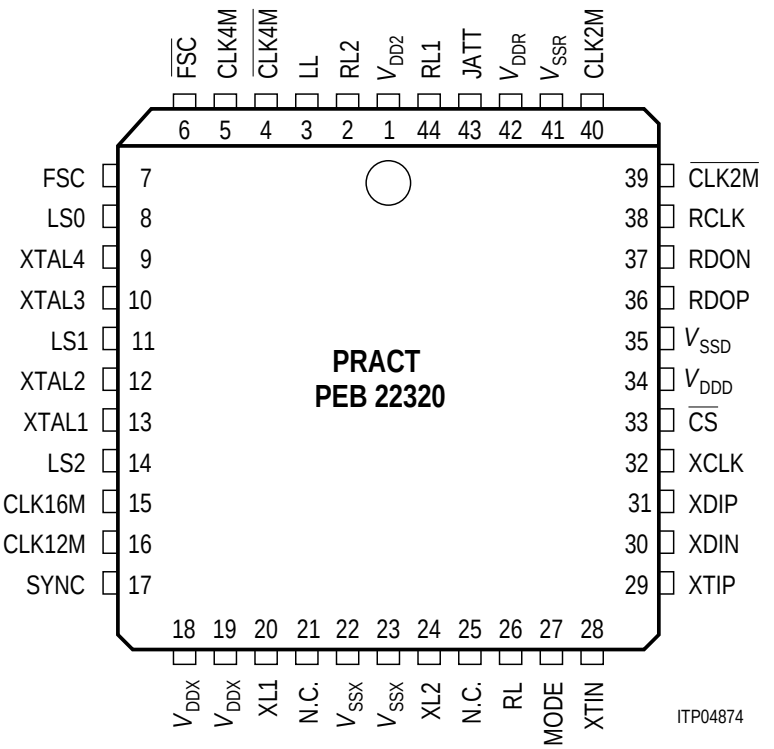
Specially designed line interface circuits simplify the tedious task of protecting the device against overvoltage damage while still meeting the return loss requirements.

The PRACT is suitable for use in a wide range of voice and data applications such as for connections of digital switches and PBX's to host computers, for implementations of primary ISDN subscriber loops as well as for terminal applications. The maximum range is determined by the maximum allowable attenuation.

In the T1 case the PRACT's power consumption is mainly determined by the line length and type of the cable.

1.1 Pin Configuration

(top view)



1.2 Pin Definitions and Functions

Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
1	V_{DD2}	O	Reference voltage for tapping the input transformer
2	RL2	I	Line receiver pin 2
3	LL	I	Local loopback: A high level selects the device for the local loopback mode.
4 5	$\overline{\text{CLK4M}}$ CLK4M	O O	System clock 4.096 MHz inverted and non-inverted
6 7	$\overline{\text{FSC}}$ FSC	O O	8-kHz frame synchronization pulse inverted and non-inverted
8	LS0	I	Line length select
9 10	XTAL4 XTAL3	O I	Crystal connection 12.352 MHz If an external clock generator is used and T1 mode is selected the PRACT works as a master.
11	LS1	I	Line length select
12 13	XTAL2 XTAL1	O I	Crystal connection 16.384 MHz When an external clock is used, normally if the MODE pin is set high, the PRACT functions as a master.
14	LS2	I	Line length select
15	CLK16M	O	System clock 16.384 MHz
16	CLK12M	O	System clock 12.352 MHz
17	SYNC	I	If a clock is detected at the SYNC pin the PRACT synchronizes to this clock (2.048 MHz for CEPT, 1.544 MHz for T1). (Please refer to **table 3**).
18, 19	V_{DDX}	I	Positive power supply for transmit subcircuits
20	XL1	O	Line transmit pin 1
21, 25	N.C.		not connected
22, 23	V_{SSX}	I	Ground for transmit subcircuits
24	XL2	O	Line transmit pin 2

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
26	RL	I	Remote loopback: High level puts the device to the remote loopback mode.
27	MODE	I	Master/Slave selection If the MODE pin is set to a low level the PRACT functions as a slave. (Please refer to **table 3**)
28 29	XTIN XTIP	I I	Positive and negative test data inputs, active low, full bauded
30 31	XDIN XDIP	I I	Positive and negative data inputs, active low, full bauded
32	XCLK	I/O	If the T1 mode is selected the XCLK is a clock output with a clock frequency of 1.544 MHz. Otherwise the XCLK is a clock input whose frequency is 2.048 MHz. (Please refer to **table 3**)
33	$\overline{CS}$	I	$\overline{\text{Chip Select}}$: A low level selects the PEB 22320 for a register write operation.
34	V_{DDD}	I	Positive power supply for the digital subcircuits.
35	V_{SSD}	I	Power ground supply for digital subcircuits.
36 37	RDOP RDON	O O	Receive data output positive and negative, fully bauded, active low.
38	RCLK	O	Receive clock refer to **table 3**.
39 40	$\overline{CLK2M}$ CLK2M	O O	System clock 2.048 MHz inverted and non-inverted.
41	V_{SSR}	I	Power ground supply for receive subcircuits.
42	V_{DDR}	I	Positive power supply for the receive subcircuits.
43	JATT	I	If the JATT pin is set to a low level the jitter attenuator is bypassed.
44	RL1	I	Line receiver pin 1.

1.3 System Integration

Figure 1 shows the architecture of a primary access board for data transmission. It exhibits the following functions:

– Line Interface (PEB 22320, PRACT)
– Clock and Data Recovery (PEB 22320, PRACT)
– Jitter Attenuation (PEB 22320, PRACT)
– Clock Generation (PEB 22320, PRACT)
– Coding/Decoding (PEB 2035, ACFA)
– Framing (PEB 2035, ACFA)
– Elastic Buffer (PEB 2035, ACFA)
– Multichannel Protocol Controller (PEB 20320, MUNICH32)
– System Adaptation (PEB 20320, MUNICH32)
– µP Interface (all devices)

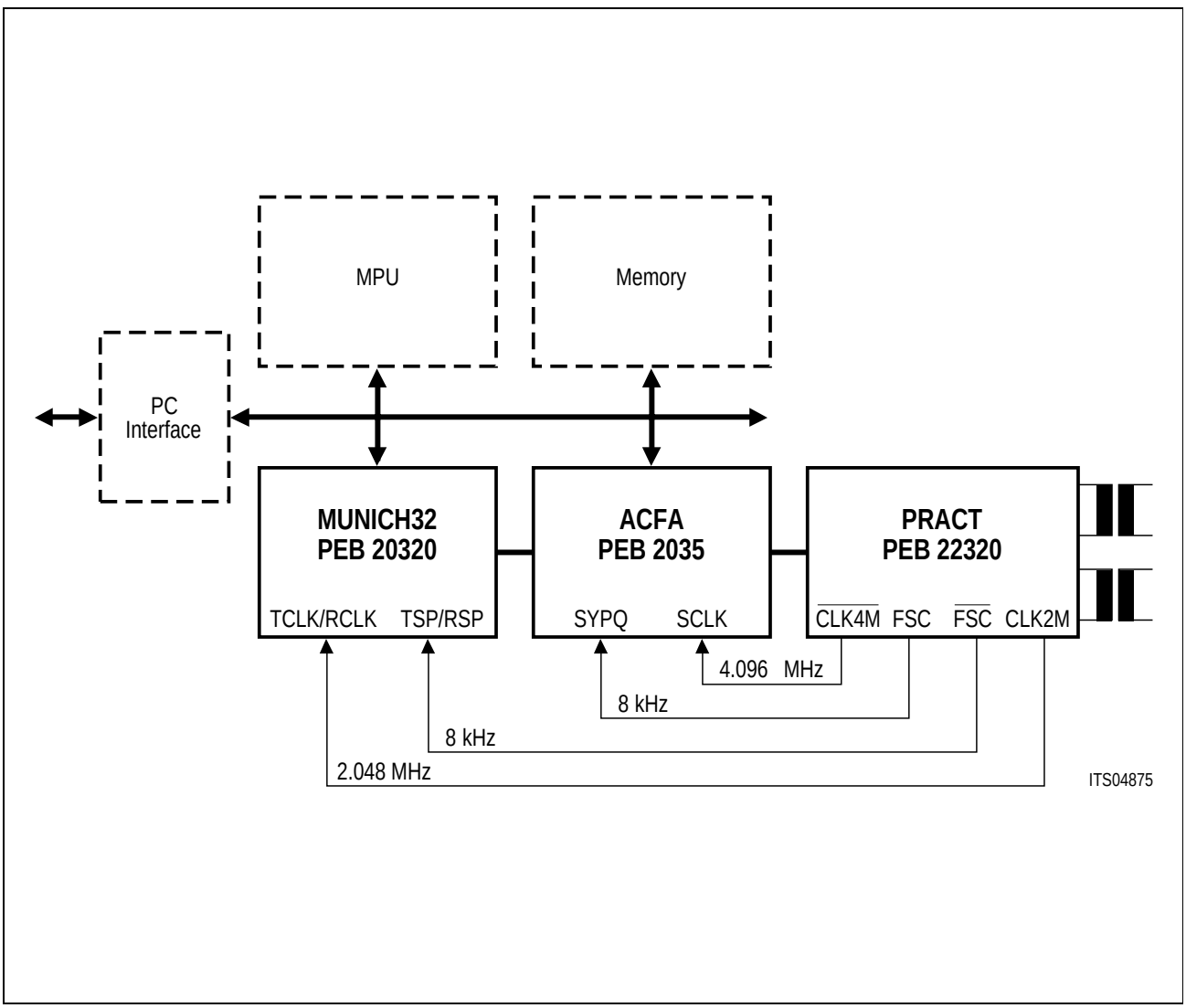


Figure 1
Architecture of the PRACT

2 Functional Description

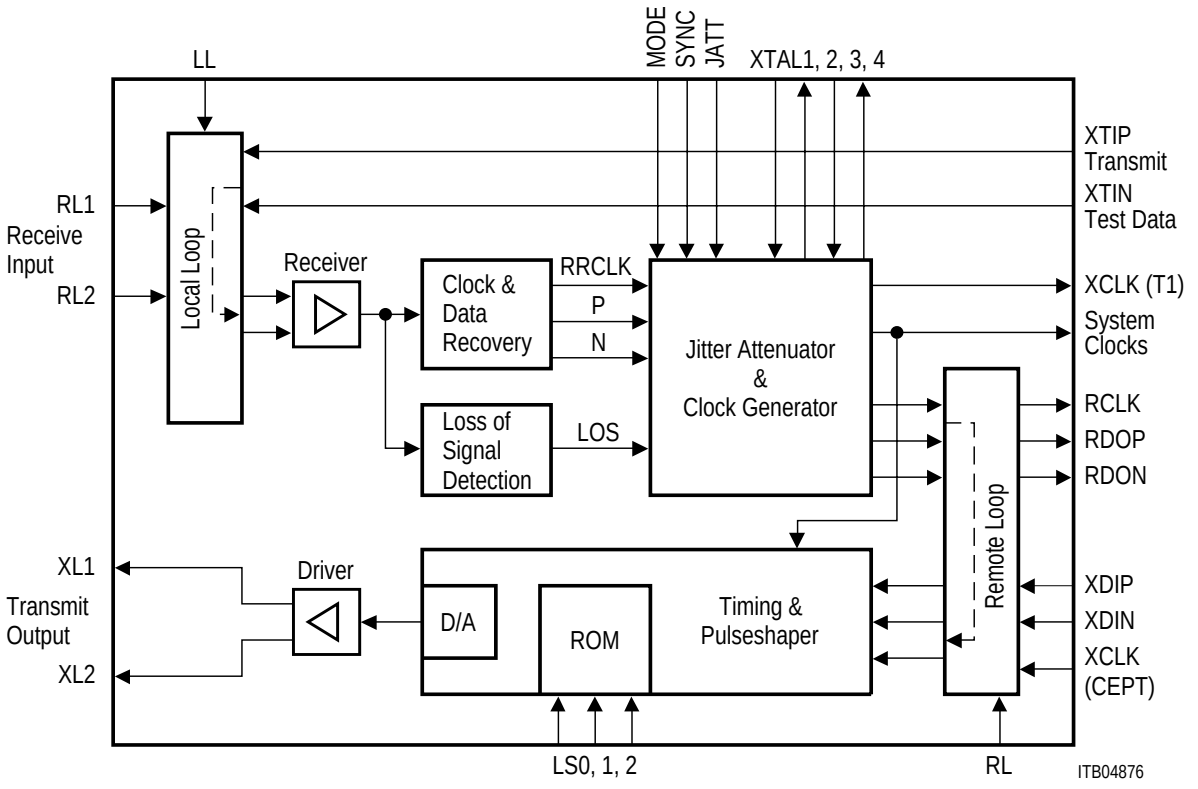


Figure 2
Functional Block Diagram of the PRACT

2.1 Receiver

2.1.1 Basic Functionality

The receiver recovers data from the ternary coded signal at the ternary interface and outputs it as 2 unipolar signals at the dual rail interface. One of the lines carries the positive pulses, the other the negative pulses of the ternary signal.

The signal at the ternary interface is received at both ends of a center-tapped transformer as shown in **figure 3**.

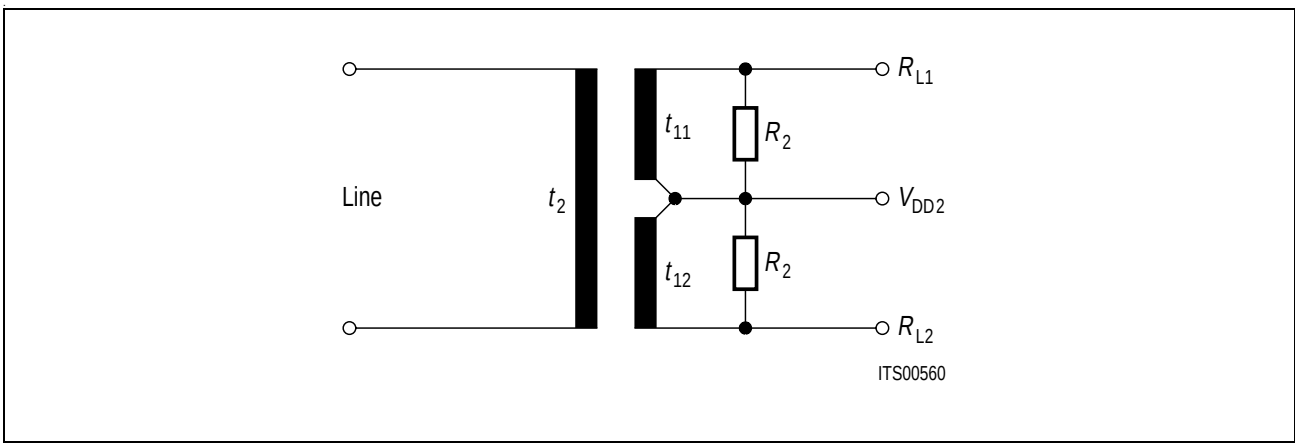


Figure 3
Receiver Configuration

The transformer is center-tapped at the PRACT side. The recommended transmission factors for the different line characteristic impedances are listed in **table 1**.

Table 1
Recommended Receiver Configuration Values

Application	T1		CEPT	
Characteristic Impedances [Ω]	100	140 (ICOT)	120	75
$R_2 \pm (2.5\%)$ [Ω]	28.7	39.2	60	60
$t_2 : t_1 = t_2 : (t_{11} + t_{12})$	69:52 69:(26 + 26)	69:52 69:(26 + 26)	52:52 52:(26 + 26)	41:52 41:(26 + 26)

Wired in this way the receiver has a return loss

a_r > 12 dB for 0.025 $f_b \leq f \leq$ 0.05 f_b,
a_r > 18 dB for 0.05 $f_b \leq f \leq$ 1.0 f_b and
a_r > 14 dB for 1.0 $f_b \leq f \leq$ 1.5 f_b,

with f_b being 2048 kHz. Thus it complies with CCITT G.703.

The receiver is transparent to the logical 1's polarity and outputs positive logical 1's on RDOP and negative logical 1's on RDON. RDON and RDOP are active low and fully bauded. The comparator threshold to detect logical 1's and logical 0's is automatically adjusted to be 45% of the peak signal level.

Provided the noise is below 10 μV/√Hz the bit error rate will be less than 10^{-7}.

2.1.2 Clock and Data Recovery

An analog PLL extracts the internal recovered route clock RRCLK from the data stream received at the RL1 and RL2 lines. The PLL uses as a reference the system clock CLK16M for CEPT and CLK12M for T1 applications. The clock and data recovery is tolerant to long strings of consecutive zeros, because the data sampler will continuously sample data based on its last input. A block diagram of the clock and data recovery circuit is shown in **figure 4**.

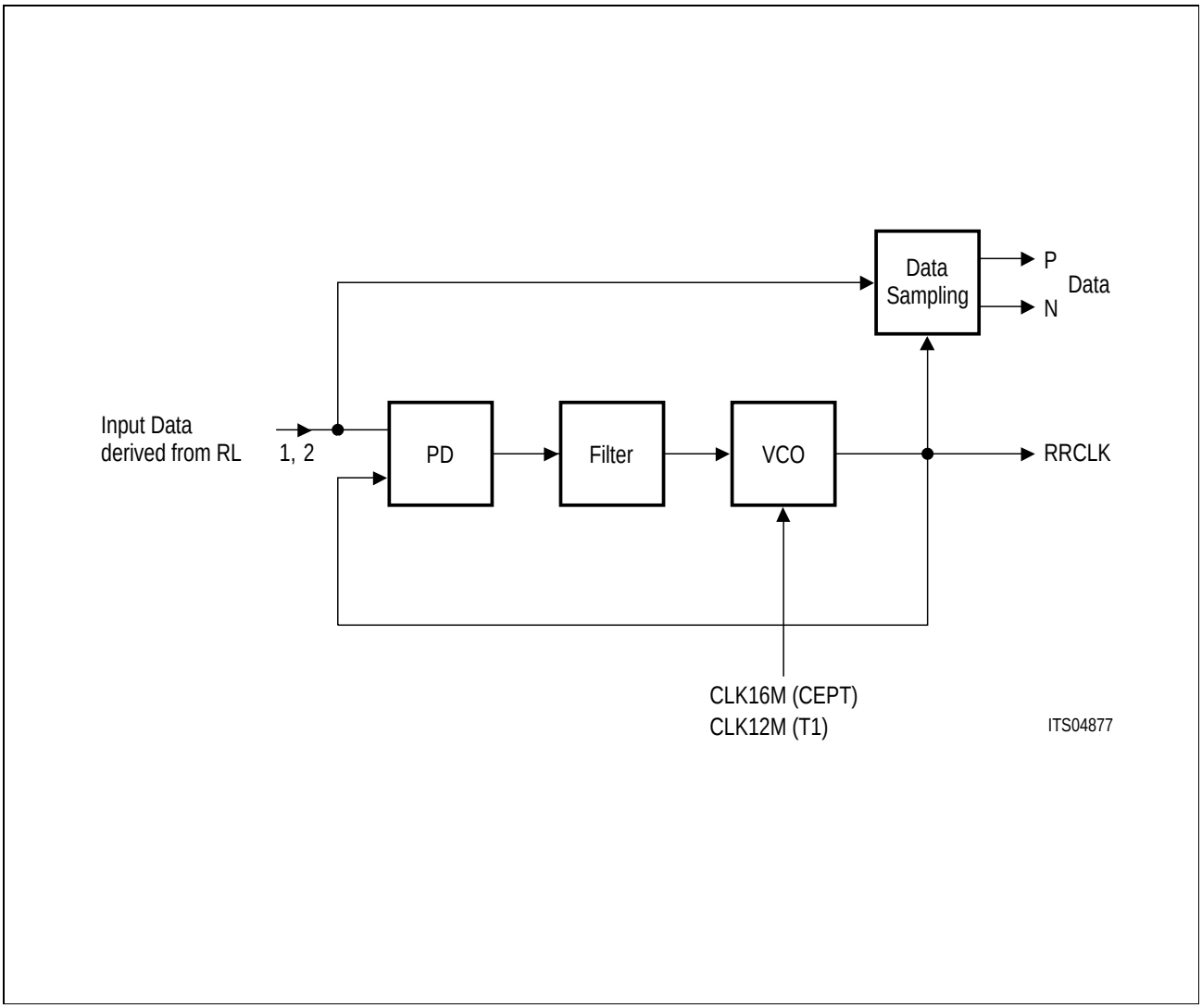


Figure 4
Clock and Data Recovery Circuit

2.1.3 Input Jitter Tolerance

The PRACT receiver's tolerance to input jitter complies to CCITT and Bellcore requirements for CEPT and T1 application.

Figure 5 shows the curves of the different input jitter specifications stated above as well as the PRACT performance for the various line codes used at the S1/S2 interfaces.

In **figure 5** the curves show that the PRACT at low frequencies has more than 20 dB/ decade fall off, and at high frequencies is in a steady state of 0.5 UI (horizontal).

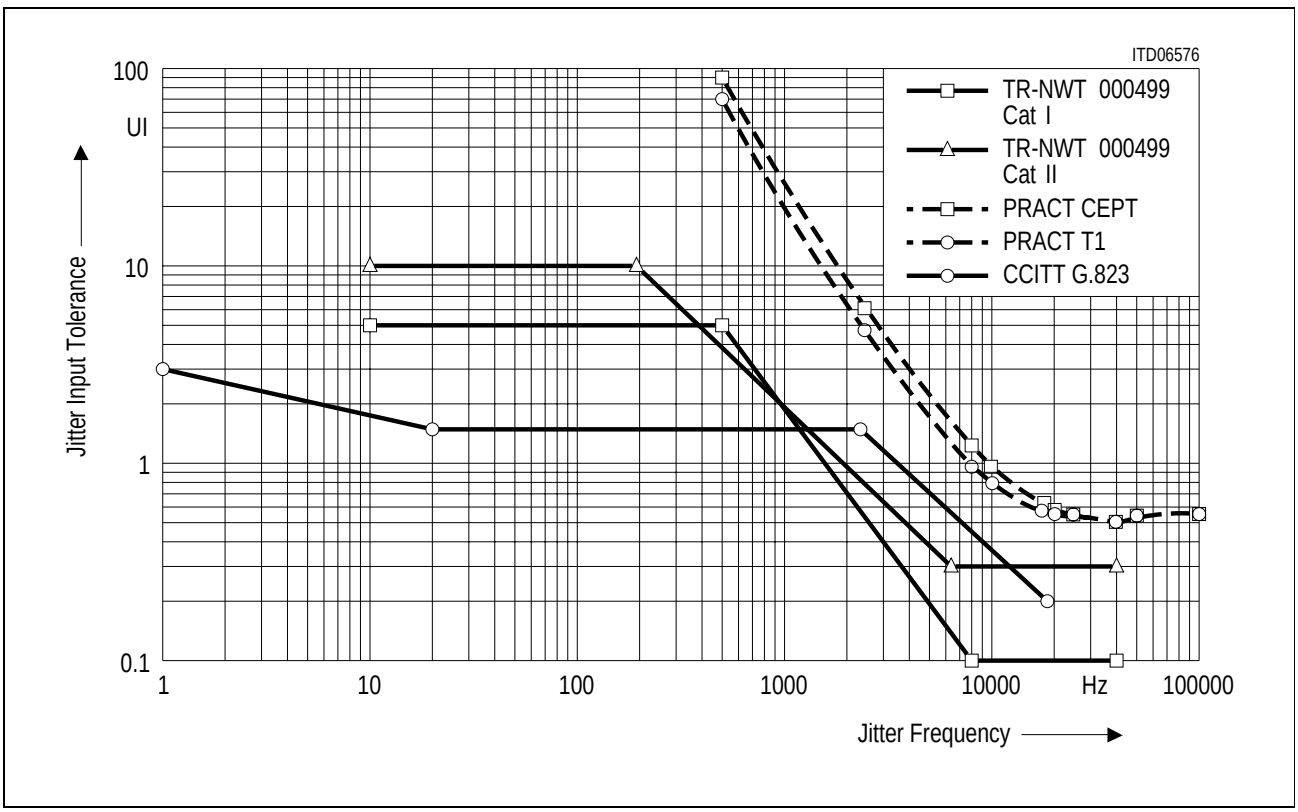


Figure 5
Comparison of Input Jitter Specification and PRACT Performance

Table 2
Jitter Input Tolerance

Frequency		TR-NWT 000499	TR-NWT 000499	PRACT	PRACT
Hz	**CCITT G.823**	**Cat I**	**Cat II**	**CEPT**	**T1**
1	2.9				
10		5	10		
20	1.5				
192.9			10		
500		5		90	70
2400	1.5			5.8	4.5
6430			0.3		
8000		0.1		1.15	0.95
10000				0.95	0.8
18000	0.2			0.62	0.58
20000				0.58	0.55
25000				0.55	0.55
40000		0.1	0.3	0.5	0.5
50000				0.55	0.55
100000				0.55	0.55

2.1.4 Jitter Attenuator and Clock Generator

The jitter attenuator reduces wander and jitter in the recovered clock which are produced by the line-, clock- and data-recovery characteristics. The attenuator consists of one PLL with a tunable crystal oscillator and a 288-bit FIFO. To provide for T1 mode a 1.544-MHz clock (XCLK) and a 2.048-MHz clock (CLK2M) for the system, a second PLL is placed in series with the first one (refer to **figure 6**).

If the JATT pin is set to low the FIFO is bypassed and the propagation delay from RL1, 2 to RDOP/RDON is reduced by the pass time of the FIFO.

After loss of signal detection, the internal PLL is synchronized to the 2.048 MHz (CEPT) provided at the SYNC pin (1.544 MHz in the case of T1). If this SYNC pin is not connected or connected to logical zero, the PRACT switches automatically to master operating mode (refer to **table 3**).

With the MODE pin a master selection is provided. That means if the MODE pin is set to high the master function is selected in which the VCO's of the jitter attenuator are centered (± 50 ppm of the crystal frequencies). If a clock is detected at the SYNC pin the PRACT automatically synchronized to this clock.

The jitter attenuator meets the jitter transfer requirements of the Bellcore TR-NWT 000 499 and Rec. I.431 (refer to **figure 7 and table 4**).

The amount of generated output jitter when no input jitter is shown in **table 5**.

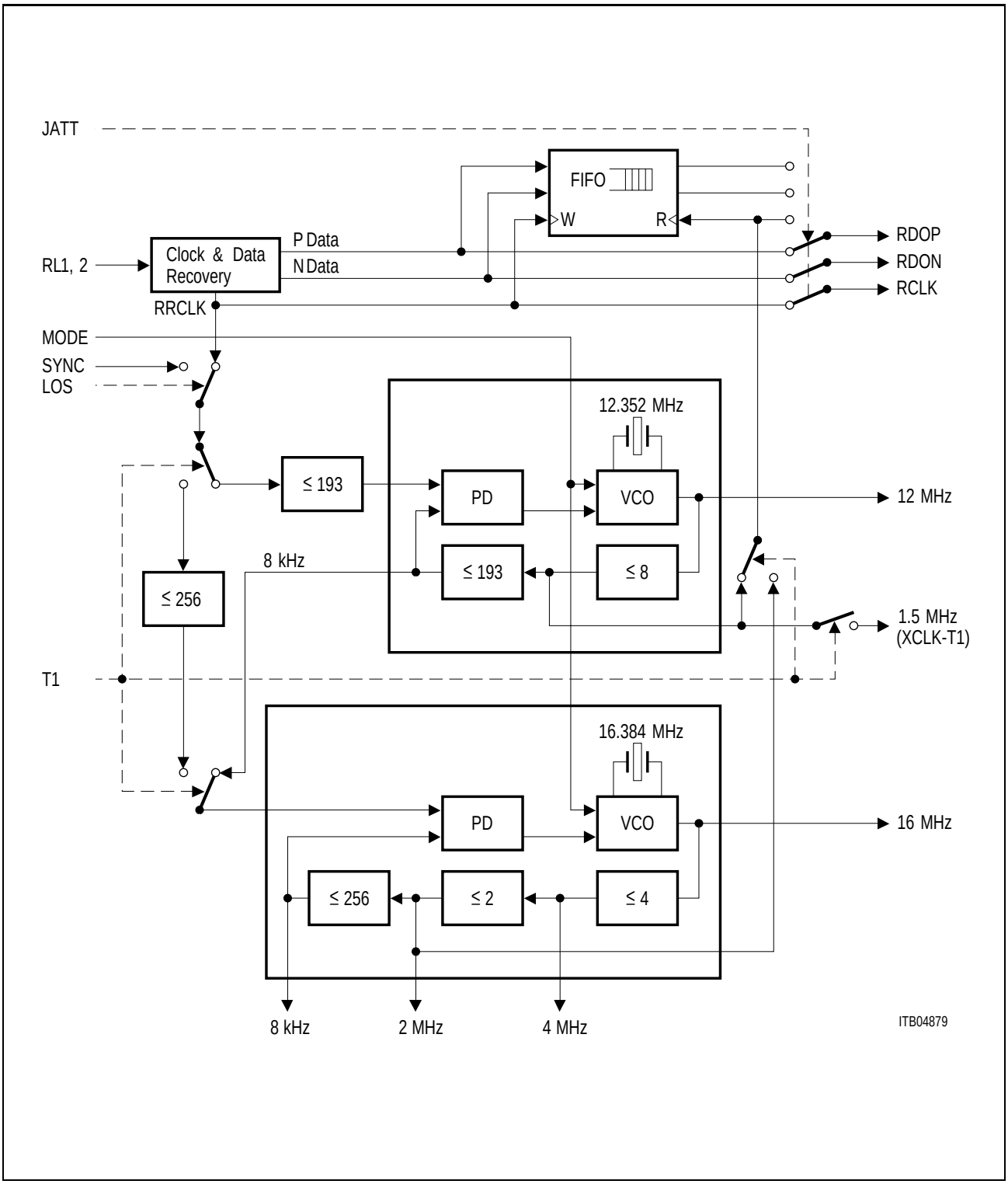


Figure 6
Jitter Attenuator Block Diagram

Table 3
Clock and Synchronization Table

Pin JATT	Int. Sig LOS	Pin SYNC	Pin MODE	Pin LS0..2	Pin XTAL3	Pin XTAL4	Pin XTAL1	Pin XTAL2	System Clocks 4M, 2M, 8K Derived from	Pin XCLK	Pin RCLK
1	0	X	0	T1	12 M Crystal		16 M Crystal		16 M crystal sync. on XCLK	output: 1.5 M sync. on RRCLK	=1.5 M
1	1	0	0	T1	12 M Crystal		16 M Crystal		16 M crystal sync. on XCLK	output: 1.5 M, freq. centered	=1.5 M
1	1	1.5 M	0	T1	12 M Crystal		16 M Crystal		16 M crystal sync. on XCLK	output: 1.5 M sync. on SYNC	=1.5 M
1	X	1.5 M	1	T1	12 M Crystal		16 M Crystal		16 M crystal sync. on XCLK	output: 1.5 M sync. on SYNC	=1.5 M
1	X	0	1	T1	12 M Crystal		16 M Crystal		16 M crystal sync. on XCLK	output: 1.5 M freq. centered	=1.5 M
1	X	X	X	T1	12 M in	N.C.	16 M Crystal		16 M crystal sync. on XCLK	output: 1.5 M sync. on XTAL3	=1.5 M
1	0	X	0	CEPT	X	X	16 M Crystal		16 M crystal sync. on RRCLK	input (2 M from ACFA)	=2 M
1	1	0	0	CEPT	X	X	16 M Crystal		16 M crystal sync. freq. centered	input (2 M from ACFA)	=2 M
1	1	2 M	0	CEPT	X	X	16 M Crystal		16 M crystal sync. on SYNC	input (2 M from ACFA)	=2 M
1	X	2 M	1	CEPT	X	X	16 M Crystal		16 M crystal sync. on SYNC	input (2 M from ACFA)	=2 M
1	X	0	1	CEPT	X	X	16 M Crystal		16 M crystal sync. freq. centered	input (2 M from ACFA)	=2 M
1	X	X	X	CEPT	X	X	16 M in	N.C.	16 M in	input (2 M from ACFA)	=2 M
0	0	X	0	T1	12 M Crystal		16 M Crystal		16 M crystal sync. on XCLK	output: 1.5 M sync. on RRCLK	=RRCLK
0	1	0	0	T1	12 M Crystal		16 M Crystal		16 M crystal sync. on XCLK	output: 1.5 M, freq. centered	=RRCLK
0	1	1.5 M	0	T1	12 M Crystal		16 M Crystal		16 M crystal sync. on XCLK	output: 1.5 M sync. on SYNC	=RRCLK
0	X	1.5 M	1	T1	12 M Crystal		16 M Crystal		16 M crystal sync. on XCLK	output: 1.5 M sync. on SYNC	=RRCLK
0	X	0	1	T1	12 M Crystal		16 M Crystal		16 M crystal sync. on XCLK	output: 1.5 M freq. centered	=RRCLK
0	X	X	X	T1	12 M in	N.C	16 M Crystal		16 M crystal sync. on XCLK	output: 1.5 M sync. on XTAL3	=RRCLK
0	0	X	0	CEPT	X	X	16 M Crystal		16 M crystal sync. on RRCLK	input (2 M from ACFA)	=RRCLK
0	1	0	0	CEPT	X	X	16 M Crystal		16 M crystal sync. freq. centered	input (2 M from ACFA)	=RRCLK
0	1	2 M	0	CEPT	X	X	16 M Crystal		16 M crystal sync. on SYNC	input (2 M from ACFA)	=RRCLK
0	X	2 M	1	CEPT	X	X	16 M Crystal		16 M crystal sync. on SYNC	input (2 M from ACFA)	=RRCLK
0	X	0	1	CEPT	X	X	16 M Crystal		16 M crystal sync. freq. centered	input (2 M from ACFA)	=RRCLK
0	X	X	X	CEPT	X	X	16 M in	N.C.	16 M in	input (2 M from ACFA)	=RRCLK

JATT = 1: Jitter attenuator enabled
JATT = 0: Bypass jitter attenuator

LOS = 0: Input above receiver threshold
LOS = 1: Input below receiver threshold

12 M = 12.352 MHz
16 M = 16.384 MHz
4 M = 4.096 MHz
2 M = 2.048 MHz
1.5 M = 1.544 MHz

RRCLK = Internal recovered route clock
SYNC = 0: Input tied to low
SYNC = 2 M: Input connected to 2 M
SYNC = 1.5 M: Input connected to 1.5 M

MODE = 0 Slave mode selected
MODE = 1: Master mode selected
8 k = 8.0 kHz
X = don't care
N.C. = No Connection

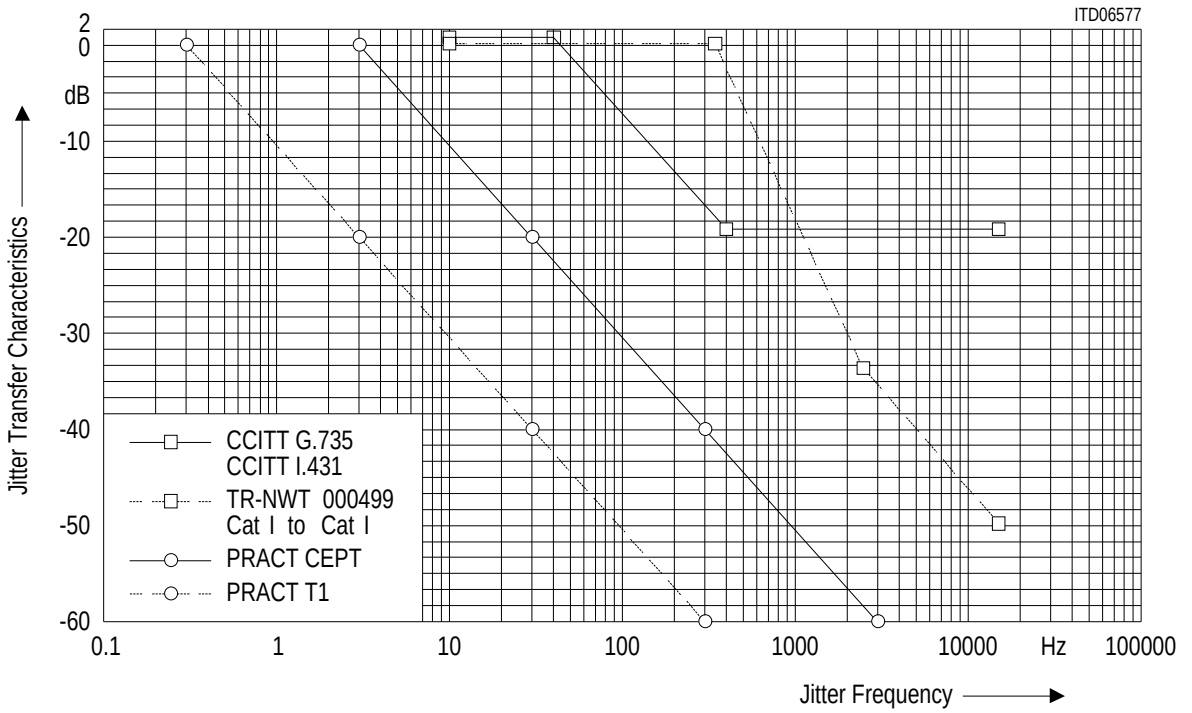


Figure 7
Jitter Attenuation Characteristics

Table 4
Jitter Transfer Characteristics

Frequency	CCITT G. 735	TR-NWT 000499	PRACT	PRACT
Hz	CCITT I.431	Cat I to Cat II	CEPT	T1
0.3				0.00
1				
3			0.00	– 20.00
10	0.5	0.10		
30			– 20.00	– 40.00
40	0.5			
100				

Table 4
Jitter Transfer Characteristics (cont'd)

Frequency	CCITT G. 735	TR-NWT 000499	PRACT	PRACT
Hz	**CCITT I.431**	**Cat I to Cat II**	**CEPT**	**T1**
200				
250				
300			– 39.40	– 60.00
350				
400	– 19.50			
9650				
1000				
1412				
2500		– 34.07		
3000			– 60.00	– -80.00
10000				
15000	– 19.50	– 49.63		

Table 5
Generated Output Jitter

Specification	Measurement Filter Bandwidth		Output Jitter
	Lower Cutoff	**Upper Cutoff**	**(UI peak to peak)**
I.431	20 Hz 700 Hz	100 kHz 100 kHz	≤ 0.125 ≤ 0.02
PUB 62411 Dez. 90	10 Hz 8 kHz 10 Hz	8 kHz 40 kHz 40 kHz	≤ 0.02 ≤ 0.025 ≤ 0.025
	broad band		≤ 0.05
ETS 300 011	40 Hz	100 kHz	≤ 0.11

2.2 Transmitter

2.2.1 Basic Functionality

The transmitter transforms unipolar data to ternary (alternate bipolar) return to zero signals of the appropriate shape. The unipolar data is provided at XDIP (positive pulses) and XDIN (negative pulses), synchronously with the transmit clock XCLK. XDIP and XDIN are active low and full bauded. Data is sampled on the falling edge of the input clock (XCLK). The input clock (XCLK) must be derived from the (system) clocks generated by the PRACT. This ensures the recommended fixed relationship between XLCK and internal generated clock (4 times XCLK) for the pulse shaper.

The transmitter includes a programmable pulse shaper to satisfy the requirements of the AT&T Technical Advisory # 34 at the cross connect point for T1 applications. The pulse shaper is programmed via the line length selection pins LS0, LS1 and LS2.

For T1 application the line length selection supports both low capacitance cable with a characteristic line capacitance of C' ≤ 40 nF/km = 65 nF/mile (e.g. MAT, ICOT) and higher capacitance cable with a characteristic line capacitance of 40 nF/km ≤ C' ≤ 54 nF/km (65 nF/mile ≤ C' ≤ 87 nF/mile) e.g. ABAM, PIC and PULP cables. This ensures that for various cable types the signal at the DSX-1 cross connect point complies with the pulse shape of the AT&T Technical Advisory # 34.

The line length is selected programming the LS0, LS1 and LS2 pins as shown for typical values in **table 6**.

Table 6
Line Length Selection

LS2	LS1	LS0		PIC/PULP Cable 24 AWG range/m			ICOT Cable range/m*		
0	0	0	CEPT		–			–	
0	0	1	T1/G.703	0	–	50	0	–	80
0	1	0	T1	20	–	80	65	–	145
0	1	1	T1	60	–	130	130	–	210
1	0	0	T1	110	–	200	195	–	275
1	0	1	T1	140	–	230	260	–	340
1	1	0	T1	210	–	290	325	–	405
1	1	1	T1	270	–	320	390	–	470

Note: * For ICOT-cable the characteristic impedance is 140 Ω
By selecting an all-zero code for LS0, LS1 and LS2 the PRACT can be adapted for CEPT applications.

The pulse shape according to CCIT G.703 (1544-kbit/s interface) is achieved by using the same line length selection code as for the lowest T1 cable range. To switch the device into a low power dissipation mode, XDIP and XDIN should be held high.

The transmitter requires an external step up transformer to drive the line. The transmission factor and the source serial resistor values can be seen in **figure 8** and **table 7** for the various applications.

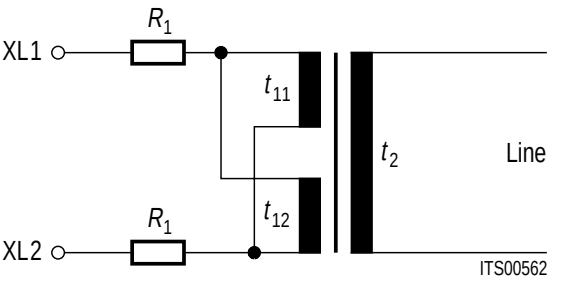


Figure 8
Transmitter Configuration

Table 7
Transmitter Configuration Values

Application	T1		CEPT	
Characteristic line impedance [Ω]	100	140 (ICOT)	120	75
$t_{11} : t_2 = t_{12} : t_2$	26:69	26:69	26:52	26:41
R_1 (± 2.5%) [Ω]	4.3	6	15	15

Wired in this way the transmitter has a return loss

a_r > 8 dB for 0.025 f_b ≤ f ≤ 0.05 f_b,
a_r > 14 dB for 0.05 f_b ≤ f ≤ 1.0 f_b and
a_r > 10 dB for 1.0 f_b ≤ f ≤ 1.5 f_b,

with f_b being 2048 kHz (CEPT applications). A termination resistor of 120 Ω is assumed.

In T1 applications the return loss is higher than 10 dB.

Please note, that the transformer ratio at the receiver is half of that at the transmitter. The same type of transformer can thus be used at the receiver and at the transmitter. At the transmitter the two windings are connected in parallel, at the receiver in series. Thus, unbalances are avoided.

2.2.2 Output Jitter

In the absence of any input jitter the PRACT generates the output jitter, which is specified in **table 5**.

Note: The generated output jitter on the line is the same as the output jitter of the system clocks.

2.3 Local Loopback

The local loopback mode disconnects the receive lines RL1 and RL2 from the receiver. Instead of the signals coming from the line the data provided at XTIP and XTIN are routed through the receiver. The XDIN and XDIP signals continue to be transmitted on the line. The local loopback occurs in response to LL going high.

2.4 Remote Loopback

In the remote loopback mode the clock and data recovered from the line inputs RL1 and RL2 are routed back to the line outputs XL1 and XL2 via the transmitter. As in normal mode they are also output at RDOP and RDON. XDIP and XDIN are disconnected from the transmitter.

The remote loopback mode is selected by a high RL signal.

2.5 Bypass Jitter Attenuator

If the JATT pin is set to low the jitter attenuator (FIFO) is bypassed and the propagation delay from the line to the dual rail interface is reduced by the path time of the FIFO. Also in this mode the jitter in the system clocks (CLK2M, CLK4M, FSC) is attenuated.

2.6 Microprocessor Interface

The PRACT is fully controlled by six parallel data lines (LS0, LS1, LS2, LL, RL and JATT) and one control line ($\overline{CS}$). To adapt the device to a standard microprocessor interface the low state of $\overline{CS}$ is decoded from the microprocessor address, $\overline{CS}$, $\overline{WR}$ and ALE lines.

To hardwire the chip, $\overline{CS}$ must be fixed to ground.

2.7 Receiver Loss of Signal Indication

In the case that the signal at the line receiver input (pins RL1, RL2) becomes smaller than $V_{in} \leq 0.3\ V_{OP}$ loss of signal is indicated. This voltage value corresponds to a line attenuation of about 14 dB in the CEPT case. This is performed by turning both signals RDOP, RDON after at least 32 bits simultaneously to 5 V, i.e. a logical 0 on both lines. The following ACFA processes this indication for the system. In this mode the PRACT synchronizes to the clock at the SYNC pin.

2.8 Master/Slave Selection

If the MODE pin is set to high and the SYNC pin is not connected or connected to V_{SS} the PRACT works as a master for the system. The VCO's of the jitter attenuator are centered ($\pm$ 50 ppm of the crystal frequencies) and the system clocks are stable (divided from the VCO frequencies). If a clock (2.048 MHz for CEPT, 1.544 MHz for T1) is detected at the SYNC pin the PRACT synchronizes automatically to this clock. In master mode, the PRACT is independent from the receiver loss of signal detection.

Note: The MODE pin can not be controlled by the µP interface and requires CMOS levels as input signals. It must always be connected either to V_{DD} or V_{SS}.
A voltage of 2.5 V at the MODE Pin switch the PRACT into test mode.

3 Operational Description

3.1 Reset

After power up resetting the device is necessary to synchronize the internal circuitries. After reset a stabel RCLK is available after 65536 clock cycles. This results in 32 ms in CEPT mode and 42.5 ms in T1 mode. A reset can be performed by two ways.

3.1.1 Reset with $\overline{CS}$ Pin Fixed to V_{SS}

In this reset operation the $\overline{CS}$ pin is normally hardwired to V_{SS}. Before giving a reset the operational mode has to be selected (CEPT, T1) by setting the pins LS2, LS1, LS0 to 000 for CEPT-application, to 001 for NTT-application or 001 … 111 for T1 application.

A reset is made by simultaneously setting both RL and LL to high ($\overline{CS}$ = 0) for at least 1 µs. Reset will be initiated on the falling edge of RL or LL, the one that falls first.

The following figures explain the procedure in some examples.

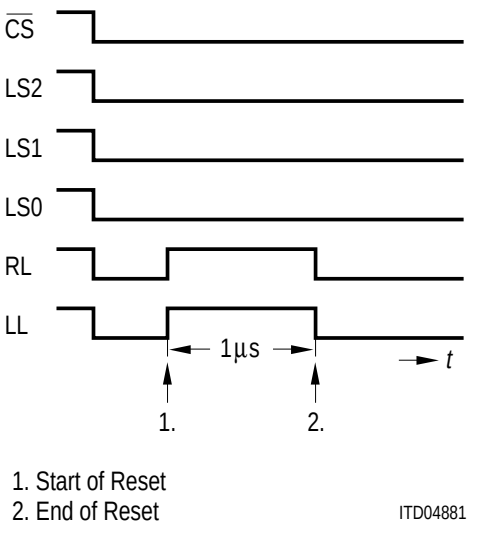
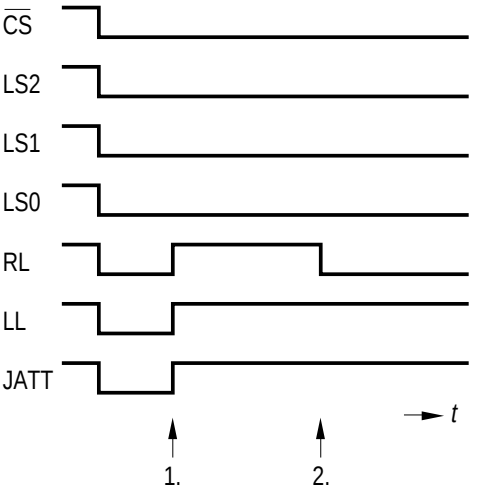


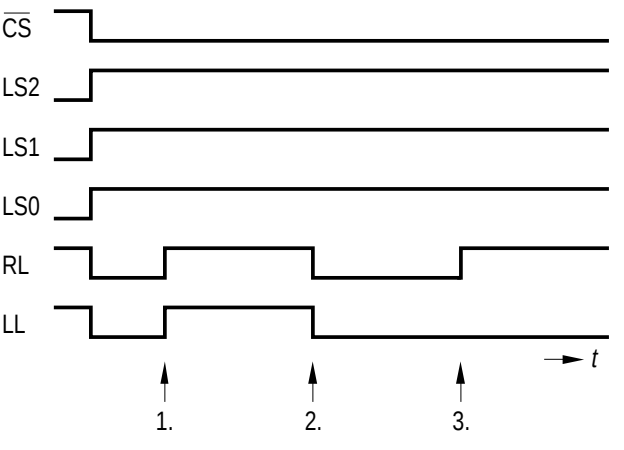
Figure 9
Resetting PRACT for CEPT Applications



1. Start of Reset
2. End of Reset and local loop is initiated

ITD04882

Figure 10
Resetting PRACT for CEPT Applications and Setting Local Loop with Jitter Attenuation



1. Start of Reset
2. End of Reset, regular operation in T1 Mode
3. Remote loop is initiated

ITD04883

Figure 11
Resetting PRACT for T1 Applications (max. line length selected) and Setting Remote Loop

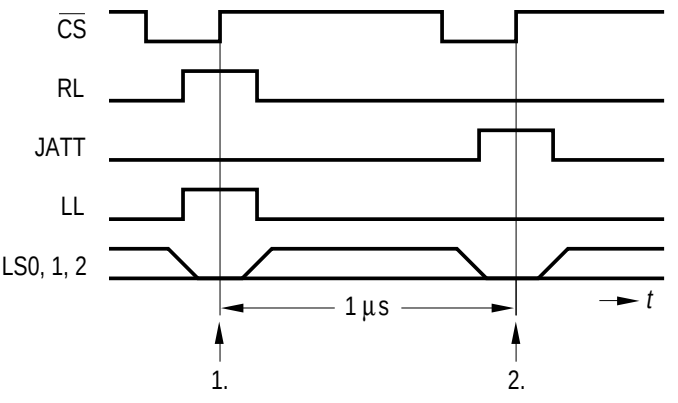
Note: If the PRACT is initiated for T1 applications the line length selection can be changed without a new reset.

3.1.2 Reset Using $\overline{CS}$ Pin to Latch Programming (a controller is used)

Reset is done by setting the pins RL and LL to logical 1 for at least 1 µs and latching these values into PRACT by a rising edge at pin $\overline{CS}$.

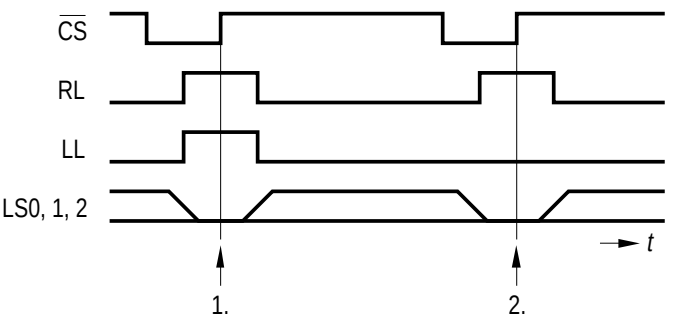
The selection of CEPT, T1 applications is achieved by setting the pins LS2, LS1, LS0 simultaneously with the reset to 000 for CEPT application or a T1 line length code (001 … 111 see **table 6**). The logical level of the RL, LL, LS2, LS1, LS0, JATT input parts are latched with the rising edge of the $\overline{CS}$. Refer to **figure 20**.

The following figures explain the procedure in some examples.



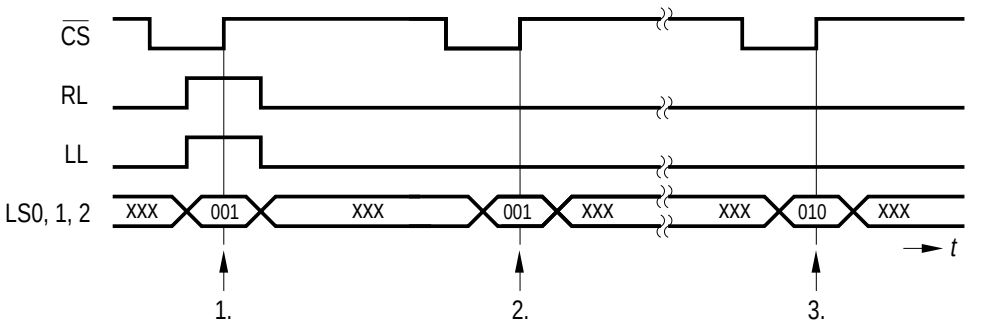
1. Start of Reset
2. End of Reset, Regular operation in CEPT Mode ITD04884

Figure 12
Resetting PRACT for CEPT Applications and Jitter Attenuation



1. Start of Reset
2. End of Reset and setting remote loop ITD04885

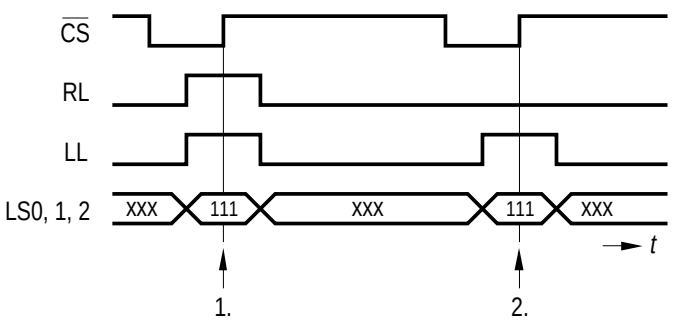
Figure 13
Resetting PRACT for CEPT Application and Setting Remote Loop



1. Start of Reset
2. End of Reset and setting line length code, Regular operation in T1 Mode
3. Changing line length code, Regular operation in T1 Mode with changed line length code

ITD04886

Figure 14
Resetting PRACT for T1 Applications and Changing Line Length Code



1. Start of Reset
2. End of Reset and setting local loop and line length code

ITD04887

Figure 15
Resetting PRACT for T1 Application and Setting Local Loop

3.2 Operation

The PRACT is in normal operation as soon as the reset phase is finished. The $\overline{CS}$ pin is activated again only when PRACT is reprogrammed (for example setting a loop or changing line length code). That means $\overline{CS}$ pin could be kept high for normal operation.

4 Electrical Specification

4.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Voltage on any pin with respect to ground	V_S	– 0.4 to V_{DD} + 0.4	V
Ambient temperature under bias	T_A	0 to 70	°C
Storage temperature	T_{stg}	– 65 to 125	°C

4.2 Delay Times

4.2.1 Delay from XDIP/XDIN to XL1/XL2

The delay from XDIP/XDIN to XL1,XL2 is 770 ns in T1 mode and 860 ns in CEPT mode. This relates to the falling edge of the XCLK and the leading edge of XL1 or XL2.

4.2.2 Delay from RL1/RL2 to RDOP/RDON

The delay from RL1/RL2 to RDOP/RDON is given with 700 ns in T1 mode and 540 ns in CEPT mode. This relates to the leading edge of the RL1 or RL2 to the falling edge of RDOP or RDON.

4.3 DC Characteristics

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5%, V_{SS} = 0 V

DC Characteristics

Parameter	Symbol	Limit Values		Unit	Test Condition	Pins
		min.	max.			
L-input voltage	V_{IL}	– 0.4	0.8	V		All pins except MODE, RLx, XLx XTALx, V_{DD2}, SYNC
H-input voltage	V_{IH}	2.0	V_{DD} + 0.4	V		
L-output voltage	V_{OL}		0.45	V	I_{OL} = 2 mA	
H-output voltage	V_{OH}	2.4		V	I_{OH} = – 400 µA	
H-output voltage	V_{OH}	V_{DD} – 0.5		V	I_{OH} = – 100 µA	
Input leakage current	I_{LI}		1	µA	0 V < V_{IN} < V_{DD} to 0 V	
Output leakage current	I_{LO}				0 V < V_{OUT} < V_{DD} to 0 V	
Peak voltage of a mark (CEPT)	V_{XCEPT}	2.7	3.3	V	wired according **figure 8** and **table 7**	XL1, XL2
Peak voltage of a mark (T1)	V_{XT1}	1.8	3.4	V	T1 application: depending on line length	
Transmitter output impedance	R_X		0.3	Ω		
Transmitter output current	I_X		50	mA	CEPT application	
			150	mA	T1 application: depending on line length	
Receiver input peak voltage of a mark	V_R [1)]	0.4	2.5	V		RL1, RL2
Loss of signal threshold	V_{LOS}	0.3		V		
Receiver input threshold	V_{RTH}		45	%		
Voltage at V_{DD2}	V_{DD2}	2.4	2.6	V		

DC Characteristics (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Condition	Pins
		min.	max.			
L-input voltage	V_{XTALIL}	– 0.4	1.0	V		XTAL1, XTAL2, XTAL3, XTAL4
H-input voltage	V_{XTALIH}	4.0	V_{DD} + 0.4	V		
Input leakage current	I_{XTALI}		1	µA	0 V ≤ V_{IN} ≤ V_{DD} to 0 V	
Operational power supply current	I_{CC}	40 55	110 190	mA mA	CEPT application T1 application, min value for all zeros, max value for all ones and max. line length for T1 appl.	
L-input voltage	V_{IL}	– 0.4	0.8	V		MODE, SYNC
H-input voltage	V_{IH}	4.0	V_{DD} + 0.4	V		
Input leakage current	I_{LI1} I_{LI2} I_{LI3} I_{LI4}		800 100 800 200	µA µA µA µA	V_{IL} = 0.8 V V_{IL} = 0.1 V V_{IH} = 4 V V_{IH} = V_{DD}	

1) Measured against V_{DD2}

4.4 Characteristics

T_A = 25 °C; V_{DD} = 5 V ± 5 %, V_{SS} = 0 V

Parameter	Symbol	Limit Values		Unit	Pins
		min.	max.		
Input capacitance	C_{IN}		10	pF	all except RLx, XLx, XTALx
Output capacitance	C_{OUT}		15	pF	all except RLx, XLx, XTALx
Input capacitance	C_{IN}		7	pF	RLx
Output capacitance	C_{OUT}		20	pF	XLx

4.5 Recommended Oscillator Circuits

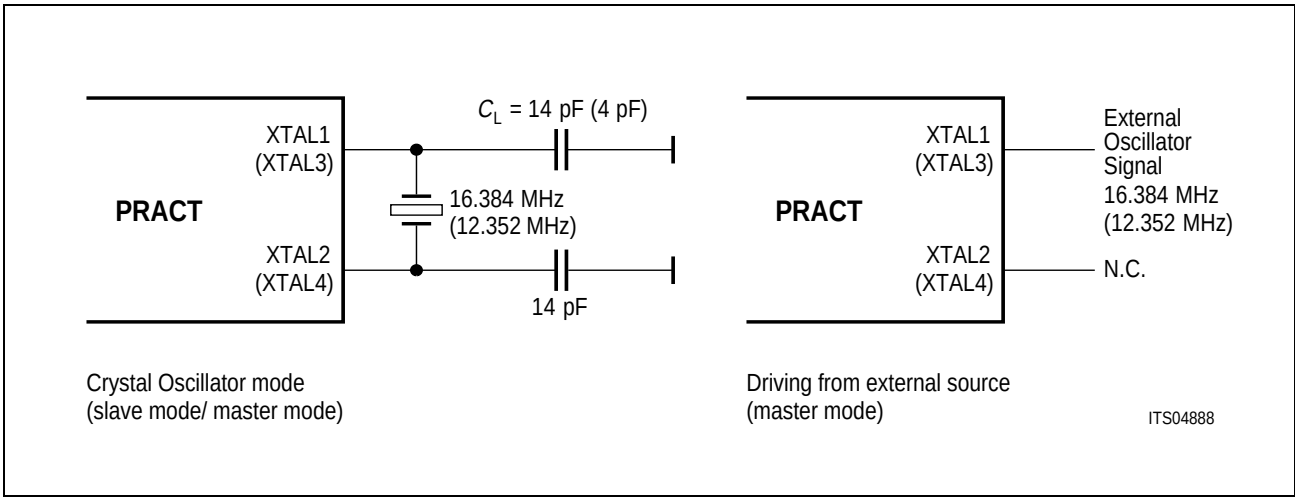


Figure 16
Oscillator Circuits

In CEPT mode if an external source is connected to XTAL1, the PRACT works, independent of the MODE pin, in master mode.

In T1 mode if an external source is connected to XTAL3, the PRACT works, independent of the MODE pin, in master mode. This operational mode requires a crystal (16.384 MHz) at pins XTAL1 and XTAL2. The frequency is locked to the external source.

The jitter attenuator requires unique performance specifications for the crystals.

The following typical crystal parameters will meet this specifications:

- Motional capacitance C_1 = 25 fF min
- Shunt capacitance C_0 = 7 pF max
- Load capacitance C_L = 18 pF typ, f_0 = 16.384 MHz
  C_L = 10 pF typ, f_0 = 12.352 MHz
- Resonance resistance $R_r \leq 25\ \Omega$

PRACT Tuning Range 16.384 MHz PLL
Crystal specified for C_L = 18 pF

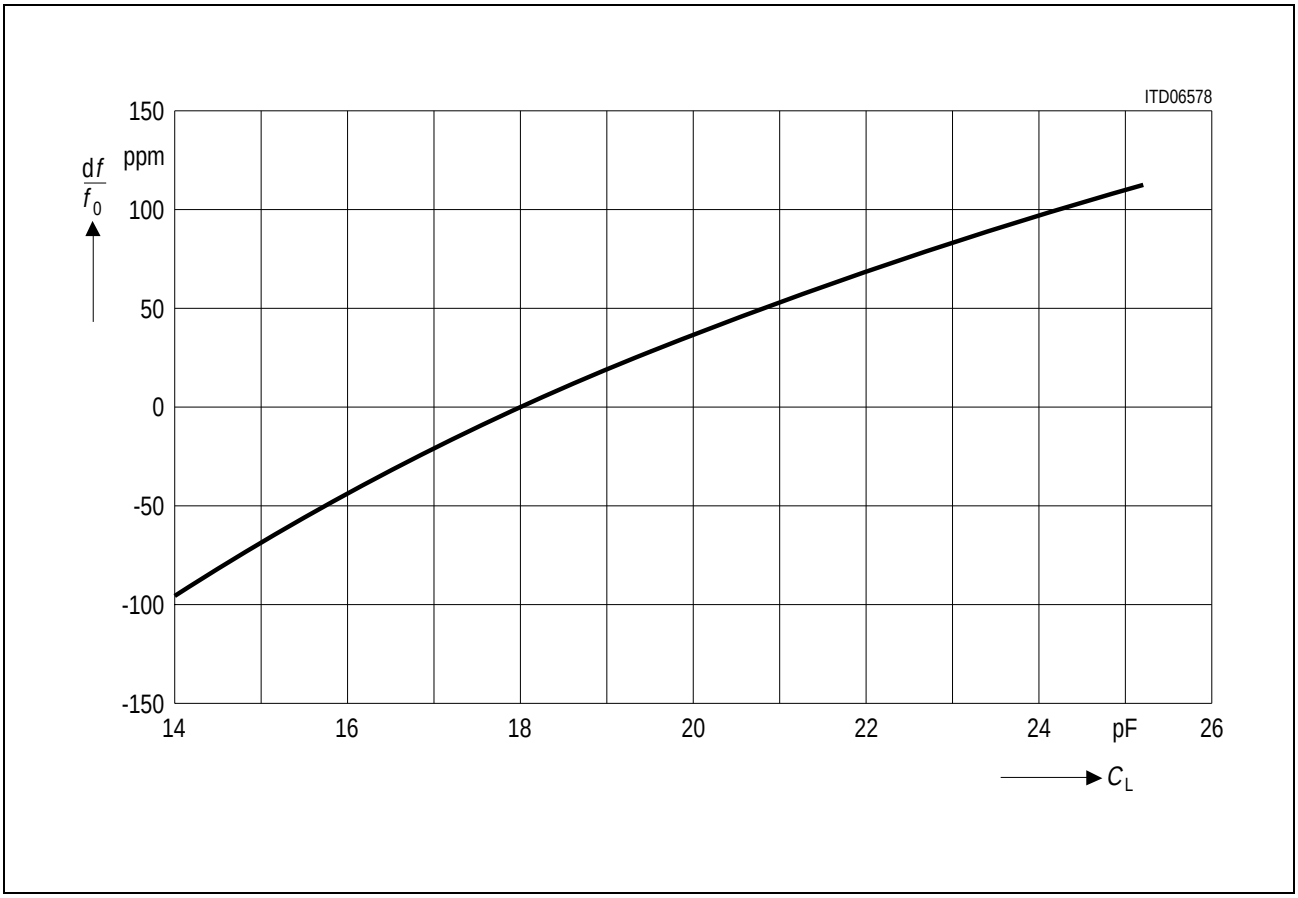


Figure 17
16.384-MHz Crystal Tuning Range

PRACT Tuning Range 12.352 MHz PLL
Crystal specified for C_L = 10 pF

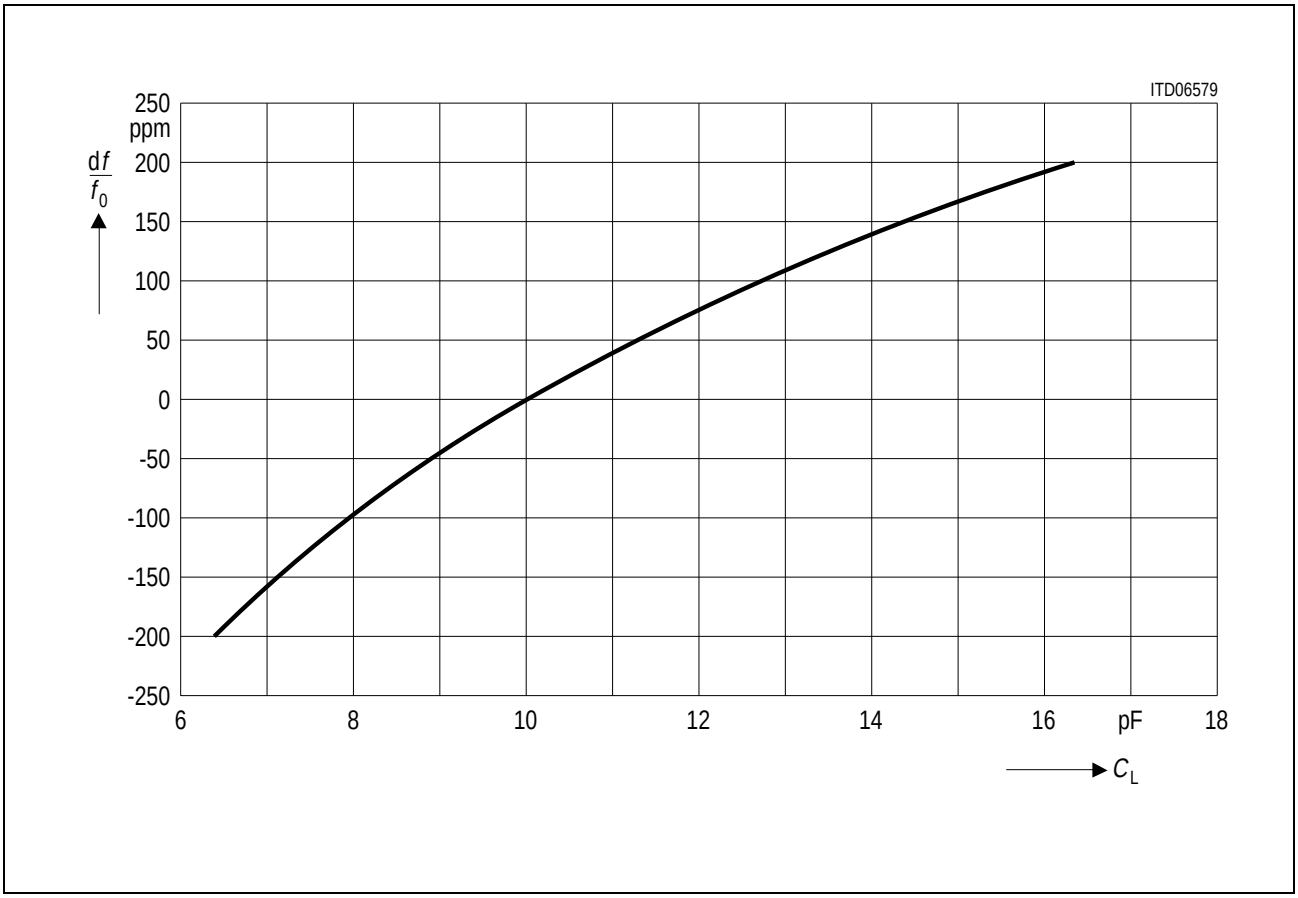


Figure 18
12.352-MHz Crystal Tuning Range

4.6 AC Characteristics

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %

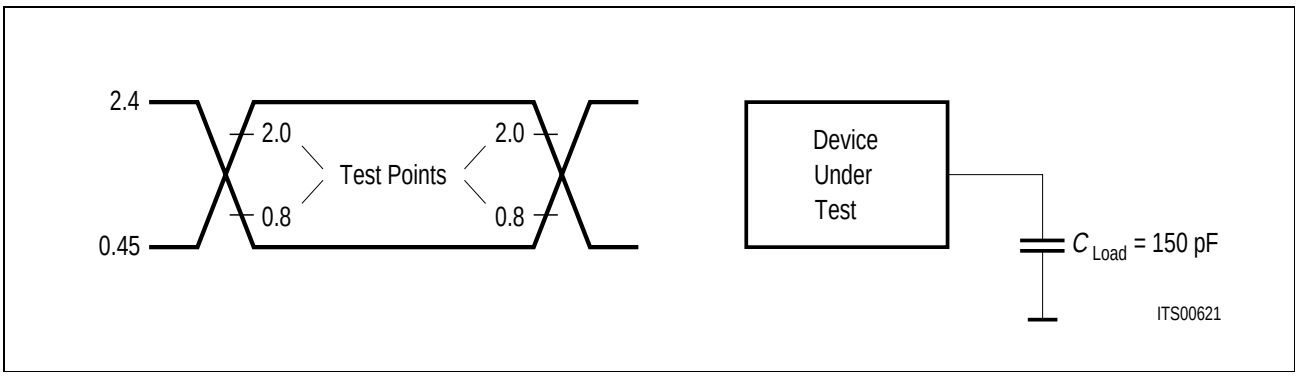


Figure 19
Input/Output Waveforms for AC Tests

Except from the line interface, inputs are driven at 2.4 V for a logical 1 and 0.4 V for a logical 0. Timing measurements are made at 2.0 V for a logical 1 and at 0.8 V for a logical 0. AC testing input/output waveforms are shown in **figure 19**.

4.6.1 Dual Rail Interface

RDOP, RDON, XDIP, XDIN, XTIP, XTIN are active low.

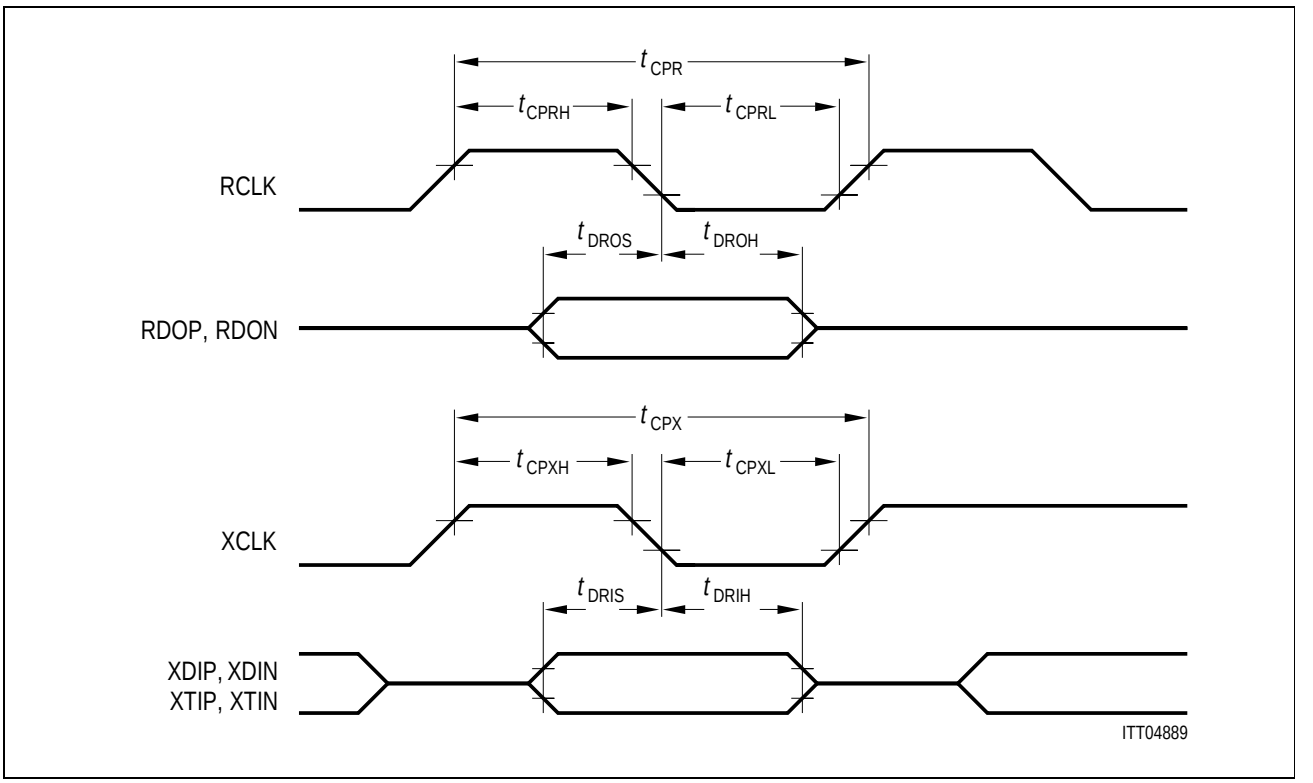


Figure 20
Timing of the Dual Rail Interface

Parameter	Symbol	Limit Values				Unit
		PCM 30		PCM 24		
		min.	max.	min.	max.	
RCLK clock period	t_{CPR}	typ. 488		typ. 648		ns
RCLK clock period low	t_{CPRL}	200		260		ns
RCLK clock period high	t_{CPRH}	200		260		ns
Dual rail output setup	t_{DROS}	200		260		ns
Dual rail output hold	t_{DROH}	200		260		ns
XCLK clock period	t_{CPX}	typ. 488		typ. 648		ns
XCLK clock period low	t_{CPXL}	200		250		ns
XCLK clock period high	t_{CPXH}	200		250		ns
Dual rail input setup	t_{DRIS}	25		25		ns
Dual rail input hold	t_{DRIH}	25		25		ns

4.6.2 System Clock Interface

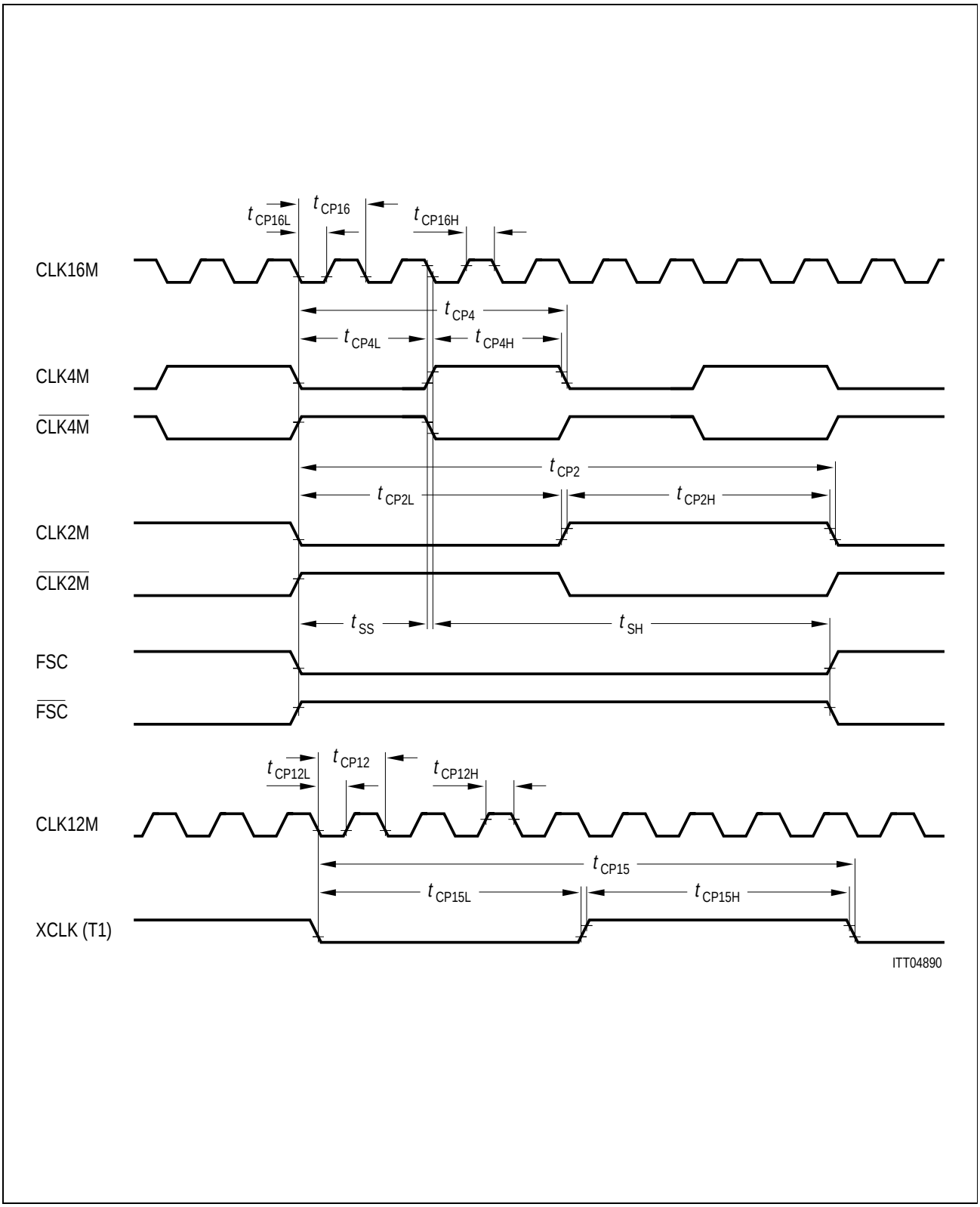


Figure 21
Timing of the System Clock Interface

System Clock Interface Timing Parameter Values

Parameter	Symbol	Limit Values		Unit
		min.	max.	
CLK16M period 16 MHz	t_{CP16}	typ. 61		ns
CLK16M period 16 MHz low	t_{CP16L}	20		ns
CLK16M period 16 MHz high	t_{CP16H}	20		ns
CLK4M period 4 MHz	t_{CP4}	typ. 244		ns
CLK4M period 4 MHz low	t_{CP4L}	110		ns
CLK4M period 4 MHz high	t_{CP4H}	110		ns
CLK2M period 2 MHz	t_{CP2}	typ. 488		ns
CLK2M period 2 MHz low	t_{CP2L}	220		ns
CLK2M period 2 MHz high	t_{CP2H}	220		ns
FSC setup time	t_{SS}	110		ns
FSC hold time	t_{SH}	240		ns
CLK12M period 12 MHz	t_{CP12}	typ. 81		ns
CLK12M period 12 MHz low	t_{CP12L}	30		ns
CLK12M period 12 MHz high	t_{CP12H}	30		ns
XCLK period 1.5 MHz	t_{CP15}	typ. 648		ns
XCLK period 1.5 MHz low	$t_{CP15\ L}$	300		ns
XCLK period 1.5 MHz high	$t_{CP15\ H}$	300		ns

4.6.3 Microprocessor Interface

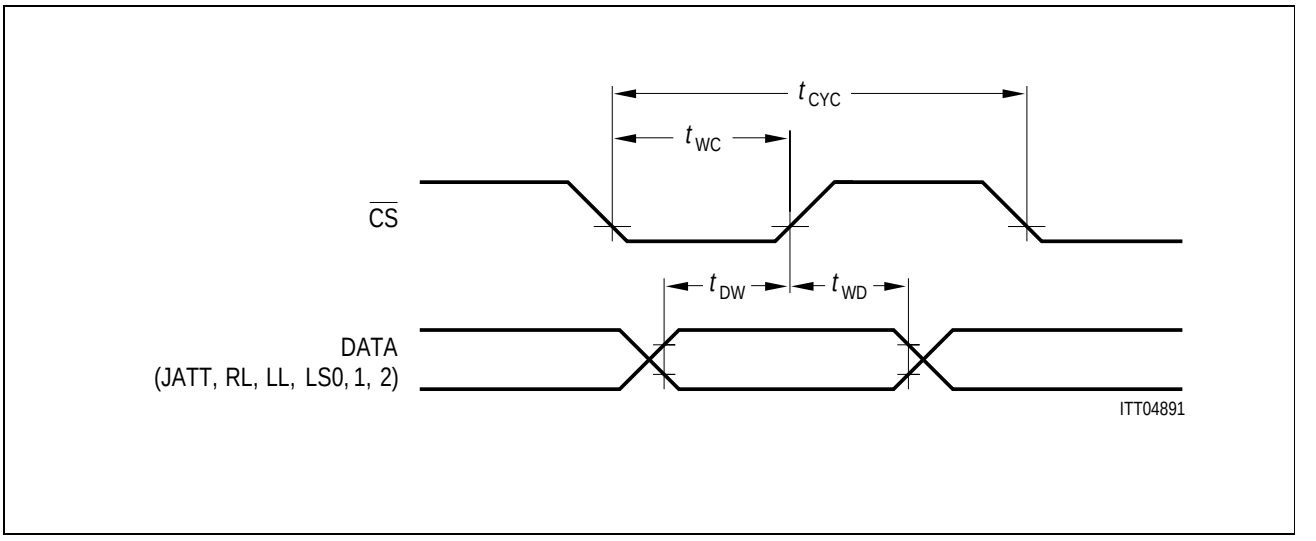


Figure 22
Timing of the Microprocessor Interface

Parameter	Symbol	Limit Values		Unit
		min.	max.	
$\overline{CS}$ pulse width	t_{WC}	60	–	ns
Data setup time to $\overline{CS}$	t_{DW}	35	–	ns
Data hold time from $\overline{CS}$	t_{WD}	10	–	ns
Cycle time	t_{CYC}	120		ns

4.6.4 XTAL Timing

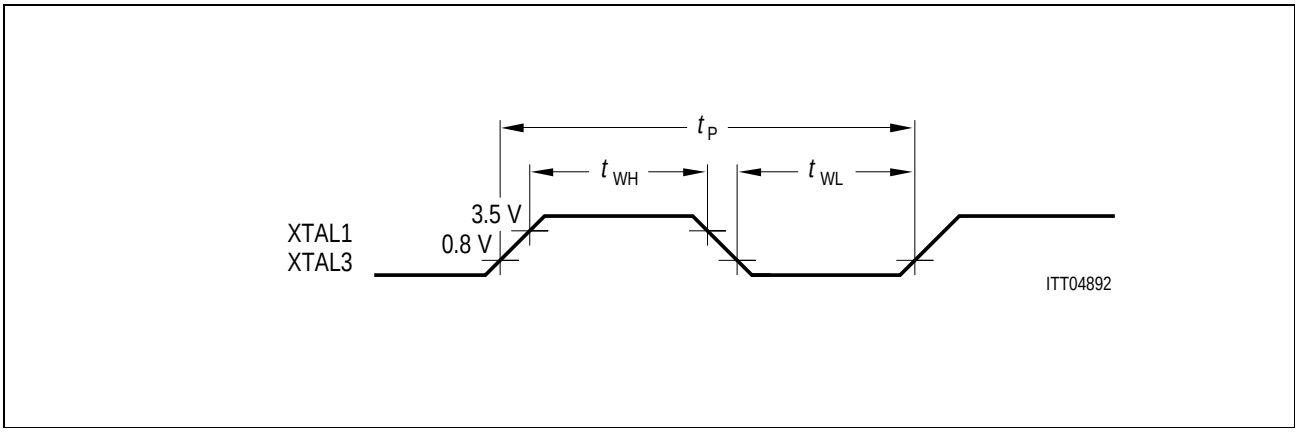


Figure 23
Timing of XTAL1/XTAL3

XTAL1/XTAL3 Timing Parameter Values

Parameter	Symbol	Limit Values			Unit	Condition
		min.	typ.	max.		
Clock period of crystal/ clock	t_P		61 81		ns	XTAL1 XTAL3
High phase crystal/clock	t_{WH}	20 30			ns	XTAL1 XTAL3
Low phase of crystal/clock	t_{WL}	20 30			ns	XTAL1 XTAL3

Note: If an external clock is used the PRACT works as a master. Please refer to Pin Definitions.

4.7 Pulse Templates - Transmitter

The PRACT meets both CCITT and T1 pulse template requirements.

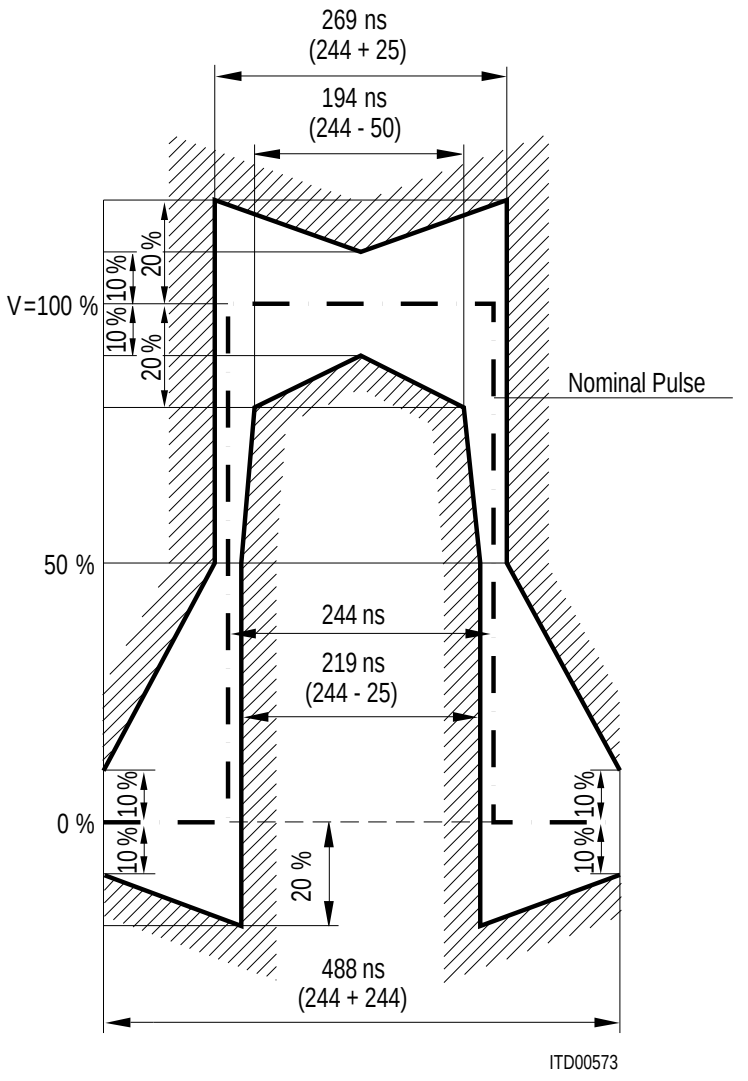


Figure 24
Pulse Template at the Transmitter Output for CEPT Applications

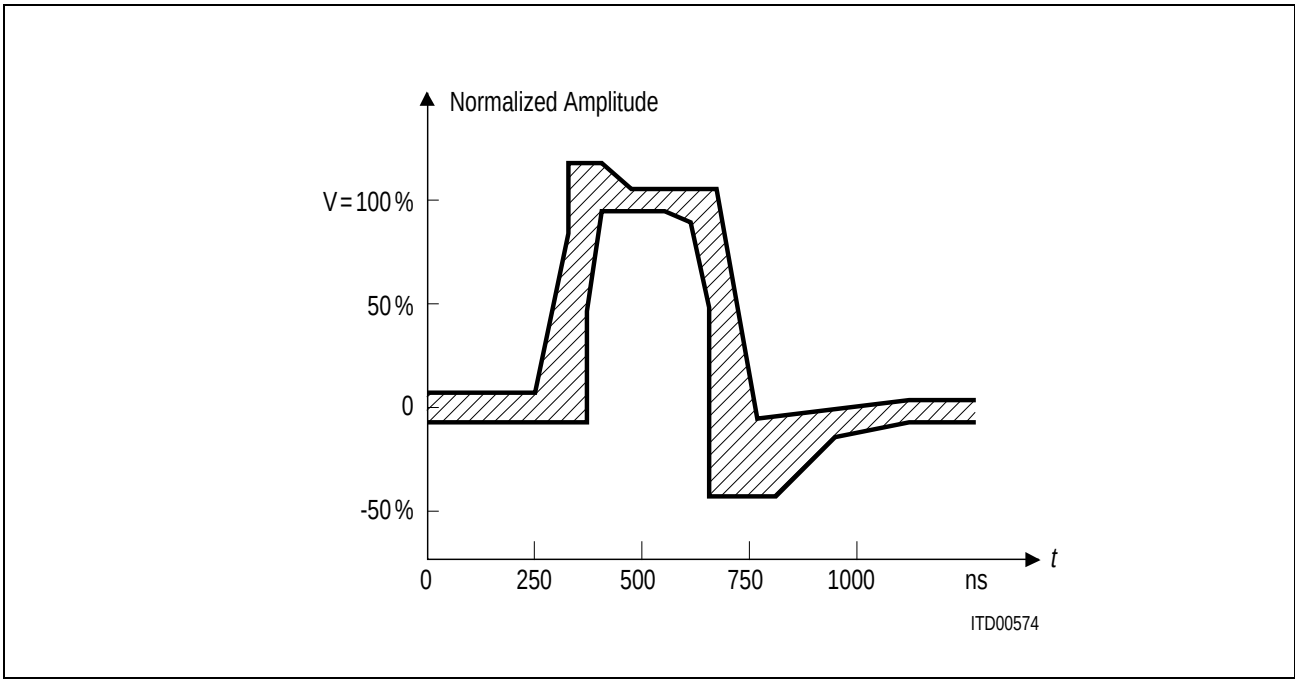


Figure 25
T1 Pulse Shape at the Cross Connect Point

Table 8
T1 Pulse Template Corner Points at the Cross Connect Point

Maximum Curve		Minimum Curve	
(0	0.05)	(0,	– 0.05
(250,	0.05)	(350,	– 0.05)
(325,	0.80)	(350,	– 0.50)
(325,	1.15)	(400,	0.95)
(425,	1.15)	(500,	0.95)
(500,	1.05)	(600,	0.90)
(675,	1.05)	(650,	0.50)
(725,	– 0.07)	(650,	– 0.45)
(1100,	0.05)	(800,	– 0.45)
(1250,	0.05)	(925,	– 0.20)
		(1100,	– 0.05)
		(1250,	– 0.05)

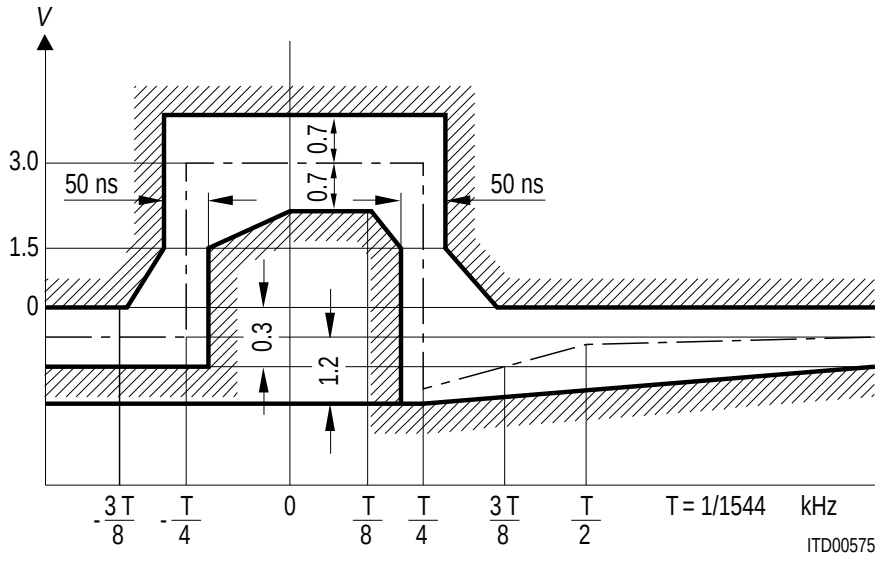


Figure 26
Pulse Shape According to CCITT G.703

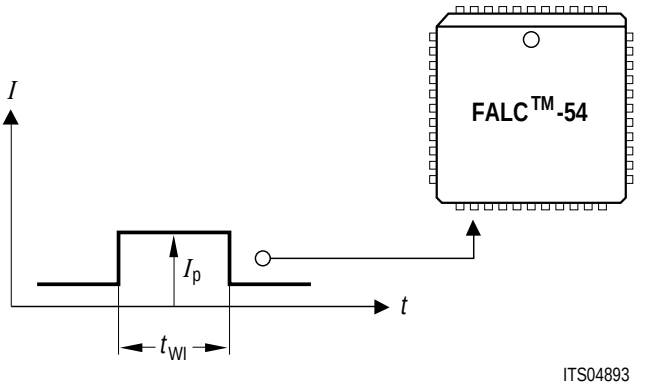
4.8 Overvoltage Tolerance

To prevent the PRACT from being damaged by overvoltage (i.e. from lightning), external devices like diodes or resistors have to be connected to one or both sides of the line interface transformers. Thus, overvoltage peaks are cut off. However, some residual overvoltage may remain.

The PRACT simplifies the task of designing external protection circuits. Its transmitter exhibits a low line impedance so that reasonable external resistors can be connected to the line outputs. **Figure 8** with the element values of **table 7** gives an example of how an overvoltage protection against residual overvoltages at the ternary interface can be accomplished. The solution shown also meets the stated return loss requirements.

A similar consideration applies to the receiver. The resistors R2 of **figure 3** provide protection against residual overvoltages by attenuating voltages of both polarities across RL1 and RL2.

The maximum input current allowed to reach the PRACT pins under overvoltage conditions is given as a function of the width of a rectangular input current pulse according to **figure 27**. **Figure 29** shows the curve of the maximum allowed input current across the pins RL1 and RL2, **figure 28** across the pins XL1 and XL2.



Condition: All other pins grounded

Figure 27
Measurement of Overvoltage Stress

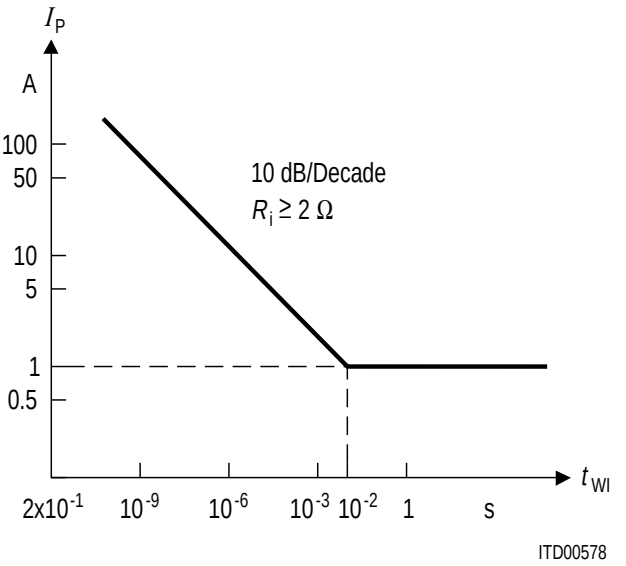


Figure 28
Tolerated Input Current at the XL1, XL2 Pins

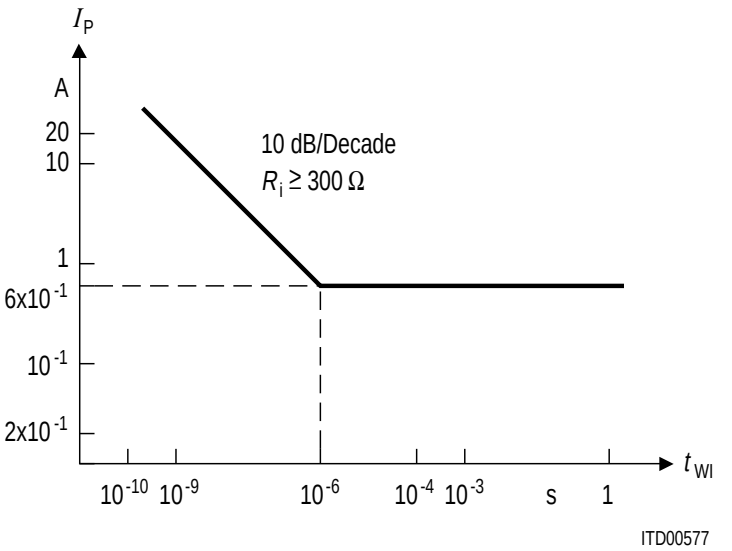
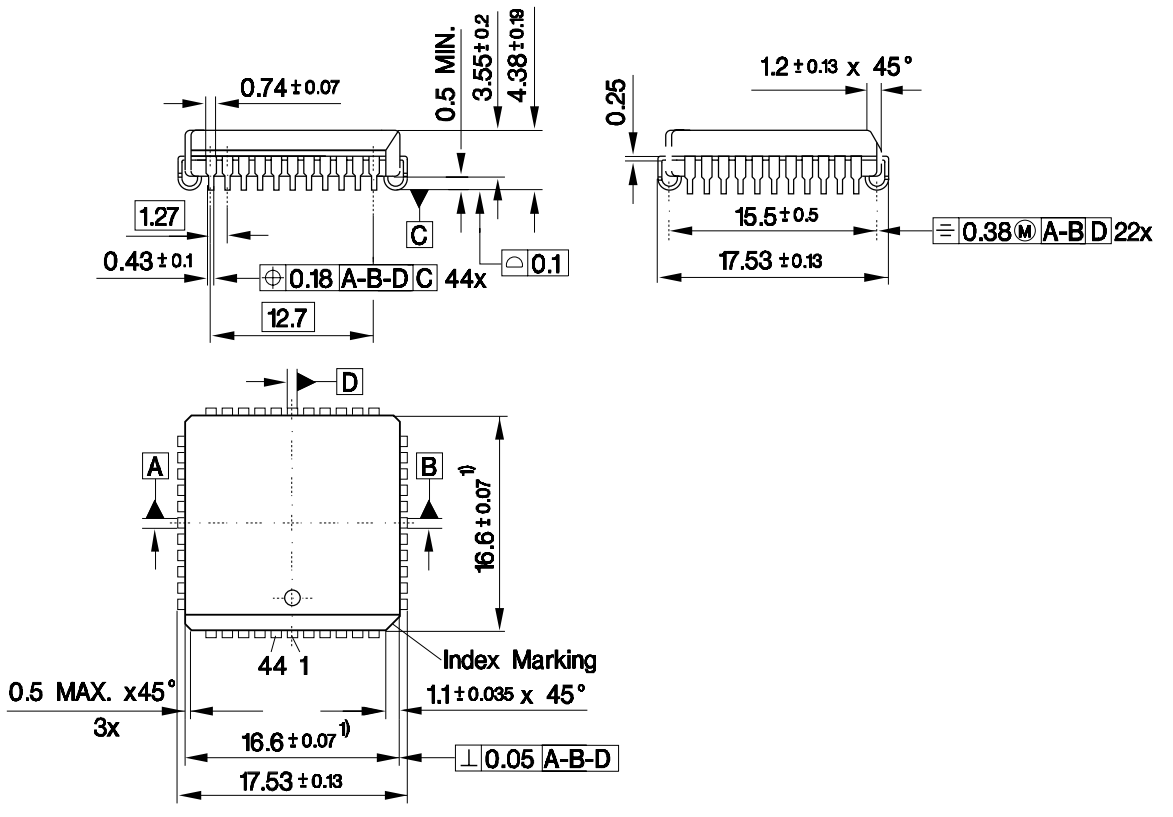


Figure 29
Tolerated Input Current at the RL1, RL2 Pins

5 Package Outlines

Plastic Package, P-LCC-44 (SMD)
(Plastic Leaded Chip Carrier)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm