

SIEMENS

ICs for Consumer Electronics

ADC with Built in Antialiasing filter and
Clock generation UnitS
ABACUS
SDA 9206

Data Sheet 1999-02-10

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| | | |
|----------------------------------|---------------------------------|--|
| SDA 9206 | | |
| Revision History: | | Current Version: 1999-02-10 |
| Previous Version: | | |
| Page (in previous Version) | Page (in current Version) | Subjects (major changes since last revision) |
| 21 | 21 | Update of Table 2 concerning Straight Binary |

Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Recommended Operating Conditions

Under this conditions the functions given in the circuit description are fulfilled. Nominal conditions specify mean values expected over the production spread and are the proposed values for interface and application. If not stated otherwise, nominal values will apply at $T_A=25^{\circ}\text{C}$ and the nominal supply voltage.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit.

Edition 1999-02-10

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ADC with Built in Antialiasing filter and Clock generation Units ABACUS

SDA 9206

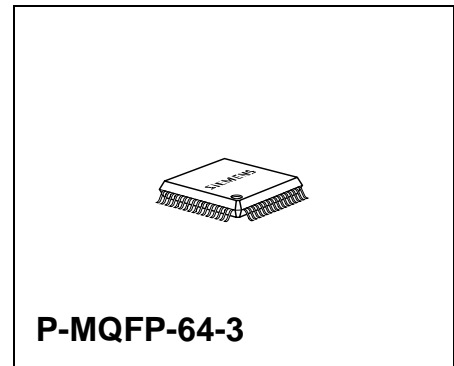
Preliminary Data

CMOS

1 Overview

1.1 Features

- Three equivalent CMOS A/D converters on chip
- 30 MHz sampling rate
- 8-Bit resolution
- No external sample & hold required
- Internal clamping circuits for each of the ADCs
- Internal amplification of input signals can be set by I²C Bus
- Internal pre-filtering of analog input signals
- High performance decimation filters
- Two data sampling modes (4:2:2 and 4:1:1)
- 3 output data interfaces
 - CCIR 656 interface (8 wires)
 - Parallel data interface (2 x 8 wires)
 - Quasi Parallel data interface (8 + 4 wires)
- Overflow and underflow I²C status bits
- On-chip sync and clock generation
- Separate SYNC input with clamping for sync and clock generation (max. line frequency of SYNC input: 38 kHz)
- positive and negative polarity of SYNC signal (switchable by I²C Bus)
- Lock-in behavior can be set via I²C Bus
- Frequency generator function possible with digitally adjustable frequency
- Clock generation for single and double line input frequencies supported (1fh / 2fh mode)
- Vertical noise suppression and 50/60 Hz detection (for 1fh mode only)



| Type | Ordering Code | Package |
|----------|-------------------|-------------|
| SDA 9206 | Q67101-H5185-A704 | P-MQFP-64-3 |

- I²C-Bus interface
- P-MQFP-64-3
- 5 V supply voltage for input signals
- 3.3 V or 5 V supply voltage for output signals

1.2 General Description

The SDA 9206 is a single monolithic IC containing three separate 8-Bit A/D converters for video (YUV) applications and a clock sync generator which is delivering the sample clock for the A/D converters. It utilizes an advanced VLSI 0.5 μm CMOS process providing 30 MHz sampling rates at 8-Bits.

The YUV processing consists of following functional blocks:

- Analog input buffers and clamping circuits
- Three 30 MHz A/D converters
- Digital decimation filters
- Delay compensation in Y-path
- Output formatter and buffer

The clock sync generator consists essentially of the following functional blocks:

- Analog clamping
- 7-Bit A/D converter
- Sync processor with digital horizontal PLL, vertical sync processor and pulse generator
- Clock generator with discrete timing oscillator, D/A converter, analog PLL and divider, as well as a crystal oscillator

1.4 Pin Description

| Pin No. | Symbol | Type | Description |
|---------|-------------|----------|--|
| 22, 36 | V_{SS} | S | Supply ground (V_{SS}) for digital parts |
| 21, 45 | V_{DD} | S | Supply voltage (V_{DD}) for digital parts |
| 23, 55 | V_{SSQ} | S | Supply ground for output stages and input stages |
| 32, 50 | V_{DDQ} | S | Supply voltage for output stages and input stages (3.3 V / 5 V) |
| 1 | V_{ADDY} | S | Analog positive supply voltage of ADC AINY (5 V) |
| 2 | V_{REFHY} | | Reference voltage high of ADC AINY (4.2 V) |
| 3 | AINY | I/ana | Analog voltage input of ADC AINY input range selectable via I ² C Bus (subaddress 11 _H , YAMP) |
| 4 | V_{REFLY} | | Reference voltage low of ADC AINY (2.2 V) |
| 5 | V_{AGNDY} | S | Analog ground of ADC AINY |
| 6 | V_{ADDU} | S | Analog positive supply voltage of ADC AINU (5 V) |
| 7 | V_{REFHU} | | Reference voltage high of ADC AINU (4.2 V) |
| 8 | AINU | I/ana | Analog voltage input of ADC AINU input range selectable via I ² C Bus (subaddress 12 _H , UAMP) |
| 9 | V_{REFLU} | | Reference voltage low of ADC AINU (2.2 V) |
| 10 | V_{AGNDU} | S | Analog ground of ADC AINU |
| 11 | V_{ADDV} | S | Analog positive supply voltage of ADC AINV (5 V) |
| 12 | V_{REFHV} | | Reference voltage high of ADC AINV (4.2 V) |
| 13 | AINV | I/ana | Analog voltage input of ADC AINV input range selectable via I ² C Bus (subaddress 12 _H , VAMP) |
| 14 | V_{REFLV} | | Reference voltage low of ADC AINV (2.2 V) |
| 15 | V_{AGNDV} | S | Analog ground of ADC AINV |
| 16 | RESIN | I/TTL/pu | Reset input signal: active low |
| 17 | H111 | Q/TTL | Pin function defined by I ² C Bus: Line frequent pulse output or programmable digital control output |
| 18 | RESOUTN | Q/TTL | Reset output signal: active low; reset for other ICs |
| 19 | BLN | Q/TTL | Blanking signal output, high level indicates active video line |

1.4 Pin Description (cont'd)

| Pin No. | Symbol | Type | Description |
|-----------|---------------------|----------|---|
| 20 | H2I2 | Q/TTL | Pin function defined by I ² C Bus: Line frequent pulse output or programmable digital control output |
| 24 ... 31 | PAQ7 ... 0 | Q/TTL | Data output Port A (see Data Format) |
| 33 | SDA | IQ | I ² C-Bus data line |
| 34 | SCL | I | I ² C-Bus clock line |
| 35 | ADR0 | I/TTL/pd | I ² C-Chip select |
| 37 ... 44 | PBQ7... 0 | Q/TTL | Data output port B (see Data Format) |
| 46 | V _{DDDTO} | S | Positive supply voltage of DTO (5 V) |
| 47 | X2 | Q/ana | Crystal connection |
| 48 | X1 | I/ana | Crystal connection (clock input) |
| 49 | V _{SSDTO} | S | Ground of DTO |
| 51 | VS | Q/TTL | Vertical sync pulse output |
| 52 | CLK2 | Q/TTL | Clock out: tristate / 6.75 / 13.5 / 27 MHz; selectable via I ² C |
| 53 | CLK1 | Q/TTL | Clock out: tristate / 6.75 / 13.5 / 27 MHz; selectable via I ² C |
| 54 | HS | Q/TTL | Horizontal sync pulse output |
| 56 | TEST | I/TTL/pd | Input signal for test mode selection (0 V: no test mode selected) Leave unconnected or connect to V _{SS} |
| 57 | EXSYN | I/TTL/pd | Input signal for test mode selection (0 V: no test mode selected) Leave unconnected or connect to V _{SS} |
| 58 | V _{AGNDPA} | | Analog ground of analog PLL and DACs |
| 59 | V _{ADDPA} | | Analog positive supply voltage of analog PLL and DACs (5 V) |
| 60 | V _{AGNDC} | | Analog ground of ADC SYNC |
| 61 | V _{REFLC} | | Reference voltage low of ADC SYNC (2.2 V) |
| 62 | SYNC | I/ana | SYNC input Input range selectable via I ² C Bus (subaddress 11 _H , SYNAMP) |

1.4 Pin Description (cont'd)

| Pin No. | Symbol | Type | Description |
|---------|-------------|------|--|
| 63 | V_{REFHC} | | Reference voltage high of ADC SYNC (4.2 V) |
| 64 | V_{ADDC} | | Analog positive supply voltage of ADC SYNC (5 V) |

S: supply, I: input, Q: output, TTL: digital (TTL)
 ana: analog, pu: internal pullup-circuit, pd: internal pulldown-circuit

1.5 Internal Pin Configuration

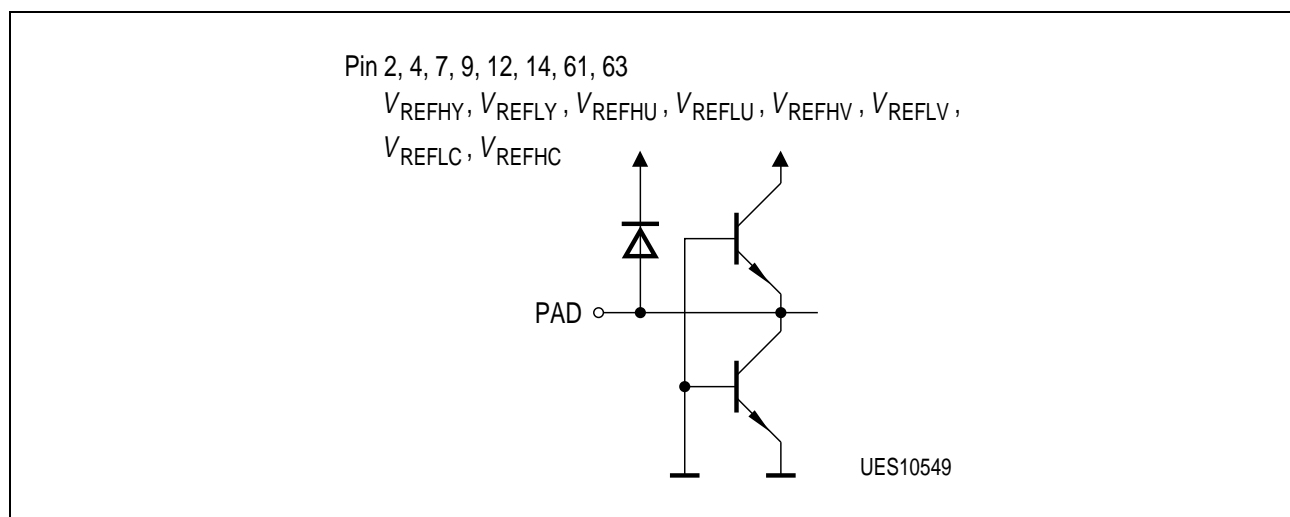


Figure 2

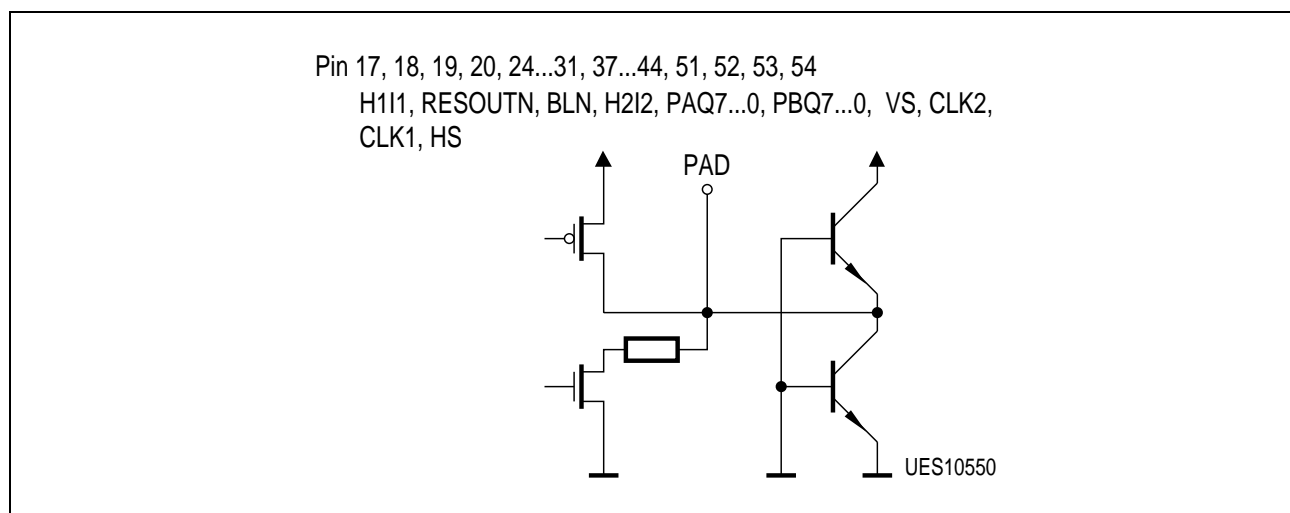


Figure 3

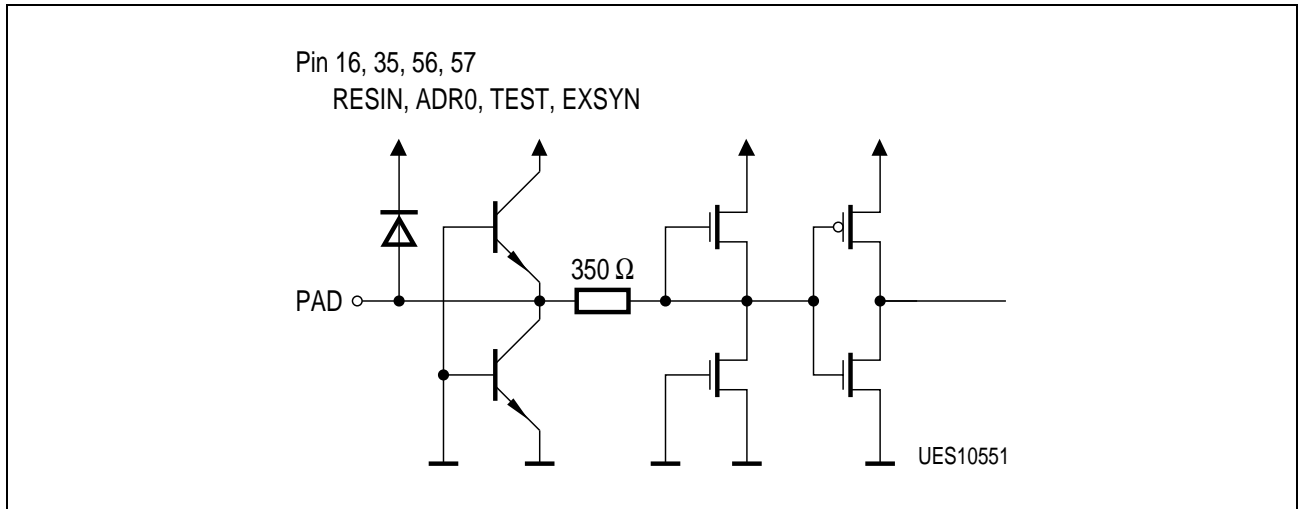


Figure 4

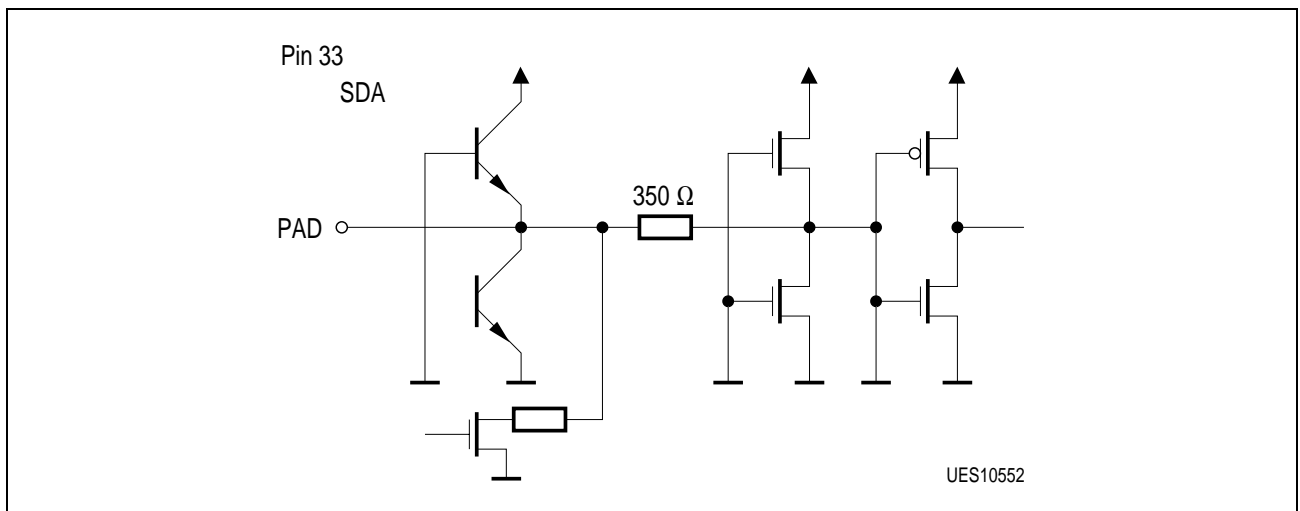


Figure 5

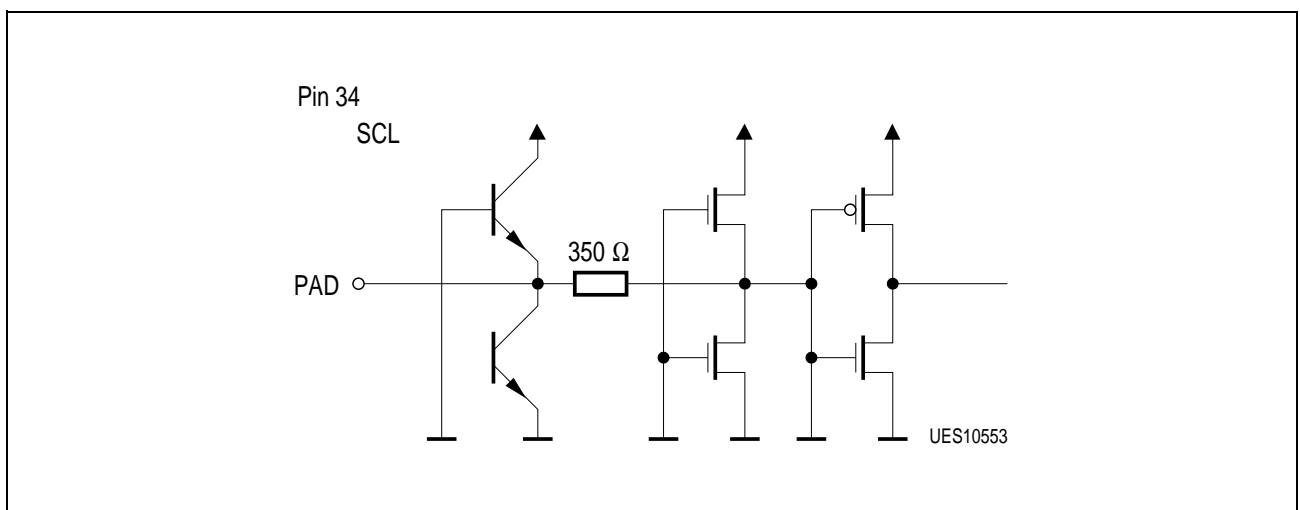


Figure 6

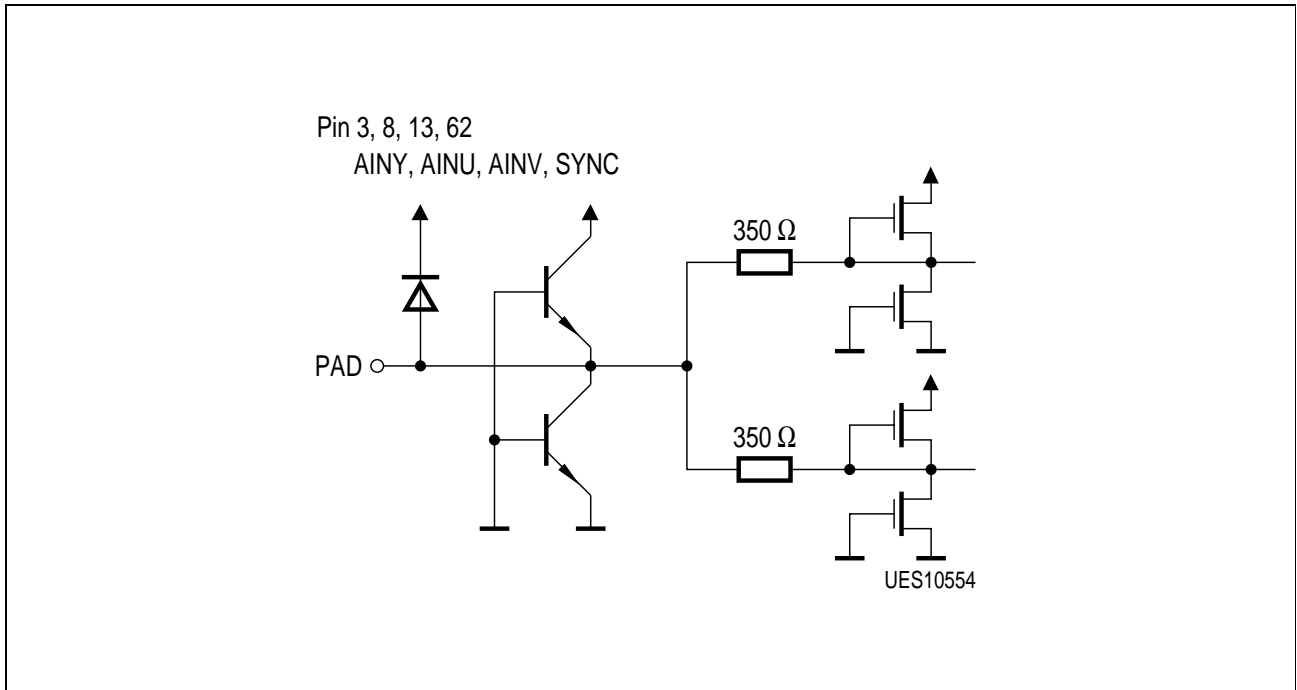


Figure 7

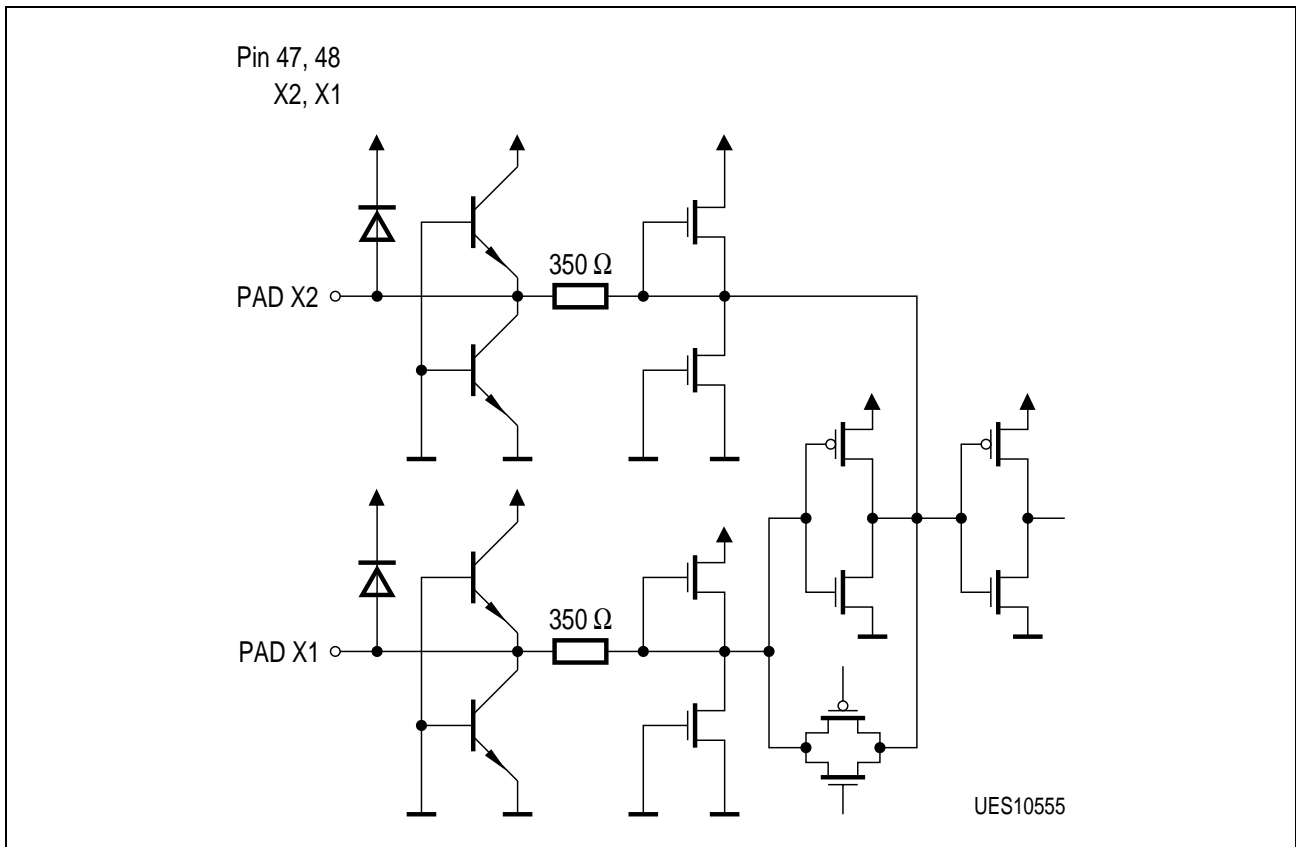


Figure 8

1.6 Block Diagram

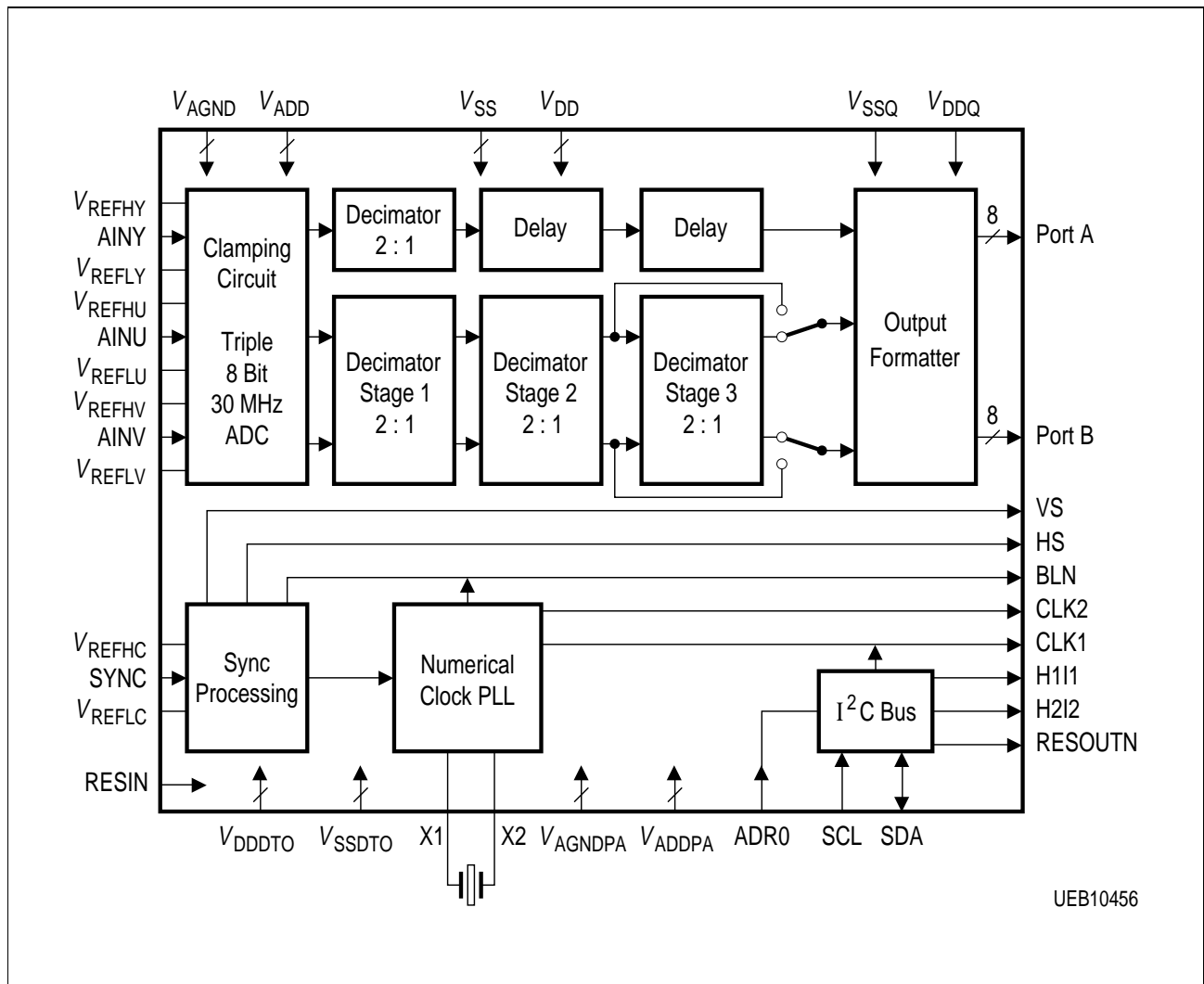


Figure 9

2 System Description

2.1 A/D Converter for YUV Inputs

2.1.1 Introduction

The SDA 9206 implements 3 independent 8-Bit A/D converters. Maximum conversion rate is 30 MHz.

2.1.2 Input Signal Amplification, Prefiltering

The amplification of the input signals can be adjusted via I²C Bus. An internal prefiltering of the analog input signals is implemented. The typ. frequency response of the analog antialiasing prefilter is shown in **figure 10**.

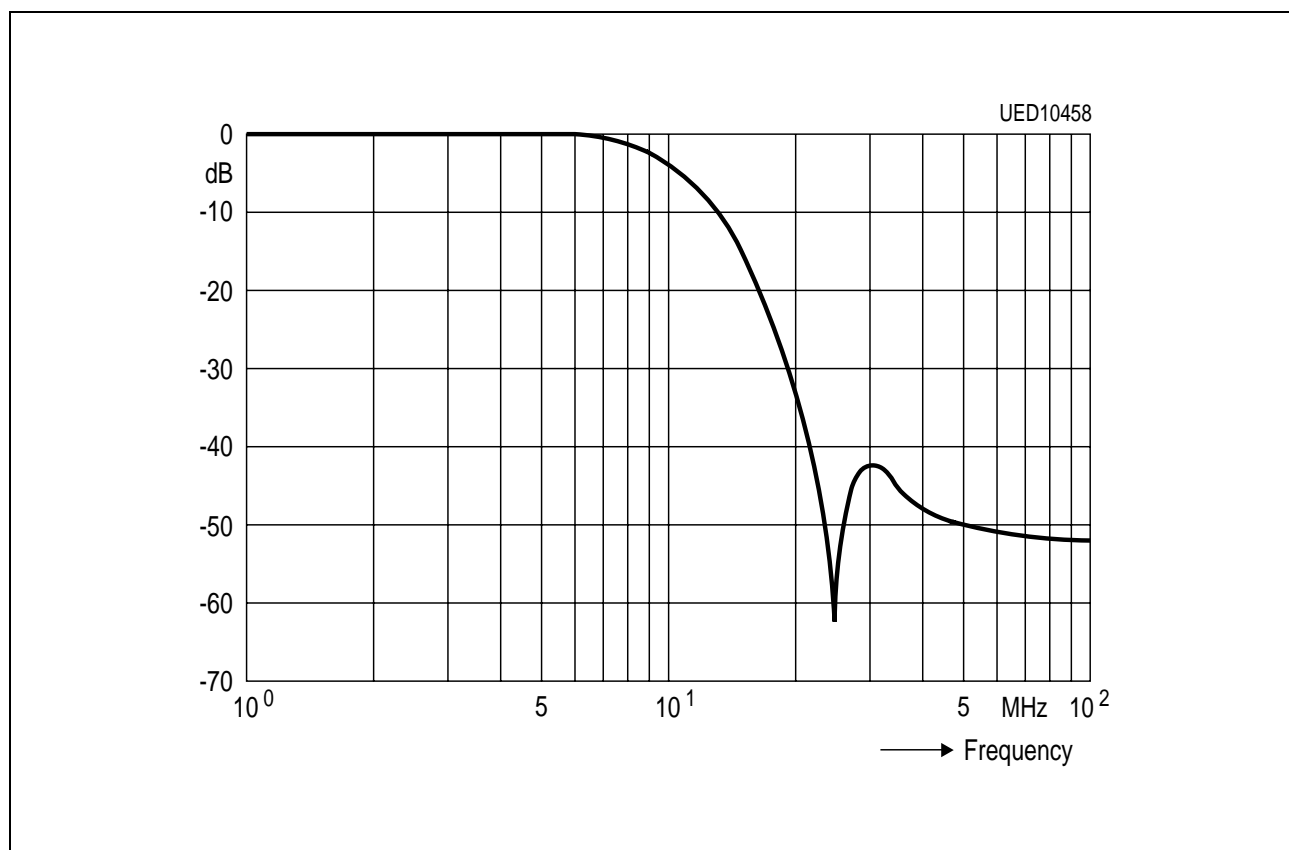


Figure 10
Frequency Response of the Analog Antialiasing Prefilter

2.1.3 Clamping

The analog pins AINY, AINU, AINV are switched simultaneously to on chip generated clamping levels by an on chip clamping pulse H2.

| Analog Channel | Straight Binary Code | Two's Complement Code | Components |
|----------------|----------------------|-----------------------|------------|
| AINY | 0001 0000 | 1001 0000 | Y |
| AINU, AINV | 1000 0000 | 0000 0000 | U, V |

The external clamping capacitance is loaded by on chip current sources during clamping. So loading time depends on the values of $C_{ext\ cl}$.

2.1.4 Digital Decimation Filters for YUV

The data rates of digital YUV signals are reduced in decimation filters following the A/D conversion. The overall performance of the decimation filters is tuned to the requirements for TV signals.

In **figure 11** the frequency response of the filter for the Y channel is shown. The input sampling rate is 27 MHz, the output sampling rate is 13.5 MHz.

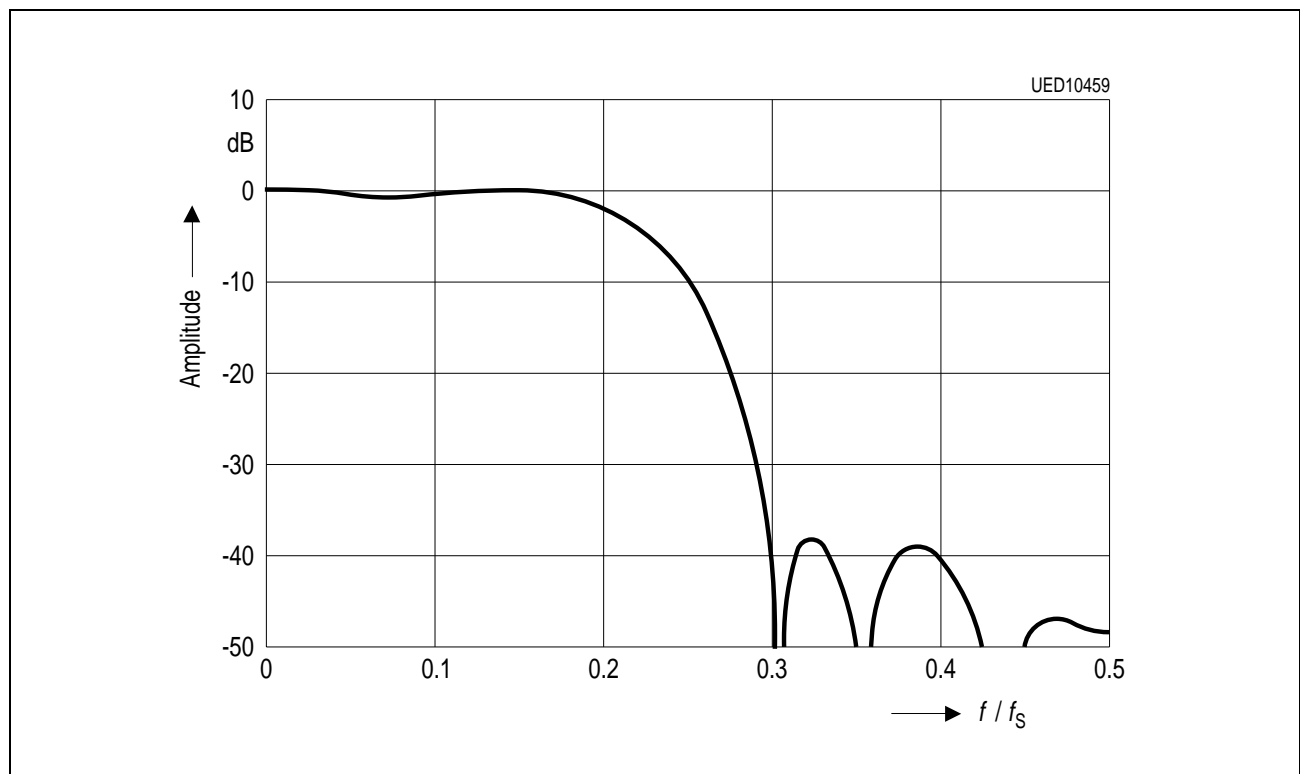


Figure 11
Magnitude Frequency Response of the Luminance Filter
The Input Sampling Frequency f_s is 27 MHz

The total frequency response of the decimator stages 1 and 2 of the UV channels for an input sampling rate of 27 MHz and an output sampling rate of 6.75 MHz is shown in figure 12.

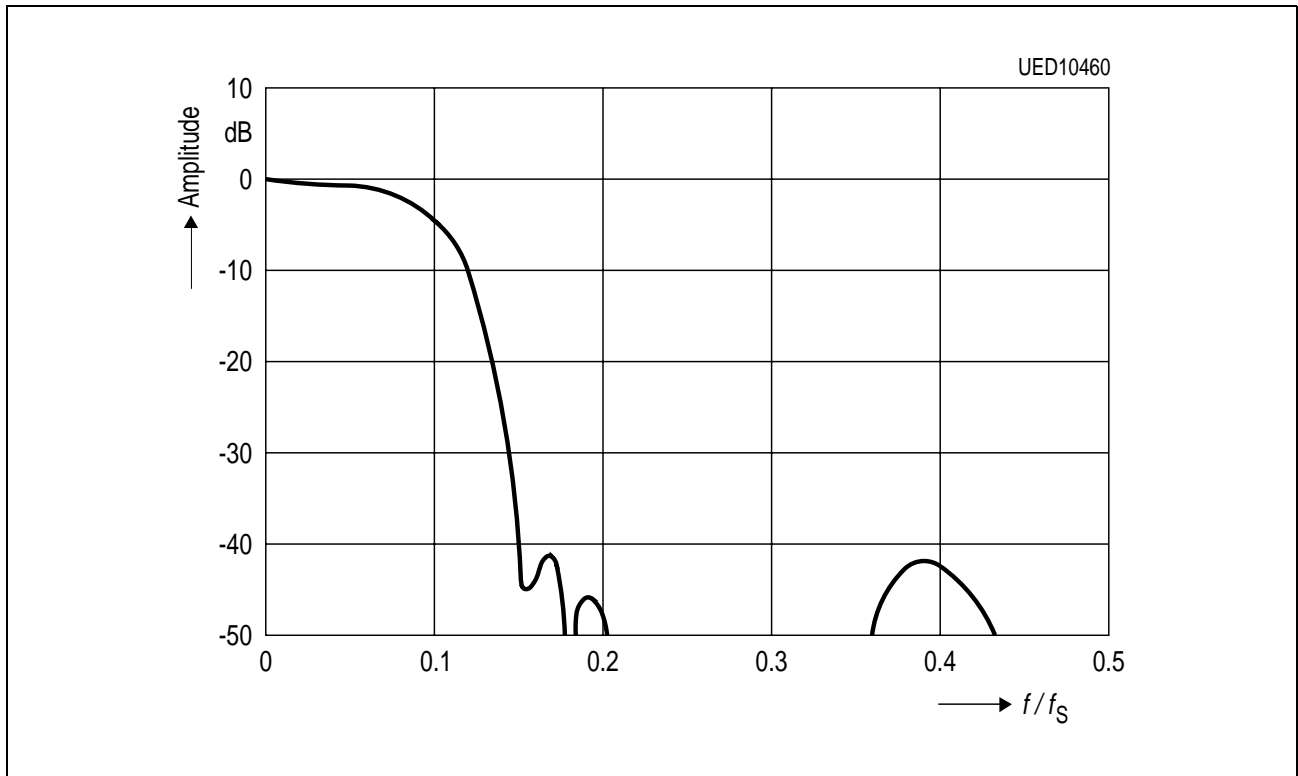


Figure 12
Magnitude Frequency Response for Chroma Signals (Decimator Stages 1 and 2)
The Input Sampling Frequency f_s is 27 MHz

The frequency response of the decimator filter stage 3 of the UV channels for an input sampling rate of 6.75 MHz and an output sampling rate of 3.375 MHz is shown in **figure 13**. The decimator stage 3 is active for 4:1:1 mode and can also be activated for 4:2:2 mode by I²C Bus (control bit UV3FIL).

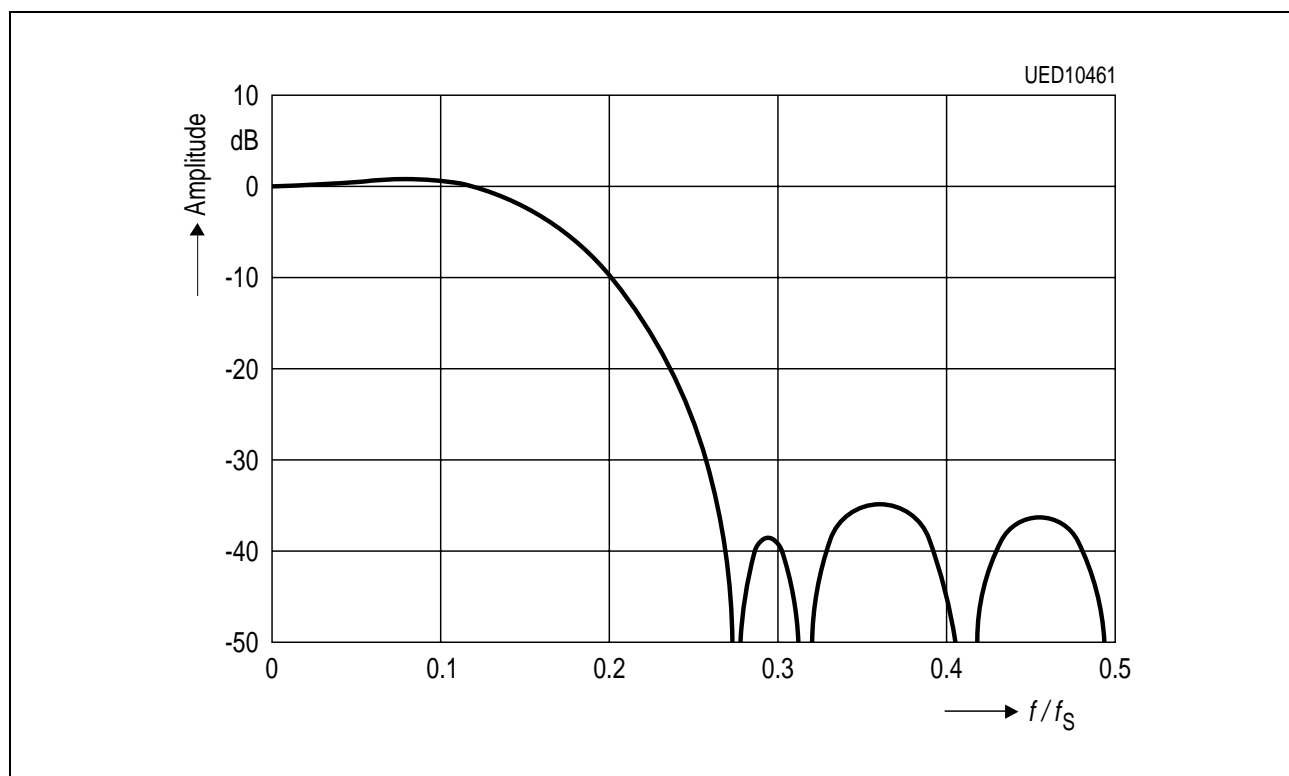


Figure 13
Frequency Response of the Chroma Decimator Stage 3
The Input Sampling Frequency f_s is 6.75 MHz

2.2 Data Output Formatter

Three output data formats can be selected via I²C Bus (control Bits FORMAT). One format corresponds to CCIR 656 (8-Bit bus at a data rate of 27 MHz), an other format makes available Y and UV data separately on 2 parallel 8-Bit buses for Y and UV at a data rate of 13.5 MHz each. The third format is a 12-Bit bus with 8 connections for Y and 4 connections for multiplexed UV data.

| Output Pin | Quasiparallel Data FORMAT = 10 or 11 (13.5 MHz) | | | | Parallel Data FORMAT = 01 (13.5 MHz) | | CCIR 656 FORMAT = 00 (27 MHz) | | | |
|------------|---|-----------------|-----------------|-----------------|--|-----------------|-------------------------------------|-----------------|-----------------|-----------------|
| | Y ₀₇ | Y ₁₇ | Y ₂₇ | Y ₃₇ | Y ₀₇ | Y ₁₇ | U ₀₇ | Y ₀₇ | V ₀₇ | Y ₁₇ |
| PAQ7 | Y ₀₇ | Y ₁₇ | Y ₂₇ | Y ₃₇ | Y ₀₇ | Y ₁₇ | U ₀₇ | Y ₀₇ | V ₀₇ | Y ₁₇ |
| PAQ6 | Y ₀₆ | Y ₁₆ | Y ₂₆ | Y ₃₆ | Y ₀₆ | Y ₁₆ | U ₀₆ | Y ₀₆ | V ₀₆ | Y ₁₆ |
| PAQ5 | Y ₀₅ | Y ₁₅ | Y ₂₅ | Y ₃₅ | Y ₀₅ | Y ₁₅ | U ₀₅ | Y ₀₅ | V ₀₅ | Y ₁₅ |
| PAQ4 | Y ₀₄ | Y ₁₄ | Y ₂₄ | Y ₃₄ | Y ₀₄ | Y ₁₄ | U ₀₄ | Y ₀₄ | V ₀₄ | Y ₁₄ |
| PAQ3 | Y ₀₃ | Y ₁₃ | Y ₂₃ | Y ₃₃ | Y ₀₃ | Y ₁₃ | U ₀₃ | Y ₀₃ | V ₀₃ | Y ₁₃ |
| PAQ2 | Y ₀₂ | Y ₁₂ | Y ₂₂ | Y ₃₂ | Y ₀₂ | Y ₁₂ | U ₀₂ | Y ₀₂ | V ₀₂ | Y ₁₂ |
| PAQ1 | Y ₀₁ | Y ₁₁ | Y ₂₁ | Y ₃₁ | Y ₀₁ | Y ₁₁ | U ₀₁ | Y ₀₁ | V ₀₁ | Y ₁₁ |
| PAQ0 | Y ₀₀ | Y ₁₀ | Y ₂₀ | Y ₃₀ | Y ₀₀ | Y ₁₀ | U ₀₀ | Y ₀₀ | V ₀₀ | Y ₁₀ |
| PBQ7 | U ₀₇ | U ₀₅ | U ₀₃ | U ₀₁ | U ₀₇ | V ₀₇ | Z | Z | Z | Z |
| PBQ6 | U ₀₆ | U ₀₄ | U ₀₂ | U ₀₀ | U ₀₆ | V ₀₆ | Z | Z | Z | Z |
| PBQ5 | V ₀₇ | V ₀₅ | V ₀₃ | V ₀₁ | U ₀₅ | V ₀₅ | Z | Z | Z | Z |
| PBQ4 | V ₀₆ | V ₀₄ | V ₀₂ | V ₀₀ | U ₀₄ | V ₀₄ | Z | Z | Z | Z |
| PBQ3 | Z | Z | Z | Z | U ₀₃ | V ₀₃ | Z | Z | Z | Z |
| PBQ2 | Z | Z | Z | Z | U ₀₂ | V ₀₂ | Z | Z | Z | Z |
| PBQ1 | Z | Z | Z | Z | U ₀₁ | V ₀₁ | Z | Z | Z | Z |
| PBQ0 | Z | Z | Z | Z | U ₀₀ | V ₀₀ | Z | Z | Z | Z |

X_{AB}: X: signal component A: sample number B: bit number
 Z: Pin is in tristate mode.

The BLN signal marks the active part of the video line (see figure 14).

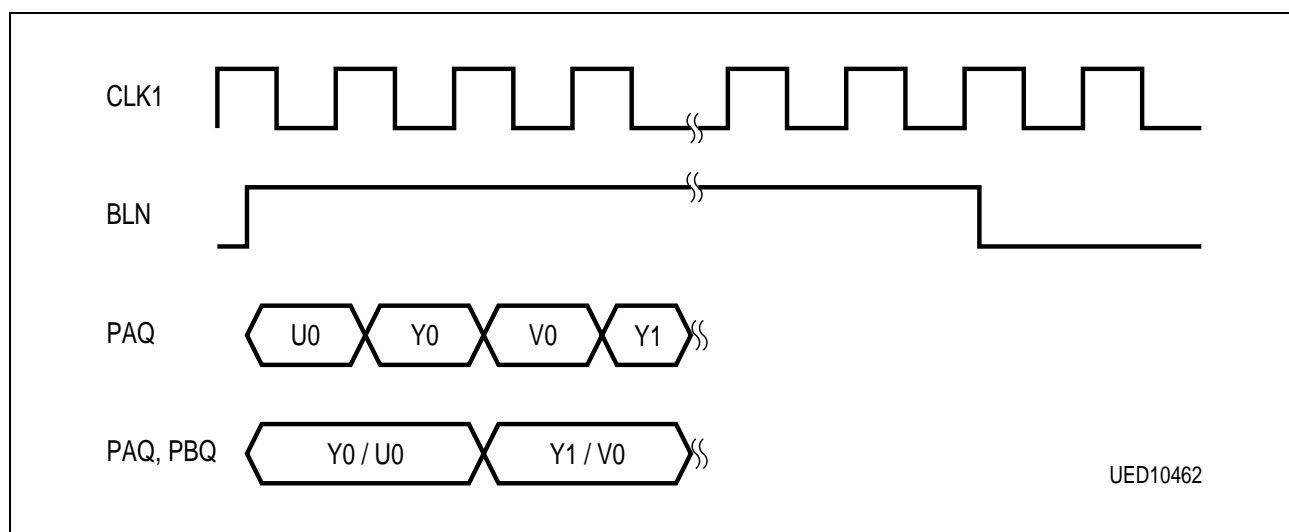


Figure 14

2.2.1 Output Coding for Straight Binary / Two's Complement Mode

Straight binary or Two's complement output coding is selectable for each separate signal component (Y and UV) via I²C-Bus control bits YCODE and UVCODE.

For straight binary coding a special suppression of code 0 and code 255 is provided in output format mode according CCIR 656.

**Table 1
Output Coding**

| Step | AINY | AINU, AINV | OFL Bit | UFL Bit | Straight Binary | | Two's Complement | |
|-----------|----------------------|-----------------------|---------|---------|-----------------|------|------------------|------|
| | | | | | 7654 | 3210 | 7654 | 3210 |
| Underflow | $< V_{CY} - 0.125 V$ | $< V_{CU, v} - 1.0 V$ | 0 | 1 | 0000 | 0000 | 1000 | 0000 |
| 0 | $V_{CY} - 0.125 V$ | $V_{CU, v} - 1.0 V$ | 0 | 0 | 0000 | 0000 | 1000 | 0000 |
| 1 | $V_{CY} - 0.117 V$ | $V_{CU, v} - 0.992 V$ | 0 | 0 | 0000 | 0001 | 1000 | 0001 |
| 2 | $V_{CY} - 0.109 V$ | $V_{CU, v} - 0.984 V$ | 0 | 0 | 0000 | 0010 | 1000 | 0010 |
| • | • | • | • | • | • | | • | |
| • | • | • | • | • | • | | • | |
| 253 | $V_{CY} + 1.859 V$ | $V_{CU, v} + 0.984 V$ | 0 | 0 | 1111 | 1101 | 0111 | 1101 |
| 254 | $V_{CY} + 1.867 V$ | $V_{CU, v} + 0.992 V$ | 0 | 0 | 1111 | 1110 | 0111 | 1110 |
| 255 | $V_{CY} + 1.875 V$ | $V_{CU, v} + 1.0 V$ | 0 | 0 | 1111 | 1111 | 0111 | 1111 |
| Overflow | $> V_{CY} + 1.875 V$ | $> V_{CU, v} + 1.0 V$ | 1 | 0 | 1111 | 1111 | 0111 | 1111 |

V_{CY} , $V_{CU, v}$: ext. clamping level during clamping at $C_{ext cl}$ on channel AINY resp. AINU, AINV

Table 1 is valid for $V_{REFL} = 2.2 V$ and $V_{REFH} = 4.2 V$, xAMP = 0000

Table 2
Output Coding in Case of CCIR 656 Format, FORMAT = 00

| Step | AINY | AINU, AINV | OFL Bit | UFL Bit | Straight Binary 7654 3210 | Two's Complement 7654 3210 |
|-----------|------------------------------|------------------------------|---------|---------|------------------------------|-------------------------------|
| Underflow | $< V_{CY} - 0.125 \text{ V}$ | $< V_{CU,V} - 1.0 \text{ V}$ | 0 | 1 | 0000 0001 | 1000 0000 |
| 0 | $V_{CY} - 0.125 \text{ V}$ | $V_{CU,V} - 1.0 \text{ V}$ | 0 | 0 | 0000 0001 | 1000 0000 |
| 1 | $V_{CY} - 0.117 \text{ V}$ | $V_{CU,V} - 0.992 \text{ V}$ | 0 | 0 | 0000 0001 | 1000 0001 |
| 2 | $V_{CY} - 0.109 \text{ V}$ | $V_{CU,V} - 0.984 \text{ V}$ | 0 | 0 | 0000 0010 | 1000 0010 |
| • | • | • | • | • | • | • |
| • | • | • | • | • | • | • |
| 253 | $V_{CY} + 1.859 \text{ V}$ | $V_{CU,V} + 0.984 \text{ V}$ | 0 | 0 | 1111 1101 | 0111 1101 |
| 254 | $V_{CY} + 1.867 \text{ V}$ | $V_{CU,V} + 0.992 \text{ V}$ | 0 | 0 | 1111 1110 | 0111 1110 |
| 255 | $V_{CY} + 1.875 \text{ V}$ | $V_{CU,V} + 1.0 \text{ V}$ | 0 | 0 | 1111 1110 | 0111 1111 |
| Overflow | $> V_{CY} + 1.875 \text{ V}$ | $> V_{CU,V} + 1.0 \text{ V}$ | 1 | 0 | 1111 1110 | 0111 1111 |

V_{CY} , $V_{CU,V}$: ext. clamping level during clamping at $C_{ext\ cl}$ on channel AINY
 resp. AINU, AINV

Table 2 is valid for $V_{REFL} = 2.2 \text{ V}$ and $V_{REFH} = 4.2 \text{ V}$, xAMP = 0000

2.3 Clock Sync Generation

The clock sync generator is a phase locked loop that locks on a horizontal SYNC input signal and generates the clock signals as well as additional control output signals.

2.3.1 Horizontal PLL (HPLL)

The input signal SYNC may be either a CVBS signal or a composite sync signal. The polarity of the SYNC signal can be both positive or negative (I²C-Bit SYPOL). The edges of the SYNC input pulses should not be steeper than 100 ns. The frequency of the SYNC signal can be of normal or double line frequency (I²C-Bit 2FH).

The SYNC is clamped before A/D conversion. For DC-input signals clamping can be disabled (I²C-Bit CLOF). A/D conversion takes place with 7 bits and a nominal frequency of 27 MHz.

The digital HPLL filters the signal with a cutoff frequency of 1 MHz (2 MHz for 2fh mode). If 1fh mode is used the sampling frequency is decimated to 13.5 MHz. Following the low pass filtering a black- and sync bottom- level measurement takes place in order to calculate a threshold value. By means of this value the phase difference between the HPLL output and the SYNC input pulse is determined. Using a digital PI filter an increment is calculated from this for the Discrete Timing Oscillator (DTO). It is possible

to adapt the nominal frequency of the DTO by means of 5 I²C-Bus bits (INC4...INC0) such shifting the center frequency according to the momentary standard used.

For the different applications the following values of INC are allowed (values valid for a crystal frequency of 24.576 MHz):

| Application | FH [Hz] | 2FH | YUV-ADCs | INC |
|-------------------|---------|-----|----------|-----|
| PAL | 15625 | 0 | active | 6 |
| NTSC | 15750 | 0 | active | 6 |
| PAL (100 Hz/VGA) | 31250 | 1 | inactive | 6 |
| NTSC (120 Hz/VGA) | 31500 | 1 | inactive | 6 |
| ATV | 32400 | 1 | inactive | 8 |
| MUSE | 33750 | 1 | inactive | 11 |
| Macintosh | 35000 | 1 | inactive | 14 |
| VGA | 38000 | 1 | inactive | 21 |

Note: A change of INC causes spontaneous changes of the generated clock frequencies!

The DTO generates a saw-tooth with a frequency that is proportional to the increment. The saw-tooth is converted into a sinusoidal clock signal by means of a D/A converter and applied to an analog PLL which multiplies the frequency and minimizes residual jitter.

By means of the I²C bits S1CL and S2CL the output frequency on pins CLK1 and CLK2 can be set. In this manner a clock is provided that is line-locked with the SYNC-input signal. The ratio of these clock frequencies to the horizontal frequency of SYNC depends only on the I²C-Bus bits S1CL, S2CL, HPLL and 2FH.

For the different modes the following values of S1CL and S2CL are allowed:

| Mode | YUV-ADC | 2FH | S1CL | S2CL | f_{CLK1} (MHz) | f_{CLK2} (MHz) |
|--------------|----------|-----|------|------|---------------------|---------------------|
| CCIR | enabled | 0 | 11 | 11 | 27 | 27 |
| CCIR | enabled | 0 | 11 | 00 | 27 | tristate |
| 4:2:2, 4:1:1 | enabled | 0 | 11 | 11 | 27 | 27 |
| 4:2:2, 4:1:1 | enabled | 0 | 10 | 00 | 13.5 | tristate |
| VGA | disabled | 1 | 01 | 11 | 6.25 ... 8.75 | 25 ... 35 |
| VGA | disabled | 1 | 10 | 11 | 12.5 ... 17.5 | 25 ... 35 |

The digital horizontal PLL supplies a noise-suppressed horizontal pulse.

During 1fh mode (2FH = 0) the digital HPLL also supplies a noise-suppressed vertical pulse obtained by digital integration of the main equalizing pulses. An integration time of 26.6 μs or 11.3 μs can be set by the I²C Bus. This functionality is switched off during 2fh mode (2FH = 1).

2.3.2 Vertical Sync Processing (only available for 1fh mode)

Vertical sync processing consists of:

- 625/525 line detection
- vertical noise suppression

The vertical pulses are obtained from the SYNC signal by integration. The 625/525 line detector measures the number of lines per field. By taking the average of the individual measurements with two up/down counters, the status bits 'FF' and 'FFGF' are obtained.

When vertical noise suppression is switched on (VOFF = 0), the vertical pulse obtained from the SYNC signal by integration is admitted only within a preset window (refer to timing diagram) and appears as a VS pulse. The width of the window can be set via the I²C Bus.

In the temporary absence of vertical pulses in SYNC, a continuous VS can be generated by switching on a 'flywheel mode' (SCHW = 1) providing a number of lines per field of 312.5 or 262.5 respectively.

When interference to SYNC is heavy, missing vertical pulses can be supplemented by switching on the flywheel mode and vertical interference can be eliminated by switching on the noise suppression circuitry. Noise suppression and the flywheel mode can be enabled independently of each other.

There is also the possibility of generating VS in the free-running mode. The VS pulses are then completely independent of the vertical sync pulse in SYNC. When FREE = 1 and SCHW = 1, a VS pulse is generated every 262.5 or 312.5 lines (VF = 1 or 0 respectively). When FREE = 1 and SCHW = 0, a VS pulse is generated every 279 or 339 lines (VF = 1 or 0 respectively). Free-running generation of VS occurs every 262 or 312 in the terminal mode (TERM = 1).

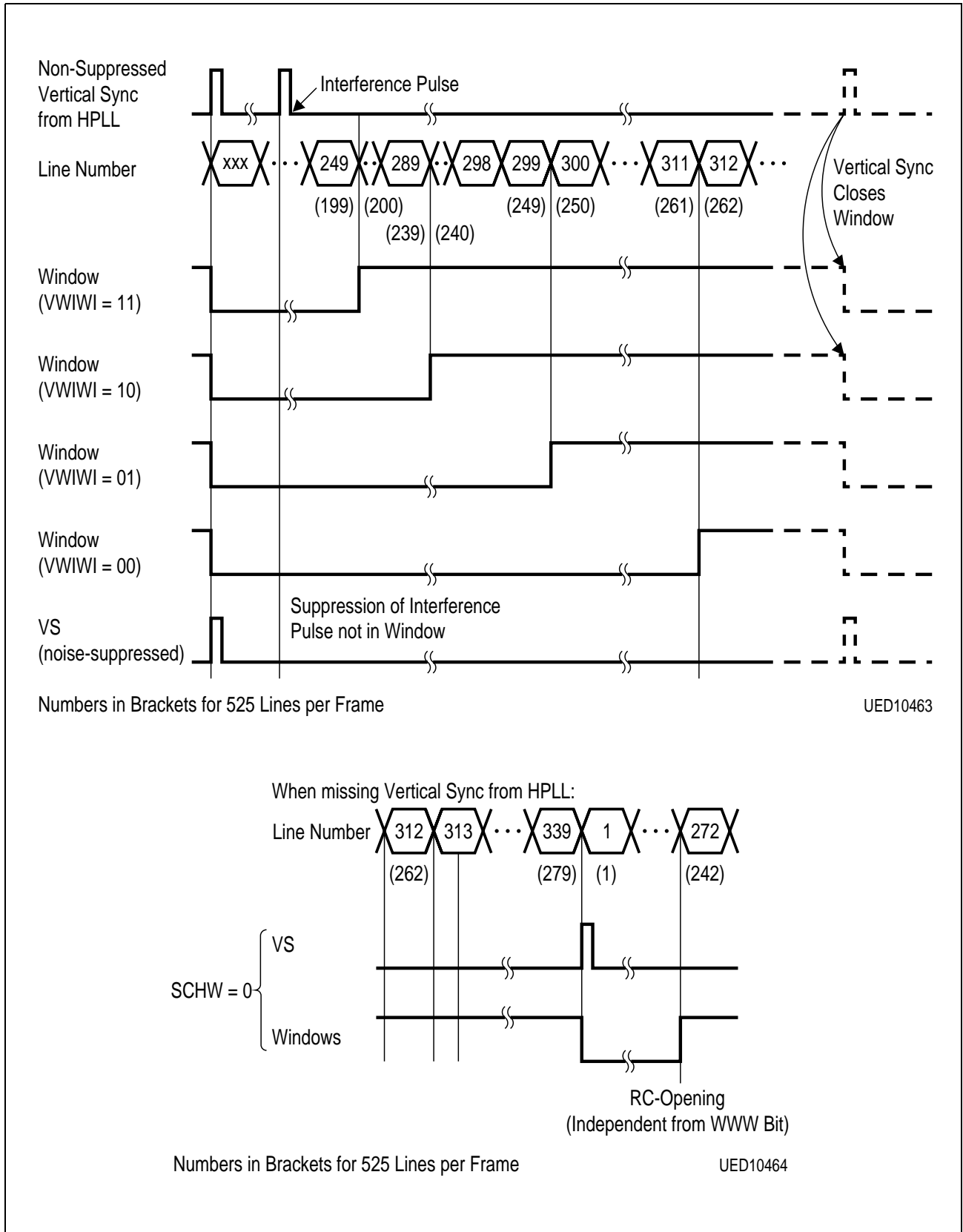


Figure 15
Window for Vertical Pulse Noise Suppression

2.3.3 Pulse Generation

The clock sync generator supplies the following pulses:

- HS
- VS
- BLN
- Two clamping pulses H1 and H2. H2 is also the internal clamping pulse of the YUV-ADCs.
- The HS pulse is 16 13.5 MHz clock periods long and can be shifted by the I²C-Bus in increments of four 13.5 MHz clock periods.
- For the VS pulse refer to vertical noise suppression.
- With the BLN pulse the start time (high-to-low edge) and the stop time (low-to-high edge) can be set within a certain range of lines in increments of 13.5 MHz clock periods by I²C Bus. The timing of BLN does not change during the field blanking interval.
- During the BLN pulse the Y-U-V output data are set to their clamping level.
- For pulse H1 the start time (low-to-high edge) and stop time can be set in increments of two 13.5 MHz clock periods.
- For pulse H2 the start time (low-to-high edge) and stop time can be set in increments of 13.5 MHz clock periods.

The timing of the BLN, H1, H2, VS and HS pulses can be set by the customer using the specified I²C-Bus bits. **Figure 9** shows the ranges of those settings.

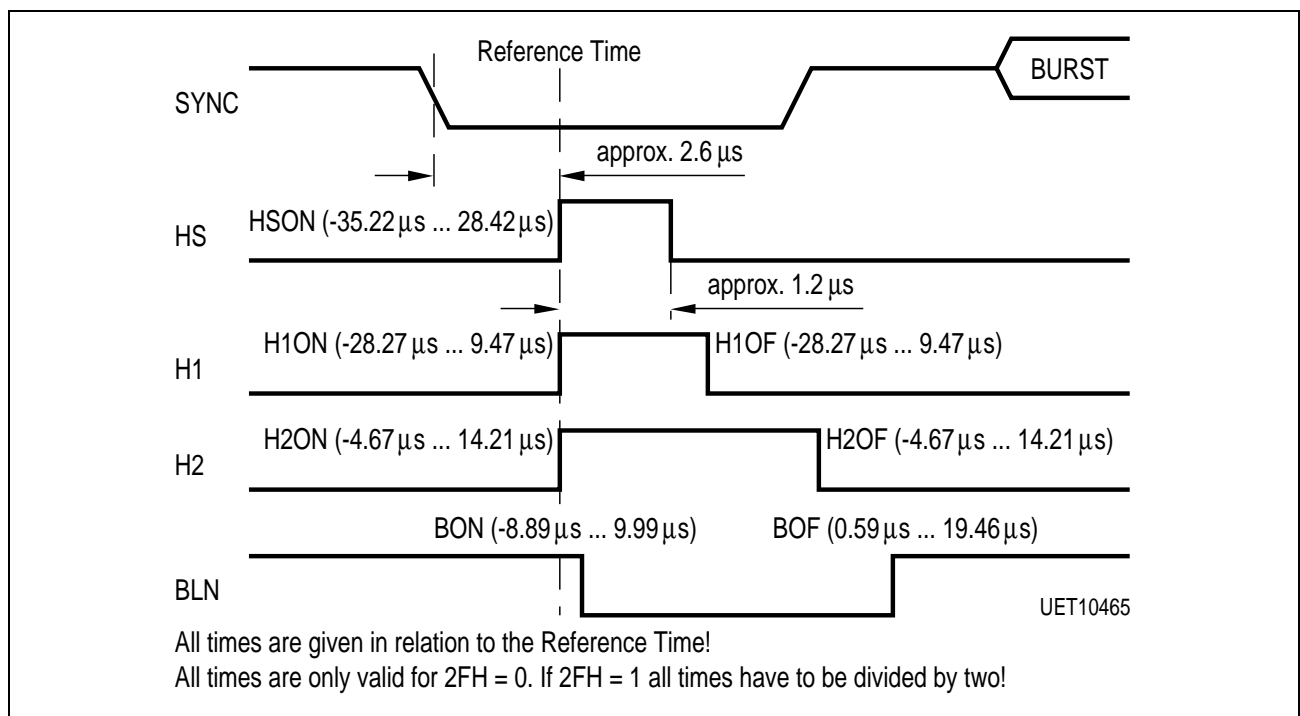


Figure 16
I²C-Bus Programming Areas of Horizontal-Frequency Pulses

2.3.4 Miscellaneous Circuit Sections

To suppress bottom flutter in VCR mode, the frequency of the clock can be 'hold' by 'freezing' the increment of the HPLL. The vertical-frequency 'freezing-time' starts a number of lines (programmable by the I²C Bus) before the vertical pulse and then lasts for a number (programmable) of lines. The settings do not depend on I²C-Bit TV. This functionality is only available for the 1fh mode (2FH = 0).

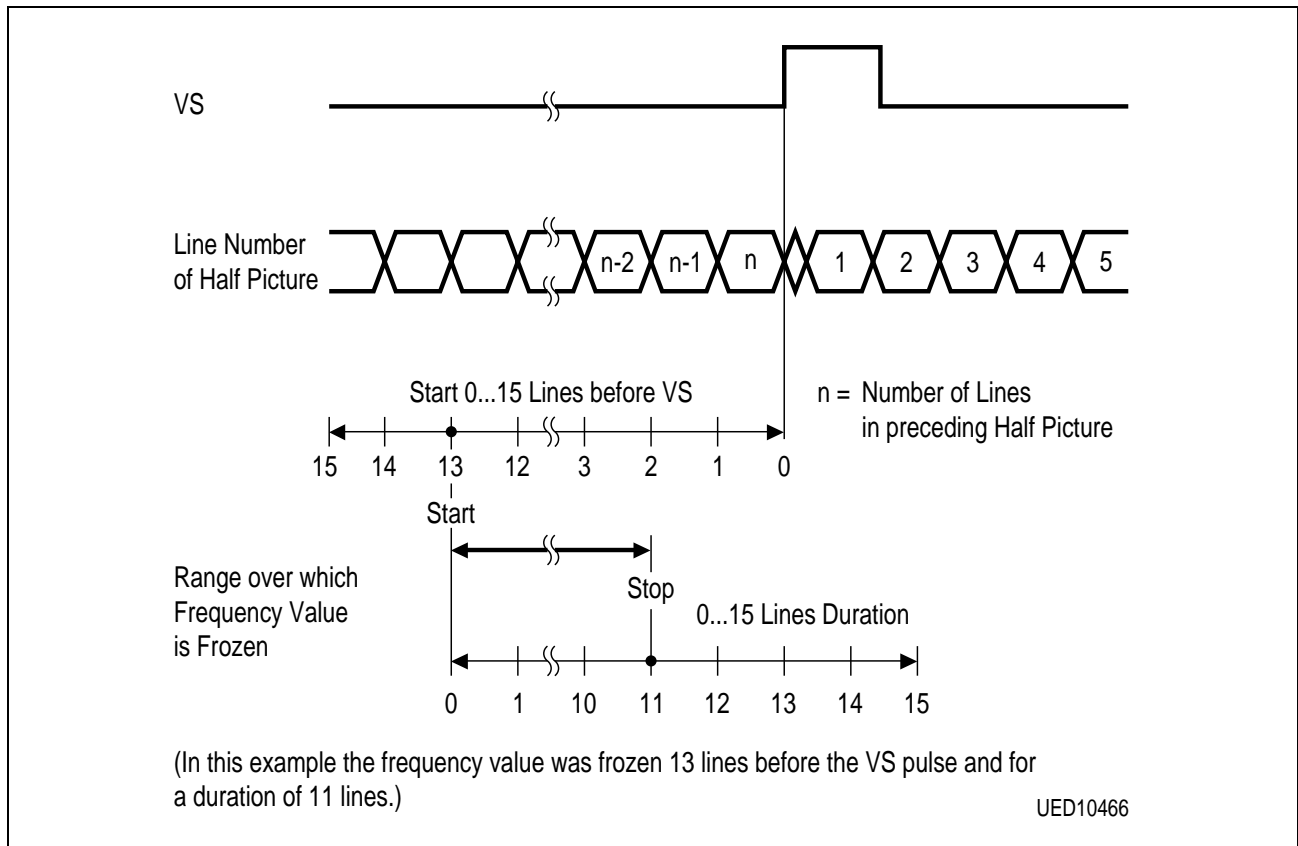


Figure 17
I²C-Bus Programming Area which Clock Frequency Value Generated by HPLL can be Frozen

An active low reset signal for other chips is available at pin RESOUTN. It is activated when the chip supply voltage V_{DD} is switched on or when voltage glitches occur on it. RESOUTN also is activated by pin RESIN. The RESOUTN pulse signal is not cancelled until the crystal oscillator resonates and in addition stretched by an internal circuit for approximately 127 lines (8 ms).

2.4 I²C Bus

2.4.1 I²C-Bus Address

| | | | | | | |
|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 1 | 0 | 0 | B |
|---|---|---|---|---|---|---|

B: equal to the value set on pin ADR0

2.4.2 I²C-Bus Format

Write:

| | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|------------|---|-----------|---|-------|---|---|
| S | 1 | 0 | 1 | 1 | 0 | 0 | B | 0 | A | Subaddress | A | Data Byte | A | ***** | A | P |
|---|---|---|---|---|---|---|---|---|---|------------|---|-----------|---|-------|---|---|

Read:

| | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|-------------|---------------|-----------------|---------------|-------|-----------|---|
| S | 1 | 0 | 1 | 1 | 0 | 0 | B | 1 | A | ... | Status Byte 0 | A | Status Byte 1 | A | Data***** | |
| | | | | | | | | | | **** Byte n | A | Data Byte (n+1) | A | ***** | NA | P |

Reading starts with status byte 0, followed by status byte 1 and then in succession by data byte n, data byte n+1..., where n is the last write address. Specification of a subaddress in reading mode is not possible.

S: Start condition

A: Acknowledge

P: Stop condition

NA: Not Acknowledge

An automatic address increment function is implemented.

After switching on the IC or RESIN = 0, all bits are set to defined states. Particularly:

| Register | Default value | Register | Default value |
|-----------------|-----------------|-----------------|-----------------|
| 00 _H | 10 _H | 0C _H | 00 _H |
| 01 _H | 40 _H | 0D _H | 00 _H |
| 02 _H | 00 _H | 0E _H | 00 _H |
| 03 _H | 00 _H | 0F _H | 00 _H |
| 04 _H | 28 _H | 10 _H | 00 _H |
| 05 _H | 00 _H | 11 _H | 00 _H |
| 06 _H | 00 _H | 12 _H | 00 _H |
| 07 _H | 06 _H | 13 _H | 00 _H |
| 08 _H | 00 _H | 14 _H | 13 _H |
| 09 _H | 00 _H | 15 _H | 00 _H |
| 0A _H | 00 _H | 16 _H | 00 _H |
| 0B _H | 00 _H | 17 _H | 00 _H |

2.4.3 I²C-Bus Commands

| Subadd. | Data Byte | | | | | | | |
|-----------------|-----------|---------|---------|---------|----------|----------|--------|--------|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00 _H | 0 | UV3FIL | FORMAT1 | FORMAT0 | UVCODE | YCODE | OENB | OENA |
| 01 _H | YD3 | YD2 | YD1 | YD0 | 0 | 0 | 0 | 0 |
| 02 _H | I2 | I1 | SELH2I2 | SELH1I1 | 0 | 0 | 0 | 0 |
| 03 _H | 0 | 0 | 0 | 0 | CGSUP1 | CGSUP0 | VWIWI1 | VWIWI0 |
| 04 _H | 0 | OEFB | S1CL1 | S1CL0 | S2CL1 | S2CL0 | 0 | 0 |
| 05 _H | 0 | SCHW | HPLL | VTHRE | CLOF | 0 | 0 | 0 |
| 06 _H | TV | FREE | VOFF | VF | TERM | GENMOD | 0 | SYPOL |
| 07 _H | 2FH | HSWMA | HSWMIN | INC4 | INC3 | INC2 | INC1 | INC0 |
| 08 _H | BON7 | BON6 | BON5 | BON4 | BON3 | BON2 | BON1 | BON0 |
| 09 _H | BOF7 | BOF6 | BOF5 | BOF4 | BOF3 | BOF2 | BOF1 | BOF0 |
| 0A _H | H1ON7 | H1ON6 | H1ON5 | H1ON4 | H1ON3 | H1ON2 | H1ON1 | H1ON0 |
| 0B _H | H1OF7 | H1OF6 | H1OF5 | H1OF4 | H1OF3 | H1OF2 | H1OF1 | H1OF0 |
| 0C _H | H2ON7 | H2ON6 | H2ON5 | H2ON4 | H2ON3 | H2ON2 | H2ON1 | H2ON0 |
| 0D _H | H2OF7 | H2OF6 | H2OF5 | H2OF4 | H2OF3 | H2OF2 | H2OF1 | H2OF0 |
| 0E _H | HSO7 | HSO6 | HSO5 | HSO4 | HSO3 | HSO2 | HSO1 | HSO0 |
| 0F _H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 10 _H | FION3 | FION2 | FION1 | FION0 | FILE3 | FILE2 | FILE1 | FILE0 |
| 11 _H | SYNAMP3 | SYNAMP2 | SYNAMP1 | SYNAMP0 | YAMP3 | YAMP2 | YAMP1 | YAMP0 |
| 12 _H | UAMP3 | UAMP2 | UAMP1 | UAMP0 | VAMP3 | VAMP2 | VAMP1 | VAMP0 |
| 13 _H | DATDEL2 | DATDEL1 | DATDEL0 | DATSLOP | CLKSLOP1 | CLKSLOP0 | 0 | 0 |
| 14 _H | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 15 _H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 16 _H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 17 _H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

2.4.4 Detailed Description

Subaddress 00_H

| Bit | Name | Function |
|---------|----------|---|
| D7 | <u>0</u> | Reserved |
| D6 | UV3FIL | Filter stage 3 for UV data (FORMAT = 0X) <u>0</u> : OFF 1: ON Note: For FORMAT = 1X filter stage 3 for UV data is "on" (UV3FIL = don't care) |
| D5...D4 | FORMAT | Selection of output data interface: <u>00</u> : Output data format according CCIR 656 (8 wires at Port A) <u>01</u> : Parallel output data format (2 x 8 wires) 10: Quasiparallel 12 wire interface 11: Quasiparallel 12 wire interface |
| D3 | UVCODE | Coding of UV data: <u>0</u> : Straight binary code 1: Two's complement code |
| D2 | YCODE | Coding of Y data: <u>0</u> : Straight binary code 1: Two's complement code |
| D1 | OENB | Output enable port B: <u>0</u> : Tristate 1: Port enabled |
| D0 | OENA | Output enable port A: <u>0</u> : Tristate 1: Port enabled |

Subaddress 01_H

| Bit | Name | Function |
|---------|------|---|
| D7...D4 | YD | Delay compensation in Y-signal path (13.5 MHz clocks): 0000: ... - 0.30 μs 0001 0010 0011 0100: ... 0 μs : 1110 1111: ... 0.81 μs |
| D3...D0 | 0000 | Reserved |

Subaddress 02_H

| Bit | Name | Function |
|-----|---------|--|
| D7 | I2 | Voltage level of H2I2 output (SELH2I2 = 1): 0: <u>Low voltage at pin H2I2</u> 1: High voltage at pin H2I2 |
| D6 | I1 | Voltage level of H1I1 output (SELH1I1 = 1): 0: <u>Low voltage at pin H1I1</u> 1: High voltage at pin H1I1 |
| D5 | SELH2I2 | Function of pin H2I2: 0: <u>H2 (line frequency, start and stop programmable)</u> 1: I2 (low/high programmable) |
| D4 | SELH1I1 | Function of pin H1I1: 0: <u>H1 (line frequency, start and stop programmable)</u> 1: I1 (low/high programmable) |
| D3 | 0 | Reserved |
| D2 | 0 | Reserved |
| D1 | 0 | Reserved |
| D0 | 0 | Reserved |

Subaddress 03_H

| Bit | Name | Function |
|---------|-------------|---|
| D7...D4 | <u>0000</u> | Reserved |
| D3...D2 | CGSUP | Suppression of black level disturbances caused by copy guarded tapes <u>00: No function</u> 01: Black level error is limited to + / - 32 (~ 27 mV) 10: Black level error is limited to + / - 16 (~ 14 mV) 11: Black level error is limited to + / - 8 (~ 7 mV) |
| D1...D0 | VWIWI | Width of Window in Vertical Processing: <u>00: Narrow window: open from line 312 for PAL and 262 for NTSC</u> 01: Window: open from line 300 for PAL and 250 for NTSC 10: Window: open from line 290 for PAL and 240 for NTSC 11: Very wide window: open from line 250 for PAL and 200 for NTSC |

Subaddress 04_H

| Bit | Name | Function |
|---------|-----------|---|
| D7 | <u>0</u> | Reserved |
| D6 | OEFB | Output enable for Featurebox signals BLN, HS and VS: <u>0: BLN, HS, VS outputs tristate</u> 1: BLN, HS, VS outputs enabled (2FH = 0) BLN, HS outputs enabled, VS output tristate (2FH = 1) |
| D5...D4 | S1CL | Selection of clock frequency on pin CLK1: 00: Tristate 01: 6.75 MHz <u>10: 13.5 MHz</u> 11: 27 MHz For the allowed values of S1CL refer to table chapter 2.3.1! |
| D3...D2 | S2CL | Selection of clock frequency on pin CLK2: 00: Tristate 01: 6.75 MHz <u>10: 13.5 MHz</u> 11: 27 MHz For the allowed values of S2CL refer to table chapter 2.3.1! |
| D1...D0 | <u>00</u> | Reserved |

Subaddress 05_H

| Bit | Name | Function |
|---------|------------|--|
| D7 | <u>0</u> | Reserved |
| D6 | SCHW | Mode of vertical pulse generation: 0: <u>No flywheel mode</u> 1: Flywheel mode |
| D5 | HPLL | Relationship between horizontal frequency in SYNC and default frequency on CLK1 and CLK2: 0: <u>864</u> 1: 858 |
| D4 | VTHRE | Minimum sync pulse length from which a vertical pulse is detected: 0: <u>26.6 μs</u> 1: 11.3 μs |
| D3 | CLOF | Clamping of SYNC for clock generator: 0: <u>Clamping on</u> 1: Clamping off |
| D2...D0 | <u>000</u> | Reserved |

Subaddress 06_H

| Bit | Name | Function | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|----------|--|------|--|------|----|--|------------|---|------------|---|-----|------------|---|------------|---|-----|---|----------|---|---|-------|---|----------|---|---|-------|---|----------|---|---|-----|---|----------|---|---|-----|
| D7 | TV | Selection of HPLL lock-in behavior: 0: <u>Optimum for VCR</u> 1: Optimum for SYNC from network | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D6 | FREE | Generation of V pulse: 0: <u>V derived from SYNC</u> 1: Free-running generation; vertical frequency is determined by VF bit, VOFF bit is enabled, SCHW bit should be set to 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D5 | VOFF | Vertical noise suppression: 0: <u>Noise suppression enabled</u> 1: No noise suppression | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D4 | VF | Number of lines per field: 0: <u>312.5 or 312</u> 1: 262.5 or 262 <i>Note: VF must be set to the number of lines present in SYNC for fly-wheel and noise suppression modes. VF determines the number of lines per field for the free-running or terminal mode.</i> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D3 | TERM | Terminal mode: <table border="1"> <thead> <tr> <th>FREE</th> <th>TERM</th> <th>SCHW</th> <th>VF</th> <th>Number of Lines per Field generated in Free-Running Mode</th> </tr> </thead> <tbody> <tr> <td>don't care</td> <td>1</td> <td>don't care</td> <td>0</td> <td>312</td> </tr> <tr> <td>don't care</td> <td>1</td> <td>don't care</td> <td>1</td> <td>262</td> </tr> <tr> <td>1</td> <td><u>0</u></td> <td>1</td> <td>0</td> <td>312.5</td> </tr> <tr> <td>1</td> <td><u>0</u></td> <td>1</td> <td>1</td> <td>262.5</td> </tr> <tr> <td>1</td> <td><u>0</u></td> <td>0</td> <td>0</td> <td>339</td> </tr> <tr> <td>1</td> <td><u>0</u></td> <td>0</td> <td>1</td> <td>279</td> </tr> </tbody> </table> | FREE | TERM | SCHW | VF | Number of Lines per Field generated in Free-Running Mode | don't care | 1 | don't care | 0 | 312 | don't care | 1 | don't care | 1 | 262 | 1 | <u>0</u> | 1 | 0 | 312.5 | 1 | <u>0</u> | 1 | 1 | 262.5 | 1 | <u>0</u> | 0 | 0 | 339 | 1 | <u>0</u> | 0 | 1 | 279 |
| FREE | TERM | SCHW | VF | Number of Lines per Field generated in Free-Running Mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| don't care | 1 | don't care | 0 | 312 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| don't care | 1 | don't care | 1 | 262 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | <u>0</u> | 1 | 0 | 312.5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | <u>0</u> | 1 | 1 | 262.5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | <u>0</u> | 0 | 0 | 339 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | <u>0</u> | 0 | 1 | 279 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D2 | GENMOD | Clock generator mode 0: <u>Normal PLL mode</u> 1: Generator mode (fixed frequency output, controlled by INC) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D1 | <u>0</u> | Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D0 | SYPOL | SYNC polarity: 0: <u>Negative sync signals</u> (normal SYNC input) 1: Positive sync signals | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Subaddress 07_H

| Bit | Name | Function |
|---------|-------|---|
| D7 | 2FH | Selection of input frequency range: <u>0</u> : Normal line frequencies (around 15.6 kHz) 1: Double line frequencies (31.2...38 kHz) [YUV A/D converters are switched off] |
| D6 | HSWMA | Maximum width of HSYNC (input SYNC): <u>0</u> : 6.2 μs for low FH-range 3.1 μs for high FH-range (2FH = 1) 1: 9.0 μs for low FH-range 4.5 μs for high FH-range (2FH = 1) |
| D5 | HSWMI | Minimum width of HSYNC (input SYNC): <u>0</u> : 3.0 μs for low FH-range 1.5 μs for high FH-range (2FH = 1) 1: 1.7 μs for low FH-range 0.8 μs for high FH-range (2FH = 1) |
| D4...D0 | INC | Nominal PLL output frequency: INC = <u>00110</u> For the allowed values of INC refer to table chapter 2.3.1! Calculation of INC for low FH range: $\text{INC} = \text{INT}\left(\frac{f_h}{f_q} * 110592 - 64,625\right)$ for high FH range (2FH = 1): $\text{INC} = \text{INT}\left(\frac{f_h}{f_q} * 55292 - 64,625\right)$ |

Subaddress 08_H

| Bit | Name | Function |
|---------|------|---|
| D7...D0 | BON | BLN start time in relation reference time (refer to the following table and to timing diagram) |

| BON7...BON0 | Number | 13.5 MHz Cycles | Time (2FH = 0) |
|------------------|------------------|-----------------|----------------|
| 1000 0000 | - (- 128) + 7 | = 135 | 9.99 μs |
| ... | ... | ... | ... |
| 1111 1111 | - (- 1) + 7 | = 8 | 0.60 μs |
| <u>0000 0000</u> | <u>- (0) + 7</u> | <u>= 7</u> | <u>0.52 μs</u> |
| 0000 0001 | - (+ 1) + 7 | = 6 | 0.44 μs |
| ... | ... | ... | ... |
| 0111 1111 | - (+ 127) + 7 | = - 120 | - 8.89 μs |

Subaddress 09_H

| Bit | Name | Function |
|---------|------|--|
| D7...D0 | BOF | BLN stop time in relation to reference time: (refer to the following table and to timing diagram) |

| BOF7...BOF0 | Number | 13.5 MHz Cycles | Time (2FH = 0) |
|------------------|----------------|-----------------|----------------|
| <u>0000 0000</u> | <u>(0) + 8</u> | <u>= 8</u> | <u>0.59 μs</u> |
| 0000 0001 | (+ 1) + 8 | = 9 | 0.67 μs |
| ... | ... | ... | ... |
| 0111 1111 | (+ 127) + 8 | = 135 | 9.99 μs |
| 1000 0000 | (+ 128) + 8 | = 136 | 10.06 μs |
| 1000 0001 | (+ 129) + 8 | = 137 | 10.14 μs |
| ... | ... | ... | ... |
| 1111 1110 | (+ 254) + 8 | = 262 | 19.39 μs |
| 1111 1111 | (+ 255) + 8 | = 263 | 19.46 μs |

Subaddress 0A_H

| Bit | Name | Function |
|---------|------|--|
| D7...D0 | H1ON | H1 start time in relation to reference time: (refer to the following table and to timing diagram) |

| H1ON7...H1ON0 | Number | 13.5 MHz Cycles | Time (2FH = 0) |
|------------------|------------------|-----------------|----------------|
| 1100 0000 | - (- 64) x 2 | = 128 | 9.47 μs |
| ... | ... | ... | ... |
| 1111 1111 | - (- 1) x 2 | = 2 | 0.15 μs |
| <u>0000 0000</u> | <u>- (0) x 2</u> | <u>= 0</u> | <u>0 μs</u> |
| 0000 0001 | - (+ 1) x 2 | = - 2 | - 0.15 μs |
| ... | ... | ... | ... |
| 0111 1111 | - (+ 127) x 2 | = - 254 | - 18.79 μs |
| 1000 0000 | - (+ 128) x 2 | = - 256 | - 18.94 μs |
| 1000 0001 | - (+ 129) x 2 | = - 258 | - 19.09 μs |
| ... | ... | ... | ... |
| 1011 1111 | - (+ 191) x 2 | = - 382 | - 28.27 μs |

Subaddress 0B_H

| Bit | Name | Function |
|---------|------|---|
| D7...D0 | H1OF | H1 stop time in relation to reference time: (refer to the following table and to timing diagram) |

| H1OF7...H1OF0 | Number | 13.5 MHz Cycles | Time (2FH = 0) |
|------------------|------------------|-----------------|----------------|
| 1100 0000 | - (- 64) x 2 | = 128 | 9.47 μs |
| ... | ... | ... | ... |
| 1111 1111 | - (- 1) x 2 | = 2 | 0.15 μs |
| <u>0000 0000</u> | <u>- (0) x 2</u> | <u>= 0</u> | <u>0 μs</u> |
| 0000 0001 | - (+ 1) x 2 | = - 2 | - 0.15 μs |
| ... | ... | ... | ... |
| 0111 1111 | - (+ 127) x 2 | = - 254 | - 18.79 μs |
| 1000 0000 | - (+ 128) x 2 | = - 256 | - 18.94 μs |
| 1000 0001 | - (+ 129) x 2 | = - 258 | - 19.09 μs |
| ... | ... | ... | ... |
| 1011 1111 | - (+ 191) x 2 | = - 382 | - 28.27 μs |

Subaddress 0C_H

| Bit | Name | Function |
|---------|------|--|
| D7...D0 | H2ON | H2 start time in relation to reference time: (H2 is always used as clamping reference for the YUV ADCs) (refer to the following table and to timing diagram) |

| H2ON7...H2ON0 | Number | 13.5 MHz Cycles | Time (2FH = 0) |
|------------------|--------------|-----------------|----------------|
| 0100 0000 | - (- 192) | = 192 | 14.21 μs |
| ... | ... | ... | ... |
| 0111 1111 | - (- 129) | = 129 | 9.55 μs |
| 1000 0000 | - (- 128) | = 128 | 9.47 μs |
| 1000 0001 | - (- 127) | = 127 | 9.40 μs |
| ... | ... | ... | ... |
| 1111 1111 | - (- 1) | = 1 | 0.07 μs |
| <u>0000 0000</u> | <u>- (0)</u> | <u>= 0</u> | <u>0 μs</u> |
| 0000 0001 | - (+ 1) | = - 1 | - 0.07 μs |
| ... | ... | ... | ... |
| 0011 1111 | - (+ 63) | = - 63 | - 4.67 μs |

Subaddress 0D_H

| Bit | Name | Function |
|---------|------|---|
| D7...D0 | H2OF | H2 stop time in relation to reference time: (H2 is always used as clamping reference for the YUV ADCs) (refer to the following table and to timing diagram) |

| H2OF7...H2OF0 | Number | 13.5 MHz Cycles | Time (2FH = 0) |
|------------------|--------------|-----------------|----------------|
| 0100 0000 | - (- 192) | = 192 | 14.21 μs |
| ... | ... | ... | ... |
| 0111 1111 | - (- 129) | = 129 | 9.55 μs |
| 1000 0000 | - (- 128) | = 128 | 9.47 μs |
| 1000 0001 | - (- 127) | = 127 | 9.40 μs |
| ... | ... | ... | ... |
| 1111 1111 | - (- 1) | = 1 | 0.07 μs |
| <u>0000 0000</u> | <u>- (0)</u> | <u>≡ 0</u> | <u>0 μs</u> |
| 0000 0001 | - (+ 1) | = - 1 | - 0.07 μs |
| ... | ... | ... | ... |
| 0011 1111 | - (+ 63) | = - 63 | - 4.67 μs |

Subaddress 0E_H

| Bit | Name | Function |
|---------|------|--|
| D7...D0 | HS0N | HS start time in relation to reference time: (refer to the following table and to timing diagram) |

| HS0N7...HS0N0 | Number | 13.5 MHz Cycles | Time (2FH = 0) |
|------------------|------------------|-----------------|----------------|
| 1010 0000 | - (- 96) x 4 | = 384 | 28.42 μs |
| ... | ... | ... | ... |
| 1111 1111 | - (- 1) x 4 | = 4 | 0.30 μs |
| <u>0000 0000</u> | <u>- (0) x 4</u> | <u>≡ 0</u> | <u>0 μs</u> |
| 0000 0001 | - (+ 1) x 4 | = - 4 | - 0.30 μs |
| ... | ... | ... | ... |
| 0111 0110 | - (+ 118) x 4 | = - 472 | - 34.93 μs |
| 0111 0111 | - (+ 119) x 4 | = - 476 | - 35.22 μs |

Subaddress 0F_H

| Bit | Name | Function |
|---------|-----------|----------|
| D7...D0 | 0000 0000 | Reserved |

Subaddress 10_H

| Bit | Name | Function |
|---------|------|---|
| D7...D4 | FION | Start of clock frequency freezing in number of lines before the vertical pulse (only valid for 2FH = 0): 0000: 0 (no freezing) 0001: 1 : : 1111: 15 |
| D3...D0 | FILE | Duration of clock frequency freezing in number of lines: 0000: 0 (no freezing) 0001: 1 : : 1111: 15 |

Subaddress 11_H

| Bit | Name | Function |
|---------|--------|---|
| D7...D4 | SYNAMP | Internal amplification of SYNC input signal. Allowed values: SYNAMP = 0000 : amplification 0 dB : SYNC input nom. 2 Vpp SYNAMP = 0110 : amplification 6 dB : SYNC input nom. 1 Vpp |
| D3...D0 | YAMP | Internal amplification of AINY input signal. Allowed values: YAMP = 0000 : amplification 0 dB : AINY input nom. 2 Vpp YAMP = 0110 : amplification 6 dB : AINY input nom. 1 Vpp |

Subaddress 12_H

| Bit | Name | Function |
|---------|------|--|
| D7...D4 | UAMP | Internal amplification of AINU input signal. Allowed values: UAMP = <u>0000</u> : internal amplification 0 dB : AINU input nom. 2 Vpp UAMP = 0110 : internal amplification 6 dB : AINU input nom. 1 Vpp |
| D3...D0 | VAMP | Internal amplification of AINV input signal. Allowed values: VAMP = <u>0000</u> : amplification 0 dB : AINV input nom. 2 Vpp VAMP = 0110 : internal amplification 6 dB : AINV input nom. 1 Vpp |

Subaddress 13_H

| Bit | Name | Function |
|---------|-----------|--|
| D7...D5 | DATDEL | Programmable output delay for PAQ7...PAQ0, PBQ7...PBQ0, BLN, HS, H1I1, H2I2, VS. Allowed values: <u>000</u> 001 (description see chapter 5.3) |
| D4 | DATSLOP | Adaptation of the output driver stages for PAQ7...PAQ0, PBQ7...PBQ0, BLN, HS, H1I1, H2I2, VS. Allowed values: <u>0</u> ... to be used only for 5 V output stage supply voltage 1 ... to be used only for 3.3 V output stage supply voltage and FORMAT = 00 |
| D3...D2 | CLKSLOP | Adaptation of the output driver stages for CLK1 and CLK2. Allowed values: <u>00</u> ... to be used only for 5 V output stage supply voltage 10 ... to be used only for 3.3 V output stage supply voltage |
| D1...D0 | <u>00</u> | Reserved |

Subaddress 14_H

| Bit | Name | Function |
|---------|-----------|----------|
| D7...D0 | 0001 0011 | Reserved |

Subaddress 15_H

| Bit | Name | Function |
|---------|-----------|----------|
| D7...D0 | 0000 0000 | Reserved |

Subaddress 16_H

| Bit | Name | Function |
|---------|-----------|----------|
| D7...D0 | 0000 0000 | Reserved |

Subaddress 17_H

| Bit | Name | Function |
|---------|-----------|----------|
| D7...D0 | 0000 0000 | Reserved |

2.4.5 Read Mode

Status Byte 0

| Bit | Name | Function | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|-------------|--|-----|-------------|-----|--|------|----|------|---|---|---------------|---|---|----------------|---|---|----------------|---|---|---------------|---|---|------|---|---|--------|--------|----|----|----|----|---|---|-----|-----|-----|-----|---|---|-----|-----|-----|-----|---|---|-----|-----|-----|-----|---|---|-----|-----|-----|-----|
| D7 | CON | Absolute difference between the horizontal sync pulse in SYNC and the HPLL: 0: Larger than or equal to 32 system clock cycles 1: Less than 32 system clock cycles | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D6 | THRELIM | Absolute difference between the horizontal sync pulse in SYNC and the HPLL: 0: Larger than 8 system clock cycles 1: Less than 8 system clock cycles for 8 or more successive lines (i.e. HPLL well locked in) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D5, D4 | FFGF, FF | <p>Identified number of lines per field (refer also to timing diagram figure 16):</p> <table border="0"> <thead> <tr> <th></th> <th colspan="2">Status Bits</th> </tr> <tr> <th></th> <th>FFGF</th> <th>FF</th> </tr> </thead> <tbody> <tr> <td>< N1</td> <td>0</td> <td>0</td> </tr> <tr> <td>≥ N1 and ≤ N2</td> <td>1</td> <td>0</td> </tr> <tr> <td>> N2 and < 287</td> <td>0</td> <td>0</td> </tr> <tr> <td>≥ 287 and < N3</td> <td>0</td> <td>1</td> </tr> <tr> <td>≥ N3 and ≤ N4</td> <td>1</td> <td>1</td> </tr> <tr> <td>> N4</td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p>N1 to N4 depends on Control Bits VWIWI:</p> <table border="0"> <thead> <tr> <th>VWIWI1</th> <th>VWIWI0</th> <th>N1</th> <th>N2</th> <th>N3</th> <th>N4</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>262</td> <td>264</td> <td>312</td> <td>314</td> </tr> <tr> <td>0</td> <td>1</td> <td>250</td> <td>275</td> <td>300</td> <td>325</td> </tr> <tr> <td>1</td> <td>0</td> <td>240</td> <td>285</td> <td>290</td> <td>335</td> </tr> <tr> <td>1</td> <td>1</td> <td>200</td> <td>312</td> <td>250</td> <td>362</td> </tr> </tbody> </table> | | Status Bits | | | FFGF | FF | < N1 | 0 | 0 | ≥ N1 and ≤ N2 | 1 | 0 | > N2 and < 287 | 0 | 0 | ≥ 287 and < N3 | 0 | 1 | ≥ N3 and ≤ N4 | 1 | 1 | > N4 | 0 | 1 | VWIWI1 | VWIWI0 | N1 | N2 | N3 | N4 | 0 | 0 | 262 | 264 | 312 | 314 | 0 | 1 | 250 | 275 | 300 | 325 | 1 | 0 | 240 | 285 | 290 | 335 | 1 | 1 | 200 | 312 | 250 | 362 |
| | Status Bits | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | FFGF | FF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| < N1 | 0 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| ≥ N1 and ≤ N2 | 1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| > N2 and < 287 | 0 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| ≥ 287 and < N3 | 0 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| ≥ N3 and ≤ N4 | 1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| > N4 | 0 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VWIWI1 | VWIWI0 | N1 | N2 | N3 | N4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 262 | 264 | 312 | 314 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 250 | 275 | 300 | 325 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 240 | 285 | 290 | 335 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 200 | 312 | 250 | 362 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D3 | | don't care | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D2 ... D0 | POR | Status bit POR is set by power on reset or by activating the reset pin. POR is reset after reading the status byte. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Status Byte 1

| Bit | Name | Function |
|------------|-------------|---|
| D7...D6 | | don't care |
| D5 | OFLY | Overflow detection of ADC for input AINY |
| D4 | UFLY | Underflow detection of ADC for input AINY |
| D3 | OFLU | Overflow detection of ADC for input AINU |
| D2 | UFLU | Underflow detection of ADC for input AINU |
| D1 | OFLV | Overflow detection of ADC for input AINV |
| D0 | UFLV | Underflow detection of ADC for input AINV |

3 Absolute Maximum Ratings

| Parameter | Symbol | Limit Values | | Unit | Remark |
|--|--|----------------------------------|----------------------------------|------|---|
| | | min. | max. | | |
| Storage temperature | T_{stg} | - 40 | 125 | °C | |
| Soldering temperature | T_{sold} | | 260 | °C | |
| Soldering time | t_{sold} | | 10 | sec | |
| Input/output voltage | $V_{\text{I/Q}}$ | $V_{\text{SSQ}} - 0.3 \text{ V}$ | $V_{\text{DDQ}} + 0.3 \text{ V}$ | 1 | Not valid for I ² C-Bus pins |
| Input/output voltage I ² C-pins 33, 34 (SCL, SDA) | $V_{\text{I/Q, I2C}}$ | $V_{\text{SSQ}} - 0.3 \text{ V}$ | 6 V | 1 | |
| Power supply voltage | $V_{\text{DD}},$ $V_{\text{ADDX}},$ $V_{\text{DDQ}},$ V_{DDTO} | - 0.3 | 6 | V | |
| Total power dissipation | P_{tot} | | 1.25 | W | |
| Latch-up protection | | - 100 | 100 | mA | All inputs/outputs |
| ESD protection | ESD | - 1 | 1 | kV | MIL STD 883C method 3015-6, 100 pF, 1500 Ω |

All voltages listed are referenced to ground (0 V, V_{SS}) except where noted.

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions or at any other condition beyond those indicated in the operational sections of this specification is not implied.

3.1 Recommended Operating Conditions

| Parameter | Symbol | Limit Values | | | Unit | Remark |
|---------------------|--------|--------------|------|------|------|--------|
| | | min. | nom. | max. | | |
| Ambient temperature | T_A | 0 | 25 | 70 | °C | |

Power Requirements

| | | | | | | |
|-----------------------------|----------------|--------|-----|------|---|---|
| Analog supply voltage | V_{ADDx} | 4.75 | 5.0 | 5.25 | V | |
| Digital supply voltage | V_{DD} | 4.75 | 5.0 | 5.25 | V | |
| DTO supply voltage | V_{DDDTO} | 4.75 | 5.0 | 5.25 | V | |
| Output stage supply voltage | V_{DDQ} | 4.75 | 5.0 | 5.25 | V | 5 V-Mode |
| | | 3.0 | 3.3 | 3.6 | V | 3.3 V mode, only to be used for FORMAT = 00 |
| Supply voltage differential | $V_{DD, diff}$ | - 0.25 | | 0.25 | V | Supply pins V_{ADDx} |

All TTL Inputs

| | | | | | | |
|-----------------|----------|------|--|-----------|---|--|
| H-input voltage | V_{IH} | 2.0V | | V_{DDQ} | 1 | |
| L-input voltage | V_{IL} | 0 | | 0.8 | V | |

I²C-Bus (Values are Referred to min. (V_{IH}) and max. (V_{IL}))

| | | | | | | |
|--------------------------------------|---------------|----------------------|--|----------------------|-----|--|
| H-input voltage | V_{IH} | $0.7 \times V_{DDQ}$ | | V_{DD} | 1 | |
| L-input voltage | V_{IL} | 0V | | $0.3 \times V_{DDQ}$ | 1 | |
| SCL clock frequency | f_{SCL} | 0 | | 400 | kHz | |
| Rise times of SCL, SDA | t_R | | | 0.3 | µs | |
| Fall times of SCL, SDA | t_F | | | 0.3 | µs | |
| Set-up time data | $t_{SU, Dat}$ | 100 | | | ns | |
| Hold time data | $t_{HD, Dat}$ | 0 | | | ns | |
| Bus free time before start condition | t_{Buf} | 1.3 | | | µs | |
| Set-up time start condition | $t_{SU, Sta}$ | 0.6 | | | µs | |
| Hold time start condition | $t_{HD, Sta}$ | 0.6 | | | µs | |

3.1 Recommended Operating Conditions (cont'd)

| Parameter | Symbol | Limit Values | | | Unit | Remark |
|------------------|------------|--------------|------|------|---------|--------|
| | | min. | nom. | max. | | |
| SCL low time | t_{Low} | 1.3 | | | μs | |
| SCL high time | t_{High} | 0.6 | | | μs | |
| Load capacitance | | | | 400 | pF | |

Reference Inputs for Analog Inputs AINY, AINU, AINV, SYNC

| | | | | | | |
|------------------------|-------------|-----|-----|-----|---|------------------|
| Reference voltage high | V_{REFHx} | 3.2 | 4.2 | 4.7 | V | $V_{ADDx} = 5 V$ |
| Reference voltage low | V_{REFLx} | 1.7 | 2.2 | 3.2 | V | |

Analog Inputs AINY, AINU, AINV

| | | | | | | |
|-----------------------------------|--------------|---|-----|-------------------------|----------|--|
| Input range (Peak-Peak) | V_{IPP} | | 2 V | $V_{REFHx} - V_{REFLx}$ | 1 | YAMP, UAMP, VAMP = 0000, Prefiltering see chapter 2.1.2 |
| Required ext clamp capacitance | $C_{ext cl}$ | | 100 | | nF | AINY, AINU, AINV each |
| Required signal source resistance | R_S | 0 | | 200 | Ω | |

SYNC Input for Sync and Clock Generation

| | | | | | | |
|-----------------------------------|--------------|-------|-----|-------------------------|----------|-------------------|
| Input range (Peak-Peak) | V_{IPP} | 0.5 V | 2 V | $V_{REFHC} - V_{REFLC}$ | 1 | SYNAMP = 0000 |
| Input frequency | f | 0 | | 12 | MHz | To avoid aliasing |
| Required ext clamp capacitance | $C_{ext cl}$ | | 100 | | nF | |
| Required signal source resistance | R_S | | | 200 | Ω | |

Inputs Crystal Connections X1, X2

| | | | | | | |
|-------------------|-------|--|--------|--|-----|--|
| Crystal frequency | f_c | | 24.576 | | MHz | |
|-------------------|-------|--|--------|--|-----|--|

Crystal Type Fundamental Crystal

| | | | | | | |
|----------------------------|-----------|--|-----|----|----------|------|
| Equivalent parallel C | C_O | | 3.6 | | pF | |
| Crystal resonant impedance | Z_R | | | 40 | Ω | |
| Pin capacitance | C_I | | | 10 | pF | |
| External capacitance | C_{ext} | | 18 | | pF | Each |

3.2 Characteristics (Assuming Recommended Operating Conditions)

| Parameter | Symbol | Limit Values | | | Unit | Remark |
|--|-----------|--------------|------|-----------|----------|--|
| | | min. | nom. | max. | | |
| Supply Currents | | | | | | |
| Analog supply current | I_{ADD} | | 120 | | mA | Sum of all V_{ADDx} pins |
| Digital supply current | I_{DD} | | 40 | | mA | Sum of all V_{DD} pins + V_{DDTO} |
| Output stage supply current | I_{DDQ} | | 40 | | mA | Sum of all V_{DDQ} pins |
| Reference Inputs for Analog Inputs AINY, AINU, AINV | | | | | | |
| Reference ladder resistance | R_{REF} | 175 | 250 | 325 | Ω | For each converter between REFH and REFL |
| Reference Inputs for Analog Input SYNC | | | | | | |
| Reference ladder resistance | R_{REF} | 280 | 400 | 520 | Ω | For each converter between REFH and REFL |
| All TTL Inputs | | | | | | |
| Input current | | - 300 | | 300 | μ A | $V_I = 0\text{ V} \dots V_{DDQ}$ Note: internal pullup/pulldown-circuits |
| I²C Input/Output SDA | | | | | | |
| L-output voltage | V_{QL} | | | 0.6 | V | $I = 4\text{ mA}$ |
| Analog Inputs | | | | | | |
| Analog input leakage current | I_{AIN} | - 100 | | 100 | nA | AINY, AINU, AINV, SYNC each |
| Analog input capacitance | C_1 | | | 10 | pF | AINY, AINU, AINV, SYNC each |
| TTL Outputs Port A, Port B, VS, HS, BLN, H1, H2, RESOUTN ($V_{DDQ} = 3.3\text{ V}$ or 5 V) | | | | | | |
| L-output voltage | V_{QL} | 0 | | 0.4 | V | $I = 1\text{ mA}$ |
| H-output voltage | V_{QH} | 2.4 V | | V_{DDQ} | 1 | $I = -0.5\text{ mA}$ |
| High impedance state output current | I_{QZ} | - 20 | | 20 | μ A | $V_Q = 0\text{ V} \dots V_{DDQ}$ Port A, Port B, VS, HS, BLN |
| Load capacitance | C_L | | | 25 | pF | |

3.2 Characteristics (Assuming Recommended Operating Conditions) (cont'd)

| Parameter | Symbol | Limit Values | | | Unit | Remark |
|---|----------|--------------|------|------|------|--|
| | | min. | nom. | max. | | |
| Output data delay time, t_{QD} referenced to CLK1 (not valid for ESOUTN) | | | | 25 | ns | DATDEL = 000 $C_L = 15$ pF 5 V output stage supply voltage, DATSLOP = 0 |
| | | | | 35 | ns | DATDEL = 000 $C_L = 25$ pF 5 V output stage supply voltage, DATSLOP = 0 |
| | | | | 25 | ns | DATDEL = 000 $C_L = 25$ pF 3.3 V output stage supply voltage, FORMAT = 00 DATSLOP = 1 |
| Output data hold time, t_{QH} referenced to CLK1 (not valid for RESOUTN) | t_{QH} | 6 | | | ns | |
| Pin RESOUTN Data delay/ data hold time | | - | - | - | | Asynchronous output signal |

Clock TTL Outputs CLK1, CLK2

| | | | | | | |
|------------------|------------|-------|--|----------|----|--|
| L-output voltage | V_{QL} | 0 | | 0.4 | V | $I = 1$ mA |
| H-output voltage | V_{QH} | 2.4 V | | V_{DD} | 1 | $I = -0.5$ mA |
| Load capacitance | C_L | | | 30 | pF | |
| Transition times | t_R, t_F | | | 5 | ns | 5 V output stage supply voltage, CLKSLOP = 00 3.3 V output stage supply voltage, CLKSLOP = 10 |

3.2 Characteristics (Assuming Recommended Operating Conditions) (cont'd)

| Parameter | Symbol | Limit Values | | | Unit | Remark |
|---|------------|--------------|------|------|------|---|
| | | min. | nom. | max. | | |
| Low time 13.5 MHz | t_{WL13} | 26 | | | ns | 13.5 MHz |
| High time 13.5 MHz | t_{WH13} | 26 | | | ns | 13.5 MHz |
| Low time 27 MHz | t_{WL27} | 10 | | | ns | 27 MHz |
| High time 27 MHz | t_{WH27} | 10 | | | ns | 27 MHz |
| Skew | t_{SK} | - 2 | 0 | 2 | ns | $C_{L,CLK1} = C_{L,CLK2}$ |
| Frequency range when PLL is locked at SYNC input signal | f | 25 | 27 | 35 | MHz | $\pm 4.8\%$ at 27 MHz S1CL = 11, S2CL = 11 |

Performance of A/D Conversion (8-Bit)

Test Conditions: ADC Clock = 27 MHz, DATDEL = 000, xAMP = 0000, VIPP = 2 Vpp

| | | | | | | |
|--|----------------|----|-----|-----------|-----|-------------------|
| Sampling rate | | | 27 | | MHz | |
| Differential linearity (DC) | DNLE | | | ± 0.5 | LSB | |
| Integral linearity (DC) | INLE | | | ± 1 | LSB | |
| Clamping level accuracy | CLA | | 0.5 | ± 3 | LSB | |
| Gain error (DC) | GE | | | ± 6 | LSB | |
| Gain matching error (DC) | GME | | | ± 3 | LSB | |
| Differential gain | DG | | | 3 | % | Not tested |
| Differential phase | DP | | | 3 | deg | Not tested |
| Signal to noise ratio at 4.4 MHz sinus | $\alpha_{S/N}$ | 45 | 48 | | dB | Without harmonics |

Harmonic Distortion

| | | | | | | |
|-------------|--|--|--|------|----|---------------------|
| 2./4. order | | | | - 42 | dB | 4.4 MHz fundamental |
| 3. order | | | | - 42 | dB | 4.4 MHz fundamental |
| 5./6. order | | | | - 48 | dB | 4.4 MHz fundamental |

4 Application Information

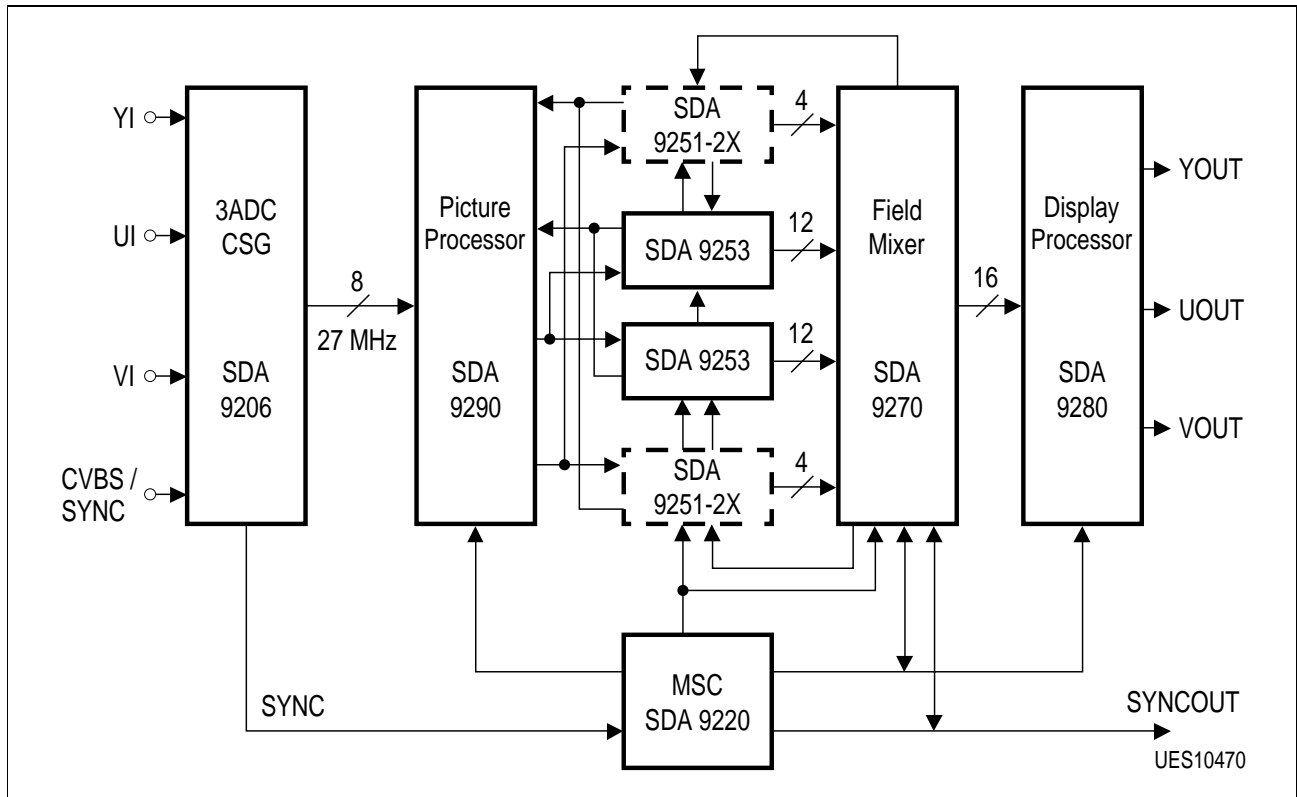


Figure 18
Application Circuit 1

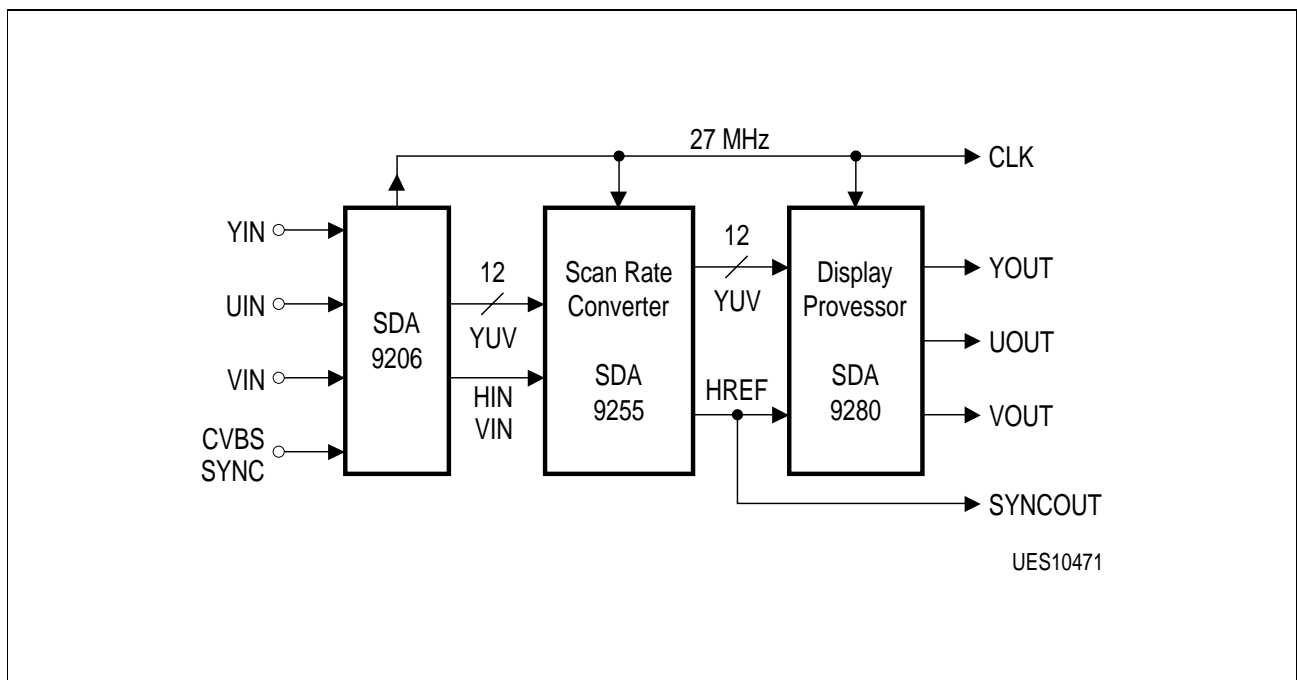


Figure 19
Application Circuit 2

5 Waveforms

5.1 Timing Diagram Data Input/Output Referenced to the Clock CLK1

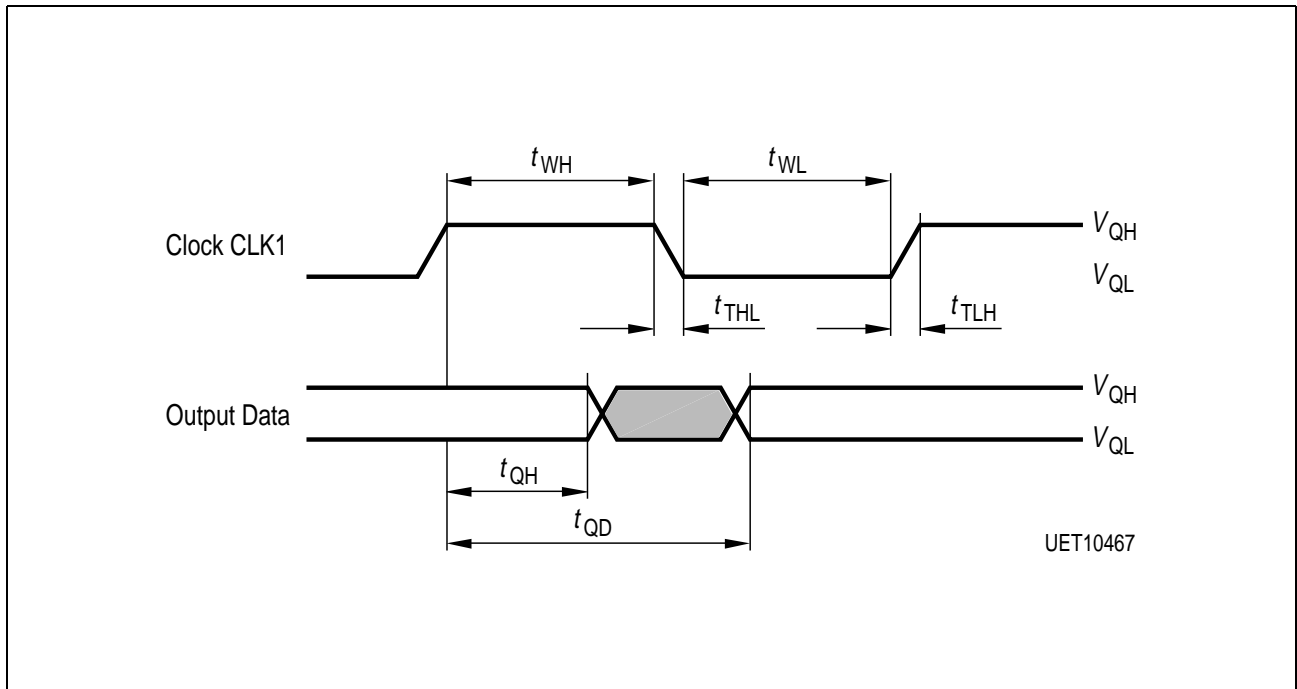


Figure 21

5.2 Timing Diagram Clock Skew CLK2 - CLK1

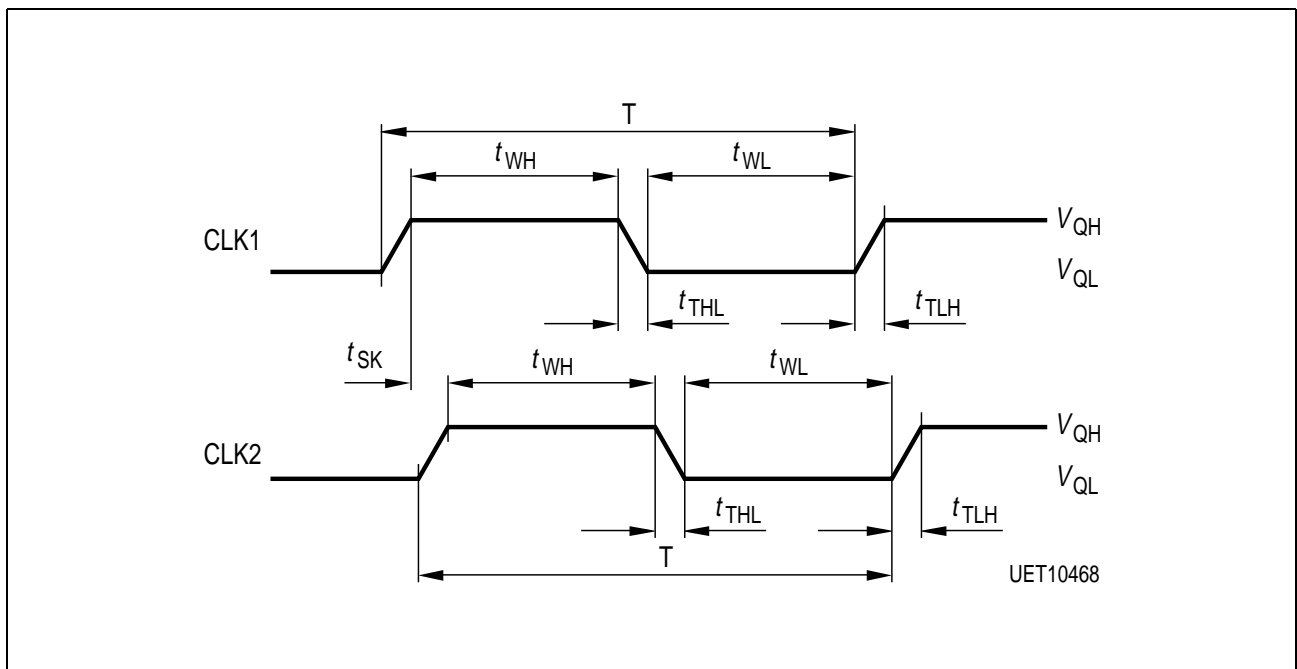


Figure 22

5.3 Programmable Data Output Delay:
DAT_OUT: Pins PAQ7...0, PBQ7...0, BLN, HS, H1I1, H2I2 and VS

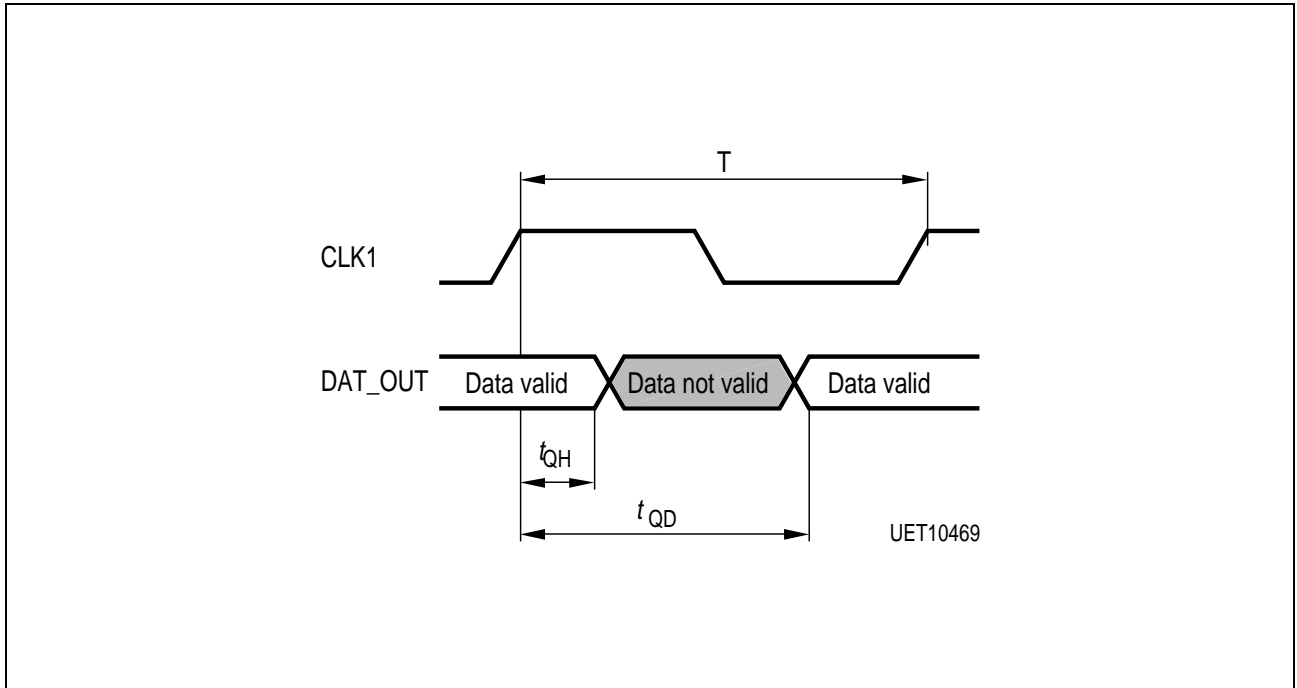


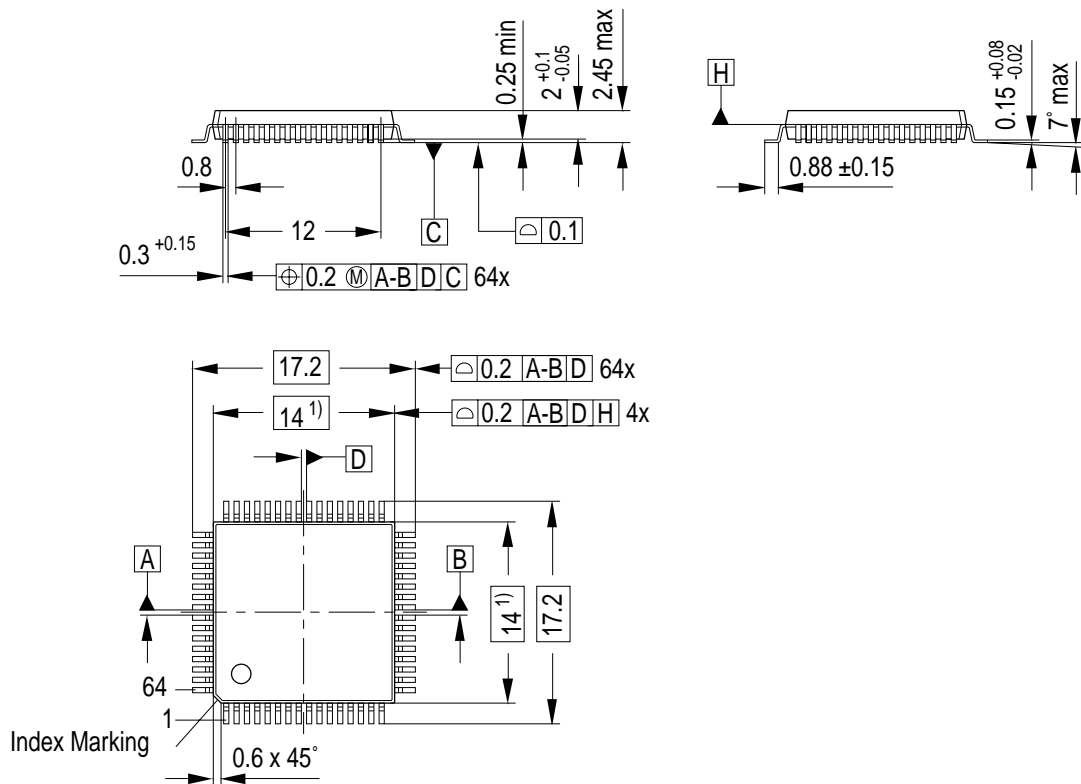
Figure 23

| DATDEL | t_{QH} ; min. | t_{QD} ; max. |
|--------|-----------------|-----------------|
| 000 | 6 ns | 25 ns |
| 001 | 10 ns | 29 ns |

The delay times are valid for a clock rate of the analog PLL of 27 MHz.

6 Package Outlines

P-MQFP-64-3
(Plastic Metric Quad Flat Package)



GPM05250

Figure 24

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm