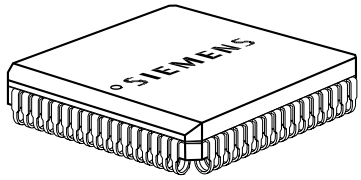
SIEMENS

Picture Processor SDA 9290-6

Preliminary Data **CMOS IC**

Features

- Noise and cross color reduction by field - or frame recursive filtering
- Adjustment of degree of noise reduction
- Automatic adaption to signal quality during vertical blanking
- Pixel adaptive movement detection
- Split screen modes for demonstration purposes
- Multi-picture facilities
- Picture decimation using vertical filtering
- 8 programmable grey levels for framing
- 4:1:1 and 4:2:2 (Y:U:V) compatibility
- 8-bit word size for all components
- IIC-Bus programming of the video line for S/N measurement in automatic adaption mode
- Optimized characteristics of the recursive filters



P-LCC-68-1

Type	Ordering Code	Package
SDA 9290-6	Q67101-H5193	P-LCC-68-1 (SMD)

Functional Description

The CMOS device SDA 9290-6 is a picture processor and belongs to a family of devices forming an extended third-generation digital TV signal-processing system for enhanced picture quality with special functions (Featurebox). Besides the Picture Processor (PP) that is described here, the system consists of a field memory (at least three triple-port, 1-Mbit generation **TV S**equential-**A**ccess **M**emory devices (SDA 9251 X), a **M**emory **S**ync **C**ontroller (MSC SDA 9220-5) and a **D**isplay **P**rozessor (SDA 9280). A block diagram of the Featurebox is shown in **figure 4**.

The Picture Processor SDA 9290-6 is a follow-on development of the Picture Processor SDA 9290-5. Modifications of the movement detector and the recursive filters permits further picture improvement by reducing the video noise and cross-color interference. The SDA 9290-6 can be set independently at the picture-signal input and output via the two pins FSBQ/FSI to the 4:1:1 and 4:2:2 formats. A 4:1:1 Featurebox (3 TV-SAMs) can therefore be operated with 4:2:2 input signals as well.

The necessary decimation and interpolation operations are activated automatically when the format is set. Together with a corresponding Memory Sync Controller (SDA 9220) it enables functions like multi-picture, tuner scanning, picture-in-still and still-in-picture. The different modes can be activated by a microcontroller on the I²C-Bus interface (slave receiver). The I²C-Bus address for accessing the device is

0	0	1	0	1	0	1	0

Circuit Description

The core of the picture processor (**see block diagram**) is formed of the Image-Improving Processor (IIP) and the Multi-Picture Processor (MPP). The IIP is responsible for noise and cross-color reduction, while the MPP together with the new Memory Sync Controller implements the functions multi-picture, tuner scanning, picture-in-still and still-in-picture.

Image-Improving Processor

The signal inputs YI0-YI7 and UVI0-UVI7 and the back-channel signal inputs YB0-YB7 and UVB0-UVB7 picture data with 12 bits in quasi-parallel format (4:1:1) and with 16 bits in parallel format (4:2:2). The clock rate for both signals is 13.5 MHz. For signal processing in the IIP and MPP the chrominance bit levels have to be separated in the case of the quasi parallel format by demultiplexers DEMUXS and DEMUXR, these being largely identical in design.

A reduction in video noise is achieved by correlating the picture contents of two successive fields, the non-correlated components (noise) being attenuated by the digital filter. To achieve this, the instantaneous digital picture signal on the outputs of the demultiplexer DEMUXS and the picture signal delayed by a field interval on the outputs of the back-channel demultiplexer DEMUXR are fed to the IIP and combined.

The signal-to-noise ratio (S/N) unit detects the noise components of the input signals and the movement detector uses this information to select an appropriate set of parameters with filter coefficients and thresholds for the comparators. For this purpose the luminance signal is assigned to one of three classes according to its S/N ratio, with each class defining a different degree of maximum noise reduction. The limits between the middle class and the upper and lower classes can be programmed by the I²C-Bus registers R1 and R2 with the values for the thresholds SU and SL. When the picture signals come from a video cassette recorder, the adaptation on the S/N ratio of the input signal should be disabled by I²L-Bus register R0, VCR bit D2.

Measurement of the signal-to-noise ratio in the automatic mode has been advanced from line 6 to line 4 in order to avoid conflicts with future text and data services.

The degree of noise reduction for the luminance and chrominance signals can be varied between 0 dB and 12 dB by selecting the appropriate filter coefficients.

A picture signal with reduced noise and cross-color appears on the output of the IIP for further processing. The signal will be forwarded via blocks MUXI and MUXO to the picture memories through the outputs (YQ0-YQ7 and UVQO-UVQ7 respectively).

The coefficients of the selected class are controlled by the movement detector as a function of pixels to prevent artifacts (loss of focus) in moving parts of the picture. The video line for S/N measurement can be programmed by the I²C-Bus register R2 (D7-D5).

Multi-Picture Processor

Signals are processed in the 4:1:1 format. The vertical-decimation line memory again operates with 208 pixels per line to adapt the 1/9th picture format to the new picture memory with TV-SAMs. Gray frame generation is similarly affected by this change in pixel value.

The signal processing in the decimation filter of the MPP reduces the picture to approximately 1/9th of its original size. This produces a basis for new features, the full implementation of which calls for a matching MSC (SDA 9220).

Figure 8 shows how the screen is divided up. The following modes can be implemented with the MPP:

1. Multi-Picture (automatic)
   Fields are extracted from a sequence of movements at fixed intervals, reduced and reproduced on the screen as a sequence of stills. At one position it is possible to show a moving picture.
2. Multi-Picture (manual)
   This differs from the above in that the viewer can determine at the push of a button what phases of movement are to be stored.
3. Multi-Picture (tuner scanning)
   The pictures of the sequence of stills are derived from the different TV channels and give an overview of the programs on offer. In this mode the picture memory is operated with a crystal-controlled clock to ensure that the picture remains stable when switching from one channel to another.
4. Still-in-Picture
   A field is extracted from the on-going program, reduced and inserted as a still in the master channel.
5. Picture-in-Still
   The on-going program is inserted as a reduced-size moving picture in a still.

The framing block that follows the decimation filter in the MPP permits frames to be inserted in order to border the reduced-size pictures on the screen. The brightness of the framing can be varied in eight steps by the I²C Bus.

The format conversion produced in the demultiplexers for signal processing in the IIP and MPP is reversed again in the multiplexer MUXO. The picture signal appears again in quasi-parallel format or parallel format on the output of the MUXO block. The inputs of the TV-SAMs are directly driven by the sixteen outputs YQ0-YQ7 and UVQ0-UVQ7.

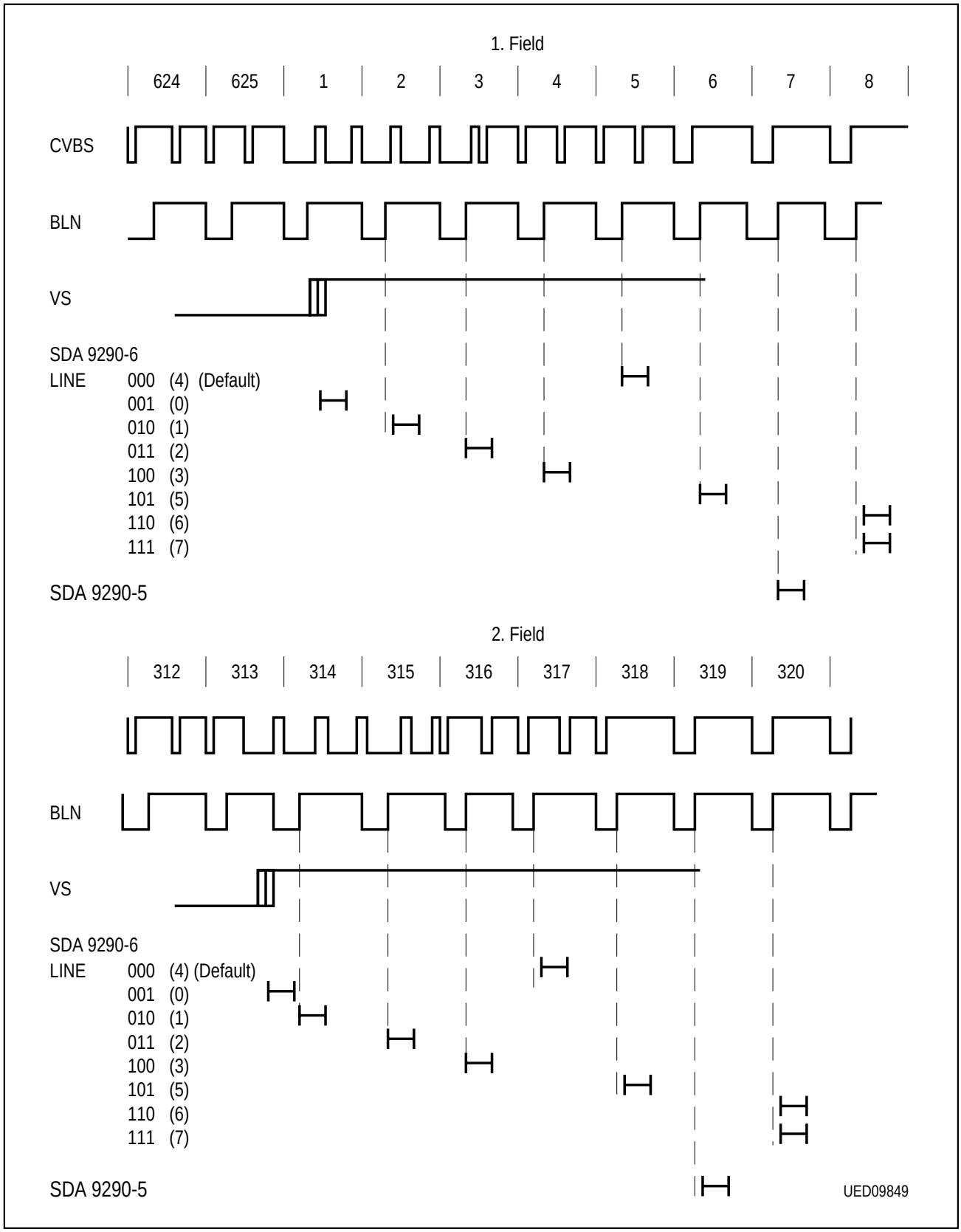
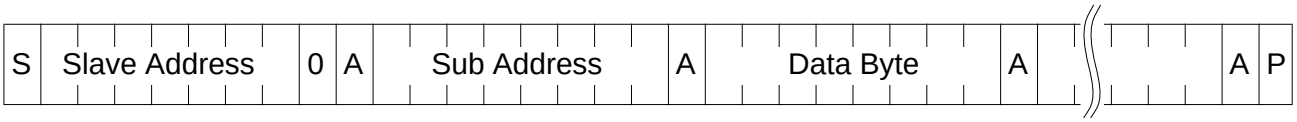


Figure 1
Programmable Video Lines

I²C Bus Interface

An I²C Bus interface configured as a “slave receiver” is used for programming the different functions and modes of the picture processor. Via this interface up to four registers can be written according to the following transfer protocol for controlling the operation mode:



S: Start condition
A: Acknowledge
P: Stop condition
Slave address: 0 0 1 0 1 0 1

(**Note:** There is a general description of the I²C Bus in the Siemens publication “I²C Bus Technical Description”.)

After every data byte that is transmitted the internal register address (subaddress) is automatically incremented to the next register so that, if necessary, several registers can be loaded with one I²C Bus telegram.

In the multi-picture mode the operating mode transmitted on the I²C Bus is switched within the vertical blanking interval, i.e. during the high phase of signal VS1, if the Memory Sync Controller (MSC) activates the DREQ line during this period.

It should be noted that the new operating mode has always to be transmitted to the picture processor first and immediately afterwards to the MSC on the I²C Bus at an interval not longer than 30 ms.

This is the only way to ensure interference-free synchronization of the picture processor and the MSC. The four I²C Bus registers are described below in more detail. The values marked “*D” in the right-hand margin are set by an internally generated reset signal (default values) when the operating voltage is applied.

Register	**Sub-address[1)]**	**Data Byte**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R0	00	B1	B0	FR	0	SS	VCR	NR	SUV8
R1	01	YF5	YF4	YF3	SL4	SL3	SL2	SL1	SL0
R2	02	LINE2	LINE1	LINE0	SU4	SU3	SU2	SU1	SU0
R3	03	SNTEN	SNT1	SNT0	KTEN	KT3	KT2	KT1	KT0

Register R0: This control register sets the operating mode of the picture processor.

Bits D7, D6:

Mode	**B1**	**B0**	
Normal	0	0	*D
Multi-picture (MP)	0	1	
Still-in-picture (SIP)	1	0	
Picture-in still (PIS)	1	1	

Bit D5:

MPP: Narrow Frame	FR		
Without narrow frame	0		*D
With narrow frame	1		

Bit D4: No function; default 0

Bit D3:

Display Mode	SS	
Full screen	0	*D
Split screen	1	

Specialities

Split Screen Display

For demonstration purposes the noise reduction can be disabled for half of the picture by means of I²C-Bus register R0, bit D3. In this way a direct comparison is possible between a noise-reduced (filtered) and an unfiltered picture.

Bit D2:

Control of SNR adaptation	VCR	
TV mode	0	*D
VCR mode	1	

Bit D1:

Noise reduction ON/OFF	NR	
Noise reduction OFF	0	*D
Noise reduction ON	1	

Bit D0:

Word width input	SUV8	
7 bits	0	*D
8 bits	1	

Register R1: This control register sets the frame luminance for multi-picture and the threshold SL for S/N adaptation.

Bits D7-D5:

Frame Luminance YF		**YF5**	**YF4**	**YF3**	
0	black	0	0	0	*D
:	:	:	:	:	
:	:	:	:	:	
:	:	:	:	:	
7	white	1	1	1	

Bits D4-D0:

Threshold SL (S/N adaptation)	**SL4**	**SL3**	**SL2**	**SL1**	**SL0**	
0	0	0	0	0	0	
:	:	:	:	:	:	
:	:	:	:	:	:	
4	0	0	1	0	0	*D
:	:	:	:	:	:	
:	:	:	:	:	:	
31	1	1	1		1	

Register R2: This control register sets the threshold SU for S/N adaptation, and the values for the line counter.

Noise Measurement: Decoded Values of the Line Counter

Bits D7-D5:

LINE2	**LINE1**	**LINE0**	**Decoded Value**	
0	0	0	4	*D
0	0	1	0	
0	1	0	1	
0	1	1	2	
1	0	0	3	
1	0	1	5	
1	1	0	7	

Bits D4-D0:

Threshold SU (S/N adaptation)	**SU4**	**SU3**	**SU2**	**SU1**	**SU0**	
0	0	0	0	0	0	
: :	: :	: :	: :	: :	: :	
16	1	0	0	0	0	*D
: :	: :	: :	: :	: :	: :	
31	1	1	1	1	1	

Register R3: This register is for testing. certain S/N classes and filter coefficients for the motion detector can be firmly set.

Bits D7-D5:

S/N Class	**SNTEN**	**SNT1**	**SNT0**	
Automatic adaptation	0	X	X	*D
Class 0	1	0	0	
Class 1	1	0	1	
Class 2	1	1	0	

Bits D4-D0:

Filter Coefficient	**KTEN**	**KT3**	**KT2**	**KT1**	**KT0**	
Motion detector ON	0	X	X	X	X	*D
K = 1	1	0	0	0	0	
K = 3/4	1	0	0	0	1	
K = 5/8	1	0	0	1	0	
K = 9/16	1	0	0	1	1	
K = 3/4	1	0	1	0	0	
K = 1/2	1	0	1	0	1	
K = 3/8	1	0	1	1	0	
K = 5/16	1	0	1	1	1	
K = 5/8	1	1	0	0	0	
K = 3/8	1	1	0	0	1	
K = 1/4	1	1	0	1	0	
K = 3/16	1	1	0	1	1	
K = 9/16	1	1	1	0	0	
K = 5/16	1	1	1	0	1	
K = 3/16	1	1	1	1	0	
K = 1/8	1	1	1	1	1	

Note: X is ignored.
**D = Default values after reset.*

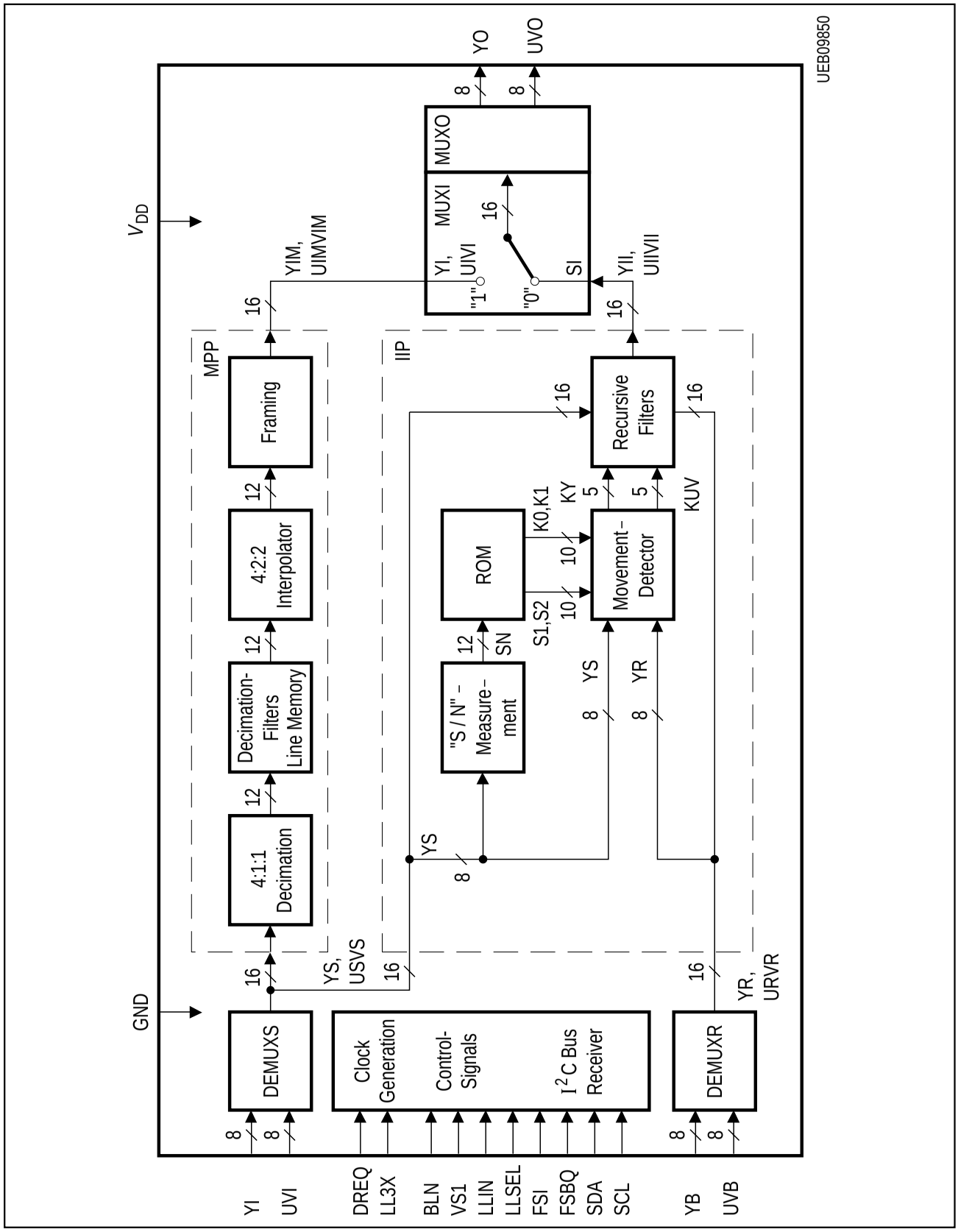


Figure 2
Block Diagram

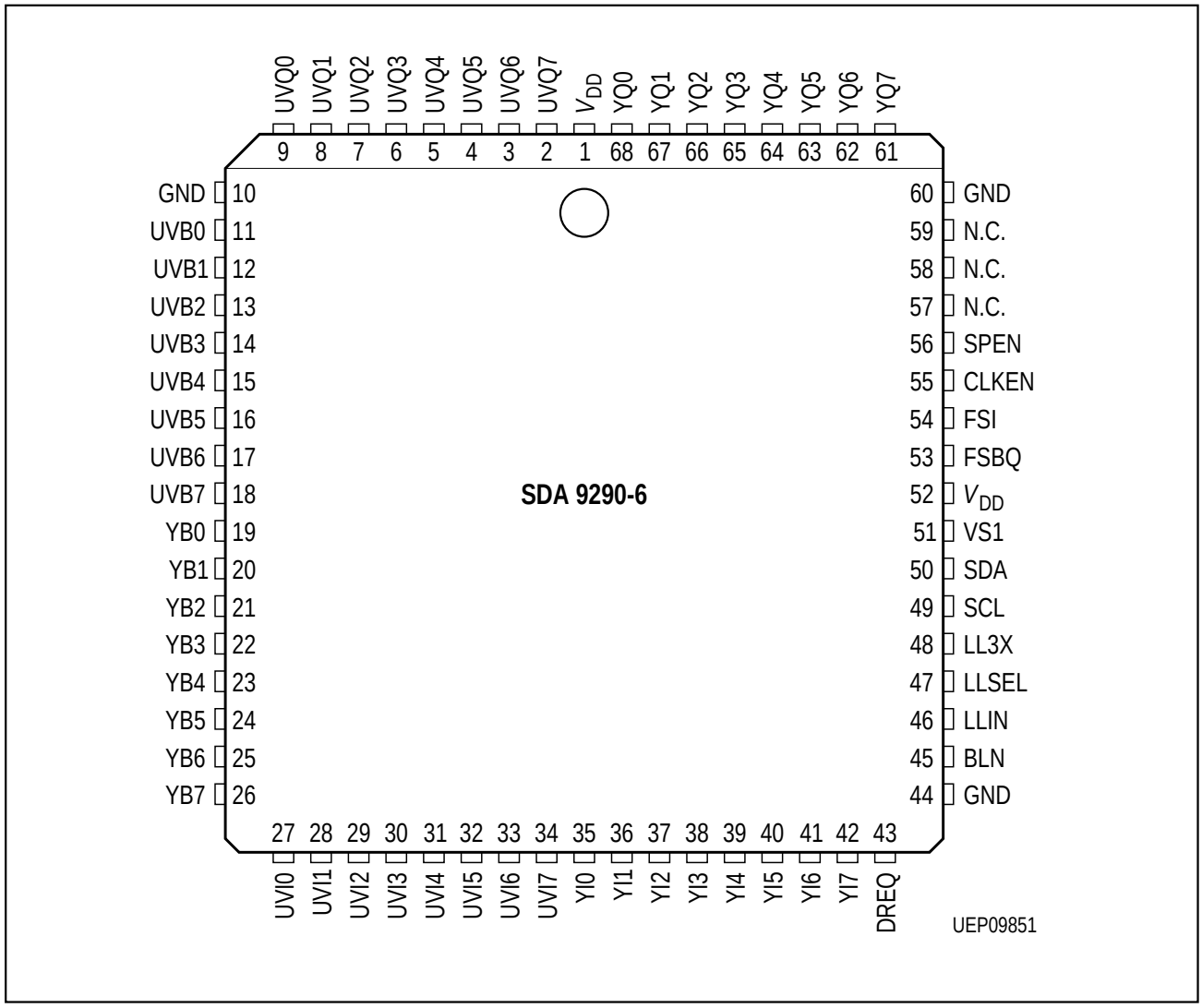


Figure 3
Pin Configuration (top view)

Pin Definitions and Functions

Pin No.	Symbol	Function	Description
1	V_{DD}	Positive supply voltage (+ 5 V)	Positive supply voltage (+ 5 V)
2-9	UVQ7 … UVQ0	Data outputs	Push-pull outputs for directly driving the TV-SAM chrominance inputs: 8 bits for 4:2:2 format; 4 bits for 4:1:1 format; [UVQ0 … UVQ3 only valid for 4:2:2 format]
10	GND	Ground	Ground (0 V)
11-18	UVB0 … UVB7	Back-channel data outputs	Back-channel inputs for chrominance data from TV-SAM
19-26	YB0 … YB7	Back- channel data inputs	Back-channel inputs for luminance data from TV-SAM
27-34	UVI0 … UVI7	Data inputs	Data inputs for chrominance data accept the dig. YUV signal
35-42	YI0 … YI7	Data inputs	Data inputs for luminance data accept the dig. YUV signal
43	DREQ	Data request signal for multi-picture mode	Data-request input; initiates data transfer in multi-picture mode and switches mode together with signal VS1
44	GND	Ground	Ground (0 V)
45	BLN	Blanking signal (15.625 kHz)	Input for line-synchronous blanking signal that determines line blanking interval (active low) and synchronizes clock and sequence control
46	LLIN	First system clock (13.5 MHz)	Input for line-locked system clock, 13.5 MHz, from which internal timing is derived. Positive edge indicates validity of input data
47	LLSEL	none	Must be connected to V_{DD} (high-level)
48	LL3X	Second system clock (13.5 MHz)	Input for line-locked 13.5-MHz clock that ensured picture stability in multi-picture mode and is used as output clock in every mode
49	SCL	I²C Bus shift clock input	I²C-Bus shift-clock input
50	SDA	I²C Bus data input/output	I²C-Bus data input/output
51	VS1	Vertical sync input (50 Hz)	Vertical sync input; determines vertical position of TV picture for 50-Hz or 60-Hz field frequency
52	V_{DD}	Positive supply voltage (+ 5 V)	Positive supply voltage (+ 5 V)

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Function	Description
53	FSBQ	Selection of output format	Switching of data output format: Low level for 4:1:1 format; high level for 4:2:2 format
54	FSI	Selection of input format	Switching of data input format: Low level for 4:1:1 format; high level for 4:2:2 format
55	CLKEN	Connect test pin 2	Has to be grounded (0 V) in normal mode
56	SPEN	Connect test pin 2	Has to be grounded (0 V) in normal mode
57-59	N.C.	Reserved	No connections possible or meaningful
60	GND	Ground	Ground (0 V)
61-68	YQ7 … YQ0	Data outputs	Push-pull outputs for directly driving TV-SAM inputs for 4:1:1 and 4:2:2 modes; (8-bit luminance)

Electrical Characteristics

Absolute Maximum Ratings

(all voltages are referred to GND)

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Ambient temperature	T_A	0	70	°C	
Storage temperature	T_{stg}	– 40	125	°C	
Total power dissipation	P_{tot}		1	W	
Supply voltage	V_{DD}	– 0.3	6	V	
Input/output voltage	$V_{I/Q}$	– 0.3	6	V	
Thermal resistance system-air	$R_{th\ SA}$		38	K/W	with heat sink

Operating Range

Supply voltage	V_{DD}	4.5	5.5	V	
Supply current	I_{DD}		180	mA	
Ambient temperature	T_A	0	70	°C	

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Note: In the operating range the functions given in the circuit description are fulfilled.

Characteristics

(all voltages are referred to GND)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
H-input voltage [1]	V_{IH}	2.0		5.5	V	
L-input voltage [1]	V_{IL}	0		0.8	V	
Input current [1]	I_{IR}			10	µA	
Input capacitance [1] (except BLN, LLIN)	C_I			10	pF	
Input capacitance [1] (only BLN, LLIN)	C_I			5	pF	
H-input voltage [2]	V_{IH}	3.0		5.5	V	
L-input voltage [2]	V_{IL}	0		0.8	V	
Input capacitance [2]	C_I			10	pF	
Input current [2]	I_{IM}			10	µA	
H-output voltage [3]	V_{QH}	2.4			V	I_{QH} = – 2.0 mA
L-output voltage [3]	V_{QL}			0.4	V	I_{QH} = 3.0 mA
L-output voltage [4]	V_{QL}			0.4	V	I_{QH} = 3.0 mA
Permissible output voltage [4]	V_{QM}			5.5	V	

[1] Input signals UVI0 … UVI7, YI0 … YI7, UVB0 … UVB7, YB0 … YB7, BLN, LLSEL, FSI, FSBQ, LLIN, LL3X, DREQ, VS1

[2] Input signals SDA, SCL (**refer to figure 6**)

[3] Output signals YQ0-YQ7, UVQ0-UVQ7

[4] Output signal SDA (open drain)

Characteristics (cont'd)
(all voltages are referred to GND)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input Clock LL3X = 13.5 MHz (refer to figure 6)						
Cycle	T_{LLL3X}	68	74	80	ns	
Fall time	t_{THL}			5	ns	
Rise time	t_{THL}			5	ns	
H-pulse width	t_{WH}	25			ns	
L-pulse width	t_{WL}	25			ns	
Change in rel to LLIN	t_{SK}	0		15	ns	
Input Clock LLIN (refer to figure 6)						
Cycle	T_{LLIN}	68	74	80	ns	LLSEL = high
H-pulse width	t_{WH}	25			ns	LLSEL = high
L-pulse width	t_{WL}	25			ns	LLSEL = high
Fall time	t_{THL}			5	ns	
Rise time	t_{THL}	2		5	ns	
Input Clock BLN (refer to figure 5)						
Setup time	t_{SU}	15			ns	LLSEL = high
Hold time	t_{IH}	5			ns	LLSEL = high
H-pulse width	t_{WH}		720		T_{LL3X}	
Cycle, 625 lines	T_{BLN}		864		T_{LL3X}	
Cycle, 525 lines	T_{BLN}		858		T_{LL3X}	

Characteristics (cont'd)
(all voltages are referred to GND)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input Signal VS1						
Setup time	t_{SU}	15			ns	Reference LL3X
Hold time	t_{IH}	5			ns	Reference LL3X
Cycle, 625 lines	T_{VS1}		312.5		T_{BLN}	
Cycle, 525 lines	T_{VS1}		262.5		T_{BLN}	
H-pulse width, 625 lines	t_{WH}			26.5	T_{BLN}	
H-pulse width, 525 lines	t_{WH}			16.5	T_{BLN}	
Input Signal DREQ						
Setup time	t_{SU}	15			ns	Reference LL3X
Hold time	t_{IH}	5			ns	Reference LL3X
H-pulse width	t_{WH}	1		16	T_{LL3X}	
Input Signal (Data) YI0 … YI7, UVI0 … UVI7, YB0 … YB7, UVB0 … UVB7 (refer to figure 5)						
Setup time	t_{SU}	15			ns	Reference LL3X
Hold time	t_{IH}	5			ns	Reference LL3X
Setup time	t_{SU}	15			ns	Reference LLIN
Hold time	t_{IH}	5			ns	Reference LLIN

Characteristics (cont'd)
(all voltages are referred to GND)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output Signal (Data) YQ0 … YQ7, UVQ0 … UVQ7 (refer to figure 5)						
Hold time	t_{QH}	6			ns	Reference LL3X
Delay time	t_{QD}			50	ns	Reference LL3X C_L = 30 pF

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

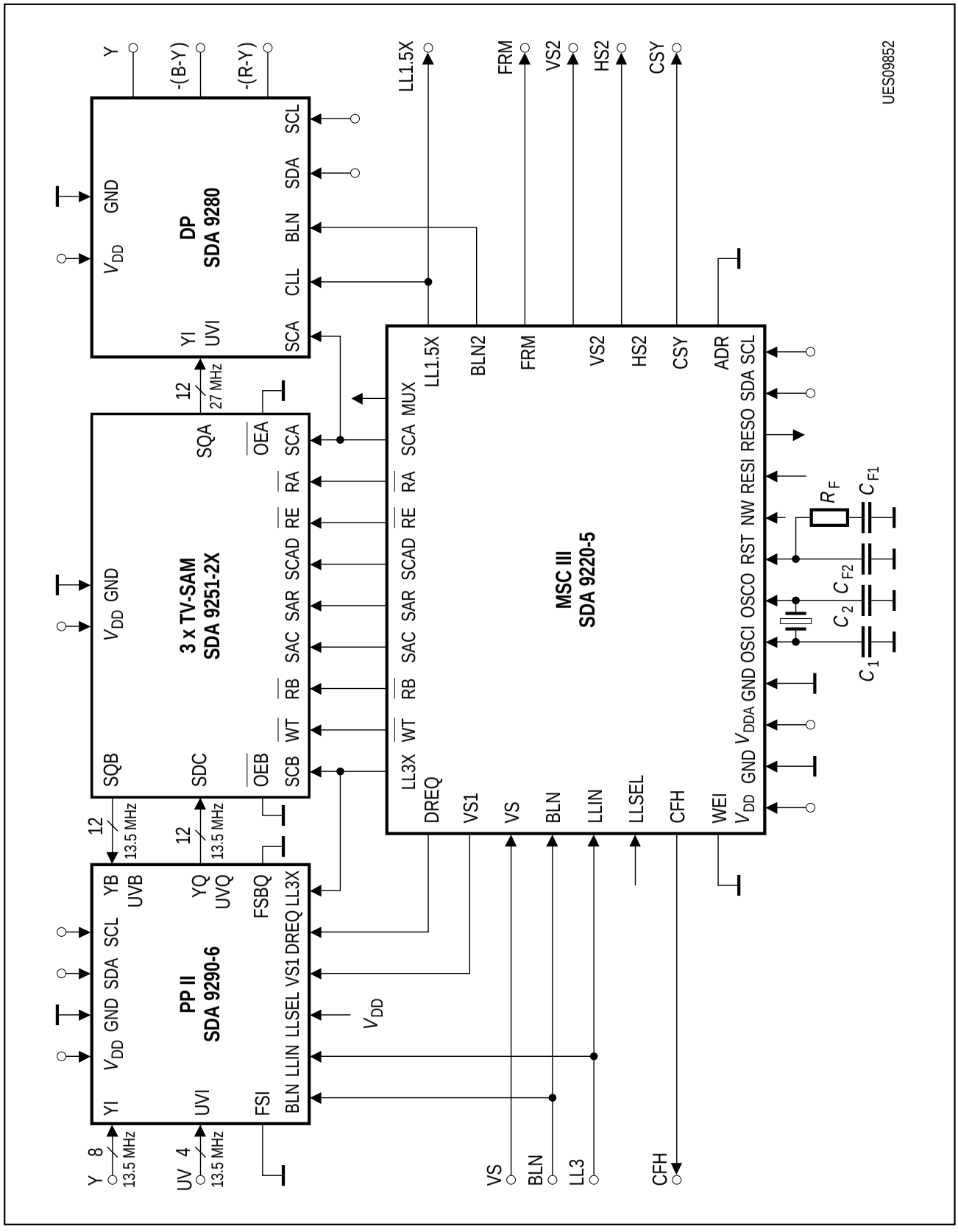


Figure 4
Application Circuit (simplified)

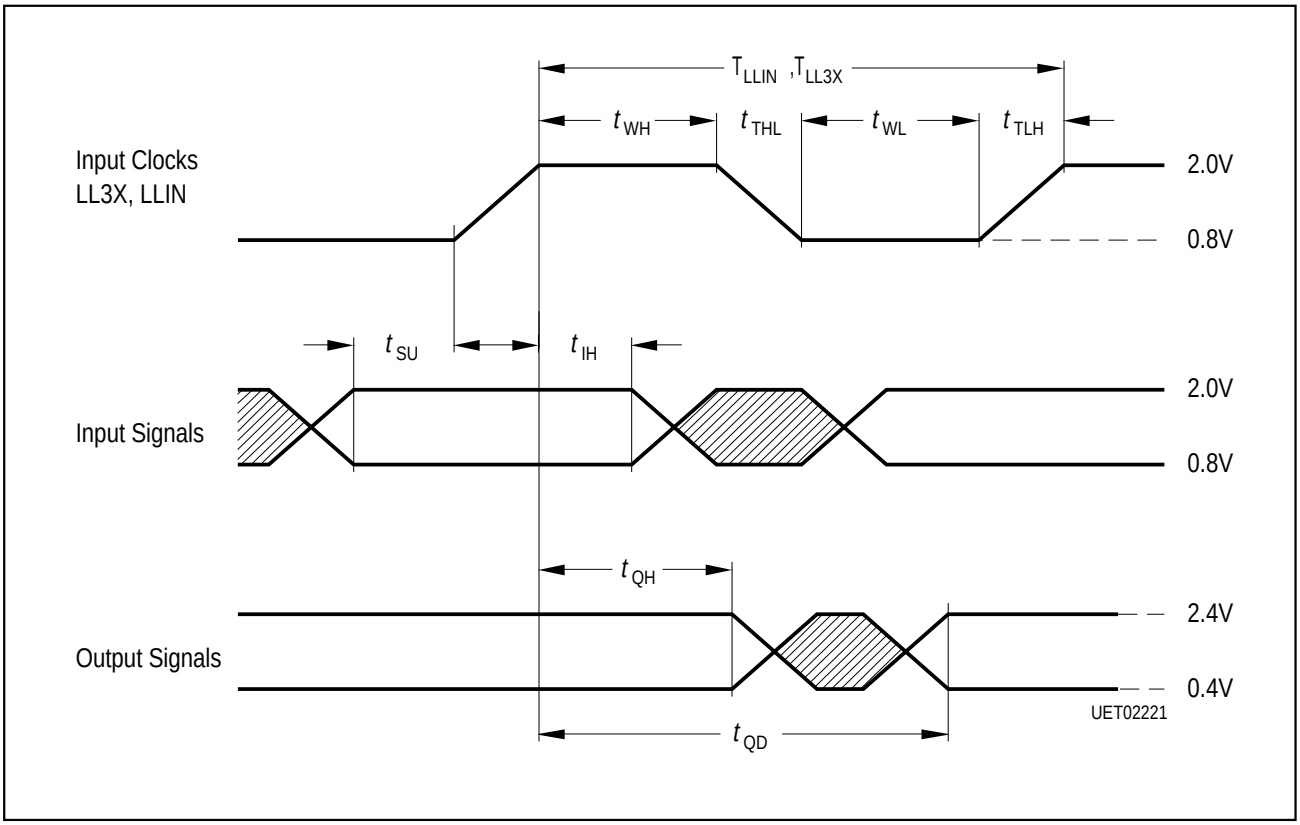


Figure 5
Timing Diagram

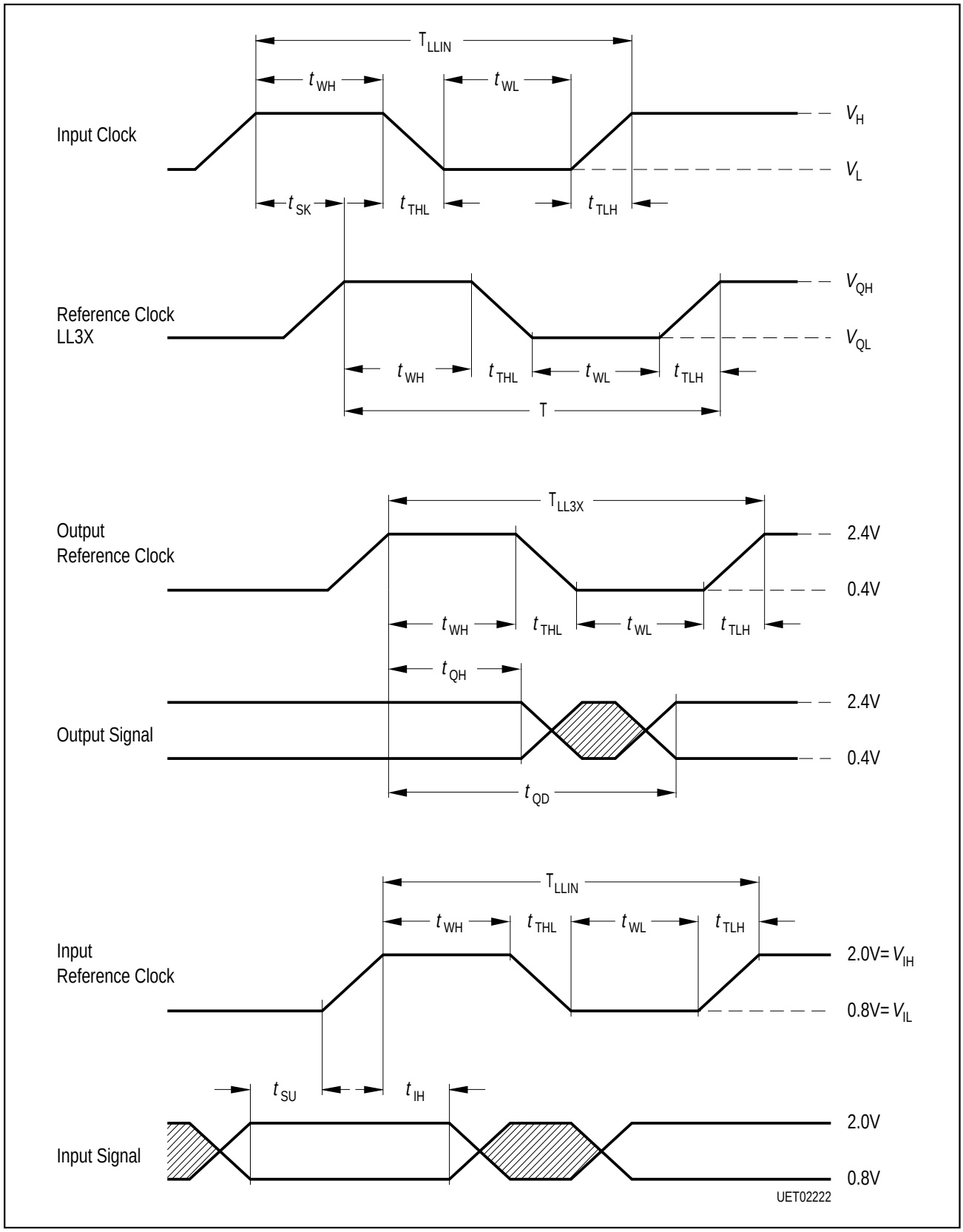


Figure 6
Timing Diagram

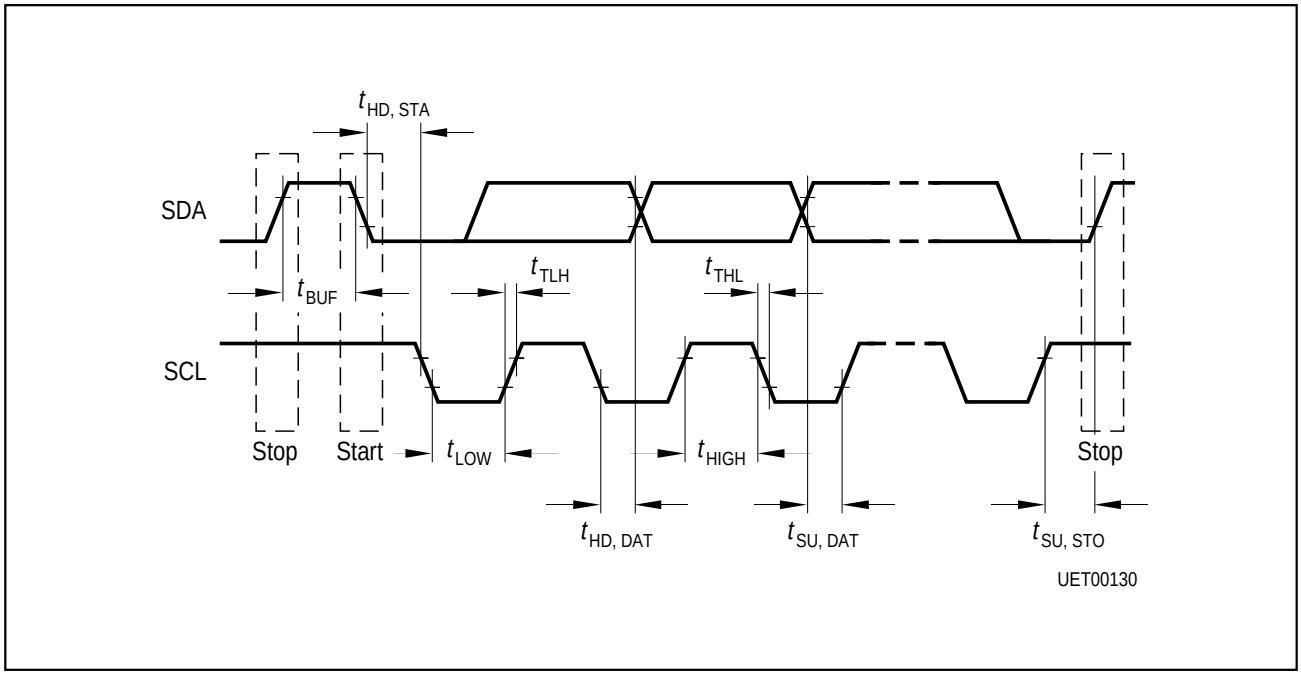


Figure 7
Timing for I²C Bus

Table 1

All values are referred to specified input levels V_{IH} and V_{IL}.

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Clock frequency	f_{SCL}	0	100	kHz
Inactive time before start of new transmission	t_{BUF}	4.7		µs
Hold time for start condition (after this time first clock pulse is generated)	$t_{HD; STA}$	4.0		µs
Low clock phase	t_{LOW}	4.7		µs
High clock phase	t_{HIGH}	4.0		µs
Setup time for data	$t_{SU; DAT}$	250		ns
Rise time for SDA and SCL signals	t_{TLH}		1	µs
Fall time for SDA and SCL signals	t_{THL}		300	ns
Setup time for SCL clock in stop condition	$t_{SU; STO}$	4.7		µs

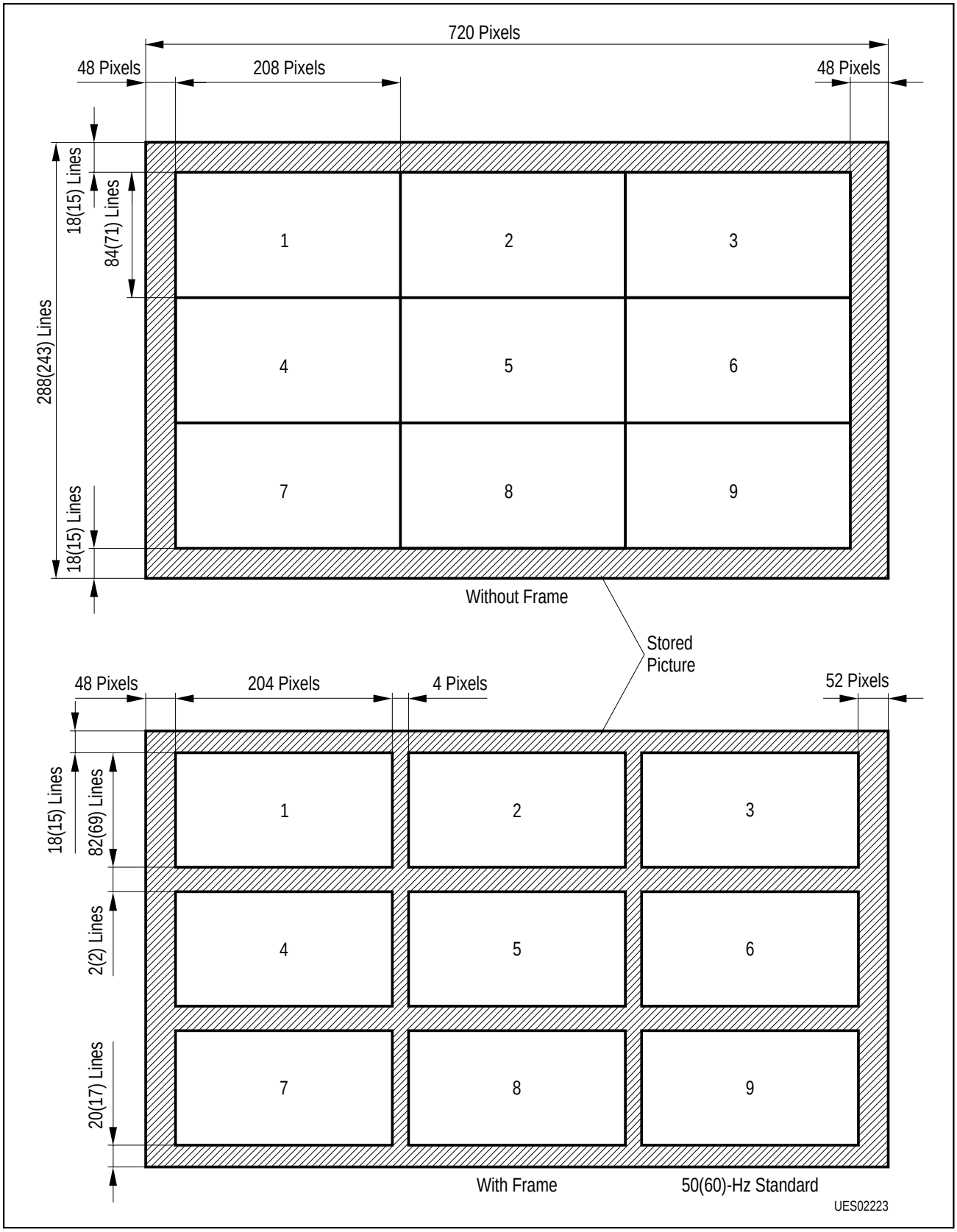


Figure 8
Picture Formats for 9-Image Display

Table 2
Assignment of Signal and Pin Names

Format 4:1:1

Y:7-Bit Signal	Y:8-Bit Signal	Picture Processor		
		Input	Back Channel Input	Output
Y6	Y7	YI7	YB7	YQ7
Y5	Y6	YI6	YB6	YQ6
Y4	Y5	YI5	YB5	YQ5
Y3	Y4	YI4	YB4	YQ4
Y2	Y3	YI3	YB3	YQ3
Y1	Y2	YI2	YB2	YQ2
Y0	Y1	YI1	YB1	YQ1
–	Y0	YI0	YB0	YQ0
U6 U4 U2 U0	U7 U5 U3 U1	UVI7	UVB7	UVQ7
U5 U3 U1	U6 U4 U2 U0	UVI6	UVB6	UVQ6
V6 V4 V2 V0	V7 V5 V3 V1	UVI5	UVB5	UVQ5
V5 V3 V1	V6 V4 V2 V0	UVI4	UVB4	UVQ4

Y: Luminance Signal
U: Chrominance Signal
V: Chrominance Signal

Table 3
Assignment of Signal and Pin Names

Format 4:2:2

Signal	Picture Processor		
	Input	Back Channel Input	Output
Y7	YI7	YB7	YQ7
Y6	YI6	YB6	YQ6
Y5	YI5	YB5	YQ5
Y4	YI4	YB4	YQ4
Y3	YI3	YB3	YQ3
Y2	YI2	YB2	YQ2
Y1	YI1	YB1	YQ1
Y0	YI0	YB0	YQ0
UV7	UVI7	UVB7	UVQ7
UV6	UVI6	UVB6	UVQ6
UV5	UVI5	UVB5	UVQ5
UV4	UVI4	UVB4	UVQ4
UV3	UVI3	UVB3	UVQ3
UV2	UVI2	UVB2	UVQ2
UV1	UVI1	UVB1	UVQ1
UV0	UVI0	UVB0	UVQ0

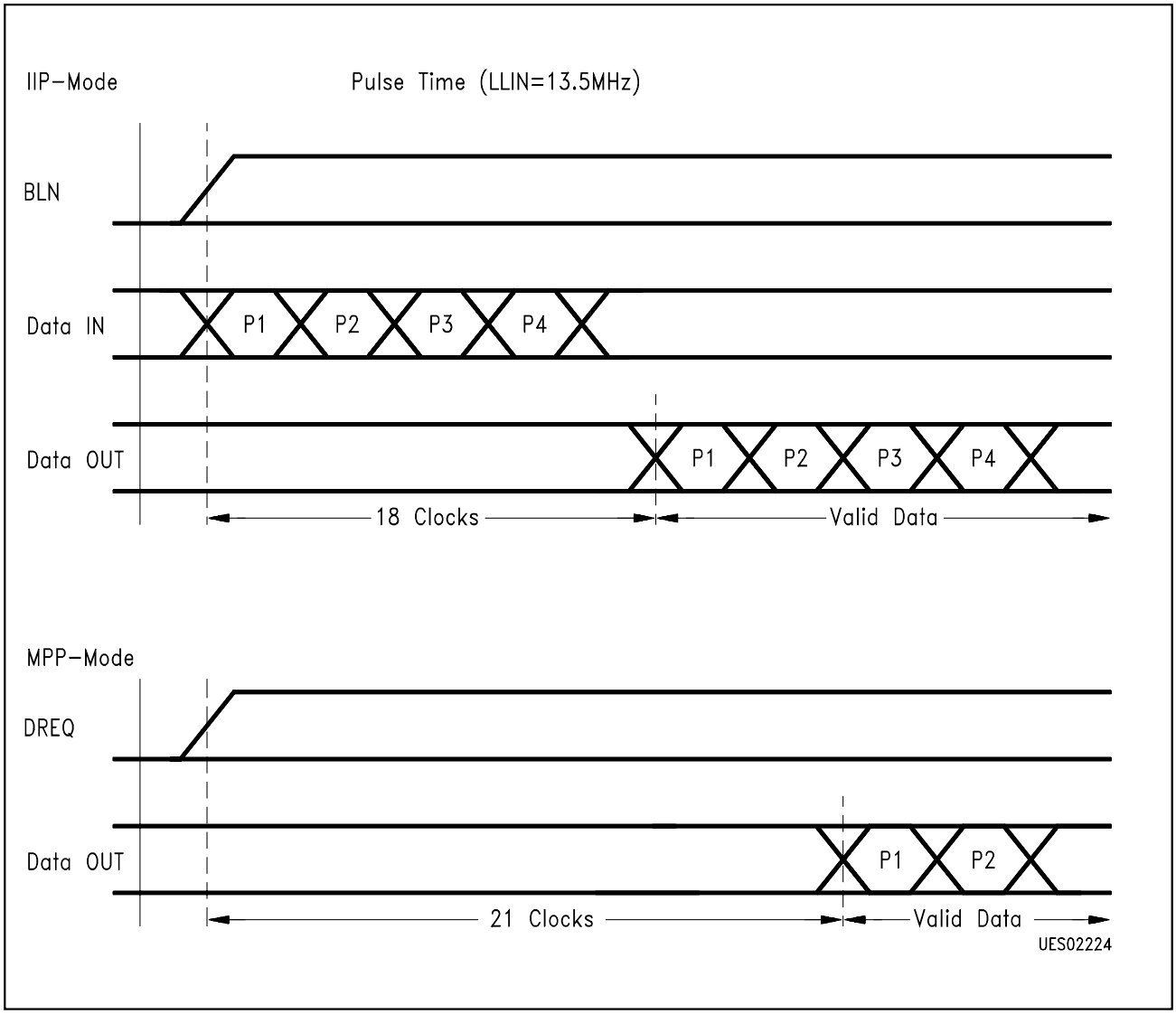
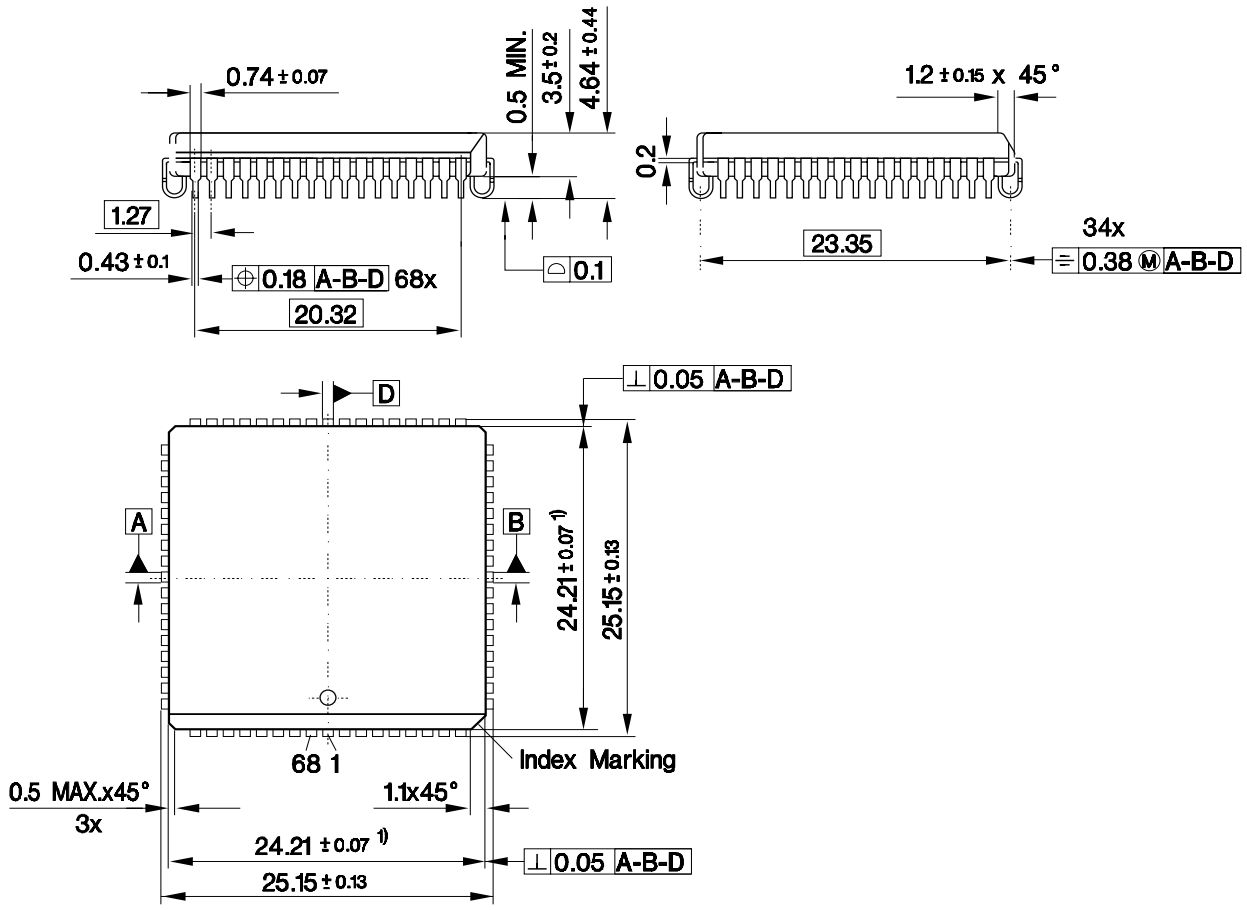


Figure 9
Output Data Delay Times

Package Outlines

P-LCC-68-1 (SMD)
(Plastic Leaded Chip Carrier)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm