SIEMENS

Microcomputer Components

8-Bit CMOS Microcontroller

C501

Data Sheet 04.97

C501 Data Sheet **Revision History :**		1997-04-01
Previous Releases :		11.92, 11.93, 08.94, 08.95, 10.96
Page (previous version)	Page (new version)	Subjects (changes since last revision)
general		C501G-1E OTP version included
4	4	Ordering information resorted and C501G-1E types added
5	5	Table with literature hints added
5-7	5-7	Pin configuration logic symbol for pins $\overline{EA}$/Vpp and ALE/$\overline{PROG}$ updated
11	11	Pin description for ALE/$\overline{PROG}$ and $\overline{EA}$/Vpp completed
8, 9, 10	8, 9, 10	Port 1, 3, 2 pin description: “bidirectional” replaced by “quasi-bidirectional”
13	13	Block diagram updated for C501G-1E
14	14	New design of register (PSW) description
-	15	“Memory organization” added
15-18	16-18	Actualized design of the SFR tables
17	17	Reset value of T2CON corrected
-	25-28	Description for the C501-1E OTP version added
-	31	DC characteristics for C501-1E added
41	41	Timing “External Clock Drive” now behind “Data Memory Cycle”
-	43, 44	AC characteristics for C501-1E added

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8-Bit CMOS Microcontroller C501

Preliminary

- Fully compatible to standard 8051 microcontroller
- Versions for 12/24/40 MHz operating frequency
- Program memory : completely external (C501-L)
  8K × 8 ROM (C501-1R)
  8K × 8 OTP memory (C501-1E)
- 256 × 8 RAM
- Four 8-bit ports
- Three 16-bit timers / counters (timer 2 with up/down counter feature)
- USART
- Six interrupt sources, two priority levels
- Power saving modes
- Quick Pulse programming algorithm (C501-1E only)
- 2-Level program memory lock (C501-1E only)
- P-DIP-40, P-LCC-44, and P-MQFP-44 package
- Temperature ranges : SAB-C501 T_A : 0 °C to 70 °C
  SAF-C501 T_A : – 40 °C to 85 °C

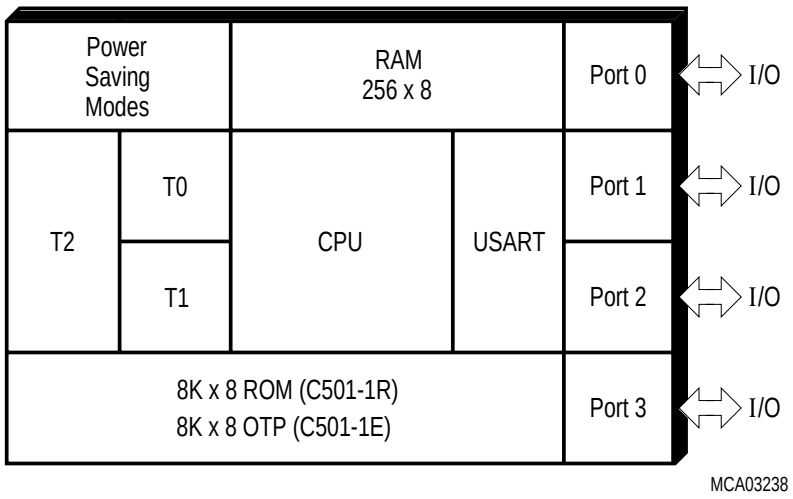


Figure 1
C501G Functional Units

The C501-1R contains a non-volatile 8K × 8 read-only program memory, a volatile 256 × 8 read/ write data memory, four ports, three 16-bit timers counters, a seven source, two priority level interrupt structure and a serial port. The C501-L is identical, except that it lacks the program memory on chip. The C501-1E contains a one-time programmable (OTP) program memory on chip. The term C501 refers to all versions within this specification unless otherwise noted. Further, the term C501 refers to all versions which are available in the different temperature ranges, marked with SAB-C501... or SAF-C501.... .

Ordering Information

Type	Ordering Code	Package	Description (8-Bit CMOS microcontroller)
SAB-C501G-LN SAB-C501G-LP SAB-C501G-LM	Q67120-C969 Q67120-C968 Q67127-C970	P-LCC-44 P-DIP-40 P-MQFP-44	for external memory (12 MHz)
SAB-C501G-L24N SAB-C501G-L24P SAB-C501G-L24M	Q67120-C1001 Q67120-C999 Q67127-C1014	P-LCC-44 P-DIP-40 P-MQFP-44	for external memory (24 MHz)
SAB-C501G-L40N SAB-C501G-L40P SAB-C501G-L40M	Q67120-C1002 Q67120-C1000 Q67127-C1009	P-LCC-44 P-DIP-40 P-MQFP-44	for external memory (40 MHz)
SAF-C501G-L24N SAF-C501G-L24P	Q67120-C1011 Q67120-C1010	P-LCC-44 P-MQFP-44	for external memory (24 MHz) ext. temp. – 40 ˚C to 85 ˚C
SAB-C501G-1RN SAB-C501G-1RP SAB-C501G-1RM	Q67120-DXXX Q67120-DXXX Q67127-DXXX	P-LCC-44 P-DIP-40 P-MQFP-44	with mask-programmable ROM (12 MHz)
SAB-C501G-1R24N SAB-C501G-1R24P SAB-C501G-1R24M	Q67120-DXXX Q67120-DXXX Q67127-DXXX	P-LCC-44 P-DIP-40 P-MQFP-44	with mask-programmable ROM (24 MHz)
SAB-C501G-1R40N SAB-C501G-1R40P SAB-C501G-1R40M	Q67120-DXXX Q67120-DXXX Q67127-DXXX	P-LCC-44 P-DIP-40 P-MQFP-44	with mask-programmable ROM (40 MHz)
SAF-C501G-1R24N SAF-C501G-1R24P	Q67120-DXXX Q67120-DXXX	P-LCC-44 P-DIP-40	with mask-programmable ROM (24 MHz) ext. temp. – 40 ˚C to 85 ˚C
SAB-C501G-1EN SAB-C501G-1EP	Q67120-C1054 Q67120-C1056	P-LCC-44 P-DIP-40	with OTP memory (12 MHz)
SAF-C501G-1EN SAF-C501G-1EP	Q67120-C2002 Q67120-C2003	P-LCC-44 P-DIP-40	with OTP memory (12 MHz)) ext. temp. – 40 ˚C to 85 ˚C
SAB-C501G-1E24N SAB-C501G-1E24P	Q67120-C2005 Q67120-C2006	P-LCC-44 P-DIP-40	with OTP memory (24 MHz)
SAF-C501G-1E24N SAF-C501G-1E24P	Q67120-C2008 Q67120-C2009	P-LCC-44 P-DIP-40	with OTP memory (24 MHz)) ext. temp. – 40 ˚C to 85 ˚C

Note: Versions for extended temperature range – 40 ˚C to 110 ˚C (SAH-C501G) on request. The ordering number of ROM types (DXXX extensions) is defined after program release (verification) of the customer.

Additional Literature

For further information about the C501 the following literature is available :

Title	Ordering Number
C501 8-Bit CMOS Microcontroller User's Manual	B158-H6723-X-X-7600
C500 Microcontroller Family Architecture and Instruction Set User's Manual	B158-H6987-X-X-7600
C500 Microcontroller Family - Pocket Guide	B158-H6986-X-X-7600

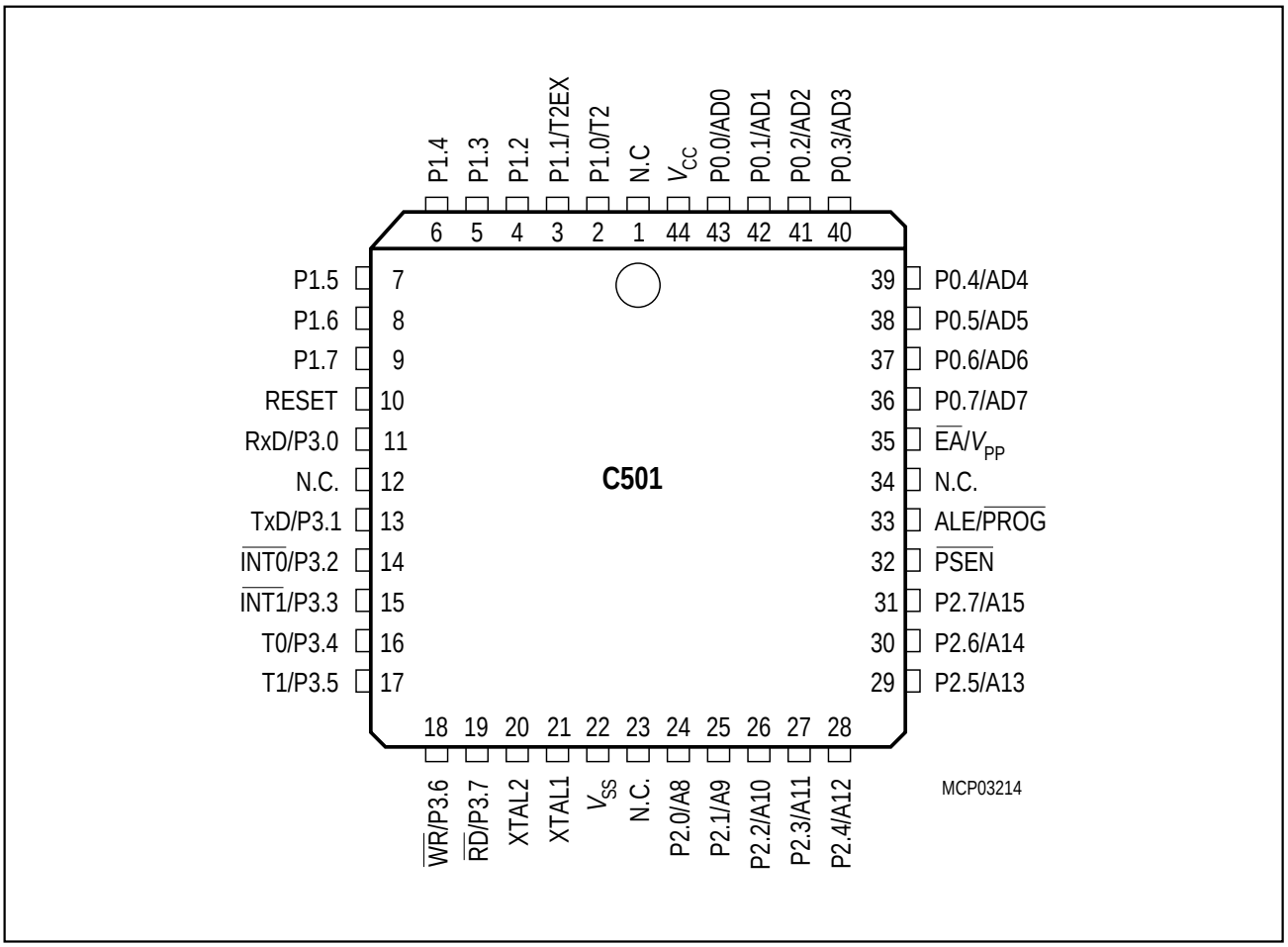


Figure 2
Pin Configuration P-LCC-44 Package (Top view)

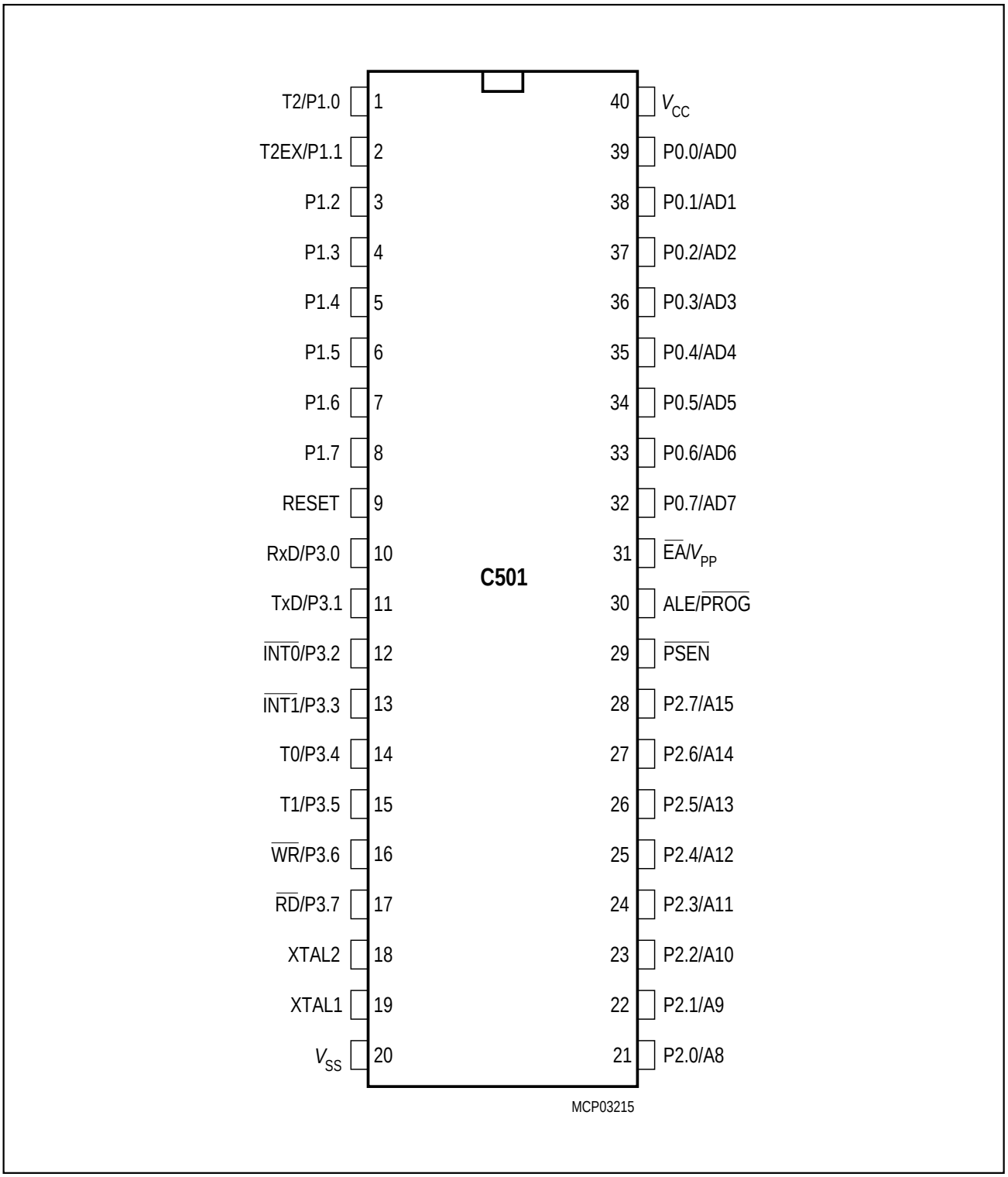


Figure 3
Pin Configuration P-DIP-40 Package (top view)

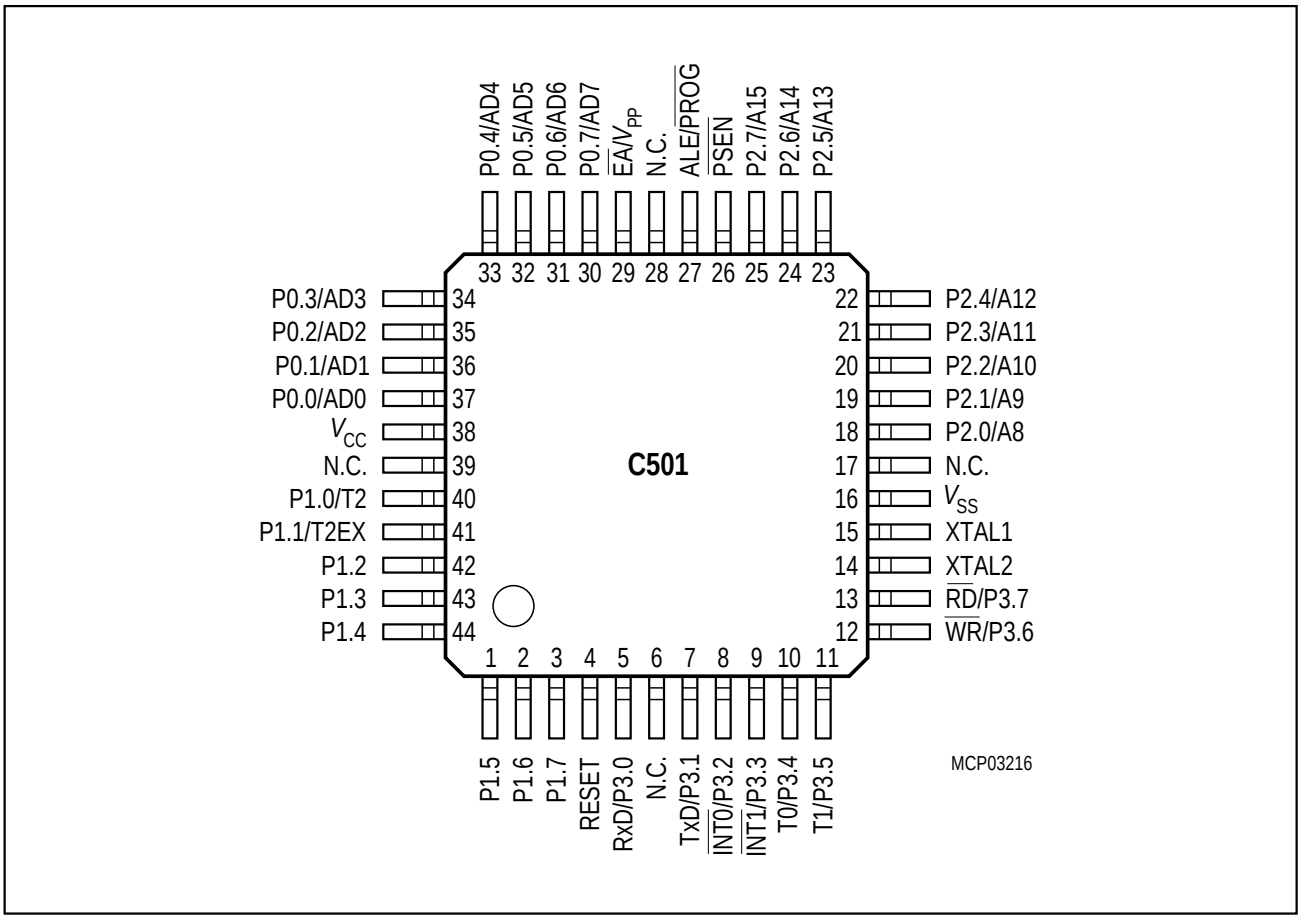


Figure 4
Pin Configuration P-MQFP-44 Package (top view)

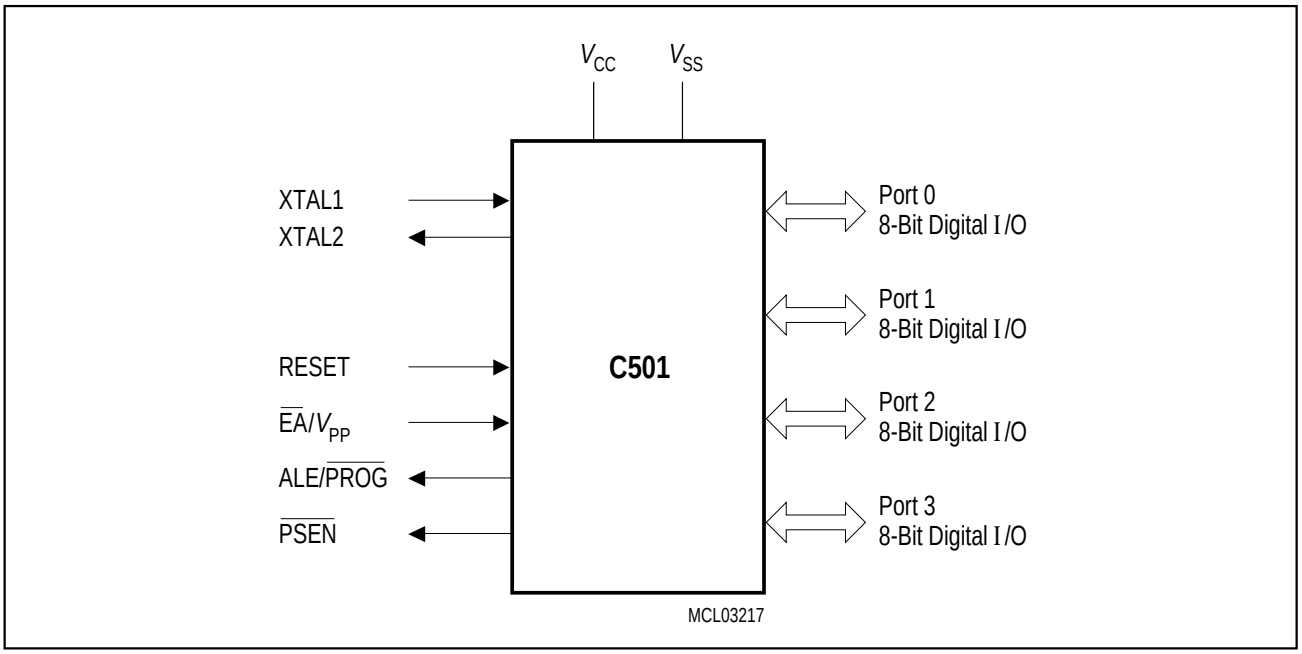


Figure 5
Logic Symbol

Table 1
Pin Definitions and Functions

Symbol	Pin Number			I/O*)	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
P1.0 – P1.7	2–9	1–8	40–44, 1–3,	I/O	**Port 1** is a quasi-bidirectional I/O port with internal pull-up resistors. Port 1 pins that have 1s written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 1 also contains the timer 2 pins as secondary function. The output latch corresponding to a secondary function must be pro-grammed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 1, as follows:
	2	1	40		P1.0 T2 Input to counter 2
	3	2	41		P1.1 T2EX Capture - Reload trigger of timer 2 / Up-Down count

*) I = Input
O = Output

Table 1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number			I/O*)	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
P3.0 – P3.7	11, 13–19	10–17	5, 7–13	I/O	**Port 3** is a quasi-bidirectional I/O port with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 3 also contains the interrupt, timer, serial port 0 and external memory strobe pins which are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows:
	11	10	5		P3.0 R×D receiver data input (asynchronous) or data input output (synchronous) of serial interface 0
	13	11	7		P3.1 T×D transmitter data output (asynchronous) or clock output (synchronous) of the serial interface 0
	14	12	8		P3.2 $\overline{INT0}$ $\overline{\text{interrupt 0 input}}$/timer 0 gate control
	15	13	9		P3.3 $\overline{INT1}$ $\overline{\text{interrupt 1 input}}$/timer 1 gate control
	16	14	10		P3.4 T0 counter 0 input
	17	15	11		P3.5 T1 counter 1 input
	18	16	12		P3.6 $\overline{WR}$ the write control signal latches the data byte from port 0 into the external data memory
	19	17	13		P3.7 $\overline{RD}$ the read control signal enables the external data memory to port 0

*) I = Input
O = Output

Table 1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number			I/O*)	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
XTAL2	20	18	14	–	**XTAL2** Output of the inverting oscillator amplifier.
XTAL1	21	19	15	–	**XTAL1** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times as well as rise fall times specified in the AC characteristics must be observed.
P2.0 – P2.7	24–31	21–28	18–25	I/O	**Port 2** is a quasi-bidirectional I/O port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state they can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pull-up resistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register.

*) I = Input
O = Output

Table 1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number			I/O*)	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
$\overline{\text{PSEN}}$	32	29	26	O	**The $\overline{\text{Program Store Enable}}$** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods except during external data memory accesses. Remains high during internal program execution.
RESET	10	9	4	I	**RESET** A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{CC}.
ALE/$\overline{\text{PROG}}$	33	30	27	I/O	The **Address Latch Enable** output is used for latching the low-byte of the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access. For the C501-1E this pin is also the program pulse input ($\overline{\text{PROG}}$) during OTP memory programming.
$\overline{\text{EA}}$/V_{PP}	35	31	29	I	**$\overline{\text{External Access Enable}}$** When held at high level, instructions are fetched from the internal ROM (C501-1R and C501-1E) when the PC is less than 2000_H. When held at low level, the C501 fetches all instructions from external program memory. For the C501-L this pin must be tied low. This pin also receives the programming supply voltage V_{PP} during OTP memory programming (C501-1E) only).

*) I = Input
O = Output

Table 1
Pin Definitions and Functions (cont'd)

Symbol	Pin Number			I/O*)	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
P0.0 – P0.7	43–36	39–32	37–30	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this application it uses strong internal pull-up resistors when issuing 1s. Port 0 also outputs the code bytes during program verification in the C501-1R and C501-1E. External pull-up resistors are required during program verification.
V_{SS}	22	20	16	–	**Circuit ground potential**
V_{CC}	44	40	38	–	**Supply terminal** for all operating modes
N.C.	1, 12, 23, 34	–	6, 17, 28, 39	–	**No connection**

*) I = Input
O = Output

Functional Description

The C501 is fully compatible to the standard 8051 microcontroller family.

It is compatible with the 80C32/52/82C52. While maintaining all architectural and operational characteristics of the 8051microcontroller family, the C501 incorporates some enhancements in the timer 2 unit.

Figure 6 shows a block diagram of the C501.

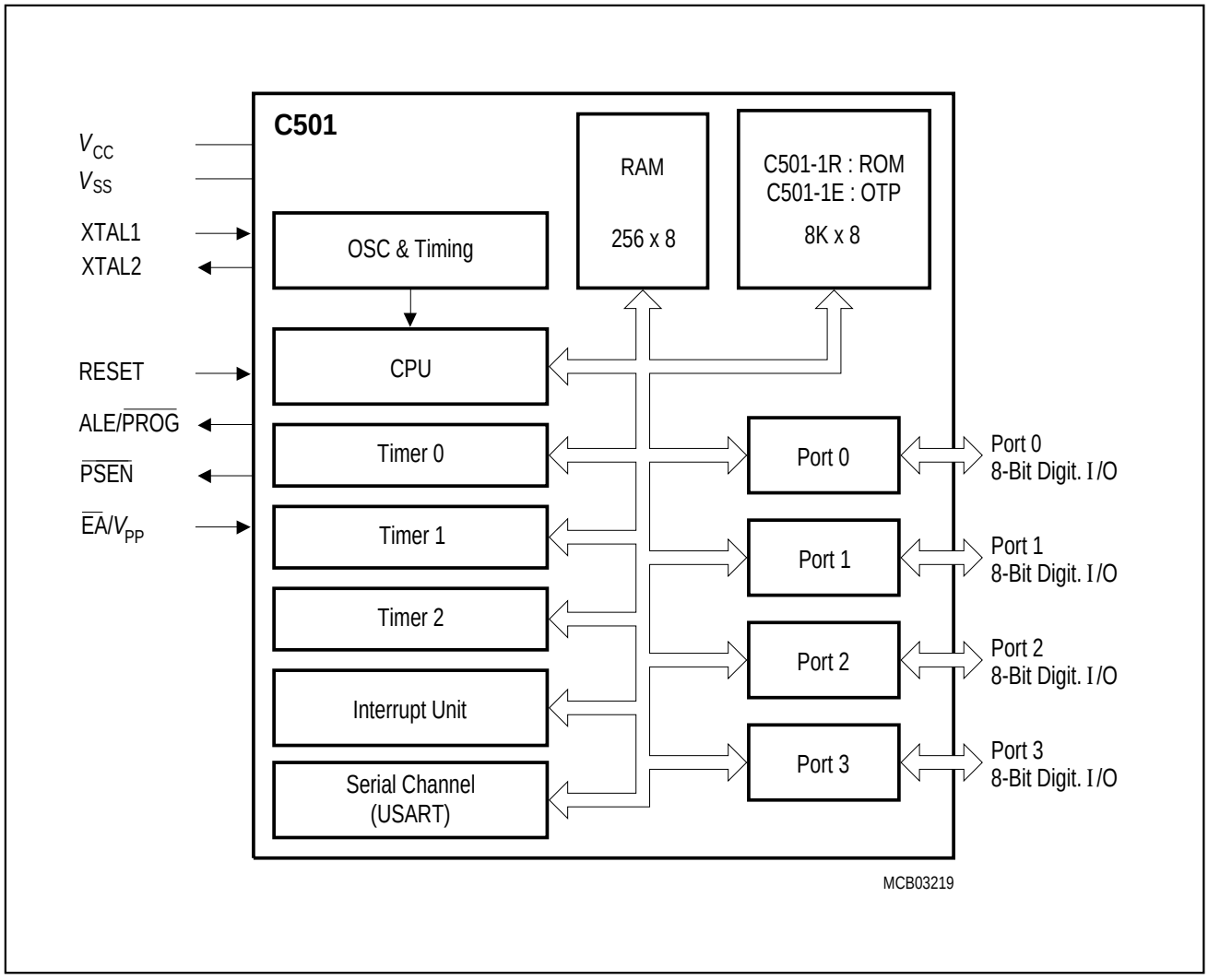


Figure 6
Block Diagram of the C501

CPU

The C501 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44 % one-byte, 41 % two-byte, and 15% three-byte instructions. With a 12 MHz crystal, 58% of the instructions are executed in 1.0 µs 24 MHz: 500 ns, 40 MHz : 300 ns).

Special Function Register PSW (Address $D0_H$) **Reset Value : 00_H**

Bit No.	MSB							LSB	
	$D7_H$	$D6_H$	$D5_H$	$D4_H$	$D3_H$	$D2_H$	$D1_H$	$D0_H$	
$D0_H$	CY	AC	F0	RS1	RS0	OV	F1	P	PSW

Bit	Function
CY	Carry Flag Used by arithmetic instruction.
AC	Auxiliary Carry Flag Used by instructions which execute BCD operations.
F0	General Purpose Flag
RS1 RS0	Register Bank select control bits These bits are used to select one of the four register banks.
OV	Overflow Flag Used by arithmetic instruction.
F1	General Purpose Flag
P	Parity Flag Set/cleared by hardware after each instruction to indicate an odd/even number of "one" bits in the accumulator, i.e. even parity.

RS1	RS0	Function
0	0	Bank 0 selected, data address 00_H-07_H
0	1	Bank 1 selected, data address 08_H-$0F_H$
1	0	Bank 2 selected, data address 10_H-17_H
1	1	Bank 3 selected, data address 18_H-$1F_H$

Memory Organization

The C501 CPU manipulates data and operands in the following four address spaces:

- up to 64 Kbyte of internal/external program memory
- up to 64 Kbyte of external data memory
- 256 bytes of internal data memory
- a 128 byte special function register area

Figure 7 illustrates the memory address spaces of the C501.

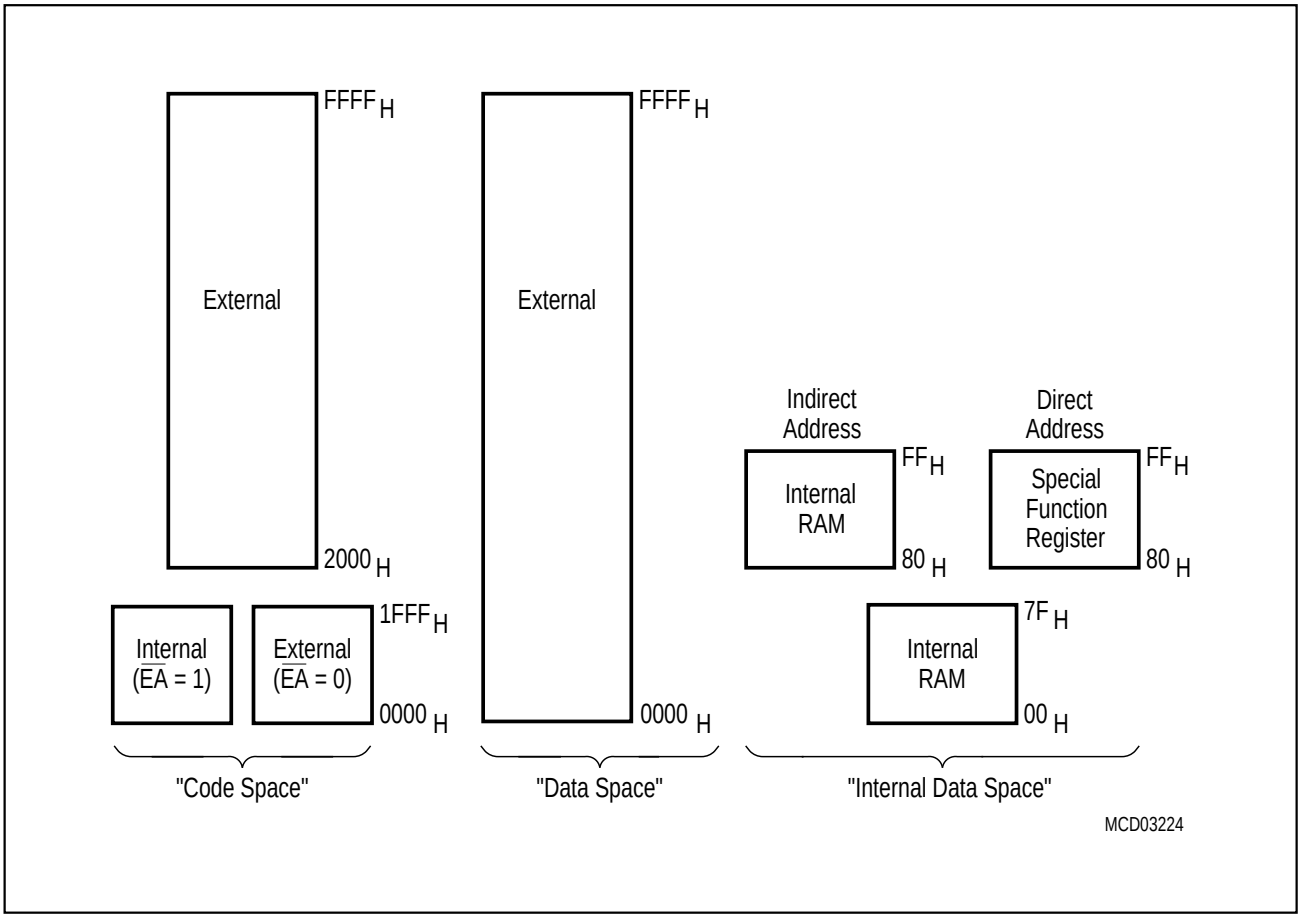


Figure 7
C501 Memory Map

Special Function Registers

The registers, except the program counter and the four general purpose register banks, reside in the special function register area.

The 27 special function registers (SFRs) include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. All SFRs with addresses where address bits 0-2 are 0 (e.g. 80_H, 88_H, 90_H, 98_H, ..., $F8_H$, FF_H) are bitaddressable.

The SFRs of the C501 are listed in **table 2** and **table 3**. In **table 2** they are organized in groups which refer to the functional blocks of the C501. **Table 3** illustrates the contents of the SFRs in numeric order of their addresses.

Table 2
Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	**$E0_H$** [1]	00_H
	B	B-Register	**$F0_H$** [1]	00_H
	DPH	Data Pointer, High Byte	83_H	00_H
	DPL	Data Pointer, Low Byte	82_H	00_H
	PSW	Program Status Word Register	**$D0_H$** [1]	00_H
	SP	Stack Pointer	81_H	07_H
Interrupt System	IE	Interrupt Enable Register	**$A8_H$** [1]	$0X000000_B$ [3]
	IP	Interrupt Priority Register	**$B8_H$** [1]	$XX000000_B$ [3]
Ports	P0	Port 0	**80_H** [1]	FF_H
	P1	Port 1	**90_H** [1]	FF_H
	P2	Port 2	**$A0_H$** [1]	FF_H
	P3	Port 3	**$B0_H$** [1]	FF_H
Serial Channel	PCON [2]	Power Control Register	87_H	$0XXX0000_B$ [3]
	SBUF	Serial Channel Buffer Register	99_H	XX_H [3]
	SCON	Serial Channel Control Register	**98_H** [1]	00_H
Timer 0 / Timer 1	TCON	Timer 0/1 Control Register	**88_H** [1]	00_H
	TH0	Timer 0, High Byte	$8C_H$	00_H
	TH1	Timer 1, High Byte	$8D_H$	00_H
	TL0	Timer 0, Low Byte	$8A_H$	00_H
	TL1	Timer 1, Low Byte	$8B_H$	00_H
	TMOD	Timer Mode Register	89_H	00_H
Timer 2	T2CON	Timer 2 Control Register	**$C8_H$** [1]	00_H
	T2MOD	Timer 2 Mode Register	$C9_H$	$XXXXXXX0_B$ [3]
	RC2H	Timer 2 Reload/Capture Register, High Byte	CB_H	00_H
	RC2L	Timer 2 Reload/Capture Register, Low Byt	CA_H	00_H
	TH2	Timer 2 High Byte	CD_H	00_H
	TL2	Timer 2 Low Byte	CC_H	00_H
Pow. Sav. Modes	PCON [2]	Power Control Register	87_H	$0XXX0000_B$ [3]

1) Bit-addressable special function registers
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
3) “X“ means that the value is undefined and the location is reserved

Table 3
Contents of the SFRs, SFRs in numeric order of their addresses

Addr	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80_H[2)]	P0	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
81_H	SP	07_H	.7	.6	.5	.4	.3	.2	.1	.0
82_H	DPL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
83_H	DPH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
87_H	PCON	$0XXX\text{-}0000_B$	SMOD	–	–	–	GF1	GF0	PDE	IDLE
88_H [2)]	TCON	00_H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89_H	TMOD	00_H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
$8A_H$	TL0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8B_H$	TL1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8C_H$	TH0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8D_H$	TH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
90_H[2)]	P1	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
98_H[2)]	SCON	00_H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99_H	SBUF	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
$A0_H$[2)]	P2	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
$A8_H$[2)]	IE	$0X00\text{-}0000_B$	EA	–	ET2	ES	ET1	EX1	ET0	EX0
$B0_H$[2)]	P3	FF_H	RD	WR	T1	T0	INT1	INT0	TxD	RxD
$B8_H$[2)]	IP	$XX00.0000_B$	–	–	PT2	PS	PT1	PX1	PT0	PX0
$C8_H$[2)]	T2CON	00_H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
$C9_H$	T2MOD	$XXXX\text{-}XXX0_B$	–	–	–	–	–	–	–	DCEN
CA_H	RC2L	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CB_H	RC2H	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CC_H	TL2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CD_H	TH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D0_H$[2)]	PSW	00_H	CY	AC	F0	RS1	RS0	OV	F1	P
$E0_H$[2)]	ACC	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F0_H$[2)]	B	00_H	.7	.6	.5	.4	.3	.2	.1	.0

1) X means that the value is undefined and the location is reserved
2) Bit-addressable special function registers

Timer / Counter 0 and 1

Timer/counter 0 and 1 can be used in four operating modes as listed in **table 4**.

Table 4
Timer/Counter 0 and 1 Operating Modes

Mode	Description	TMOD				Input Clock	
		Gate	C/$\overline{T}$	M1	M0	internal	external (max)
0	8-bit timer/counter with a divide-by-32 prescaler	X	X	0	0	$f_{OSC}/_{12 \times 32}$	$f_{OSC}/_{24 \times 32}$
1	16-bit timer/counter	X	X	1	1	$f_{OSC}/_{12}$	$f_{OSC}/_{24}$
2	8-bit timer/counter with 8-bit autoreload	X	X	0	0	$f_{OSC}/_{12}$	$f_{OSC}/_{24}$
3	Timer/counter 0 used as one 8-bit timer/counter and one 8-bit timer Timer 1 stops	X	X	1	1	$f_{OSC}/_{12}$	$f_{OSC}/_{24}$

In the “timer” function (C/$\overline{T}$ = ‘0’) the register is incremented every machine cycle. Therefore the count rate is $f_{OSC}/12$.

In the “counter” function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin (P3.4/T0, P3.5/T1). Since it takes two machine cycles to detect a falling edge the max. count rate is $f_{OSC}/24$. External inputs $\overline{INT0}$ and $\overline{INT1}$ (P3.2, P3.3) can be programmed to function as a gate to facilitate pulse width measurements. **Figure 8** illustrates the input clock logic.

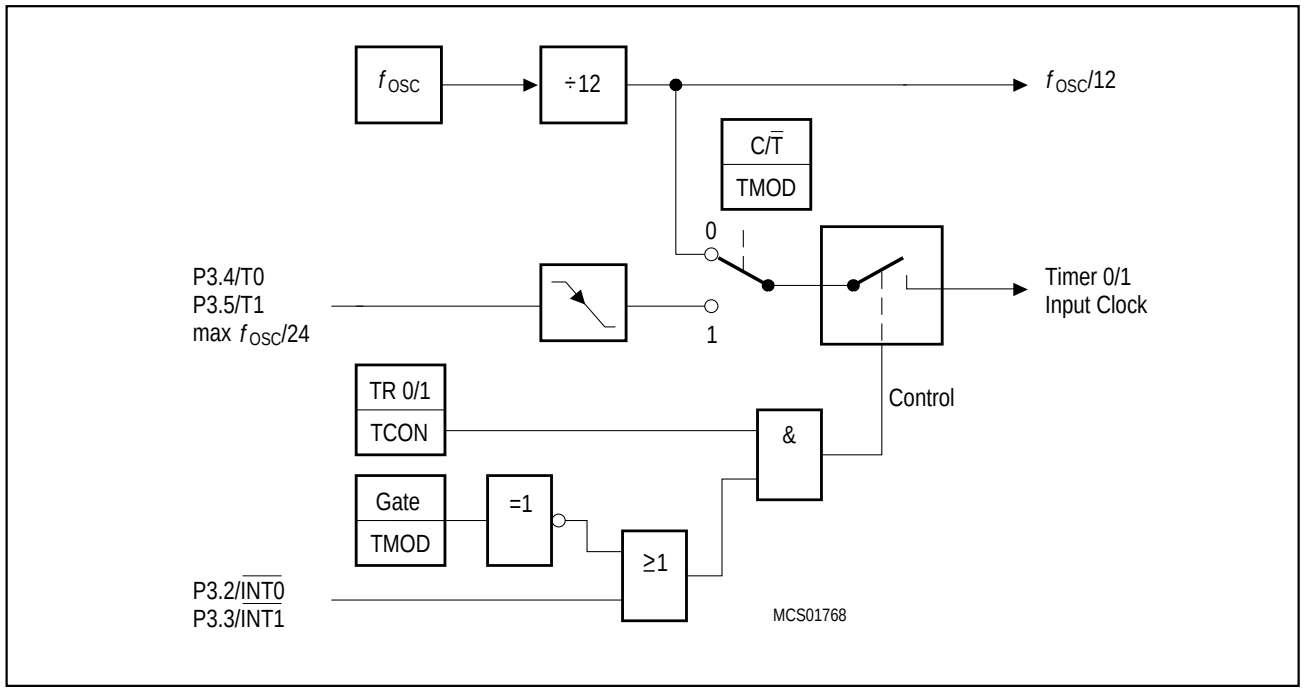


Figure 8
Timer/Counter 0 and 1 Input Clock Logic

Timer 2

Timer 2 is a 16-bit timer/counter with an up/down count feature. It can operate either as timer or as an event counter which is selected by bit C/$\overline{T2}$ (T2CON.1). It has three operating modes as shown in **table 5**.

Table 5
Timer/Counter 2 Operating Modes

Mode	T2CON			T2MOD	T2CON	P1.1/ T2EX	Remarks	Input Clock	
	R×CLK or T×CLK	CP/$\overline{RL2}$	TR2	DCEN	EXEN			internal	external (P1.0/T2)
16-bit Auto-reload	0	0	1	0	0	X	reload upon overflow	f_{osc}/12	max f_{osc}/24
	0	0	1	0	1	↓	reload trigger (falling edge)		
	0	0	1	1	X	0	Down counting		
	0	0	1	1	X	1	Up counting		
16-bit Capture	0	1	1	X	0	X	16 bit Timer/ Counter (only up-counting)	f_{osc}/12	max f_{osc}/24
	0	1	1	X	1	↓	capture TH2, TL2 → RC2H, RC2L		
Baud Rate Gene-rator	1	X	1	X	0	X	no overflow interrupt request (TF2)	f_{osc}/2	max f_{osc}/24
	1	X	1	X	1	↓	extra external interrupt (“Timer 2”)		
off	X	X	0	X	X	X	Timer 2 stops	–	–

Note: ↓ = falling edge

Serial Interface (USART)

The serial port is full duplex and can operate in four modes (one synchronous mode, three asynchronous modes) as illustrated in **table 6**. The possible baudrates can be calculated using the formulas given in **table 7**.

Table 6
USART Operating Modes

Mode	SCON		Baudrate	Description
	SM0	SM1		
0	0	0	$f_{OSC}/12$	Serial data enters and exits through R×D. T×D outputs the shift clock. 8-bit are transmitted/received (LSB first)
1	0	1	Timer 1/2 overflow rate	8-bit UART 10 bits are transmitted (through T×D) or received (R×D)
2	1	0	$f_{OSC}/32$ or $f_{OSC}/64$	9-bit UART 11 bits are transmitted (T×D) or received (R×D)
3	1	1	Timer 1/2 overflow rate	9-bit UART Like mode 2 except the variable baud rate

Table 7
Formulas for Calculating Baudrates

Baud Rate derived from	Interface Mode	Baudrate
Oscillator	0 2	$f_{OSC}/12$ $(2^{SMOD} \times f_{OSC}) / 64$
Timer 1 (16-bit timer) (8-bit timer with 8-bit autoreload)	1,3 1,3	$(2^{SMOD} \times$ timer 1 overflow rate$) /32$ $(2^{SMOD} \times f_{OSC}) / (32 \times 12 \times (256\text{-TH1}))$
Timer 2	1,3	$f_{OSC} / (32 \times (65536\text{-(RC2H, RC2L)}))$

Interrupt System

The C501 provides 6 interrupt sources with two priority levels. **Figure 9** gives a general overview of the interrupt sources and illustrates the request and control flags.

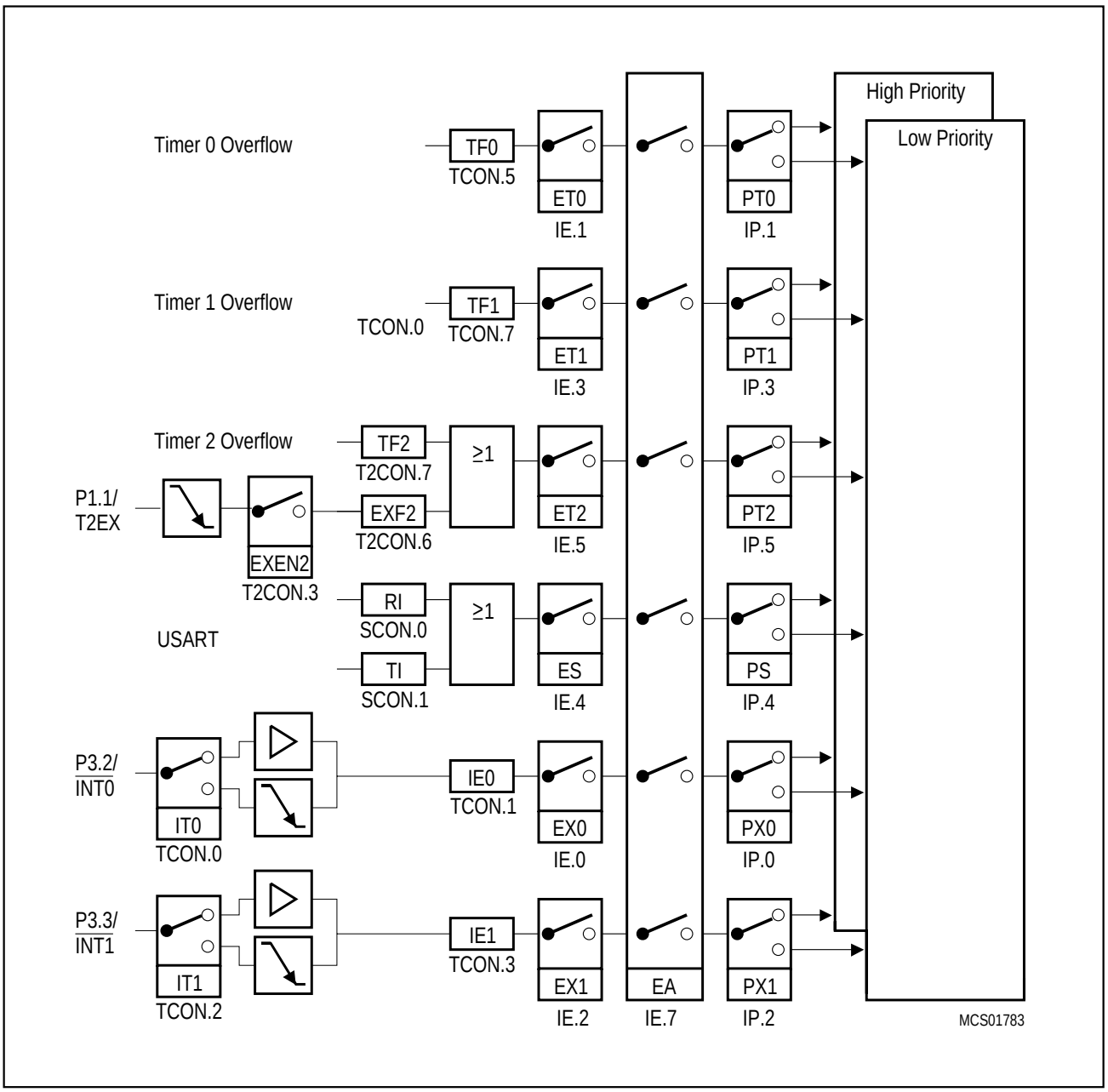


Figure 9
Interrupt Request Sources

Table 8
Interrupt Sources and their Corresponding Interrupt Vectors

Source (Request Flags)	Vector	Vector Address
IE0	External interrupt 0	0003_H
TF0	Timer 0 interrupt	$000B_H$
IE1	External interrupt 1	0013_H
TF1	Timer 1 interrupt	$001B_H$
RI + TI	Serial port interrupt	0023_H
TF2 + EXF2	Timer 2 interrupt	$002B_H$

A low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low-priority interrupt. A high-priority interrupt cannot be interrupted by any other interrupt source.

If two requests of different priority level are received simultaneously, the request of higher priority is serviced. If requests of the same priority are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence as shown in **table 9**.

Table 9
Interrupt Priority-Within-Level

Interrupt Source		Priority
External Interrupt 0,	IE0	High
Timer 0 Interrupt,	TF0	
External Interrupt 1,	IE1	↓
Timer 1 Interrupt,	TF1	
Serial Channel,	RI + TI	
Timer 2 Interrupt,	TF2 + EXF2	Low

Power Saving Modes

Two power down modes are available, the Idle Mode and Power Down Mode.

The bits PDE and IDLE of the register PCON select the Power Down mode or the Idle mode, respectively. If the Power Down mode and the Idle mode are set at the same time, the Power Down mode takes precedence. **Table 10** gives a general overview of the power saving modes.

Table 10
Power Saving Modes Overview

Mode	Entering Instruction Example	Leaving by	Remarks
Idle mode	ORL PCON, #01H	– enabled interrupt – Hardware Reset	CPU is gated off CPU status registers maintain their data. Peripherals are active
Power-Down Mode	ORL PCON, #02H	Hardware Reset	Oscillator is stopped, contents of on-chip RAM and SFR's are maintained (leaving Power Down Mode means redefinition of SFR contents).

In the Power Down mode of operation, V_{CC} can be reduced to minimize power consumption. It must be ensured, however, that V_{CC} is not reduced before the Power Down mode is invoked, and that V_{CC} is restored to its normal operating level, before the Power Down mode is terminated. The reset signal that terminates the Power Down mode also restarts the oscillator. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize (similar to power-on reset).

OTP Operation

The C501-1E is programmed by usng a modified Quick-Pulse Programming™ [1] algorithm. It differs from older methods in the value used for V_{PP} (programming supply voltage) and in the width and number of the ALE/$\overline{PROG}$ pulses. The C501-1E contains two signature bytes that can be read and used by a programming system to identify the device. The signature bytes identify the manufacturer of the device.

Table 11 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the security bits. The circuit configuration and waveforms for quick-pulse programming are shown in **figures 10** to **12**.

Table 11
OTP Programming Modes

Mode	RESET	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}/V_{PP}$	P2.7	P2.6	P3.7	P3.6
Read signature	1	0	1	1	0	0	0	0
Program code data	1	0	0	V_{PP}	1	0	1	1
Verify code data	1	0	1	1	0	0	1	1
Progam encryption table	1	0	0	V_{PP}	1	0	1	0
Program security bit 1	1	0	0	V_{PP}	1	1	1	1
Program security bit 2	1	0	0	V_{PP}	1	1	0	0

Notes :

1. “0” = valid low for that pin, “1” = valid high for that pin.
2. V_{PP} = 12.75 V ± 0.25V
3. V_{CC} = 5 V ± 10% during programming and verification.
4. ALE/$\overline{PROG}$ receives 25 programming pulses while V_{PP} is held at 12.75 V. Each programming pulse is low for 100 µs (± 10 µs) and high for a minimum of 10 µs.

[1] Quick-Pulse Programming™ is a trademark phrase of Intel Corporation

Quick-Pulse Programming

The setup for microcontroller quick-pulse programming is shown in **figure 10**. Note that the C501-1E is running with a 4 to 6 MHz oscillator The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the OTP memory location to be programmed is applied to port 1 and 2 as shown in **figure 10**. The code byte to be programmed into that location is applied to port 0. RESET, $\overline{PSEN}$ and pins of port 2 and 3 specified in **table 11** are held at the “Program code data“ levels. The ALE/$\overline{PROG}$ signal is pulsed low 25 times as shown in **figure 11**.

For programming of the encryption table, the 25 pulse programming sequence must be repeated for addresses 0 through $1F_H$, using the “Program encrytion table“ levels. After the encryption table is programmed, verification cycles will produce only encrypted data.

For programming of the security bits, the 25 pulse programming sequence must be repeat using the “Program security bit“ levels. After one security bit is programmed, further programming of the code memory and encryption table is disabled. However, the other security bit can still be programmed.

Note that the $\overline{EA}/V_{PP}$ pin must not be allowed to go above the maximum specified V_{PP} level. for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches and overshoots.

Program Verification

If security bit 2 has not been programmed, the on-chip OTP program memory can be read out for program verification. The address of the OTP program memory locations to be read is applied to ports 1 and 2 as shown in **figure 12**. The other pins are held at the “Verify code data“ levels indicated in **table 11**. The contents of the address location will be emitted on port 0. External pullups are required on port 0 for this operation.

If the encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

Reading the SIgnature Bytes

The signature bytes are read by the same procedure as a normal verification of loctions 30_H and 31_H, except that P3.6 and P3.7 need to be pulled to a logic low. The values are :

$30_H = E0_H$ indicates manufacturer
$31_H = 71_H$ indicates C501-1E

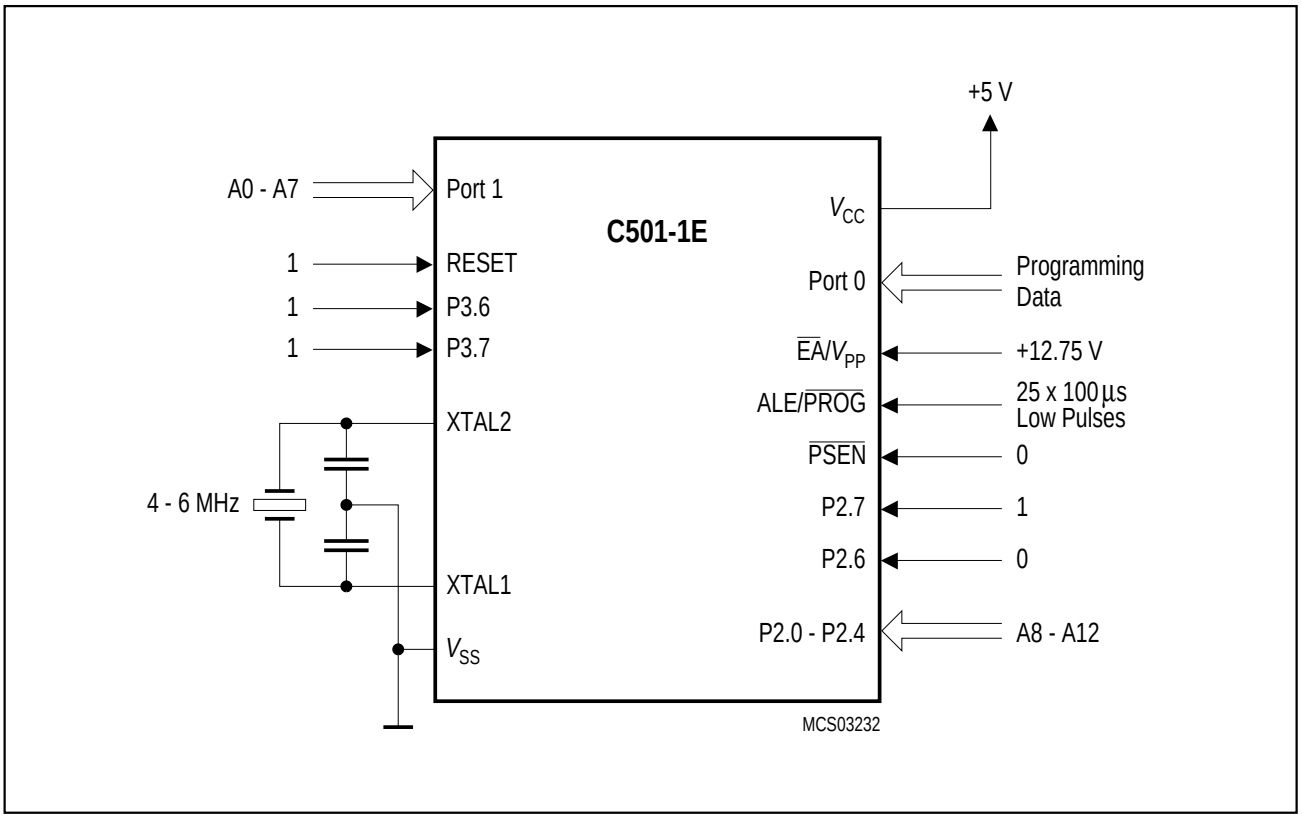


Figure 10
C501-1E OTP Memory Programming Configuration

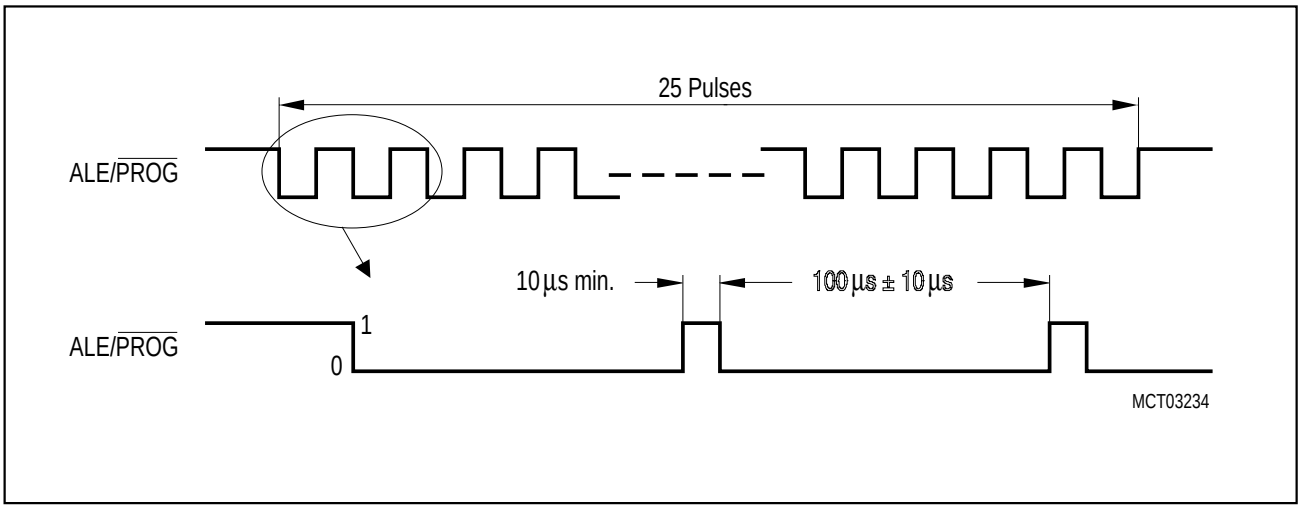


Figure 11
C501-1E ALE/$\overline{PROG}$ Waveform

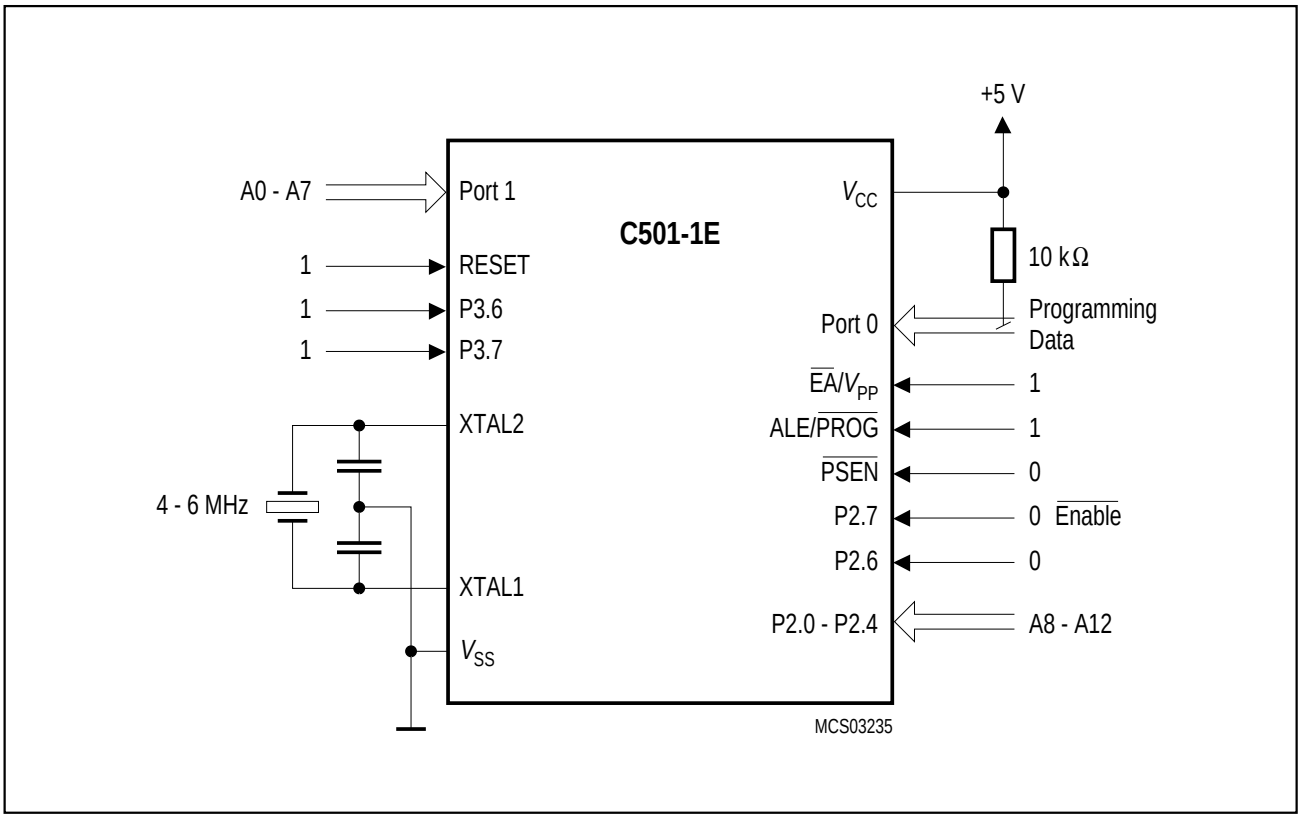


Figure 12
C501-1E OTP Memory Verification

Absolute Maximum Ratings

Ambient temperature under bias (T_A)	– 40 to 85 °C
Storage temperature (T_{stg})	– 65 °C to 150 °C
Voltage on V_{CC} pins with respect to ground (V_{SS})	– 0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS})	– 0.5 V to V_{CC} +0.5 V
Input current on any pin during overload condition	– 10 mA to 10 mA
Absolute sum of all input currents during overload condition	I 100 mA I
Power dissipation	TBD

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the Voltage on V_{CC} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.*

DC Characteristics for C501-L / C501-1R

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V; T_A = 0 ˚C to 70 ˚C for the SAB-C501
T_A = – 40 ˚C to 85 ˚C for the SAF-C501

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (except $\overline{EA}$, RESET)	V_{IL}	– 0.5	0.2 V_{CC} – 0.1	V	–
Input low voltage ($\overline{EA}$)	$V_{IL\,1}$	– 0.5	0.2 V_{CC} – 0.3	V	–
Input low voltage (RESET)	$V_{IL\,2}$	– 0.5	0.2 V_{CC} + 0.1	V	–
Input high voltage (except XTAL1, $\overline{EA}$, RESET)	V_{IH}	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	–
Input high voltage to XTAL1	$V_{IH\,1}$	0.7 V_{CC}	V_{CC} + 0.5	V	
Input high voltage to $\overline{EA}$, RESET	$V_{IH\,2}$	0.6 V_{CC}	V_{CC} + 0.5	V	–
Output low voltage (ports 1, 2, 3)	V_{OL}	–	0.45	V	I_{OL} = 1.6 mA [1]
Output low voltage (port 0, ALE, $\overline{PSEN}$)	$V_{OL\,1}$	–	0.45	V	I_{OL} = 3.2 mA [1]
Output high voltage (ports 1, 2, 3)	V_{OH}	2.4 0.9 V_{CC}	– –	V	I_{OH} = – 80 µA, I_{OH} = – 10 µA
Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$)	$V_{OH\,1}$	2.4 0.9 V_{CC}	– –	V	I_{OH} = – 800 µA [2], I_{OH} = – 80 µA [2]
Logic 0 input current (ports 1, 2, 3)	I_{IL}	– 10	– 50	µA	V_{IN} = 0.45 V
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	– 65	– 650	µA	V_{IN} = 2 V
Input leakage current (port 0, $\overline{EA}$)	I_{LI}	–	± 1	µA	0.45 < V_{IN} < V_{CC}
Pin capacitance	C_{IO}	–	10	pF	f_C = 1 MHz, T_A = 25 ˚C
Power supply current:					
Active mode, 12 MHz [7]	I_{CC}	–	21	mA	V_{CC} = 5 V, [4]
Idle mode, 12 MHz [7]	I_{CC}	–	4.8	mA	V_{CC} = 5 V, [5]
Active mode, 24 MHz [7]	I_{CC}	–	36.2	mA	V_{CC} = 5 V, [4]
Idle mode, 24 MHz [7]	I_{CC}	–	8.2	mA	V_{CC} = 5 V, [5]
Active mode, 40 MHz [7]	I_{CC}	–	56.5	mA	V_{CC} = 5 V, [4]
Idle mode, 40 MHz [7]	I_{CC}	–	12.7	mA	V_{CC} = 5 V, [5]
Power Down Mode	I_{PD}	–	50	µA	V_{CC} = 2 … 5.5 V [3]

Notes see page 32.

DC Characteristics for C501-1E

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V; T_A = 0 ˚C to 70 ˚C for the SAB-C501
T_A = – 40 ˚C to 85 ˚C for the SAF-C501

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (except $\overline{EA}$/V_{PP}, RESET)	V_{IL}	– 0.5	0.2 V_{CC} – 0.1	V	–
Input low voltage ($\overline{EA}$/V_{PP})	$V_{IL\,1}$	– 0.5	0.1 V_{CC} – 0.1	V	–
Input low voltage (RESET)	$V_{IL\,2}$	– 0.5	0.2 V_{CC} + 0.1	V	–
Input high voltage (except XTAL1, $\overline{EA}$/V_{PP}, RESET)	V_{IH}	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	–
Input high voltage to XTAL1	$V_{IH\,1}$	0.7 V_{CC}	V_{CC} + 0.5	V	
Input high voltage to $\overline{EA}$/V_{PP}, RESET	$V_{IH\,2}$	0.6 V_{CC}	V_{CC} + 0.5	V	–
Output low voltage (ports 1, 2, 3)	V_{OL}	–	0.45	V	I_{OL} = 1.6 mA [1]
Output low voltage (port 0, ALE/$\overline{PROG}$, $\overline{PSEN}$)	$V_{OL\,1}$	–	0.45	V	I_{OL} = 3.2 mA [1]
Output high voltage (ports 1, 2, 3)	V_{OH}	2.4 0.9 V_{CC}	– –	V	I_{OH} = – 80 µA, I_{OH} = – 10 µA
Output high voltage (port 0 in external bus mode, ALE/$\overline{PROG}$, $\overline{PSEN}$)	$V_{OH\,1}$	2.4 0.9 V_{CC}	– –	V	I_{OH} = – 800 µA [2], I_{OH} = – 80 µA [2]
Logic 0 input current (ports 1, 2, 3)	I_{IL}	– 10	– 50	µA	V_{IN} = 0.45 V
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	– 65	– 650	µA	V_{IN} = 2 V
Input leakage current (port 0, $\overline{EA}$/V_{PP})	I_{LI}	–	± 1	µA	0.45 < V_{IN} < V_{CC}
Pin capacitance	C_{IO}	–	10	pF	f_C = 1 MHz, T_A = 25 ˚C
Power supply current:					
Active mode, 12 MHz [7]	I_{CC}	–	21	mA	V_{CC} = 5 V, [4]
Idle mode, 12 MHz [7]	I_{CC}	–	18	mA	V_{CC} = 5 V, [5]
Active mode, 24 MHz [7]	I_{CC}	–	36.2	mA	V_{CC} = 5 V, [4]
Idle mode, 24 MHz [7]	I_{CC}	–	20	mA	V_{CC} = 5 V, [5]
Power Down Mode	I_{PD}	–	50	µA	V_{CC} = 2 … 5.5 V [3]

Notes see next page.

Notes:

1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading > 100 pF), the noise pulse on ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.

2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall bellow the 0.9 V_{CC} specification when the address lines are stabilizing.

3) I_{PD} (Power Down Mode) is measured under following conditions:
$\overline{EA}$ = Port0 = V_{CC}; RESET = V_{SS}; XTAL2 = N.C.; XTAL1 = V_{SS}; all other pins are disconnected.

4) I_{CC} (active mode) is measured with:
XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL2 = N.C.;
$\overline{EA}$ = Port0 = RESET= V_{CC}; all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (appr. 1 mA).

5) I_{CC} (Idle mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} – 0.5 V; XTAL2 = N.C.;
RESET = $\overline{EA}$ = V_{SS}; Port0 = V_{CC}; all other pins are disconnected;

7) $I_{CC\ max}$ at other frequencies is given by:
active mode: I_{CC} = 1.27 x f_{OSC} + 5.73
idle mode: I_{CC} = 0.28 x f_{OSC} + 1.45 (C501-L and C501-1R only)
where f_{OSC} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at V_{CC} = 5 V.

AC Characteristics for C501-L / C501-1R / C501-1E

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V T_A = 0 ˚C to 70 ˚C for the SAB-C501
T_A = – 40 ˚C to 85 ˚C for the SAF-C501

(C_L for port 0, ALE and $\overline{\text{PSEN}}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	127	–	$2t_{CLCL}$ – 40	–	ns
Address setup to ALE	t_{AVLL}	43	–	t_{CLCL} – 40	–	ns
Address hold after ALE	t_{LLAX}	30	–	t_{CLCL} – 53	–	ns
ALE low to valid instr in	t_{LLIV}	–	233	–	$4t_{CLCL}$ – 100	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	58	–	t_{CLCL} – 25	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	215	–	$3t_{CLCL}$ – 35	–	ns
$\overline{\text{PSEN}}$ to valid instr in	t_{PLIV}	–	150	–	$3t_{CLCL}$ – 100	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	t_{PXIZ} *)	–	63	–	t_{CLCL} – 20	ns
Address valid after $\overline{\text{PSEN}}$	t_{PXAV} *)	75	–	t_{CLCL} – 8	–	ns
Address to valid instr in	t_{AVIV}	–	302	–	$5t_{CLCL}$ – 115	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	0	–	0	–	ns

*) Interfacing the C501 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

AC Characteristics for C501-L / C501-1R / C501-1E (cont'd)

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 12 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	400	–	$6t_{CLCL} - 100$	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	400	–	$6t_{CLCL} - 100$	–	ns
Address hold after ALE	t_{LLAX2}	30	–	$t_{CLCL} - 53$	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	252	–	$5t_{CLCL} - 165$	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	97	–	$2t_{CLCL} - 70$	ns
ALE to valid data in	t_{LLDV}	–	517	–	$8t_{CLCL} - 150$	ns
Address to valid data in	t_{AVDV}	–	585	–	$9t_{CLCL} - 165$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	200	300	$3t_{CLCL} - 50$	$3t_{CLCL} + 50$	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	203	–	$4t_{CLCL} - 130$	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	43	123	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	33	–	$t_{CLCL} - 50$	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	433	–	$7t_{CLCL} - 150$	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	33	–	$t_{CLCL} - 50$	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive Characteristics

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 12 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	83.3	285.7	ns
High time	t_{CHCX}	20	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	20	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	20	ns
Fall time	t_{CHCL}	–	20	ns

AC Characteristics for C501-L24 / C501-1R24 / C501-1E24

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V T_A = 0 ˚C to 70 ˚C for the SAB-C501
T_A = – 40 ˚C to 85 ˚C for the SAF-C501

(C_L for port 0, ALE and $\overline{\text{PSEN}}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		24 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 24 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	43	–	$2t_{CLCL}$ – 40	–	ns
Address setup to ALE	t_{AVLL}	17	–	t_{CLCL} – 25	–	ns
Address hold after ALE	t_{LLAX}	17	–	t_{CLCL} – 25	–	ns
ALE low to valid instr in	t_{LLIV}	–	80	–	$4t_{CLCL}$ – 87	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	22	–	t_{CLCL} – 20	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	95	–	$3t_{CLCL}$ – 30	–	ns
$\overline{\text{PSEN}}$ to valid instr in	t_{PLIV}	–	60	–	$3t_{CLCL}$ – 65	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	t_{PXIZ} *)	–	32	–	t_{CLCL} – 10	ns
Address valid after $\overline{\text{PSEN}}$	t_{PXAV} *)	37	–	t_{CLCL} – 5	–	ns
Address to valid instr in	t_{AVIV}	–	148	–	$5t_{CLCL}$ – 60	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	0	–	0	–	ns

*) Interfacing the C501 to devices with float times up to 37 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

AC Characteristics for C501-L24 / C501-1R24 / C501-1E24 (cont'd)

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		24 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 24 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	180	–	$6t_{CLCL} - 70$	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	180	–	$6t_{CLCL} - 70$	–	ns
Address hold after ALE	t_{LLAX2}	15	–	$t_{CLCL} - 27$	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	118	–	$5t_{CLCL} - 90$	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	63	–	$2t_{CLCL} - 20$	ns
ALE to valid data in	t_{LLDV}	–	200	–	$8t_{CLCL} - 133$	ns
Address to valid data in	t_{AVDV}	–	220	–	$9t_{CLCL} - 155$	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	75	175	$3t_{CLCL} - 50$	$3t_{CLCL} + 50$	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	67	–	$4t_{CLCL} - 97$	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	17	67	$t_{CLCL} - 25$	$t_{CLCL} + 25$	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	–	$t_{CLCL} - 37$	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	170	–	$7t_{CLCL} - 122$	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	15	–	$t_{CLCL} - 27$	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive Characteristics

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 24 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	41.7	285.7	ns
High time	t_{CHCX}	12	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	12	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	12	ns
Fall time	t_{CHCL}	–	12	ns

AC Characteristics for C501-L40 / C501-1R40

V_{CC} = 5 V + 10 %, – 15 %; V_{SS} = 0 V T_A = 0 ˚C to 70 ˚C for the SAB-C501
T_A = – 40 ˚C to 85 ˚C for the SAF-C501

(C_L for port 0, ALE and $\overline{\text{PSEN}}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		40 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 40 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	35	–	2 t_{CLCL} – 15	–	ns
Address setup to ALE	t_{AVLL}	10	–	t_{CLCL} – 15	–	ns
Address hold after ALE	t_{LLAX}	10	–	t_{CLCL} – 15	–	ns
ALE low to valid instr in	t_{LLIV}	–	55	–	4 t_{CLCL} – 45	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	10	–	t_{CLCL} – 15	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	60	–	3 t_{CLCL} – 15	–	ns
$\overline{\text{PSEN}}$ to valid instr in	t_{PLIV}	–	25	–	3 t_{CLCL} – 50	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	t_{PXIZ} *)	–	20	–	t_{CLCL} – 5	ns
Address valid after $\overline{\text{PSEN}}$	t_{PXAV} *)	20	–	t_{CLCL} – 5	–	ns
Address to valid instr in	t_{AVIV}	–	65	–	5 t_{CLCL} – 60	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	– 5	–	– 5	–	ns

*) Interfacing the C501 to devices with float times up to 25ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

AC Characteristics for C501-L40 / C501-1R40 (cont'd)

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		40 MHz Clock		Variable Clock $1/t_{CLCL}$ = 3.5 MHz to 40 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	120	–	6 t_{CLCL} – 30	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	120	–	6 t_{CLCL} – 30	–	ns
Address hold after ALE	t_{LLAX2}	10	–	t_{CLCL} – 15	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	75	–	5 t_{CLCL} – 50	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	38	–	2 t_{CLCL} – 12	ns
ALE to valid data in	t_{LLDV}	–	150	–	8 t_{CLCL} – 50	ns
Address to valid data in	t_{AVDV}	–	150	–	9 t_{CLCL} – 75	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	60	90	3 t_{CLCL} – 15	3 t_{CLCL} + 15	ns
Address valid to $\overline{WR}$ or $\overline{RD}$	t_{AVWL}	70	–	4 t_{CLCL} – 30	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	10	40	t_{CLCL} – 15	t_{CLCL} + 15	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	–	t_{CLCL} – 20	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	125	–	7 t_{CLCL} – 50	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	5	–	t_{CLCL} – 20	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive Characteristics

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 3.5 MHz to 40 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	25	285.7	ns
High time	t_{CHCX}	10	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	10	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	–	10	ns
Fall time	t_{CHCL}	–	10	ns

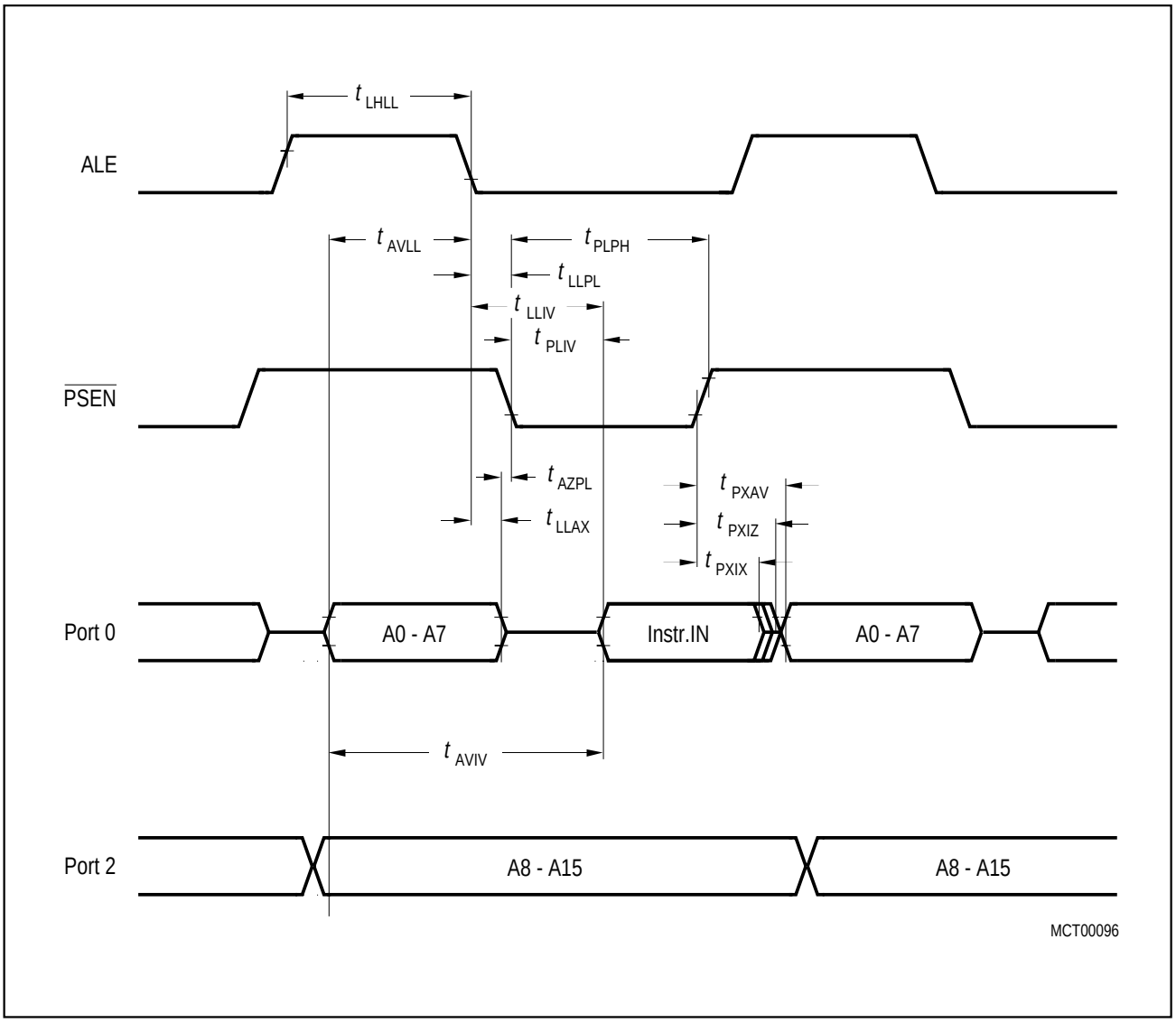


Figure 13
Program Memory Read Cycle

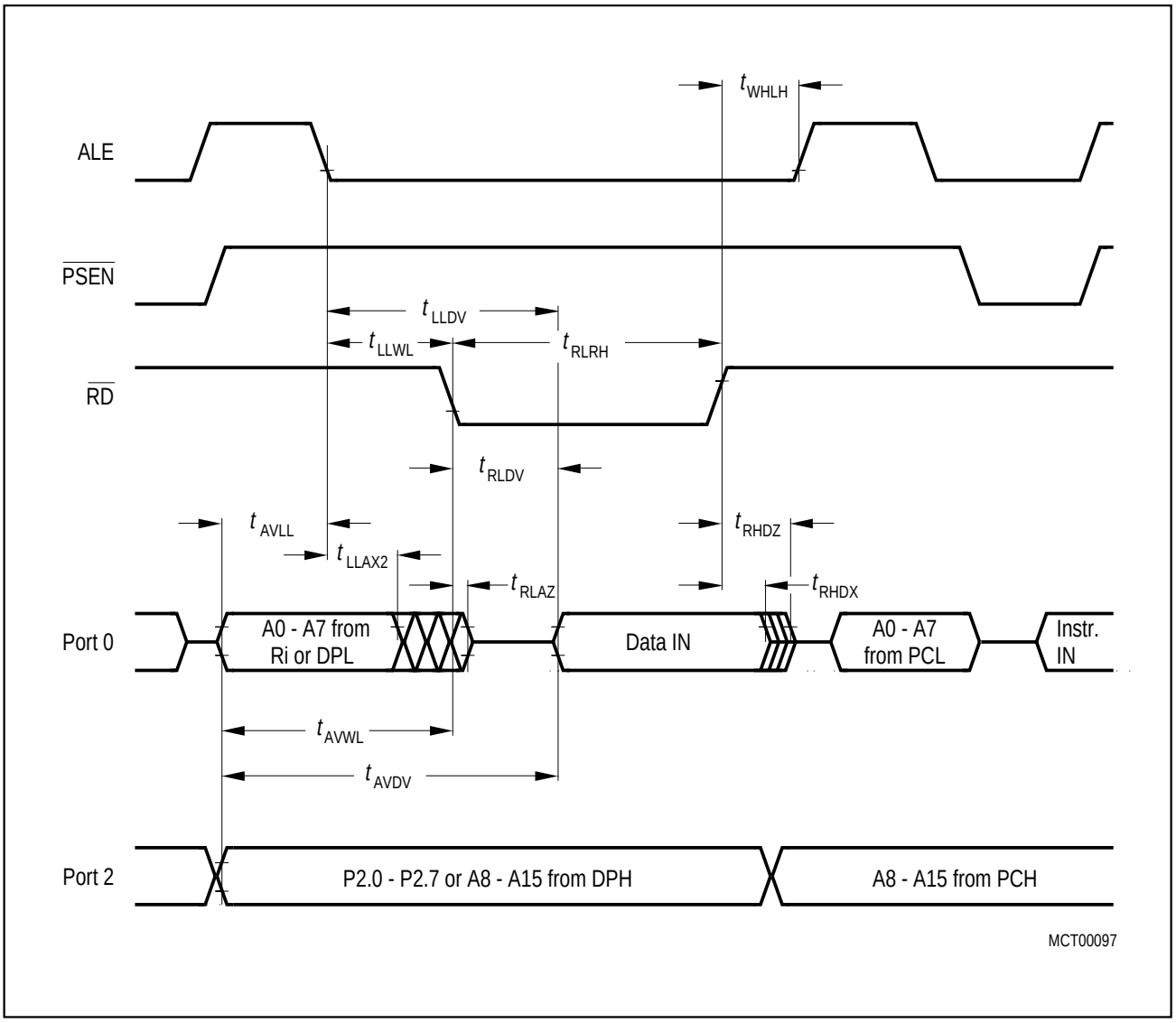


Figure 14
Data Memory Read Cycle

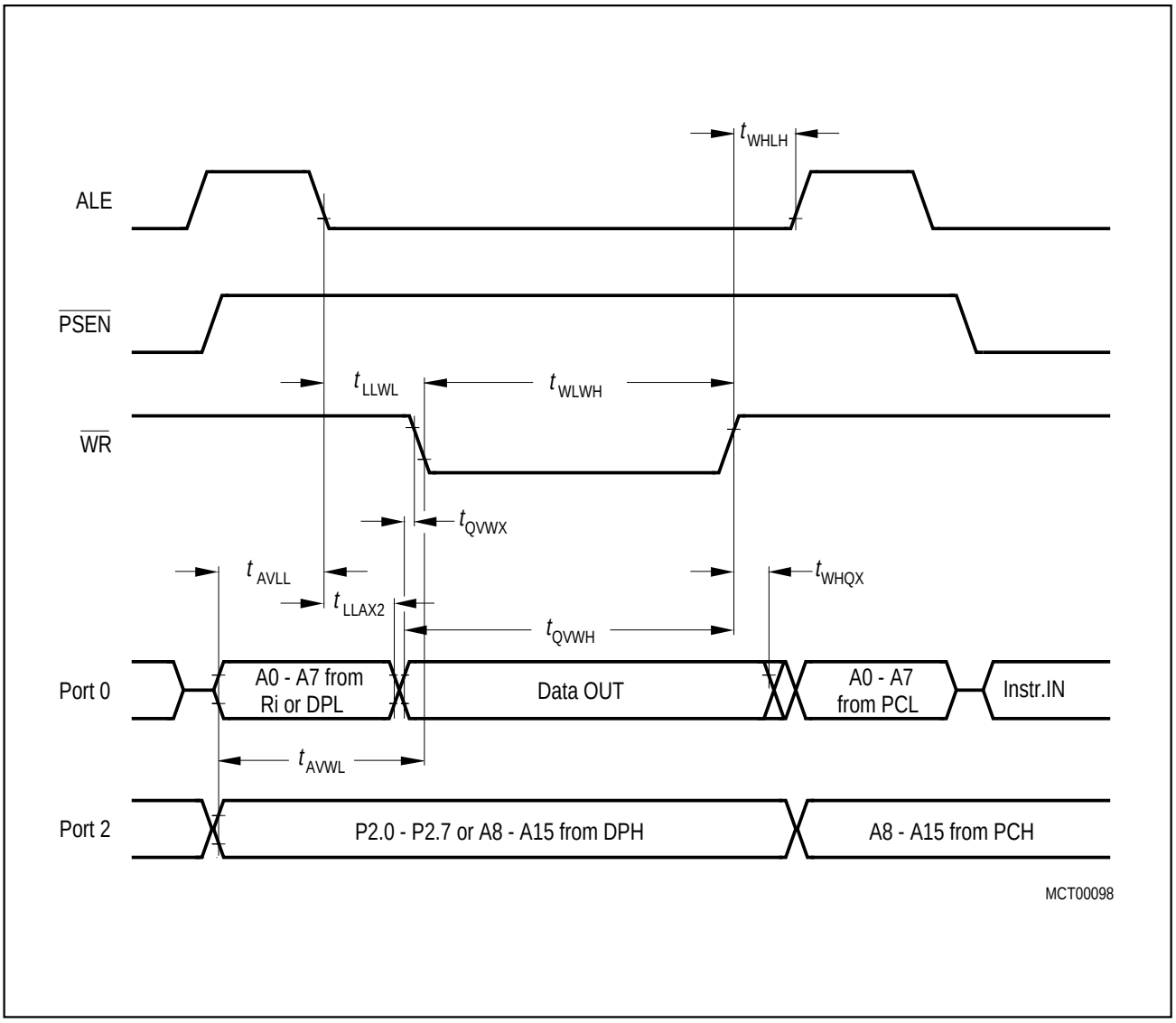


Figure 15
Data Memory Write Cycle

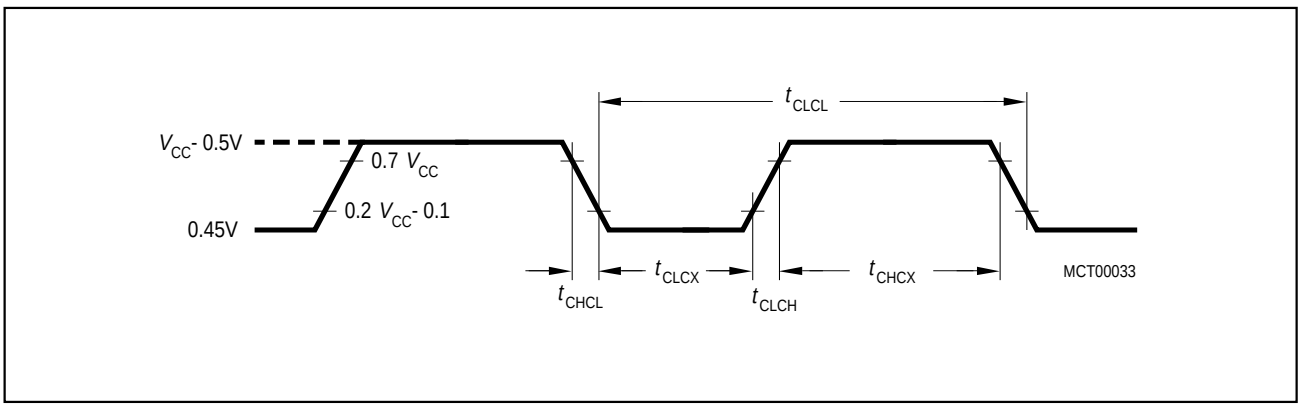
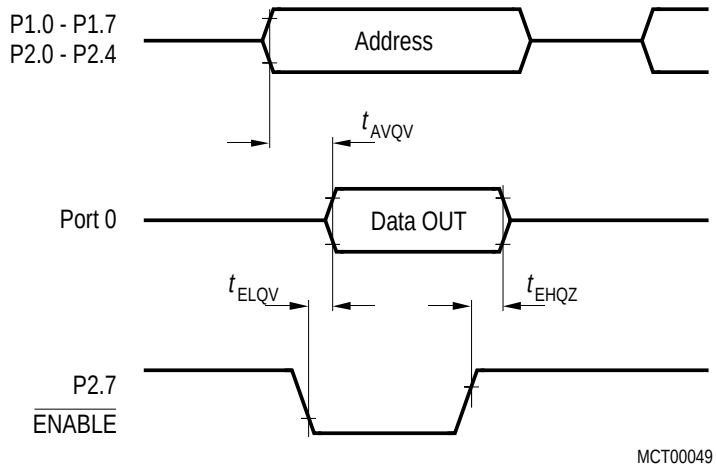


Figure 16
External Clock Drive at XTAL2

ROM Verification Characteristics for C501-1R

ROM Verification Mode 1

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	–	$48t_{CLCL}$	ns
ENABLE to valid data	t_{ELQV}	–	$48t_{CLCL}$	ns
Data float after ENABLE	t_{EHQZ}	0	$48t_{CLCL}$	ns
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz



Address: P1.0 - P1.7 = A0 - A7
P2.0 - P2.4 = A8 - A12
Data: P0.0 - P0.7 = D0 - D7

Inputs: P2.5 - P2.6, $\overline{PSEN} = V_{SS}$
$\overline{ALE}$, $\overline{EA} = V_{IH}$
$\overline{RESET} = V_{SS}$

Figure 17
ROM Verification Mode 1

OTP Programming and Verification Characteristics

V_{CC} = 5 V ± 10%, V_{SS} = 0 V, T_A = 21 ˚C to + 27 ˚C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Programming supply voltage	V_{PP}	12.5	13.0	V
Programming supply current	I_{PP}	–	50	mA
Oscillator frequency	1 / t_{CLCL}	4	6	MHz
Address setup to ALE/$\overline{\text{PROG}}$ low	t_{AVGL}	48 t_{CLCL}	–	ns
Address hold after ALE/$\overline{\text{PROG}}$	t_{GHAX}	48 t_{CLCL}	–	ns
Data setup to ALE/$\overline{\text{PROG}}$ low	t_{DVGL}	48 t_{CLCL}	–	ns
Data hold after ALE/$\overline{\text{PROG}}$	t_{GHDX}	48 t_{CLCL}	–	ns
P2.7 ($\overline{\text{ENABLE}}$) high to V_{PP}	t_{EHSH}	48 t_{CLCL}	–	ns
V_{PP} setup to ALE/$\overline{\text{PROG}}$ low	t_{SHGL}	10	–	µs
V_{PP} hold after ALE/$\overline{\text{PROG}}$ low	t_{GHSL}	10	–	µs
ALE/$\overline{\text{PROG}}$ width	t_{GLGH}	90	110	µs
Address to data valid	t_{AVQV}	–	48 t_{CLCL}	ns
$\overline{\text{ENABLE}}$ low to data valid	t_{ELQV}	–	48 t_{CLCL}	ns
Data float after $\overline{\text{ENABLE}}$	t_{EHQZ}	0	48 t_{CLCL}	ns
ALE/$\overline{\text{PROG}}$ high to ALE/$\overline{\text{PROG}}$ low	t_{GHGL}	10	–	µs

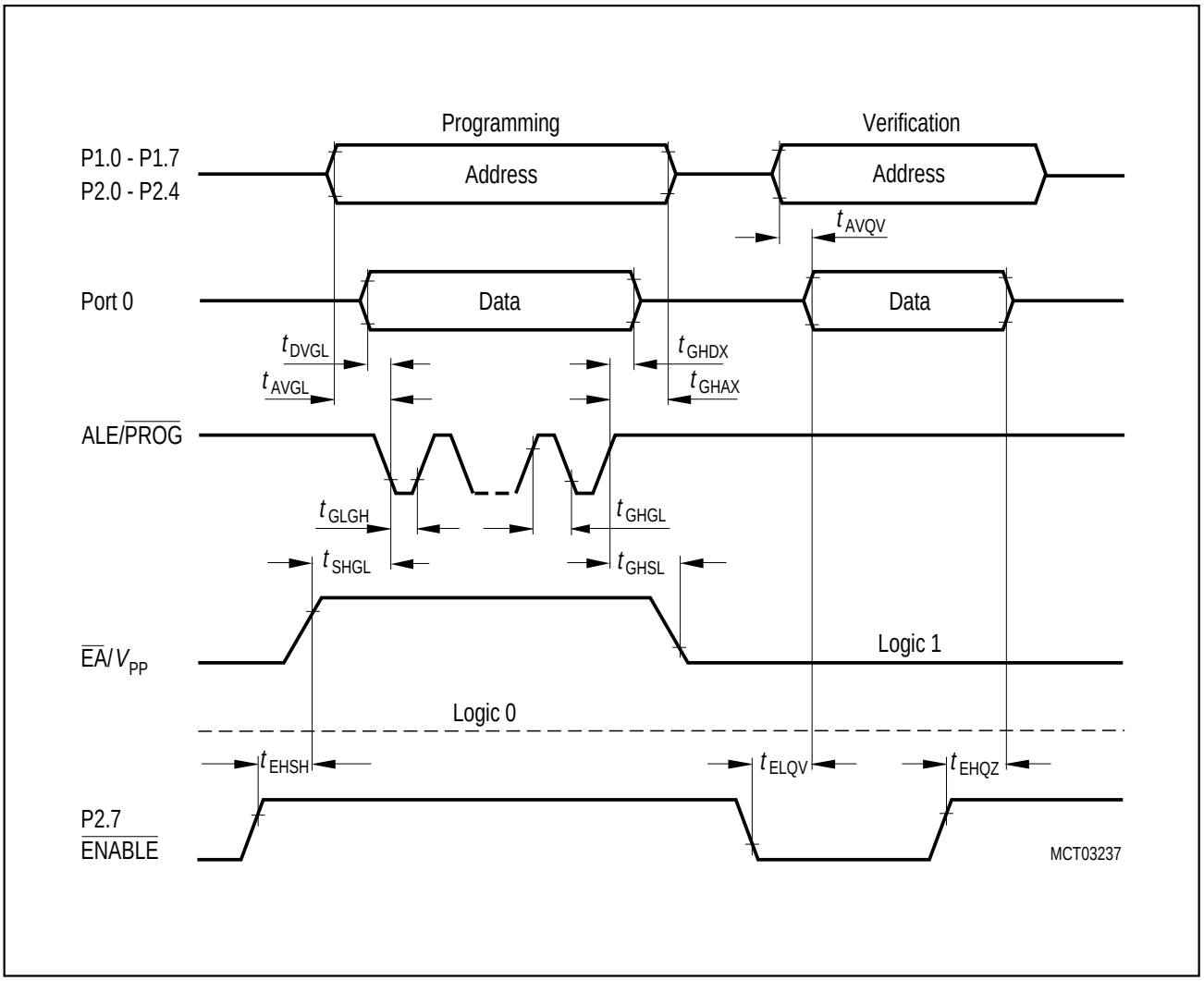
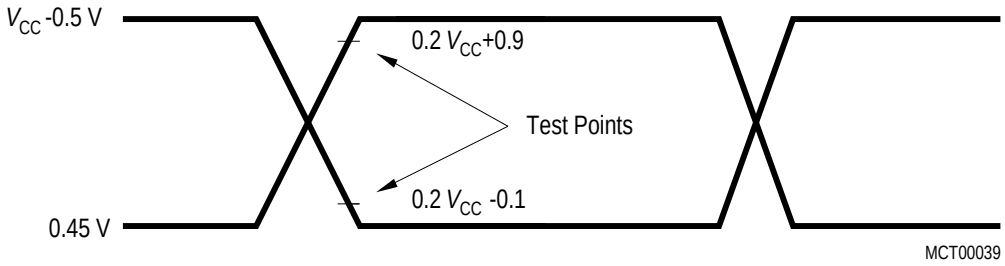
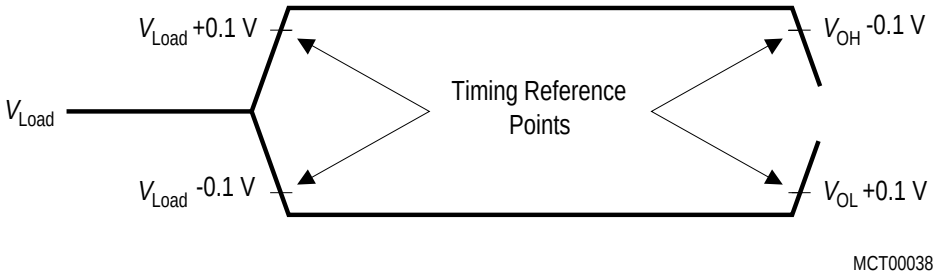


Figure 18
C501-1E OTP Memory Program/Read Cycle



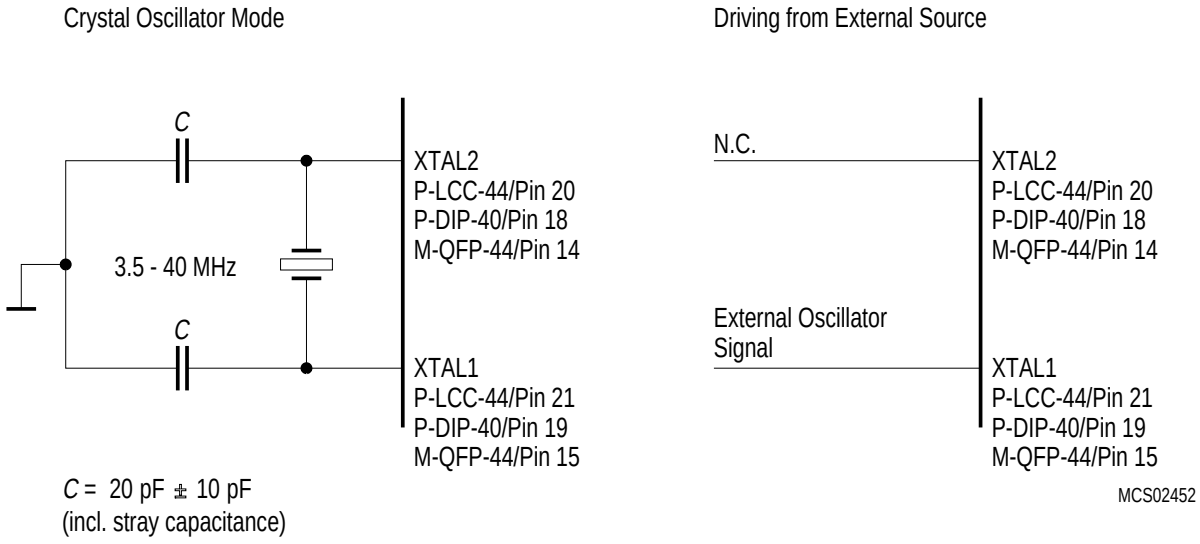
AC Inputs during testing are driven at V_{CC} – 0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

Figure 19
AC Testing: Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH} / V_{OL} level occurs.
I_{OL} / $I_{OH} \geq \pm 20$ mA.

Figure 20
AC Testing: Float Waveforms



Note: During programming and verification of the C501-1E OTP memory a clock signal of 4-6 MHz must be applied to the device.

Figure 21
Recommended Oscillator Circuits

Package Outlines

Plastic Package, P-DIP-40 for C501G-L / C501G-1R
(Plastic Dual in-Line Package)

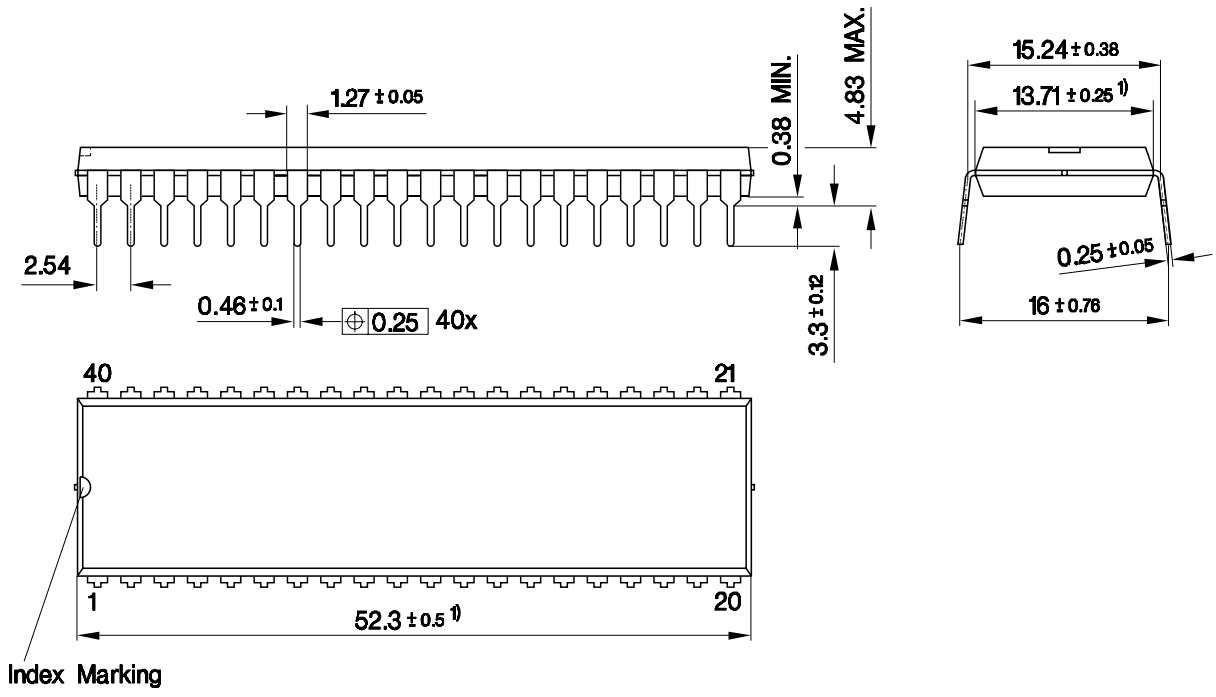


Figure 22
P-DIP-40 Package Outlines

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”

Dimensions in mm

Plastic Package, P-LCC-44 – SMD for C501G-L / C501G-1R / C501G-1E
(Plastic Leaded Chip-Carrier)

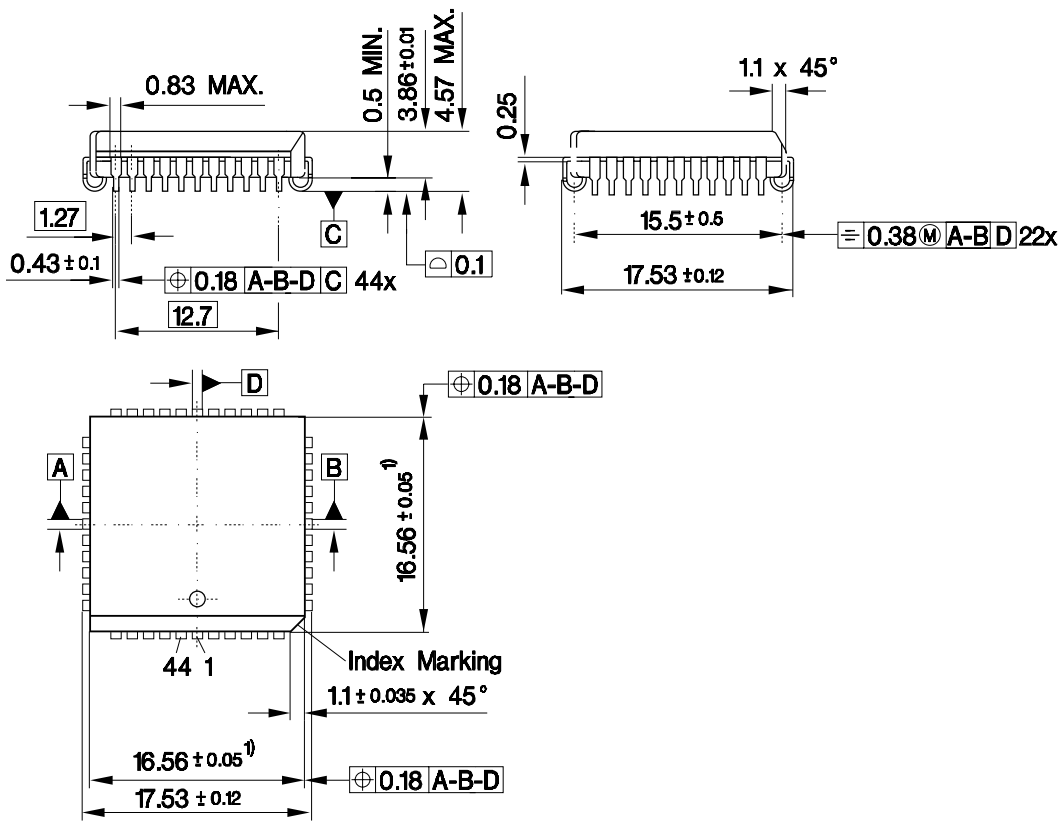


Figure 23
P-LCC-44 Package Outlines

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”
SMD = Surface Mounted Device

Dimensions in mm

Plastic Package, P-MQFP-44 – SMD for C501G-L / C501G-1R
(Plastic Metric Quad Flat Package)

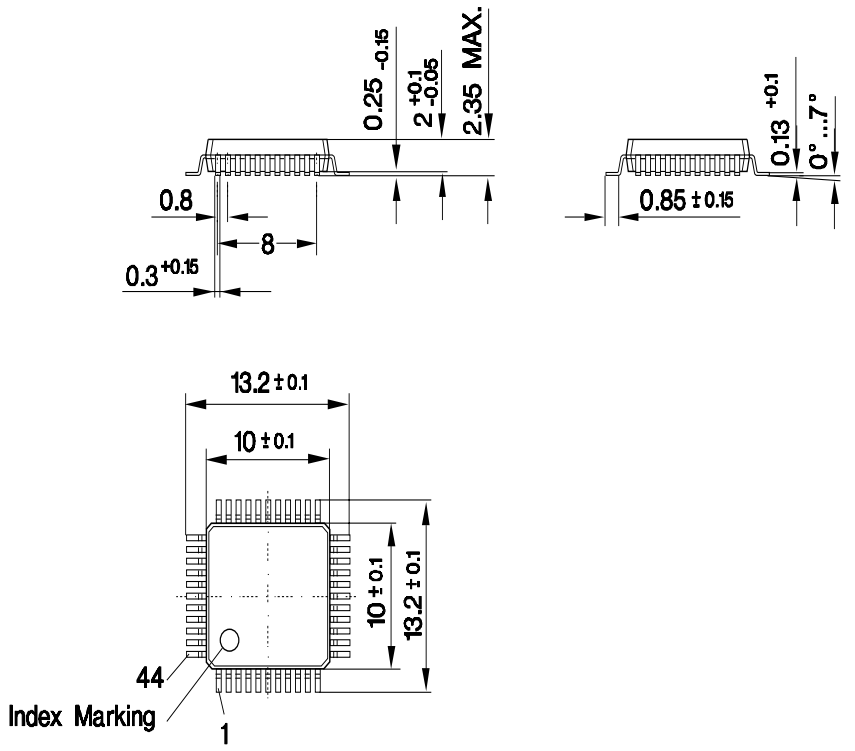


Figure 24
P-MQFP-44 Package Outlines

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”
SMD = Surface Mounted Device

Dimensions in mm