

High-Speed CMOS Bus Interface 16-Bit Transceiver in QVSOP™

QS74FCT2X646T

FEATURES/BENEFITS

- Function compatible to the 74F646, 74FCT646 and 74FCT646T
- CMOS power levels: <15mW static
- Undershoot clamp diodes on all inputs
- Fastest CMOS logic family available
- JEDEC-FCT spec compatible
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Available in 48-pin 0.4mm pitch QVSOP (Q1)
- A and C speed grades with 5.4ns t_{PD} for C
- $I_{OL} = 64mA$ Ind.

DESCRIPTION

The QS74FCT2X646T is a 16-bit high-speed CMOS TTL-compatible registered bus transceiver with three-state outputs that are ideal for driving high capacitance loads such as memory and address buses. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when V_{CC} is removed from the device.

Figure 1. Functional Block Diagram

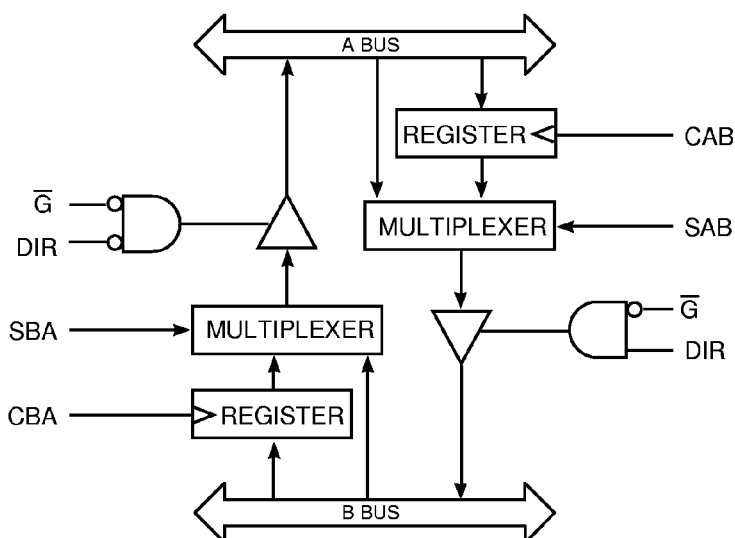


Figure 2. Pin Configuration
(All Pins Top View)

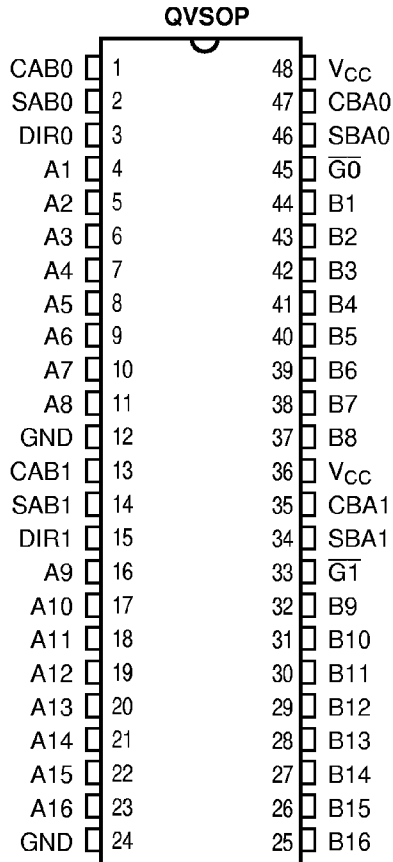


Table 1. Pin Description

Name	I/O	Description
A16-A1	I/O	A Bus
B16-B1	I/O	B Bus
CABi	I	Clock A to Register
CBAi	I	Clock B to Register
SABi	I	A Bus or Reg to B
SBAi	I	B Bus or Reg to A
DIRi	I	Direction, A → B or B → A
\overline{Gi}	I	Output Enable

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Table 2. Function Table

Inputs						Outputs		Function
\overline{G}	DIR	CAB	CBA	SAB	SBA	A	B	
H	—	—	—	—	—	Hi-Z	Hi-Z	Disabled
L	L	—	—	—	—	A	Hi-Z	Output A
L	H	—	—	—	—	Hi-Z	B	Output B
—	—	↑	—	—	—	—	—	Load A Reg
—	—	—	↑	—	—	—	—	Load B Reg
—	—	—	—	L	—	—	—	A Bus → B Bus
—	—	—	—	H	—	—	—	A Reg → B Bus
—	—	—	—	—	L	—	—	B Bus → A Bus
—	—	—	—	—	H	—	—	B Reg → A Bus

Note: CAB0, SAB0, DIR0, CBA0, SBA0, G0 control bits 8-1
CAB1, SAB1, DIR1, CBA1, SBA1, G1 control bits 9-16

Table 3. Absolute Maximum Ratings

Supply Voltage to Ground	-0.5V to 7.0V
DC Output Voltage V_{OUT}	-0.5V to 7.0V
DC Input Voltage V_{IN}	-0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	-3.0V
DC Input Diode Current with $V_{IN} < 0$	-20mA
DC Output Diode Current with $V_{OUT} < 0$	-50mA
DC Output Current Max. Sink Current/Pin	120mA
Maximum Power Dissipation	1.2 watts
T_{STG} Storage Temperature	-65° to 150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

Table 4. Capacitance

$T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$, $V_{IN} = 0\text{V}$, $V_{OUT} = 0\text{V}$

Pins	Max	Unit
1-11, 13-23, 25-35, 37-47	8	pF

Note: Capacitance is characterized but not production tested.

Table 5. Power Supply Characteristics

Symbol	Parameter	Test Conditions ⁽¹⁾	Min	Max	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$, Freq = 0 $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC}-0.2\text{V} \leq V_{IN} \leq V_{CC}$	—	3.0	mA
ΔI_{CC}	Supply Current per Input @ TTL HIGH ⁽²⁾	$V_{CC} = \text{Max.}$, $V_{IN} = 3.4\text{V}$, Freq = 0	—	2.0	mA
Q_{CCD}	Supply Current per Input per MHz ^(3,4)	$V_{CC} = \text{Max.}$, Outputs Open and Enabled One Bit Toggling @ 50% Duty Cycle Other Inputs at GND or V_{CC}	—	0.25	mA/ MHz

Notes:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input ($V_{IN} = 3.4\text{V}$).
3. For flip-flops, Q_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I_C can be computed using the above parameters as explained in the Technical Overview section.

Table 6. DC Electrical Characteristics Over Operating RangeIndustrial: $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions	Min	Typ ⁽¹⁾	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$ I_{IH} $ $ I_{IL} $	Input Current Input HIGH or LOW	$V_{CC} = \text{Max.}, 0 \leq V_{IN} < V_{CC}$	—	—	5	μA
$ I_{OZ} $	Off-State Output Current (Hi-Z)	$V_{CC} = \text{Max.}, 0 \leq V_{OUT} \leq V_{CC}$	—	—	5	μA
I_{OS}	Short Circuit Current ^(2,3)	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}$	-60	—	-225	mA
V_{IC}	Input Clamp Voltage ⁽³⁾	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$	—	-0.7	-1.2	V
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -15\text{mA}$	2.4	—	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 64\text{mA}$	—	—	0.55	V

Notes:

1. Typical values indicate $V_{CC} = 5.0\text{V}$ and $T_A = 25^{\circ}\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

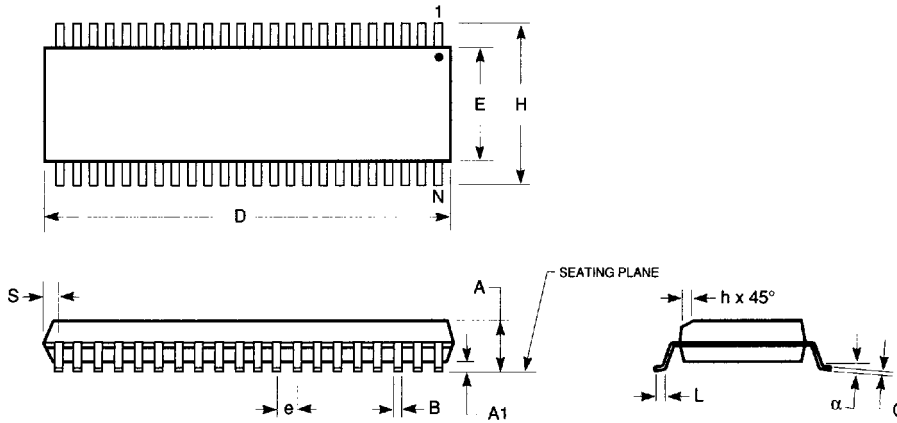
Table 7. Switching Characteristics Over Operating RangeIndustrial: $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 5.0\text{V} \pm 5\%$ $C_{LOAD} = 50\text{pF}$, $R_{LOAD} = 500\Omega$ unless otherwise noted.**5**

Symbol	Description ⁽¹⁾	2X646A		2X646C		Unit
		Min	Max	Min	Max	
t_{PHLB} t_{PLHB}	Bus to Bus Delay	2.0	6.3	1.5	5.4	ns
t_{PZH} t_{PZL}	Output Enable Time	2.0	9.8	1.5	7.8	ns
t_{PHZ} t_{PLZ}	Output Disable ⁽²⁾ Time	2.0	6.3	1.5	6.3	ns
t_{PHLC} t_{PLHC}	Clock to Bus Delay	2.0	6.3	1.5	5.7	ns
t_{PHLS} t_{PLHS}	SBA/SAB to Bus Delay	2.0	7.7	1.5	6.2	ns
t_S	Data Setup Time	2.0	—	2.0	—	ns
t_H	Data Hold Time	1.5	—	1.5	—	ns
t_{PWH} t_{PWL}	Clock Pulse Width ⁽²⁾ HIGH or LOW	5.0	—	5.0	—	ns

Notes:

1. Minimums guaranteed but not tested for all parameters except t_S and t_H .
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.

150-MIL QVSOP™ - Package Code Q1/Q2
150-Mil Wide Plastic Small Outline Gull-Wing



JEDEC#	MO-154BB			MO-154AB		
DWG#	PSS-40A (Q2)			PSS-48A (Q1)		
Symbol	Min	Nom	Max	Min	Nom	Max
A	0.059	0.065	0.069	0.059	0.065	0.069
A1	0.004	0.006	0.008	0.004	0.006	0.008
B	0.0067	0.008	0.009	0.0051	0.0063	0.008
C	0.0075	0.008	0.0098	0.0075	0.008	0.0098
D	0.386	0.390	0.394	0.386	0.390	0.394
E	0.150	0.154	0.157	0.150	0.154	0.157
e	0.0197 BSC, 0.5mm			0.0157 BSC, 0.4mm		
H	0.228	0.236	0.244	0.228	0.236	0.244
h	0.010	0.013	0.016	0.010	0.013	0.016
L	0.020	0.024	0.030	0.020	0.024	0.030
N	40			48		
α	0°	5°	8°	0°	5°	8°
S	0.006	0.008	0.010	0.012	0.014	0.016

Notes:

1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006in. per side.
5. Lead coplanarity is 0.003in. maximum.

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