



**High Speed CMOS
Bus Interface
18-Bit Universal Register
in QVSOP™**

QS74FCT2X823T

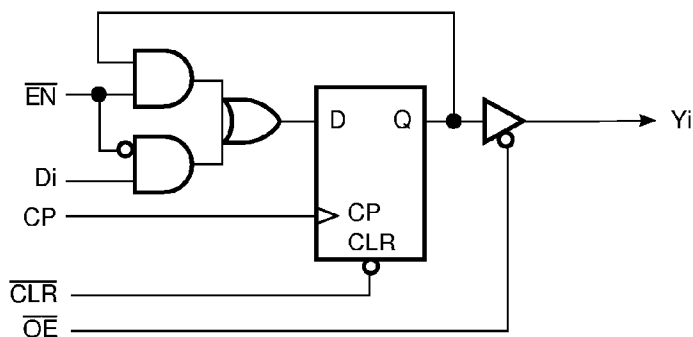
FEATURES/BENEFITS

- Function compatible to the 74F823, 74FCT823 and 74FCT823T
- CMOS power levels: <15 mW static
- Undershoot clamp diodes on all inputs
- Fastest CMOS logic family available
- JEDEC-FCT spec compatible
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Available in 48-pin 0.4 mm pitch QVSOP (Q1)
- A speed grades with 10.0 ns
- $I_{OL} = 48$ mA Conn.

DESCRIPTION

The QS74FCT2X823T is an 18-bit high-speed CMOS TTL-compatible buffered register with three-state outputs that is ideal for driving high capacitance loads such as memory and address buses. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when V_{CC} is removed from the device.

FUNCTIONAL BLOCK DIAGRAM



QS74FCT2X823T PRELIMINARY

PIN DESCRIPTION

Name	I/O	Description
Di	I	Data Inputs
Yi	O	Data Outputs-Three State
CPi	I	Clock Pulse
\overline{OE}	I	Output Enable
\overline{ENi}	I	Clock Enable
\overline{CLRi}	I	Asynchronous Reset

**PIN CONFIGURATIONS
(All Pins Top View)**

QVSOP

$\overline{OE0}$	1	48	VCC
D0	2	47	Y0
D1	3	46	Y1
D2	4	45	Y2
D3	5	44	Y3
D4	6	43	Y4
D5	7	42	Y5
D6	8	41	Y6
D7	9	40	Y7
D8	10	39	Y8
$\overline{CLR0}$	11	38	$\overline{EN0}$
GND	12	37	CP0
$\overline{OE1}$	13	36	VCC
D9	14	35	Y9
D10	15	34	Y10
D11	16	33	Y11
D12	17	32	Y12
D13	18	31	Y13
D14	19	30	Y14
D15	20	29	Y15
D16	21	28	Y16
D17	22	27	Y17
$\overline{CLR1}$	23	26	$\overline{EN1}$
GND	24	25	CP1

FUNCTION TABLE

Inputs					Int.	O/P	Function
\overline{OEi}	\overline{CLRi}	\overline{ENi}	DI	CPI	QI	YI	
H	X	L	L	↑	L	Hi-Z	High Z
H	X	L	H	↑	H	Hi-Z	High Z
H	L	X	X	X	L	Hi-Z	Clear
L	L	X	X	X	L	L	Clear
H	H	H	X	X	NC	Hi-Z	Hold
L	H	H	X	X	NC	NC	Hold
H	H	L	L	↑	L	Hi-Z	Load
H	H	L	H	↑	H	Hi-Z	Load
L	H	L	L	↑	L	L	Load
L	H	L	H	↑	H	H	Load