

# R2S15900SP

## 2ch Electronic Volume with Surround

REJ03F0126-0130

Rev.1.3

May 30, 2005

### Description

The R2S15900SP is an optimum audio signal processor IC for TV. It has a 5ch input selector, surround/pseudo stereo, tone control(2band), output gain control and 2ch master volume. It can control all of these functions with I<sup>2</sup>C bus.

### Features

Function	Features
Volume	0 to -84dB, -∞/ 1dB step Each channel is independence control.
Input selector	5 input selector + MUTE
Rec output	2 Rec output
Tone control	Bass: -15dB to +15dB/ 1dB step Treble: -15dB to +15dB/ 1dB step
Surround/ Pseudo stereo	Surround <Low/ High> Pseudo Stereo
Mode selector	Bypass/ Tone / Tone & Pseudo Stereo or Surround
Output gain control	0dB/ +4.5dB
MCU interface	I <sup>2</sup> C-BUS control.

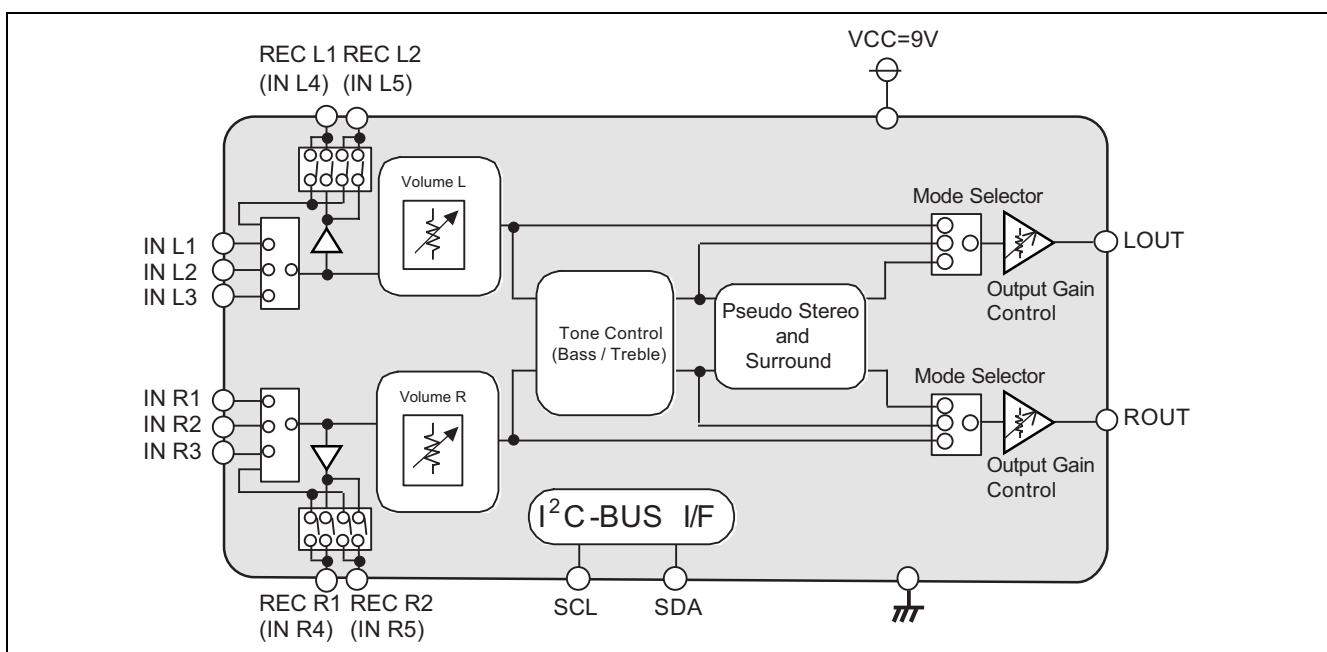
### Recommended Operating Condition

Supply voltage: V<sub>CC</sub> = 9.0V(typ)

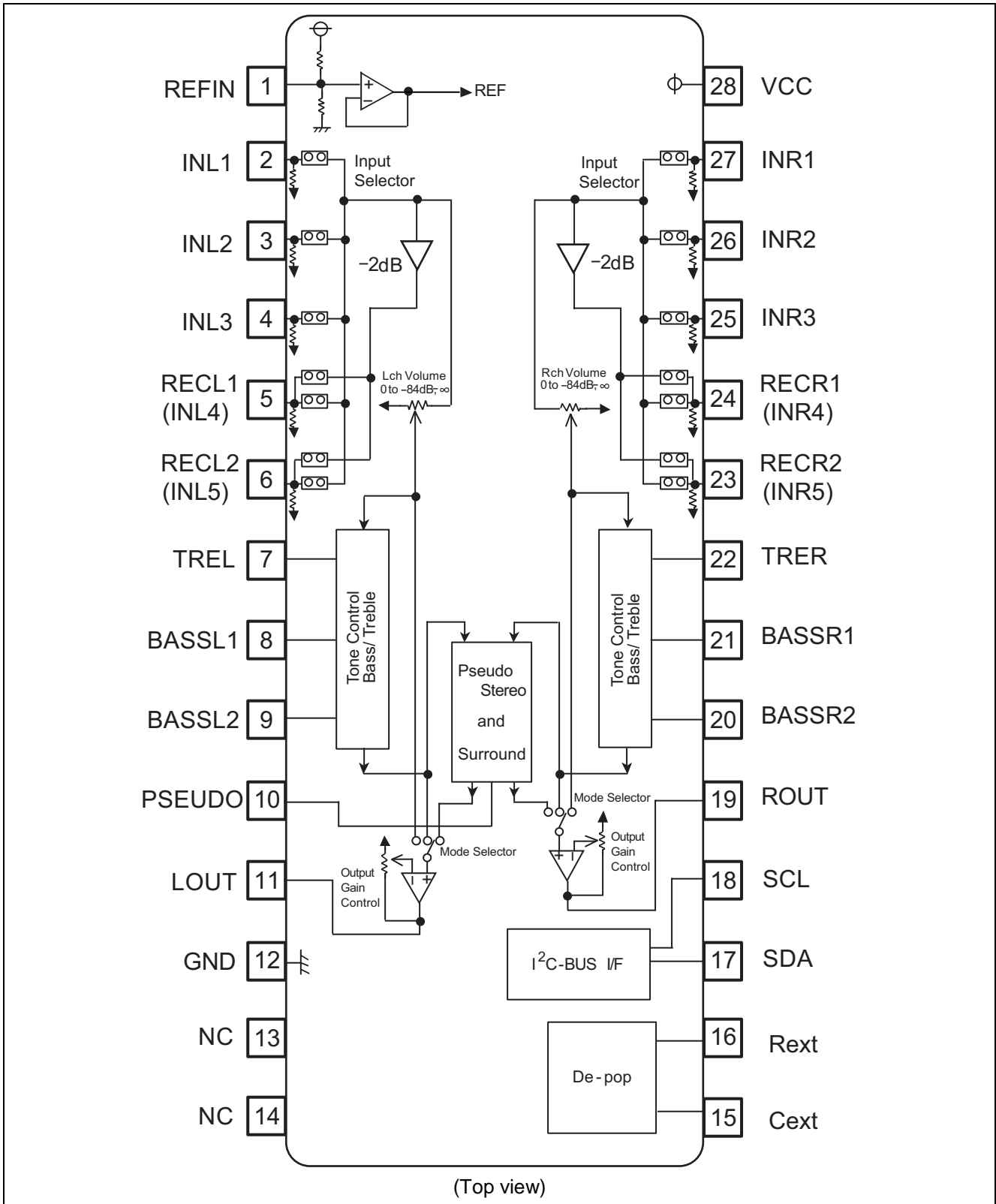
### Application

TV, Mini Stereo, etc.

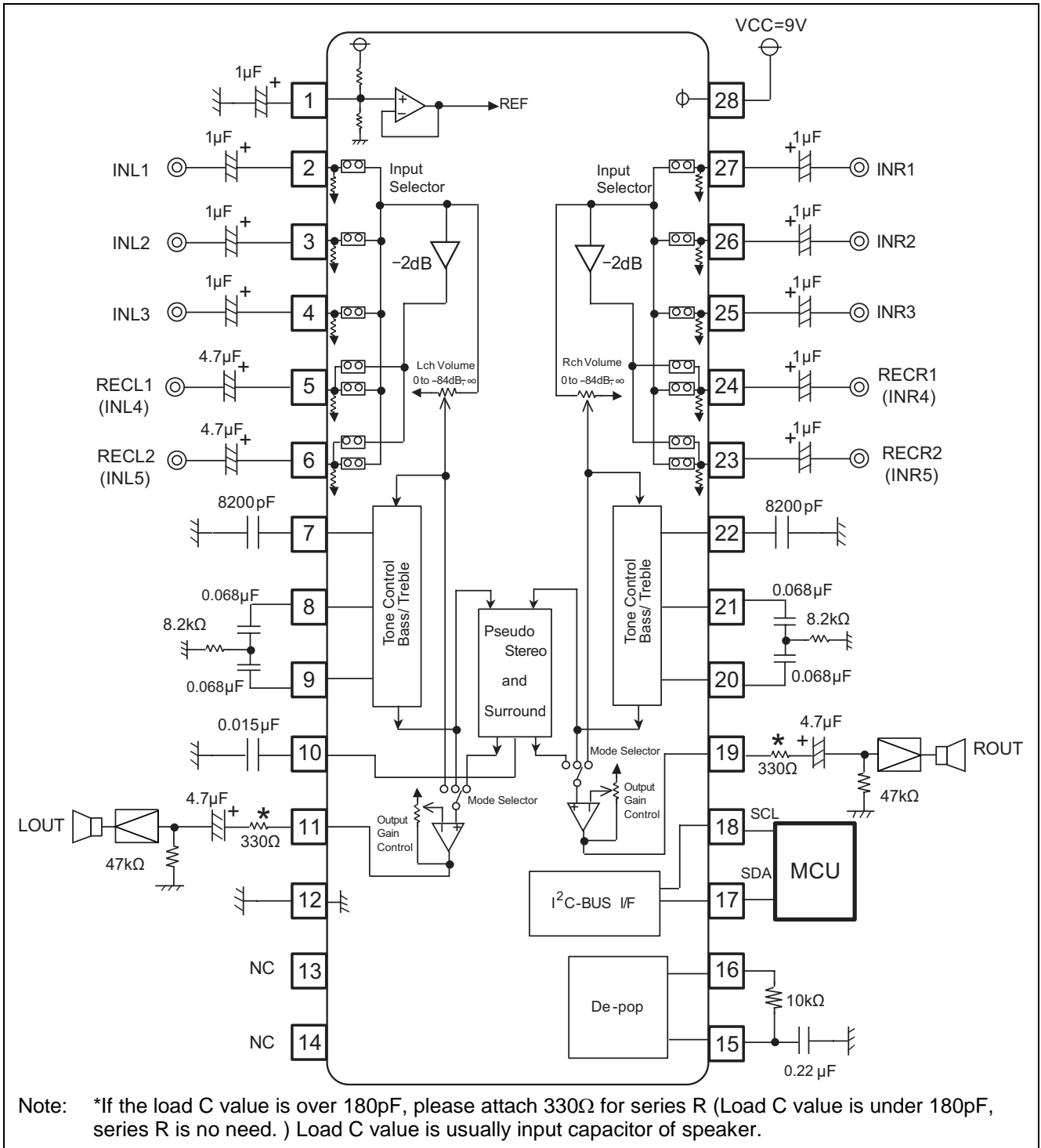
### System Configuration



Block Diagram and Pin Configuration



Application Example



**Absolute Maximum Ratings**

Parameter	Symbol	Ratings	Unit	Condition
Power supply	V <sub>CC</sub>	10	V	
Power dissipation	P <sub>d</sub>		W	T <sub>a</sub> ≤25°C
Thermal derating	K		mW/°C	T <sub>a</sub> >25°C (Circuit board installation)
Operating temperature	T <sub>opr</sub>	-20 to +75	°C	
Storage temperature	T <sub>stg</sub>	-40 to +125	°C	

## Electrical Characteristics

( $V_{CC}=9V$ ,  $T_a=25^{\circ}C$ ,  $V_i=100mV_{rms}$ ,  $f=1kHz$ , Tone control=0dB,  $R_g=0\Omega$ ,  $R_L=47k\Omega$ , unless otherwise noted)

### General Characteristics

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Operational power supply	$V_{CC}$	5.0	9.0	9.7	V	
Supply current	$I_{CC}$	—	15	25	mA	No signal
Reference voltage	$V_{ref}$	4.0	4.5	5.0	V	No signal
Input impedance	$R_{IN}$	17	25	33	$k\Omega$	
Maximum input voltage	$V_{IM}$	2.8	3.0	—	$V_{rms}$	$VOL=-20dB$ , THD=3%
Maximum output voltage	$V_{OM}$	—	2.5	—	$V_{rms}$	$VOL=0dB$ , THD=1%
Rec output gain	$G_{vrec}$	—	-2.0	—	dB	Rec out
Output gain	$G_{vout}$	—	4.5	—	dB	Output gain=4.5dB
Volume maximum	$VOL_{max}$	-2	0	+2	dB	$VOL=0dB$
Volume minimum	$VOL_{min}$	—	-85	-70	dB	$VOL=Mute$ , $V_i=1V_{rms}$ , IHF-A
Channel balance	$CBAL$	-1.5	0	1.5	dB	$VOL=0dB$
Total harmonic distortion	THD	—	—	0.5	%	400Hz to 30kHz BPF $V_o=0.5V_{rms}$
Input selector cross talk	CT	—	—	-70	dB	$V_i=1V_{rms}$ , IHF-A
Channel separation	CS	—	—	-70	dB	$V_i=1V_{rms}$ , IHF-A,
Output noise 1	$V_{no1}$	—	-90 (31.6)	-85 (56.2)	dBV ( $\mu V_{rms}$ )	$VOL=0dB$ , Output gain=0dB Tone=0dB, Surround ON, IHF-A
Output noise 2	$V_{no2}$	—	-103 (7)	-97 (14)	dBV ( $\mu V_{rms}$ )	$VOL=Mute$ , Output gain=0dB Bypass, IHF-A

### Tone Control

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Tone control voltage gain (Boost/Bass)	G (Bass) B	+12.5	+15	+17.5	dB	$f = 100Hz$ Bass= +15dB
Tone control voltage gain (Cut/Bass)	G (Bass) C	-17.5	-15	-12.5	dB	$f = 100Hz$ Bass = -15dB
Tone control voltage gain (Flat/Bass)	G (Bass) F	-2	0	+2	dB	$f = 100Hz$ Bass = 0dB
Tone control voltage gain (Boost/Treble)	G (Treble) B	+12.5	+15	+17.5	dB	$f = 10kHz$ Tre = +15dB
Tone control voltage gain (Cut/Treble)	G (Treble) C	-17.5	-15	-12.5	dB	$f = 10kHz$ Tre = -15dB
Tone control voltage gain (Flat/Treble)	G (Treble) F	-2	0	+2	dB	$f = 100Hz$ Tre = 0dB

### I<sup>2</sup>C BUS Interface

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Low level input voltage	$V_{IL}$	0	—	1.5	V	$V_{CC}=9V$
High level input voltage	$V_{IH}$	3	—	5	V	$V_{CC}=9V$
Maximum clock frequency	$f_{SCL}$			100	kHz	

Function Description

1. Tone Control Circuit

**<1> Bass Circuit**

**Boost**

$$f_o = \frac{1}{2\pi\sqrt{R_1(R_2+R_3)C_1C_2}} \text{ (Hz)}$$

$$Q \cong \frac{1}{C_1+C_2} \sqrt{\frac{C_1C_2R_2}{R_1}} \text{ (R}_3=0\text{)}$$

$$G_v = 20 \log \left[ \frac{\frac{R_2+R_3}{R_1} + 2}{\frac{R_3}{R_1} + 2} \right] \text{ (dB) (C}_1=C_2\text{)}$$

**Cut**

$$f_o = \frac{1}{2\pi\sqrt{R_1(R_2+R_3)C_1C_2}} \text{ (Hz)}$$

$$Q \cong \frac{1}{C_1+C_2} \sqrt{\frac{C_1C_2R_2}{R_1}} \text{ (R}_3=0\text{)}$$

$$G_v = 20 \log \left[ \frac{\frac{R_3}{R_1} + 2}{\frac{R_2+R_3}{R_1} + 2} \right] \text{ (dB) (C}_1=C_2\text{)}$$

**<2> Treble Circuit**

**Boost**

$$G_v = 20 \log \left[ \frac{R_1+R_2}{R_1} \right] \text{ (dB)}$$

**Cut**

$$G_v = 20 \log \left[ \frac{R_1}{R_1+R_2} \right] \text{ (dB)}$$

## I<sup>2</sup>C Bus Format

MSB		LSB		MSB		LSB		MSB		LSB	
S	Slave Address	A	Sub Address	A	Data	A	P				
1 bit	8bit	1 bit	8bit	1 bit	8bit	1 bit	1bit				

S: Starting Term

A: Acknowledge Bit

P: Stop Term

If more than one Data Byte is transmitted, then the significant SUB ADDRESS bits are auto incremented.

00H → 01H → 02H → 03H → 04H → 00H

### 1. Slave Address

MSB							LSB
1	0	0	0	0	0	1	R/W <sub>B</sub>

R/W<sub>B</sub> = 0: Write mode for register setting

R/W<sub>B</sub> = 1: Not available

### 2. Sub Address Table

Sub Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	Lch VOL<H>				Lch VOL<L>			
01H	Rch VOL<H>				Rch VOL<L>			
02H	Input selector			Rec output		Output gain	Lch mute	Rch mute
03H	Bass					Surround level	Mode selector	
04H	Treble					0	0	0

Default values are all "0".

### 3. Data Table

#### <1> Master Volume Control (Sub Address: 00H, 01H)

VOL ATT (dB)	VOL<H>			
	D7	D6	D5	D4
0	0	0	0	0
-10	0	0	0	1
-20	0	0	1	0
-30	0	0	1	1
-40	0	1	0	0
-50	0	1	0	1
-60	0	1	1	0
-70	0	1	1	1
-80	1	0	0	0

VOL ATT (dB)	VOL<L>			
	D3	D2	D1	D0
0	0	0	0	0
-1	0	0	0	1
-2	0	0	1	0
-3	0	0	1	1
-4	0	1	0	0
-5	0	1	0	1
-6	0	1	1	0
-7	0	1	1	1
-8	1	0	0	0
-9	1	0	0	1

Example: If the volume of the Lch is set to -28dB, the Data byte is transmitted as follows:

Sub Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	0	0	1	0	1	0	0	0

## &lt;2&gt; Input Selector (Sub Address: 02H)

Input	Input selector			REC1	REC2
	D7	D6	D5	D4	D3
All OFF	0	0	0	A	A
IN1	0	0	1	A	A
IN2	0	1	0	A	A
IN3	0	1	1	A	A
IN4	1	0	0	1	A
IN5	1	0	1	A	1

If A=0 means REC1 or REC2 output ON, then A=1 means REC1 or REC2 output OFF.

## &lt;3&gt; Output Gain (Sub Address: 02H)

Gain	Output gain
	D2
0dB	0
+4.5dB	1

## &lt;5&gt; Surround Mode (Sub Address: 03H)

Surround level	Surround level
	D2
Low level	0
High level	1

## &lt;4&gt; Mute Function (Sub Address: 02H)

Mute	Lch	Rch
	D1	D0
Mute ON	0	0
Mute OFF	1	1

## &lt;6&gt; Mode Selector (Sub Address: 03H)

Mode	Mode selector	
	D1	D0
Bypass	0	0
Tone	0	1
Tone & Pseudo stereo	1	0
Tone & Surround	1	1

## &lt;7&gt; Tone Control (Sub Address: 03H Bass, 04H Treble)

Gain (dB)	Bass/ Treble				
	D7	D6	D5	D4	D3
0	A	0	0	0	0
1		0	0	0	1
2		0	0	1	0
3		0	0	1	1
4		0	1	0	0
5		0	1	0	1
6		0	1	1	0
7		0	1	1	1
8		1	0	0	0
9		1	0	0	1
10		1	0	1	0
11		1	0	1	1
12		1	1	0	0
13		1	1	0	1
14		1	1	1	0
15		1	1	1	1

If A=0 means Tone control gain CUT(-), then A=1 means Tone control gain BOOST(+).



## RENESAS Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.  
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.  
The information described here may contain technical inaccuracies or typographical errors.  
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.  
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.  
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.



### RENESAS SALES OFFICES

<http://www.renesas.com>

Refer to "<http://www.renesas.com/en/network>" for the latest and detailed information.

#### **Renesas Technology America, Inc.**

450 Holger Way, San Jose, CA 95134-1368, U.S.A  
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

#### **Renesas Technology Europe Limited**

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.  
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

#### **Renesas Technology Hong Kong Ltd.**

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong  
Tel: <852> 2265-6688, Fax: <852> 2730-6071

#### **Renesas Technology Taiwan Co., Ltd.**

10th Floor, No.99, Fushing North Road, Taipei, Taiwan  
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

#### **Renesas Technology (Shanghai) Co., Ltd.**

Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China  
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

#### **Renesas Technology Singapore Pte. Ltd.**

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632  
Tel: <65> 6213-0200, Fax: <65> 6278-8001