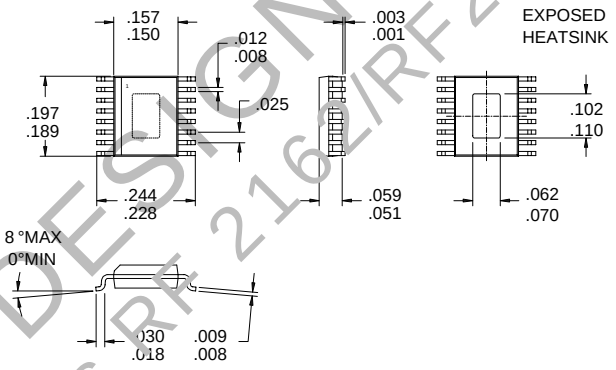
DUAL-MODE CDMA/AMPS OR TDMA/AMPS 3V POWER AMPLIFIER

Typical Applications

- 3V CDMA/AMPS Cellular Handsets
- 3V JCDMA/TACS Cellular Handsets
- 3V TDMA/AMPS Cellular Handsets
- Spread-Spectrum Systems
- CDPD Portable Data Cards
- Portable Battery-Powered Equipment

Product Description

The RF2152 is a high-power, high-efficiency linear amplifier IC targeting 3V handheld systems. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in dual-mode 3V CDMA/AMPS handheld digital cellular equipment, spread-spectrum systems, and other applications in the 800MHz to 950MHz band. The device is self-contained with 50Ω input and the output can be easily matched to obtain optimum power, efficiency, and linearity characteristics. The package is a PSSOP-16 with backside ground.

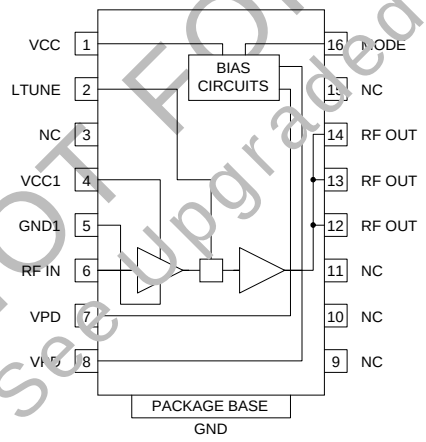


Refer to "Handling of PSOP and PSSOP Products" on page 16-15 for special handling information.

Package Style: PSSOP-16

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 3V Supply
- 28dBm Linear Output Power
- 30dB Linear Gain
- 35% Linear Efficiency
- On-board Power Down Mode
- 800MHz to 960MHz Operation

Ordering Information

RF2152	Dual-Mode CDMA/AMPS or TDMA/AMPS 3V Power Amplifier
RF2152 PCBA-N	Fully Assembled Evaluation Board 824-849MHz
RF2152 PCBA-J	Fully Assembled Evaluation Board 877-924MHz

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
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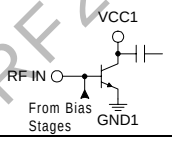
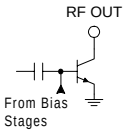
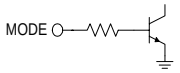
Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (RF off)	+8.0	V_{DC}
Supply Voltage ($P_{OUT} \leq 31$dBm)	+5.2	V_{DC}
DC Supply Current	1.0	A
Mode Voltage (V_{MODE})	+3.0	V_{DC}
Control Voltage (V_{PD})	+3.0	V_{DC}
Input RF Power	+12	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C
Moisture Sensitivity	JEDEC LEVEL 5	

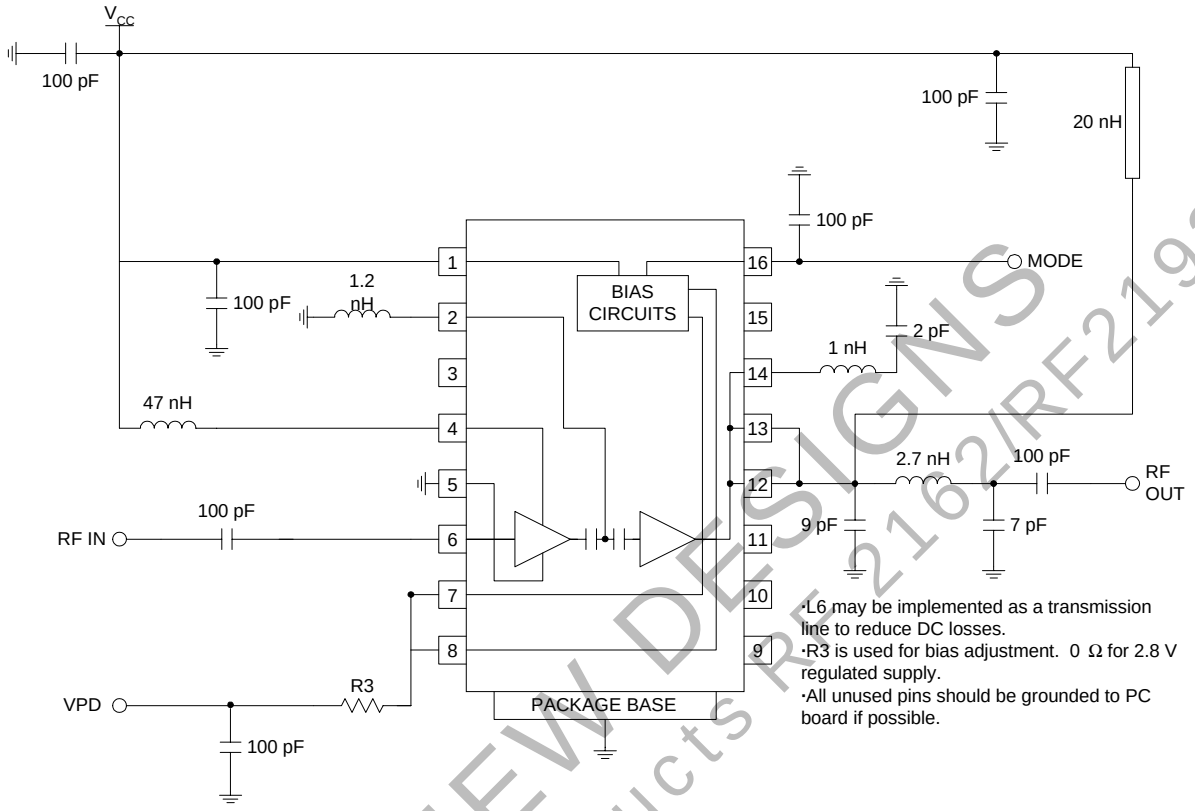
Refer to "Handling of PSOP and PSSOP Products" on page 16-15 for special handling information.

Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.4V, V_{PD}=2.8V, Freq=824MHz to 849MHz, unless otherwise specified
Usable Frequency Range	800		960	MHz	
Typical Frequency Range		824-849		MHz	
		877-925		MHz	
Linear Gain	28	30	33	dB	Pout=28dBm
Second Harmonic (including second harmonic trap)	-32	-38	-42	dBc	
Max CW Output Power	31	31.5	32	dBm	Tuned for CDMA
Total Efficiency (AMPS mode)	40	45	55	%	
Maximum Linear Output Power (CDMA Modulation)	28	28.5	29	dBm	Tuned for CDMA
Total Linear Efficiency	30	35	38	%	
Adjacent Channel Power Rejection	-44	-46	-50	dBc	ACPR@885kHz
Adjacent Channel Power Rejection	-56	-58	-62	dBc	ACPR@1980kHz
Input VSWR		< 2:1			
Output Load VSWR			10:1		No oscillations
Noise Figure		6.0	6.1	dB	V_{CC}=3.4V
Noise Power P_{OUT}=15dBm		86.5		dBm	V_{CC}=3.4V; 30KHz BW; RX Band NP measured from TX center band to RX center band
P_{OUT}=28dBm		89.3		dBm	
P_{OUT}=31dBm		92.3		dBm	
Power Supply					
Power Supply Voltage	3.0	3.4	5.2	V	
Idle current		90		mA	MODE = low Pin 16=Ground AMPS/Low Power CDMA Modes
Idle current		200		mA	MODE = high Pin 16=2.8V High Power CDMA Mode (Pout>20dBm)
V_{PD} current		10		mA	Pins7,8, Vpd=2.8V (Pin 7 typ. not connected, I=5mA for Pin 8)
Turn On/Off time			<100	ns	
Total Current (Power down)			10	µA	V_{PD} = low
V_{PD} "Low" Voltage		0	0.2	V	
V_{PD} "High" Voltage	2.7	2.8	2.9	V	
MODE "High" Voltage	2.1	2.8	2.9		
MODE "Low" Voltage		0	0.5		

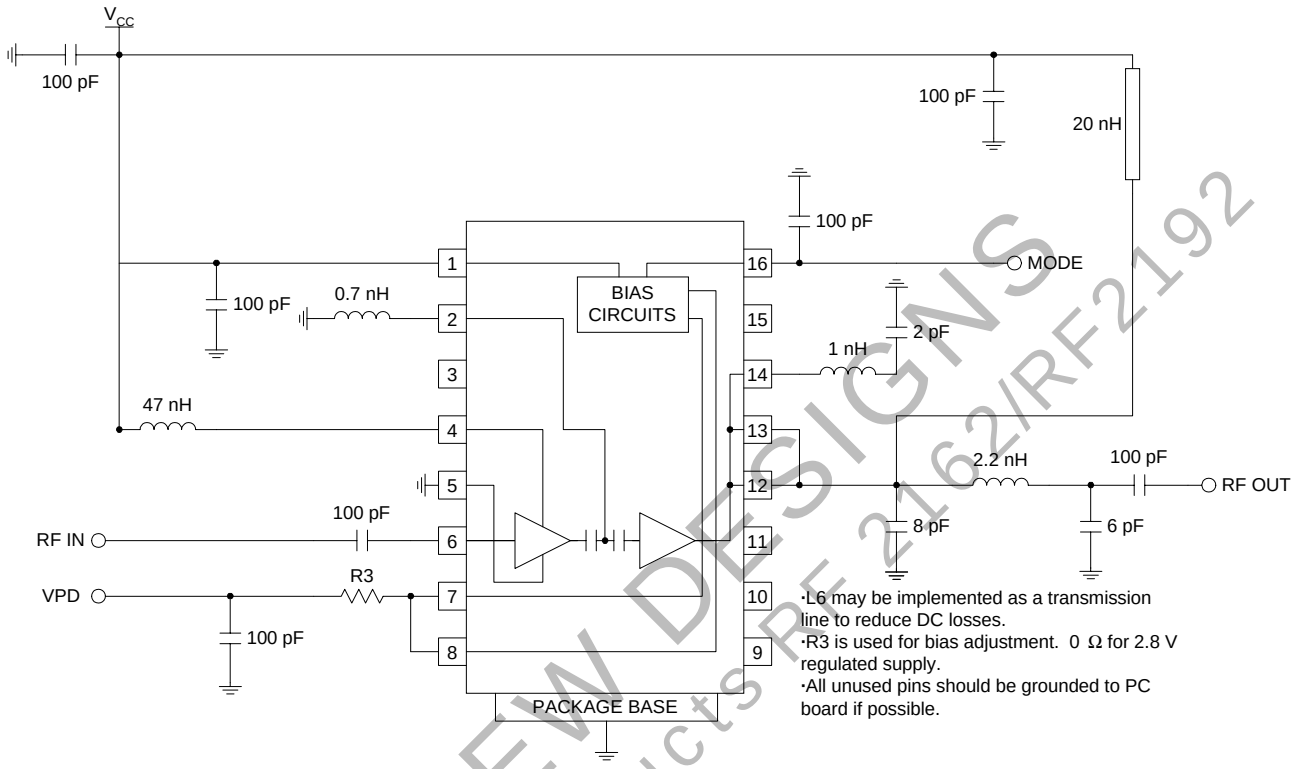
Pin	Function	Description	Interface Schematic
1	VCC	Power supply for input bias circuitry. A 100 pF high frequency bypass capacitor is recommended.	
2	LTUNE	Interstage tuning. This pin will connect to a shunt inductor used for interstage tuning. For 824MHz to 849MHz a 1.5nH discrete inductor is used; for 877MHz to 925MHz a shorted transmission line presenting 0.7 nH of inductance or discrete inductor may be used. This inductor should be placed as close to the pin as possible.	
3	NC	No connection. Grounding pin is recommended.	
4	VCC1	Power supply for stage 1. V_{CC} should be fed through a 25nH or greater inductor with a decoupling capacitor on the V_{CC} side.	See pin 6.
5	GND1	Ground for stage 1. Keep traces physically short and connect immediately to ground plane for best performance. This ground should be isolated from the backside ground contact.	See pin 6.
6	RF IN	RF input. An external DC blocking capacitor is required if this port is connected to a DC path to ground or a DC voltage.	
7	VPD	Power Down control. When this pin is “low”, all circuits are shut off. When this pin is 2.8 volts, all circuits are operating normally. V_{PD} requires a regulated 2.8 V for the amplifier to operate properly over all specified temperature and voltage ranges. A dropping resistor from a higher regulated voltage may be used to provide the required 2.8 V. A 100 pF high frequency bypass capacitor is recommended.	
8	VPD	Connect to pin 7.	
9	NC	No connection. Grounding pin is recommended.	
10	NC	No connection. Grounding pin is recommended.	
11	NC	No connection. Grounding pin is recommended.	
12	RF OUT	RF output and power supply for the output stage. The bias for the output stage is provided through this pin and pin 13. An external matching network is required to provide the optimum load impedance; see the application schematics for details. The first shunt cap of the matching circuit should be placed as close to the pin as possible.	
13	RF OUT	Same as pin 12.	See pin 12.
14	RF OUT	Harmonic trap. This pin connects to the RF output but is used for providing a low impedance to the second harmonic of the operating frequency. An inductor or transmission line resonating with a shunt capacitor at $2f_0$ is connected to this pin.	See pin 12.
15	NC	No connection. Grounding pin is recommended.	
16	MODE	The mode pin allows higher efficiency operation in AMPS and low power CDMA modes. MODE should be set “low” for highest efficiency in AMPS/TACS and in low power (<+15 dBm) CDMA operation. MODE should be set “high” for best linearity in high power CDMA operation.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

Application Schematic
824MHz to 849MHz



- L6 may be implemented as a transmission line to reduce DC losses.
- R3 is used for bias adjustment. 0 Ω for 2.8 V regulated supply.
- All unused pins should be grounded to PC board if possible.

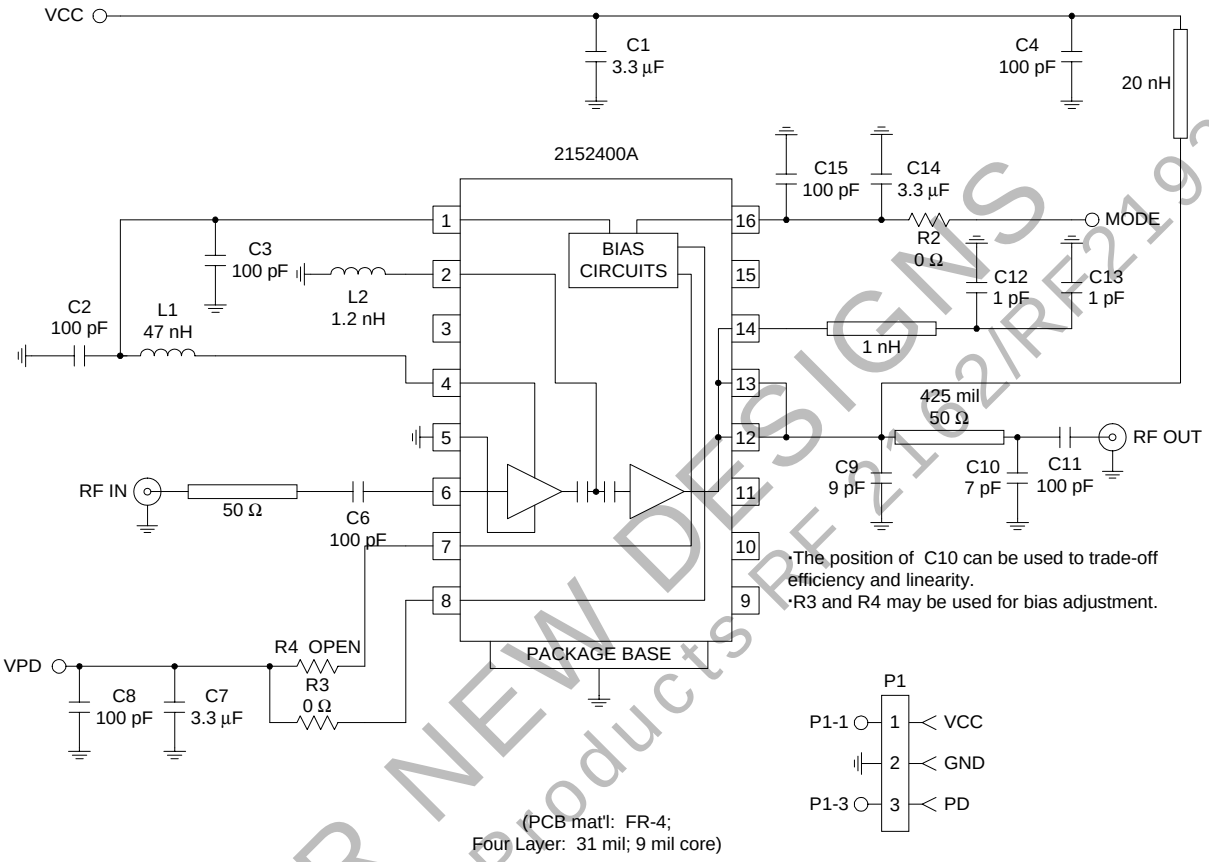
Application Schematic
877MHz to 924MHz



·L6 may be implemented as a transmission line to reduce DC losses.
·R3 is used for bias adjustment. 0 Ω for 2.8 V regulated supply.
·All unused pins should be grounded to PC board if possible.

Evaluation Board Schematic
824MHz to 849MHz

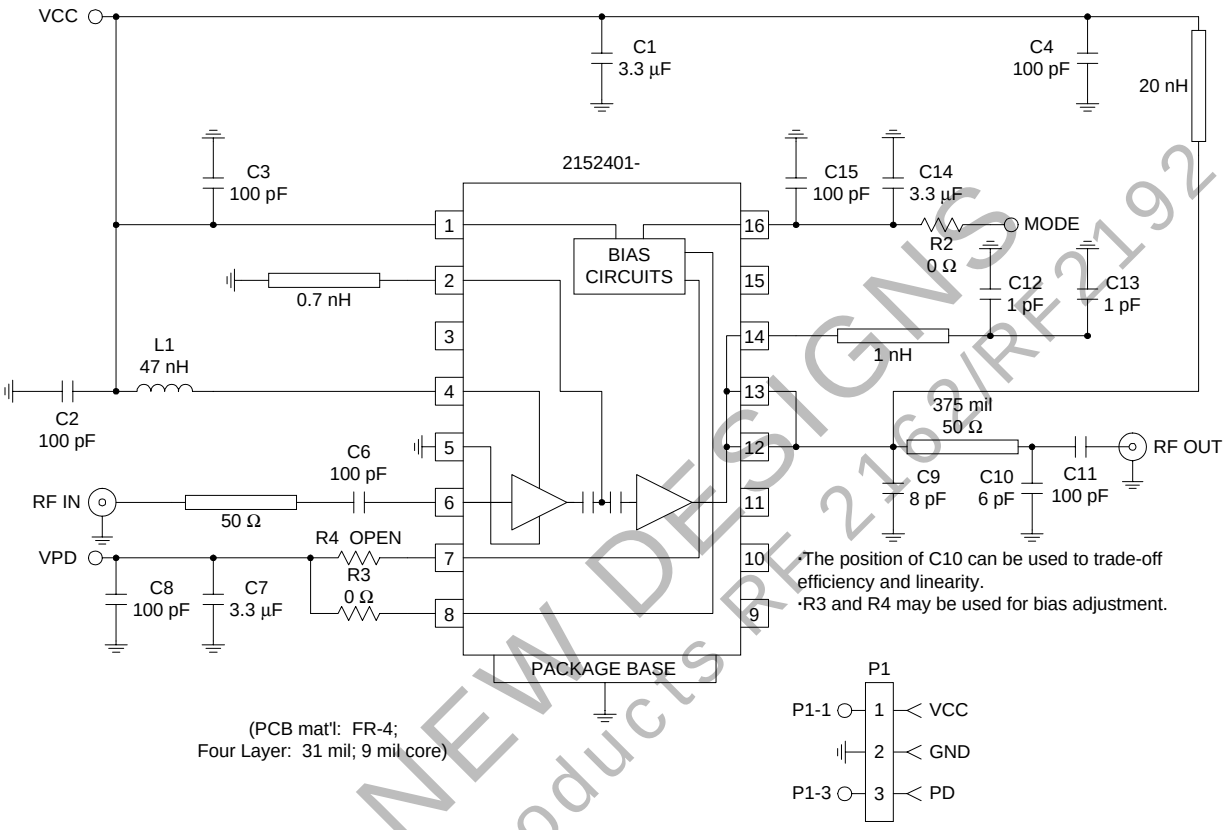
(Download Bill of Materials from www.rfmd.com.)



- The position of C10 can be used to trade-off efficiency and linearity.
- R3 and R4 may be used for bias adjustment.

(PCB mat'l: FR-4;
Four Layer: 31 mil; 9 mil core)

Evaluation Board Schematic
877MHz to 924MHz

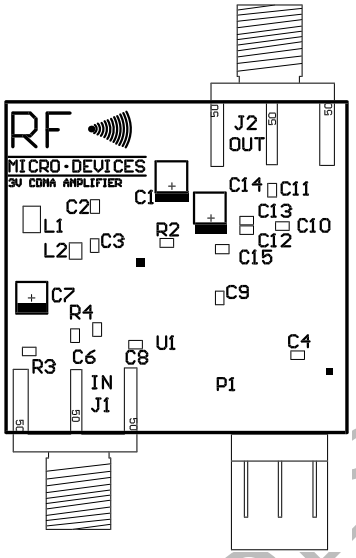


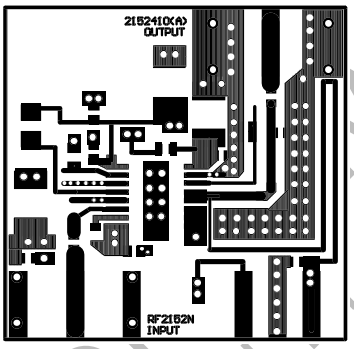
•The position of C10 can be used to trade-off efficiency and linearity.
•R3 and R4 may be used for bias adjustment.

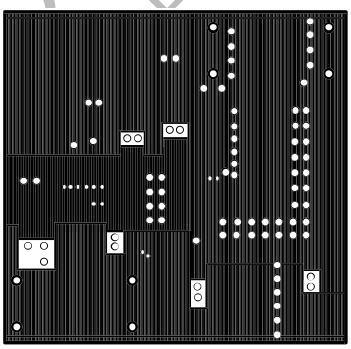
(PCB mat'l: FR-4;
Four Layer: 31 mil; 9 mil core)

Evaluation Board Layout 824MHz to 849MHz
1” x 1”

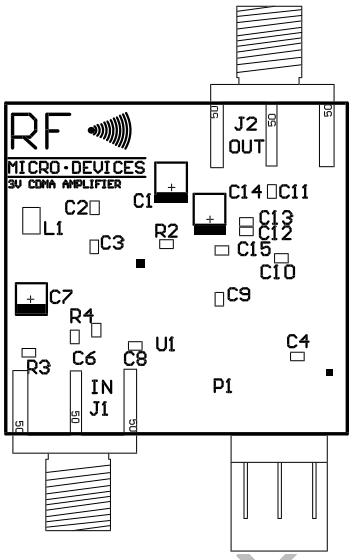
Board Thickness 0.034”, Board Material FR-4, Multi-Layer

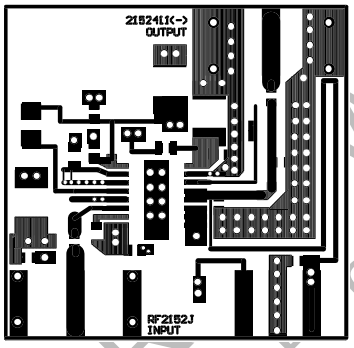


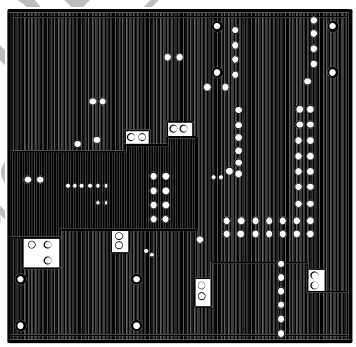


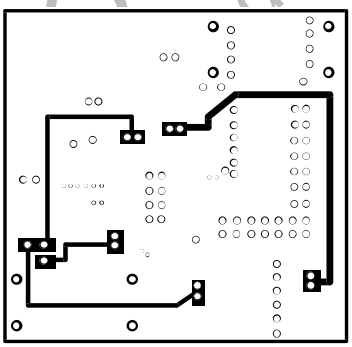


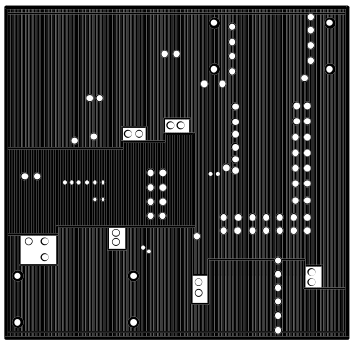
Evaluation Board Layout 877MHz to 924MHz
1" x 1"



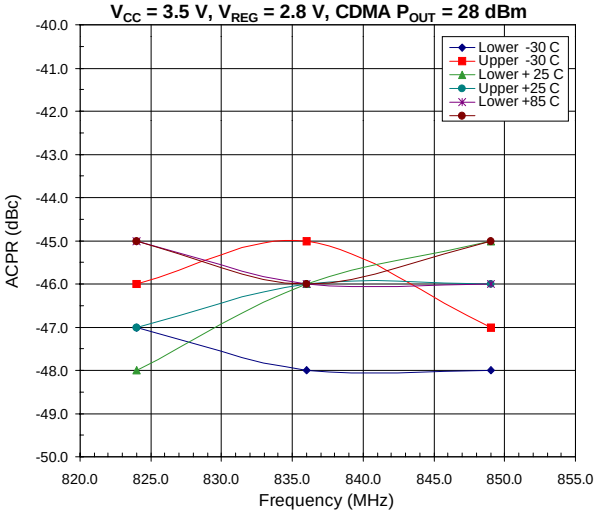




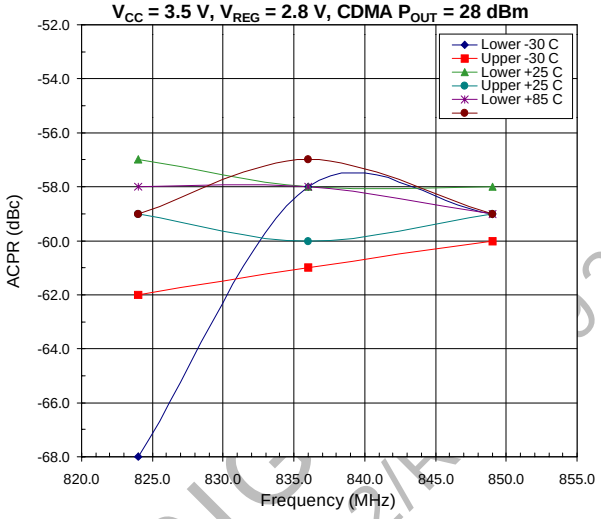




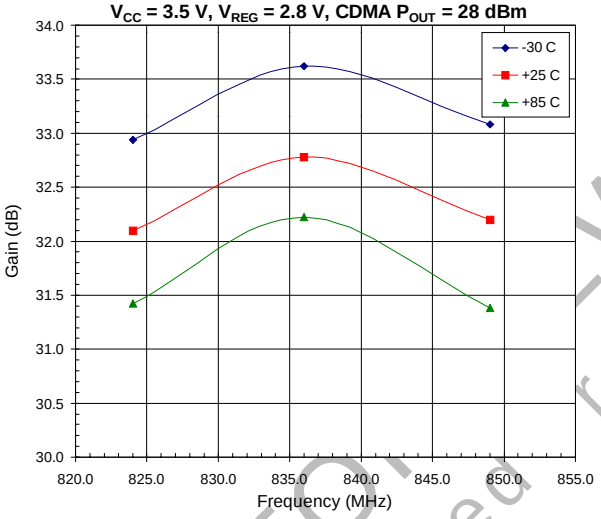
ACPR (@885 kHz offset) versus Frequency
V_{CC} = 3.5 V, V_{REG} = 2.8 V, CDMA P_{OUT} = 28 dBm



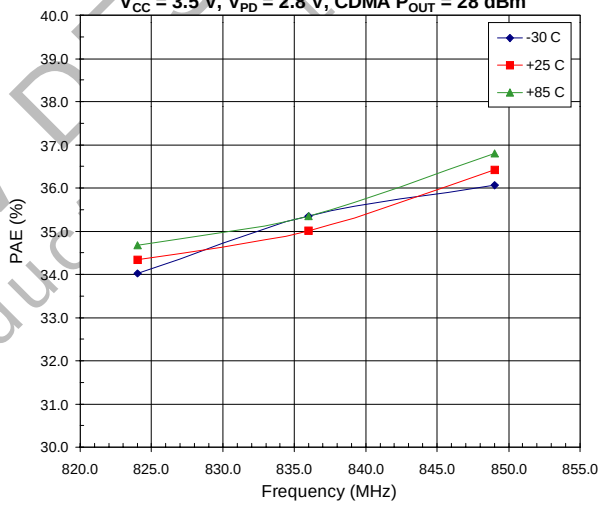
ACPR (@1980 kHz offset) versus Frequency
V_{CC} = 3.5 V, V_{REG} = 2.8 V, CDMA P_{OUT} = 28 dBm



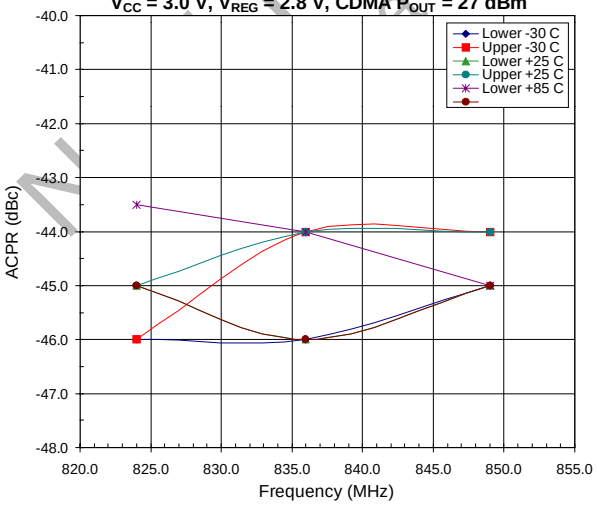
Gain versus Frequency
V_{CC} = 3.5 V, V_{REG} = 2.8 V, CDMA P_{OUT} = 28 dBm



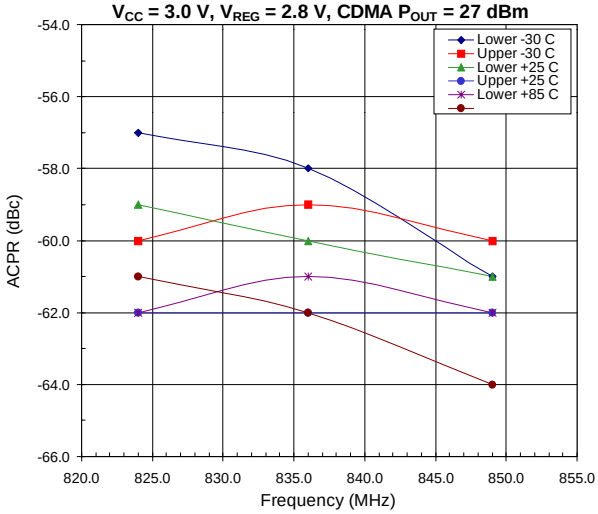
PAE versus Frequency
V_{CC} = 3.5 V, V_{PD} = 2.8 V, CDMA P_{OUT} = 28 dBm



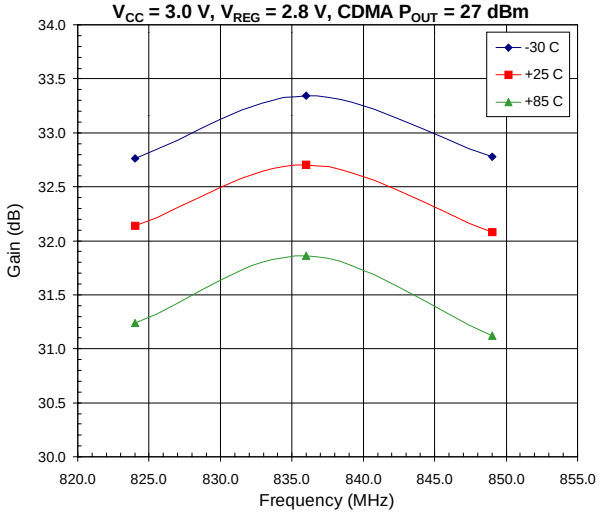
ACPR (@885 kHz offset) versus Frequency
V_{CC} = 3.0 V, V_{REG} = 2.8 V, CDMA P_{OUT} = 27 dBm



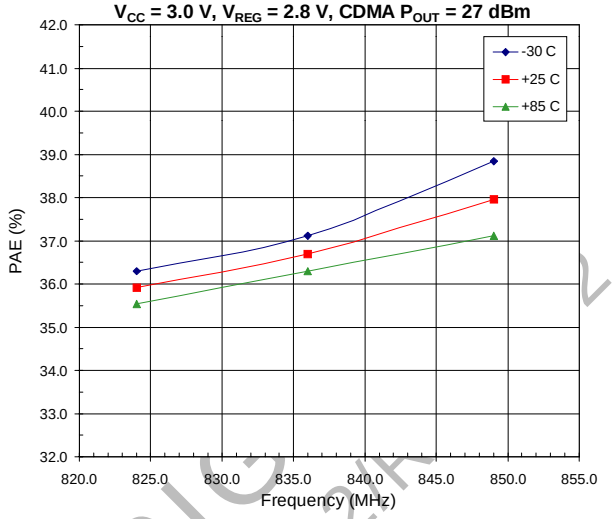
ACPR (@1908 kHz offset) versus Frequency
V_{CC} = 3.0 V, V_{REG} = 2.8 V, CDMA P_{OUT} = 27 dBm



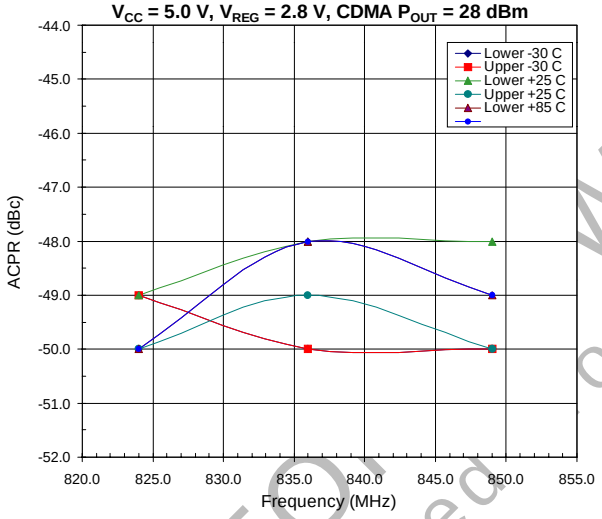
Gain versus Frequency
V_{CC} = 3.0 V, V_{REG} = 2.8 V, CDMA P_{OUT} = 27 dBm



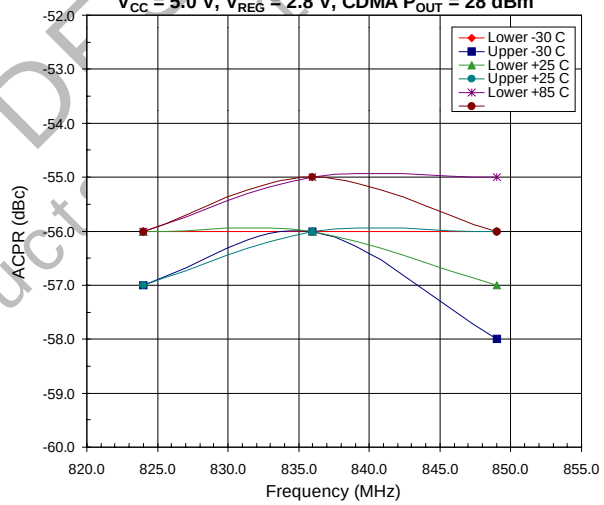
PAE versus Frequency
V_{CC} = 3.0 V, V_{REG} = 2.8 V, CDMA P_{OUT} = 27 dBm



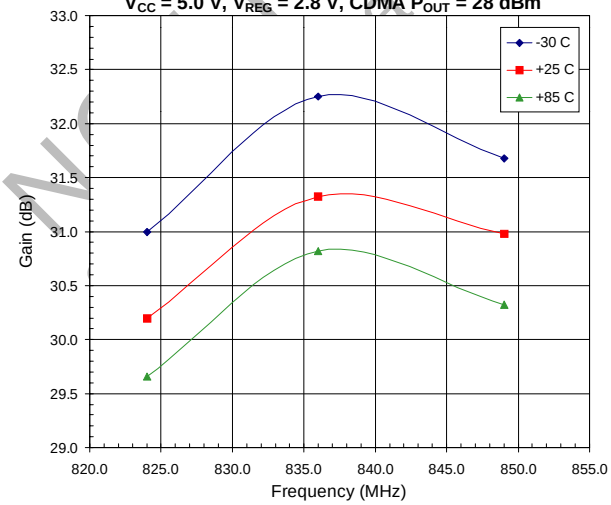
ACPR (@885 kHz offset) versus Frequency
V_{CC} = 5.0 V, V_{REG} = 2.8 V, CDMA P_{OUT} = 28 dBm



ACPR (@1908 kHz offset) versus Frequency
V_{CC} = 5.0 V, V_{REG} = 2.8 V, CDMA P_{OUT} = 28 dBm



Gain versus Frequency
V_{CC} = 5.0 V, V_{REG} = 2.8 V, CDMA P_{OUT} = 28 dBm



PAE versus Frequency
V_{CC} = 5.0 V, V_{REG} = 2.8V, CDMA P_{OUT} = 27 dBm