

**16A, 60V, 0.047 Ohm, Logic Level,  
N-Channel Power MOSFETs**

These are N-Channel power MOSFETs manufactured using a modern process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate bias in the 3V to 5V range, thereby facilitating true on-off power control directly from logic level (5V) integrated circuits.

Formerly developmental type TA49027.

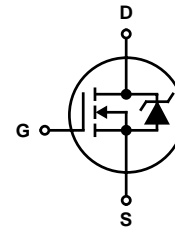
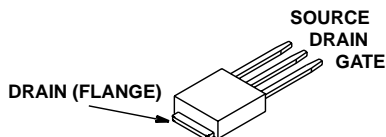
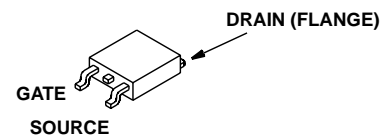
**Ordering Information**

PART NUMBER	PACKAGE	BRAND
RFD16N06LE	TO-251AA	16N06L
RFD16N06LESM	TO-252AA	16N06LE

NOTE: When ordering, use the entire part number. Add suffix 9A to obtain the TO-252AA variant in the tape and reel, i.e., RFD16N06LESM9A.

**Features**

- 16A, 60V
- $r_{DS(ON)} = 0.047\Omega$
- Temperature Compensating PSPICE® Model
- Can be Driven Directly from CMOS, NMOS, TTL Circuits
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

**Symbol**

**Packaging**
**JEDEC TO-251AA**

**JEDEC TO-252AA**


# RFD16N06LE, RFD16N06LESM

## Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

	RFD16N06LE, RFD16N06LESM	UNITS
Drain to Source Voltage (Note 1) . . . . .	$V_{DS}$	60 V
Drain to Gate Voltage ( $R_{GS} = 20k\Omega$ ) (Note 1) . . . . .	$V_{DGR}$	60 V
Gate to Source Voltage . . . . .	$V_{GS}$	+10, -8 V
Continuous Drain Current . . . . .	$I_D$	16 A
Pulsed Drain Current (Note 3) . . . . .	$I_{DM}$	Refer to Peak Current Curve
Pulsed Avalanche Rating . . . . .	$E_{AS}$	Refer to UIS Curve
Power Dissipation . . . . .	$P_D$	90 W
Derate Above $25^\circ\text{C}$ . . . . .		0.606 W/ $^\circ\text{C}$
Operating and Storage Temperature . . . . .	$T_J, T_{STG}$	-55 to $175^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s . . . . .	$T_L$	$300^\circ\text{C}$
Package Body for 10s, See Techbrief 334 . . . . .	$T_{pkg}$	$260^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- $T_J = 25^\circ\text{C}$  to  $150^\circ\text{C}$ .

## Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	$BV_{DS}$	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$ , Figure 11	60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$ , Figure 10	1	-	3	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 55\text{V}, V_{GS} = 0\text{V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 50\text{V}, V_{GS} = 0\text{V}, T_C = 150^\circ\text{C}$	-	-	250	$\mu\text{A}$
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = +10, -8\text{V}$	-	-	10	$\mu\text{A}$
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 16\text{A}, V_{GS} = 5\text{V}$	-	-	0.047	$\Omega$
Turn-On Time	$t_{ON}$	$V_{DD} = 30\text{V}, I_D = 16\text{A}, R_L = 1.88\Omega,$ $V_{GS} = 5\text{V}, R_{GS} = 5\Omega$ Figures 16, 17	-	-	100	ns
Turn-On Delay Time	$t_{d(ON)}$		-	11	-	ns
Rise Time	$t_r$		-	60	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	48	-	ns
Fall Time	$t_f$		-	35	-	ns
Turn-Off Time	$t_{OFF}$		-	-	115	ns
Total Gate Charge	$Q_g(TOT)$	$V_{GS} = 0\text{V}$ to $10\text{V}$	-	51	62	nC
Gate Charge at 5V	$Q_g(5)$	$V_{GS} = 0\text{V}$ to $5\text{V}$		29	35	nC
Threshold Gate Charge	$Q_g(TH)$	$V_{GS} = 0\text{V}$ to $1\text{V}$		1.8	2.6	nC
Input Capacitance	$C_{ISS}$	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V},$ $f = 1\text{MHz}$ Figure 12	-	1350	-	pF
Output Capacitance	$C_{OSS}$		-	300	-	pF
Reverse Transfer Capacitance	$C_{RSS}$		-	90	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	1.65	$^\circ\text{C/W}$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-251AA, TO-252AA	-	-	80	$^\circ\text{C/W}$

## Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	$V_{SD}$	$I_{SD} = 16\text{A}$	-	-	1.5	V
Diode Reverse Recovery Time	$t_{rr}$	$I_{SD} = 16\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	125	ns

NOTES:

- Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
- Repetitive Rating: Pulse Width limited by max junction temperature.

Typical Performance Curves Unless Otherwise Specified

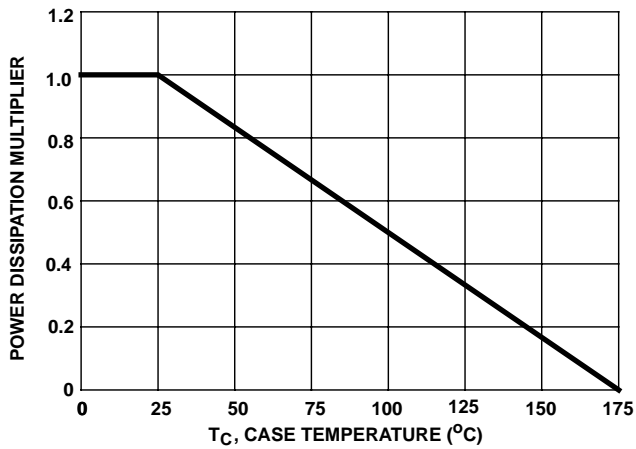


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

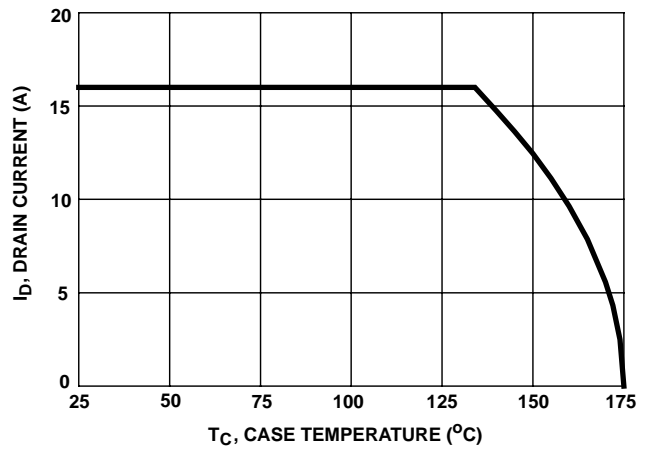


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

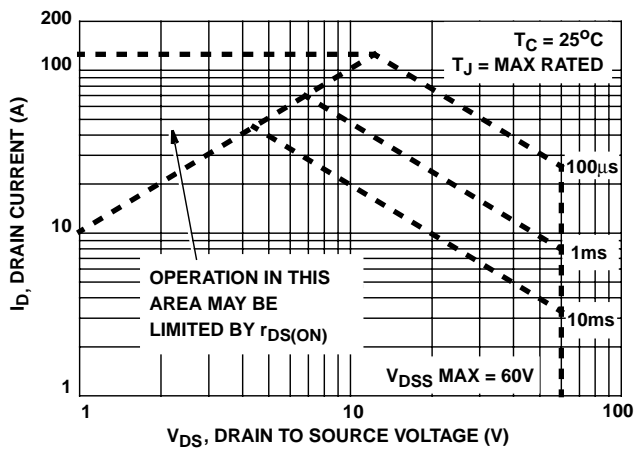


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

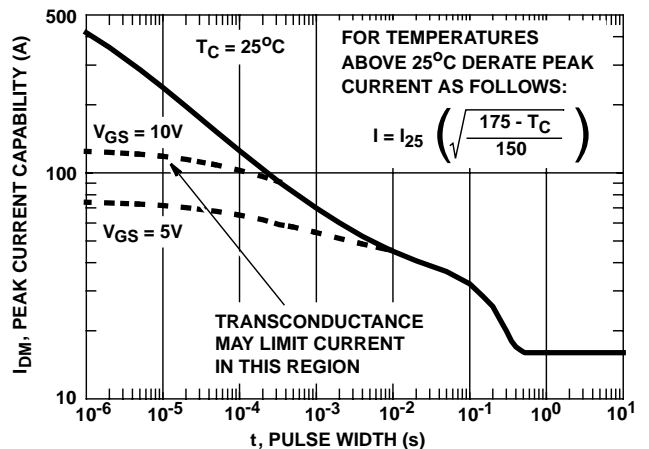


FIGURE 4. PEAK CURRENT CAPABILITY

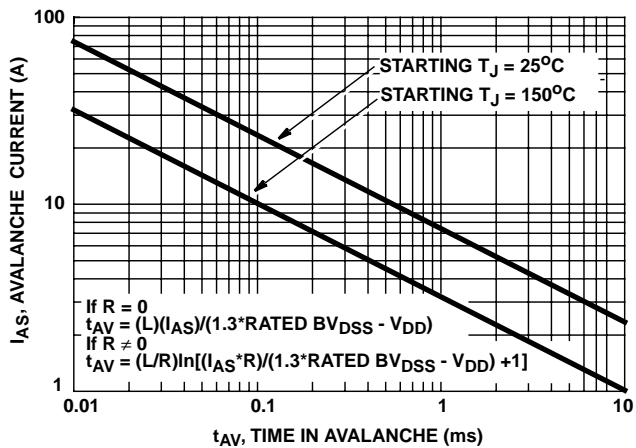


FIGURE 5. UNCLAMPED INDUCTIVE SWITCHING

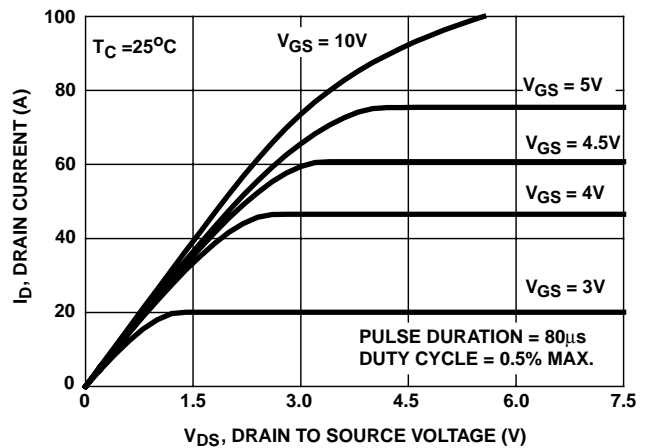


FIGURE 6. SATURATION CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified (Continued)

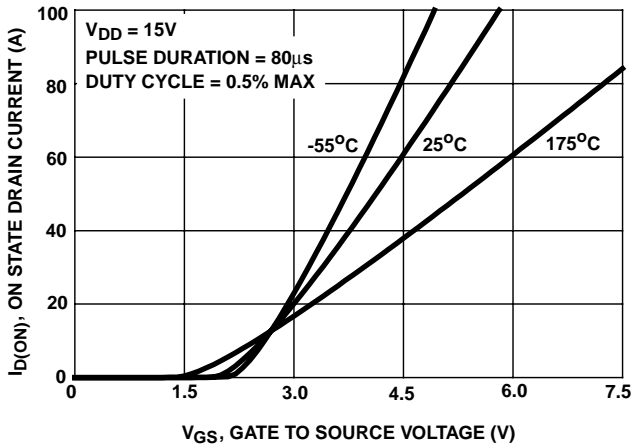


FIGURE 7. TRANSFER CHARACTERISTICS

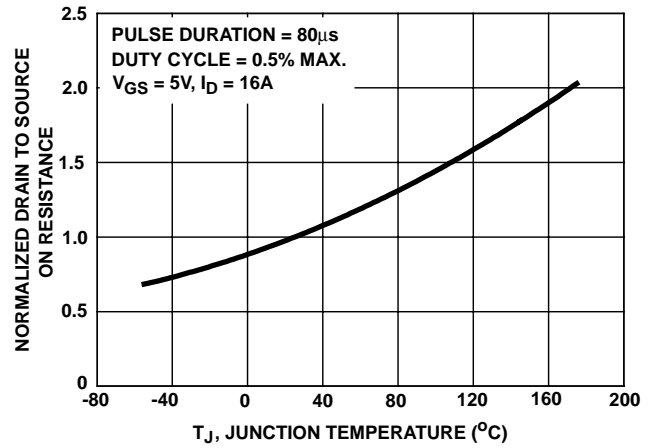


FIGURE 8. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

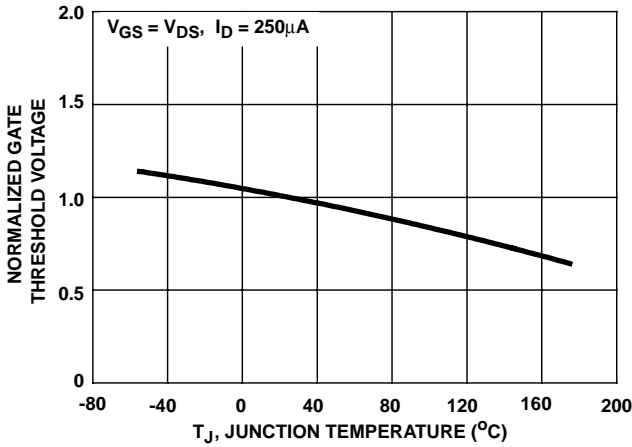


FIGURE 9. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

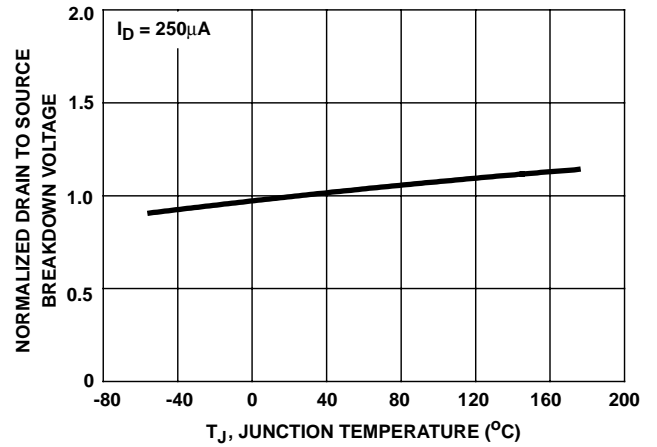


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

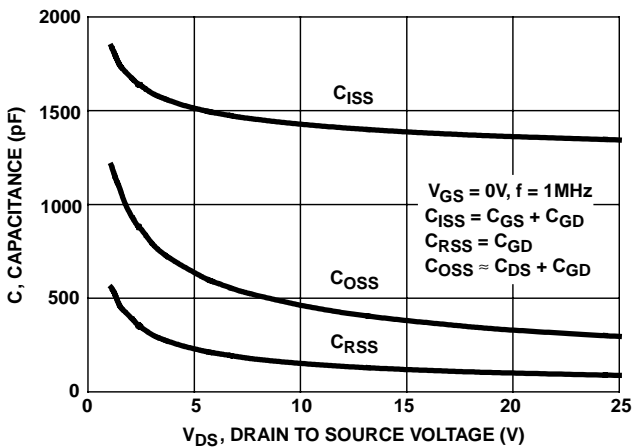
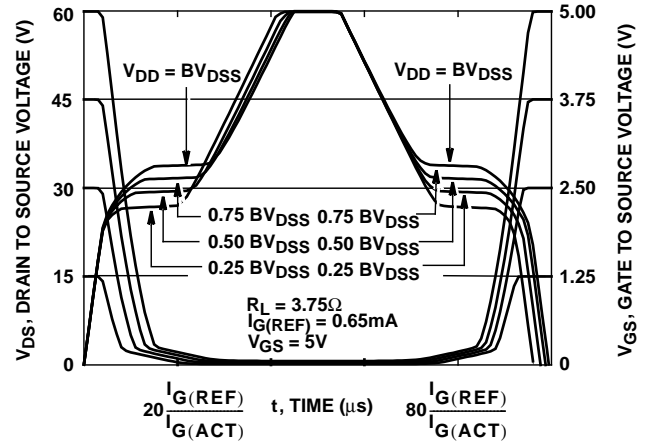


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

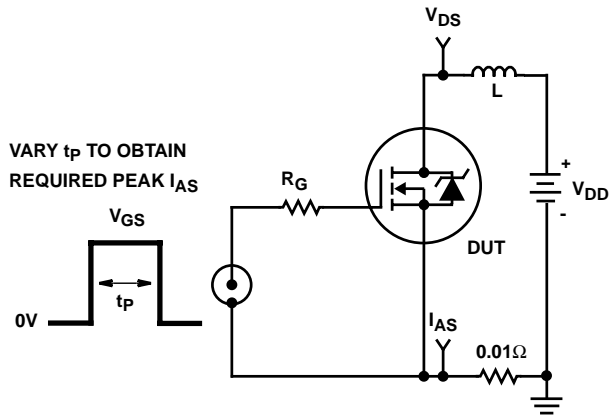


FIGURE 13. UNCLAMPED ENERGY TEST CIRCUIT

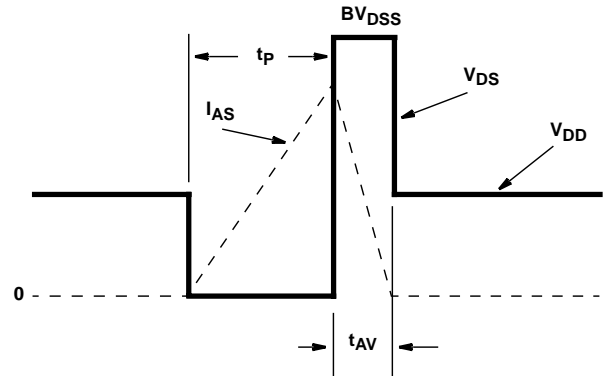


FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

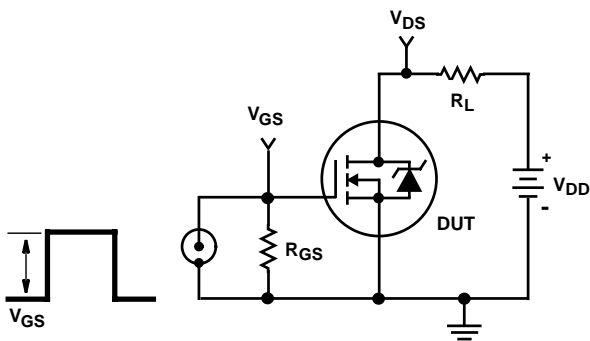


FIGURE 15. SWITCHING TIME TEST CIRCUIT

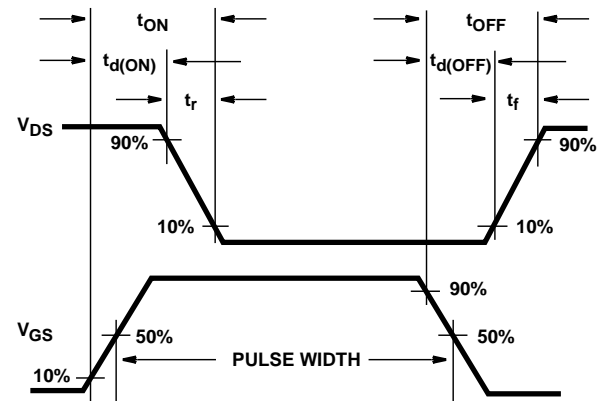


FIGURE 16. RESISTIVE SWITCHING WAVEFORMS

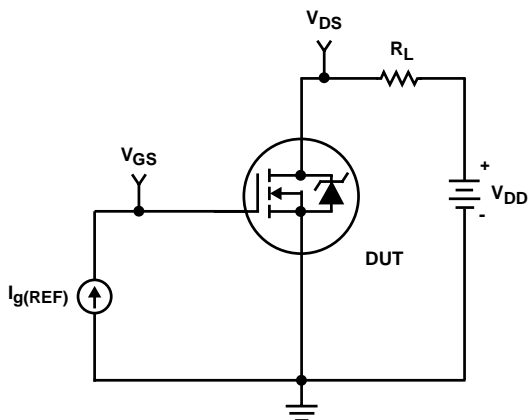


FIGURE 17. GATE CHARGE TEST CIRCUIT

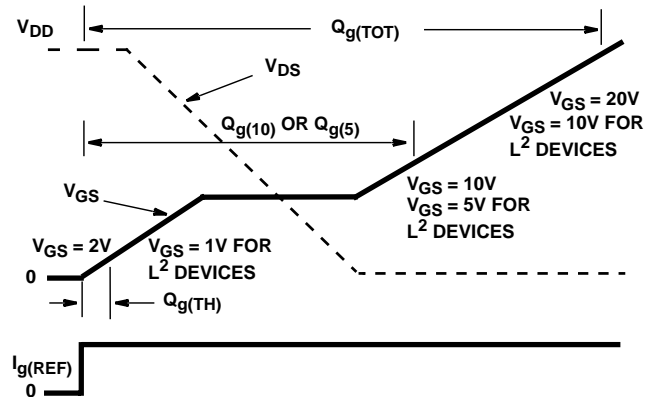


FIGURE 18. GATE CHARGE WAVEFORMS

**PSPICE Electrical Model**

SUBCKT RFD16N06LE 2 1 3 ; rev 8/2/93

CA 12 8 1.46e-9  
 CB 15 14 1.46e-9  
 CIN 6 8 1.0e-9

DBODY 7 5 DBODYMOD  
 DBREAK 5 11 DBREAKMOD  
 DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 66.0  
 EDS 14 8 5 8 1  
 EGS 13 8 6 8 1  
 ESG 6 10 6 8 1  
 EVTHRES 6 21 19 8 1  
 EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9  
 LGATE 1 9 5.5e-9  
 LSOURCE 3 7 4.4e-9

MMED 16 6 8 8 MMEDMOD  
 MSTRO 16 6 8 8 MSTROMOD  
 MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1  
 RDRAIN 50 16 RDRAINMOD 7.0e-3  
 RGATE 9 20 3.6  
 RLDRAIN 2 5 10  
 RLGATE 1 9 55  
 RLSOURCE 3 7 44  
 RSLC1 5 51 RSLCMOD 1e-6  
 RSLC2 5 50 1e3  
 RSOURCE 8 7 RSOURCEMOD 1.45e-2  
 RVTHRES 22 8 RVTHRESMOD 1  
 RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD  
 S1B 13 12 13 8 S1BMOD  
 S2A 6 15 14 13 S2AMOD  
 S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

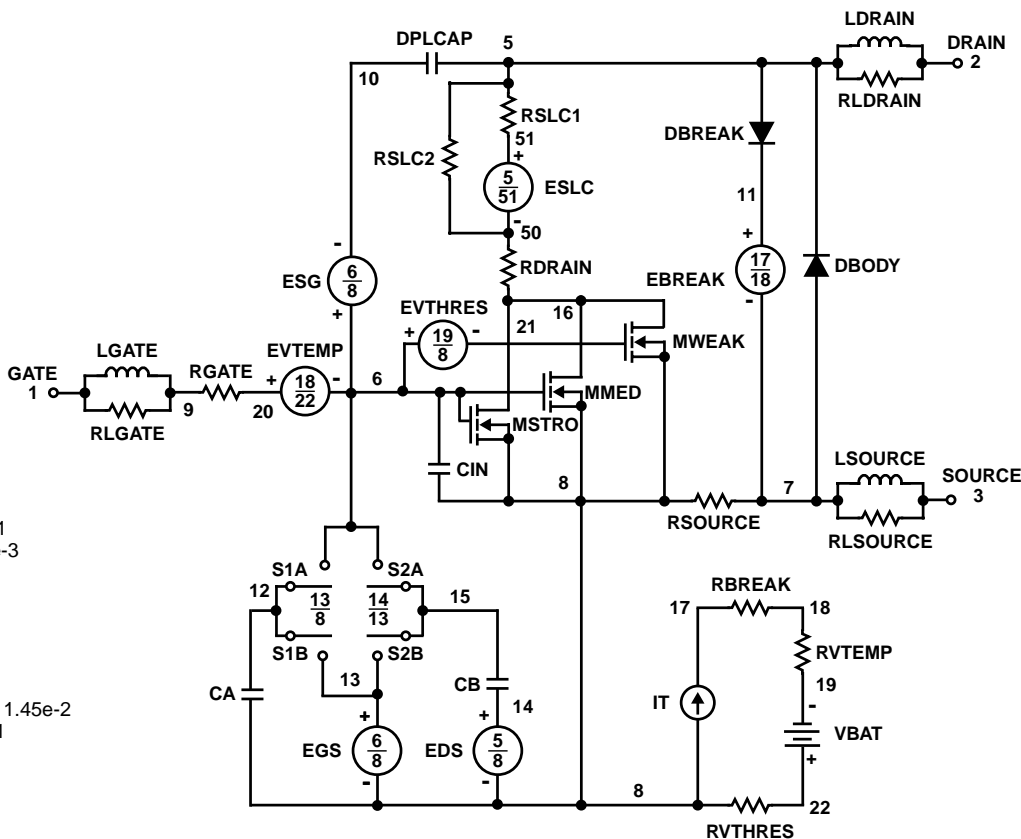
ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))\*(PWR(V(5,51))/(1e-6\*100),3.5))}

.MODEL DBODYMOD D (IS = 6.3e-13 RS = 6.8e-3 TRS1 = 1e-3 TRS2 = 1e-6 XTI = 4.3 CJO = 1.28e-9 TT = 5.1e-8 M = 0.5)  
 .MODEL DBREAKMOD D (RS = 2.9e-1 TRS1 = 1e-4 TRS2 = 0)  
 .MODEL DPLCAPMOD D (CJO = 9.5e-10 IS = 1e-30 N = 10 M = 0.82)  
 .MODEL MMEDMOD NMOS (VTO = 2.10 KP = 6 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 3.6)  
 .MODEL MSTROMOD NMOS (VTO = 2.45 KP = 60.5 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)  
 .MODEL MWEAKMOD NMOS (VTO = 1.79 KP = 0.13 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 36 RS = 0.1)  
 .MODEL RBREAKMOD RES (TC1 = 1.2e-3 TC2 = -5e-7)  
 .MODEL RDRAINMOD RES (TC1 = 1.3e-2 TC2 = 3.1e-5)  
 .MODEL RSLCMOD RES (TC1 = 5.5e-3 TC2 = 7e-6)  
 .MODEL RSOURCEMOD RES (TC1 = 1e-3 TC2 = 1e-6)  
 .MODEL RVTHRESMOD RES (TC1 = -1.8e-3 TC2 = -5.8e-6)  
 .MODEL RVTEMPMOD RES (TC1 = -1.7e-3 TC2 = 8e-7)  
 .MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.8 VOFF = -2.8)  
 .MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.8 VOFF = -4.8)  
 .MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.6 VOFF = 0.5)  
 .MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.5 VOFF = -0.6)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

NOTE:



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

*Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>

### **Sales Office Headquarters**

#### **NORTH AMERICA**

Intersil Corporation  
P. O. Box 883, Mail Stop 53-204  
Melbourne, FL 32902  
TEL: (407) 724-7000  
FAX: (407) 724-7240

#### **EUROPE**

Intersil SA  
Mercure Center  
100, Rue de la Fusee  
1130 Brussels, Belgium  
TEL: (32) 2.724.2111  
FAX: (32) 2.724.22.05

#### **ASIA**

Intersil (Taiwan) Ltd.  
7F-6, No. 101 Fu Hsing North Road  
Taipei, Taiwan  
Republic of China  
TEL: (886) 2 2716 9310  
FAX: (886) 2 2715 3029