Fiber Optic "Light to Logic" Receiver with Clock Recovery

Preliminary Technical Data

RGR1551

Features

- **Light to Logic 20-Pin DIP Receiver Offers ECL Compatibility**
- **Long Reach, High Performance**
- **Sensitivity:** –36 dBm
- **Phase-Locked Loop (PLL) Timing Recovery Circuit**
- **Meets SONET Jitter Tolerance Requirements (CCITT G.958)**
- **Single +5 V Supply, Typically <700 mW**
- **SONET OC3 and SDH STM1 Compatible**
- **Multisourced**

Applications

- **Telecommunication Networks**
- **SONET OC3 and SDH STM1 Compatible**
- **Local and Metropolitan Area Networks**
- **ATM Single Mode Public Network**
- **Military Communications and Control Systems**
- **Digital Cable TV Networks**

Description

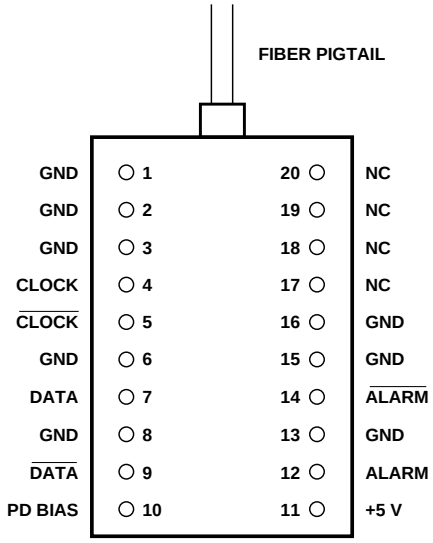
The RGR1551 receiver provides optical signal conversion and processing. It converts 1200 nm to 1600 nm wavelength light wave information into an electrical signal at a data rate of 155 Mb/s.

The receiver contains an InGaAs PIN photodiode, a high sensitivity, wide dynamic range transimpedance amplifier, capacitively coupled to a PLL based clock recovery circuit. The clock and data outputs are retimed complementary PECL.

A complementary CMOS compatible low light alarm is also provided.

Connection Diagram

Top View



Pin Descriptions

Pins 1, 2, 3, 6, 8, 13, 15, 16, GND:

These pins should be connected to the circuit ground.

Pins 4, 5, CLOCK, $\overline{\text{CLOCK}}$:

These pins provide complementary differential PECL CLOCK and $\overline{\text{CLOCK}}$ outputs.

Pins 7, 9, DATA, $\overline{\text{DATA}}$:

These pins provide complementary differential PECL DATA and $\overline{\text{DATA}}$ outputs.

The RGR1551 DATA output is noninverting, an optical pulse causes the DATA output to go to the PECL logic high state (+4 V nominal).

Pin 10, PD Bias:

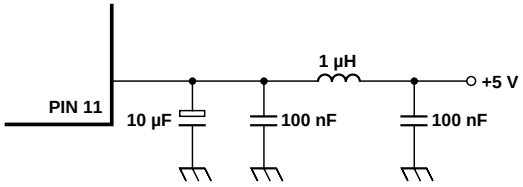
This pin must be connected to any voltage between 0 V (GND) and –5 V. This provides the photodiode bias. The current drawn is directly proportional to the average received photocurrent.

I = Responsivity x Mean Power.

The Responsivity will be between 0.7 A/W and 1.0 A/W.

Pin 11, +5 V:

This pin should be connected to +5 V supply. The network shown below should be placed as close as possible to pin 11.



Pins 12, 14, ALARM, $\overline{\text{ALARM}}$:

These pins provide complementary ALARM and $\overline{\text{ALARM}}$ outputs.

This is the low light alarm. ALARM goes to a logic low (CMOS compatible) state when the optical power drops below the threshold level (insufficient optical power).

The optical power must increase to a higher level than the level where the alarm went low before ALARM will return to a logic high. This difference is the alarm hysteresis.

Pins 17, 18, 19, 20, NC:

These pins are not connected and should be left open circuit on the application PCB.

Functional Description

Design

The receiver contains an InGaAsP photodetector, transimpedance amplifier, and interface amplifier circuit, including a clock recovery and data retiming function. It is designed with a multimode fiber pigtail to allow maximum flexibility in connector options.

The interface amplifier is ac coupled to the preamplifier circuit.

Terminating the Outputs

The data outputs of the RGR1551 are PECL compatible. Care should be taken to match termination impedances to the interconnect to minimize reflection effects. In order to balance the drive currents drawn from the module, all serial data outputs (DATA and $\overline{\text{DATA}}$, CLOCK and $\overline{\text{CLOCK}}$) should be terminated identically, even if only one output is used. This will lower the power supply noise generated by the receiver and improve performance at low optical input power levels.

Power Supplies

The RGR1551 will operate to specifications with a single +5 V power supply (Pin 10 grounded). The –5 V PIN bias is provided to maintain functional compatibility with second sources.

Circuit Layout

The RGR1551 uses very high bandwidth circuitry to achieve its high level of performance. Care must be taken to ensure stable operation. The use of ground planes and transmission line interconnects is required. The use of a standard evaluation board is highly recommended for those users who are not familiar with these techniques. Signal traces should conform to ECL design rules to prevent reflections and ringing from degrading performance. Useful guidelines are contained in ECL manufacturer design manuals.

Manufacturing

The fiber pigtail on the device requires normal fiber handling considerations. Care should be taken to avoid tight bends as well as excessive tension on the fiber pigtail.

The allowable temperature range for the RGR1551 is limited by the material used in the pigtail. Exposure to temperatures over +85°C is not recommended. Low profile sockets or hand soldering are recommended for this part.

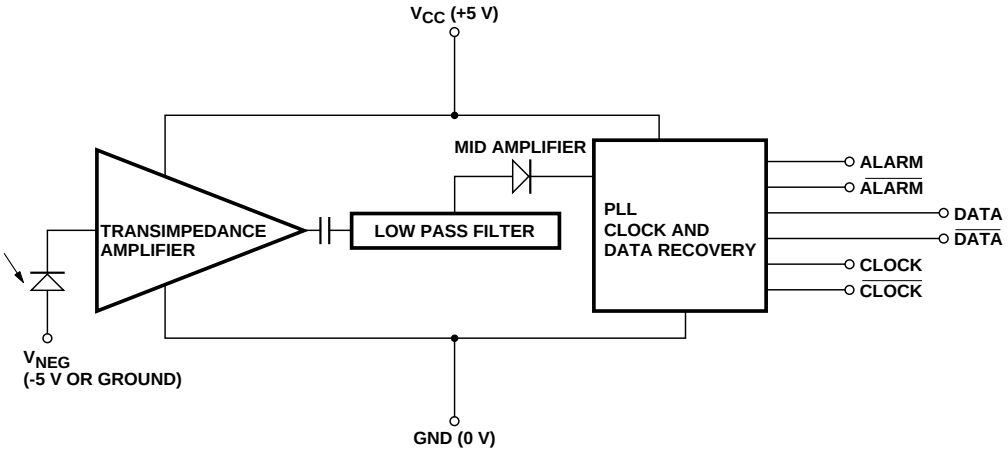


Figure 1. Block Diagram.

Performance Specifications
Absolute Maximum Ratings

Absolute maximum limits mean that no catastrophic damage will occur if the product is subjected to these ratings for short periods, provided that each limiting parameter is in isolation and all other parameters have values within the performance specification. It should not be assumed that limiting values of more than one parameter can be applied to the product at the same time.

Parameter	Symbol	Minimum	Maximum	Units	Note
Supply Voltage	V_{CC}	–0.5	+5.5	V	1
Supply Voltage	V_{NEG}	–10	+0.5	V	-

Environmental Parameters

Parameter	Symbol	Minimum	Maximum	Units	Note
Operating Temperature	-	–40	+85	℃	-
Storage Temperature	-	–40	+85	℃	-
Humidity	-	-	85	%RH	-

Electrical Parameters (–40℃ to +85℃)

Parameter	Symbol	Minimum	Maximum	Units	Note
Supply Voltage	V_{CC}	4.75	5.25	V	-
V_{CC} Supply Current	-	-	130	mA	4
DATA Output Level (high)	-	3.8	4.15	V	2, 3
DATA Output Level (low)	-	3.1	3.5	V	2, 3
ALARM Output Level (high)	V off	4.5	5.0	V	2, 3
ALARM Output Level (low)	V on	0	0.5	V	2, 3

Notes:
1. V_{CC} of –0.5 V and V_{NEG} of +0.5 V may not be applied simultaneously.
2. Output terminated to (V_{CC} -2) with 50 Ω load or equivalent.
3. Output voltages are for V_{CC} = 5.0 V.
4. Outputs not loaded.

Optical Parameters (–40℃ to +85℃)

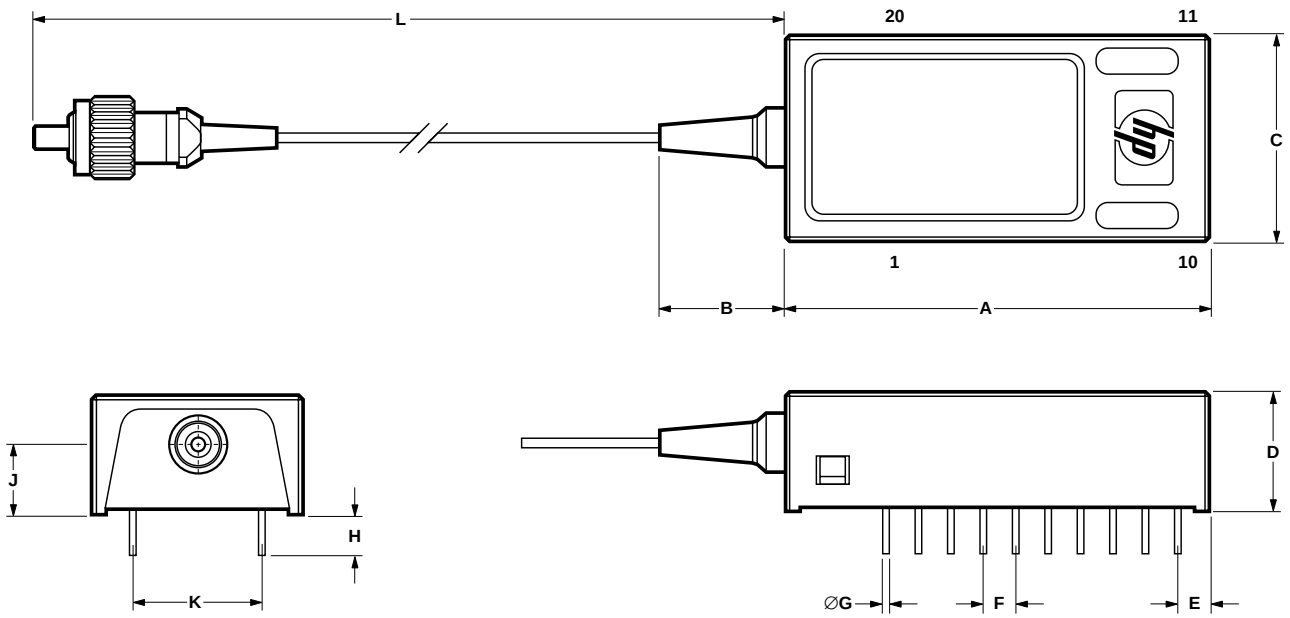
Parameter	Symbol	Minimum	Maximum	Units	Note
Wavelength	-	1200	1600	nm	-
Receiver Sensitivity	-	-	–35	dBm	1
Maximum Input Power	-	0	-	dBm	-
Alarm ON	-	–45	–36	dBm	1
Hysteresis	-	0.5	7.0	dB	-
Alarm Response Time	-	-	600	µS	-
Reliability Target	-	-	1000	FIT	-

Note:
1. At a BER of 1 x 10^{-10}, 2^{23-1} PRBS pattern NRZ data at 155.52 Mb/s with 10:1 extinction ratio. EOL.

Jitter Tolerance	ITU G.958 Compliant

Fiber Pigtail	Typical	Units
Core Diameter	50	microns
Cladding Diameter	125	microns
Secondary Coating Diameter	900	microns

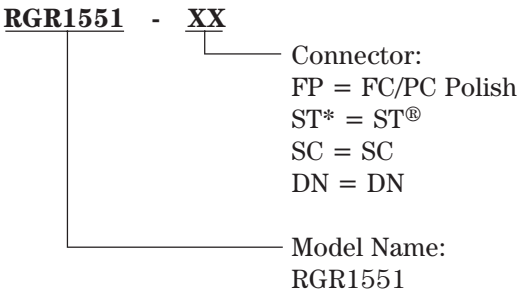
Drawing Dimensions



DIM.	MIN.	NOM.	MAX.
A	32.9	–	33.1
B	9.9	–	10.1
C	16.0	–	16.3
D	–	–	9.27
E	2.26	–	2.62
F	–	2.54	–
∅G	–	0.46	–
H	2.7	–	3.2
J	5.2	–	5.6
K	–	10.16	–
L	400	–	1220

ALL DIMENSIONS IN MILLIMETERS

Ordering Information



Allowable part numbers:
RGR1551 - FP
RGR1551 - ST
RGR1551 - SC
RGR1551 - DN

Handling Precautions

1. The RGR1551 can be damaged by current surges or overvoltage. Power supply transient precautions should be taken.
2. Normal handling precautions for electrostatic sensitive devices should be taken.

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