CONEXANT™

ServiceSAR Controller

RS8234

Full-Featured ATM xBR Service Segmentation and Reassembly Controller (ServiceSAR)

Conexant's RS8234 accelerates service interworking by emphasizing performance under worst-case short packet conditions. In addition, the PCI host interface is one of the most efficient in the industry in terms of bus occupancy.

The RS8234 not only meets the stringent requirements of T.M. 4.1, but also enables advanced traffic control functions such as GFR, CBR tunneling and virtual path shaping.

The RS8234's service-specific features allow system designers to accelerate specific protocol interworking functions for applications like IP over ATM, Frame Relay or LAN emulation.

The device's unique architecture enables advanced network-level functionality and topologies. A few examples of these features include echo suppression of multicast data frames on ELAN channels, and peak cell rate (PCR) control established per VCC, per tunnel, and/or per scheduling priority.

Distinguishing Features

- Fully T.M. 4.1-compliant
- 3.3V/5V low power utilization (< 1 watt)
- PCI 2.1/UTOPIA Level 1
- Industrial temperature
- 16 multiservice tunnels
- 64K VCCs
- 388-pin BGA

ServiceSAR Controller
RS8234

Integrated Management

The RS8234 complies with ATM Forum specifications UNI 3.1, T.M. 4.1 and all other relevent standards. The RS8234 provides integrated traffic management for all service categories, including constant bit rate (CBR), variable bit rate (VBR) (single- and dual-leaky bucket), real-time VBR, unspecified bit rate (UBR), available bit rate (ABR), guaranteed frame rate (GFR) (guaranteed MCR on UBR VCCs), and generic flow control (GFC). The xBR traffic management block automatically schedules each VCC according to user assigned-parameters to maximize line utilization.

Advanced Architecture

The RS8234's architecture is designed to minimize and control host traffic congestion. The host manages the RS8234 terminal using write-only control and status queues. The control queues are also isolated from their associated data buffers via buffer descriptors, allowing the data buffers to hold payload data only. For example, the host submits data for transmit by writing buffer descriptor pointers to one of 32 transmit queues. These entries may be thought of as task lists for the ServiceSAR to perform. The 32 receive queues couple with the transmit structure to create complete host peers. The RS8234 enables control of traffic congestion through mechanisms like receive buffer memory limitations (called firewalls), and through explicit notification of congestion by the host. This architecture reduces the control burden on the host system while minimizing PCI bus utilization, by eliminating reads across the PCI bus from host control activities. It also provides control points to manage congestion, which is critical for ABR.

The RS8234 System

The RS8234 consists of five separate coprocessors (incoming and outgoing DMA, segmentation, reassembly and xBR traffic manager), each of which maintains state information in shared, off-chip memory. This memory is controlled by the SAR through the local bus interface, which arbitrates access to the bus between the various coprocessors. These coprocessors, though they run off the same system clock, operate asynchronously from each other. Communication between the coprocessors takes place through on-chip FIFOs or through queues in local memory.

The RS8234's on-chip coprocessor blocks are surrounded by high-performance PCI and UTOPIA ports for glueless interface to a variety of system components with full line-rate throughput and low bus occupancy. Figure 1 illustrates these functional blocks.

xBR Cell Scheduler

The cell scheduler rate-shapes all segmentation traffic according to per-channel parameters. The RS8234 supports eight user-assigned scheduling priorities in addition to CBR. The user assigns a priority to each channel. The user can further control consumption of bandwidth by assigning peak cell rate limits to four of those scheduling priorities.

The user sets the range of available transmission rates for the scheduler by setting the size of the dynamic schedule table and the duration of each scheduling slot in the table.

a software driver to the RS8234, on top of which a system designer can develop and place proprietary driver software. This interface allows users to easily port their applications to the RS8234EVM. This software is written in C, and source code is available under license agreement.

The RS8234EVM also includes documentation, a full set of design schematics, and artwork for the RS8234EVM PCI card.

RS823xHPI Hardware Programming Interface

The RS8234 Hardware Programming Interface (HPI) provides a set of fully-defined software primitives to interface with an ATM UNI port based on the RS8234 SAR. It serves as an interface point for system software designed to configure and manage the RS8234-based UNI without the necessity of detailed manipulation of hardware-related structures. It thus provides a layer of abstraction from the hardware for the system designer and user.

RS8234HPI primitives are used by higher-level application software (such as network management and device drivers) to obtain ATM services as required by their upper protocol layers. These primitives handle SAR resource, control and status management. The RS823xHPI performs functions in the following categories:

- RS8234 SAR device initialization
- Memory resource allocation
- Resource management
- Connection management (including VCC setup and teardown, and processing status)
- Segmentation/data transmission
- Data reception/reassembly
- Statistics gathering/error reporting
- Diagnostic testing

Features	Benefits
Software reference design	Shortens development time of customer system-specific ATM applications.
Modular software design	Allows users to utilize only those functions they want and to incorporate those functions into their own applications.
Dynamic rate control per virtual channel	Users can establish ABR, CBR, UBR or VBR connections at VCC setup on each of over 32,000 channels.
SAR initialization and VCC control	Provides detailed examples for control and management of the RS8234. Significantly shortens design time.
Well-defined, robust RS823xHPI interface	Enables users to easily port their application to the RS8234EVM.
Well-documented C source code	Gives users a clear description of how the software and hardware function.
RS823xHPI macro layer software	Offers a layer of abstraction for ease of use of the RS823xHPI primitives. Reference device driver for VxWorks.

The RS823xHPI provides a reference implementation of these critical functions in order to shorten the development of a production-quality, customer system-specific ATM application. The RS823xHPI is implemented in well-documented C source code, specifically written to be highly portable across a multiplicity of processors, compilers and development environments.

RS8234EVM Evaluation Software

The RS8234EVM system software is a complete reference implementation of an ATM terminal for device testing and evaluation using the RS8234EVM, RS823xHPI and the VxWorks operating system. This evaluation system software provides a reference design that the system designer can utilize in part or in full in tailoring customer-specific ATM applications.

The RS823xHPI macro layer, together with the RS823xHPI, forms a complete device driver for the RS8234 in a VxWorks environment. The user does not need an advanced knowledge of the device or full understanding of every detail to successfully operate the RS8234 device.

Also provided is the traffic generator and checker (TGC), which utilizes the RS823xHPI primitives to send ATM traffic and check the data on its return on the reassembly side. This module was designed to exercise the functionality of the RS8234 device.

RS8234 xBR SAR

Special Features:

Service-Specific Performance Accelerators

- **LECID filtering and echo suppression**
- **Dual leaky bucket based on CLP (Frame Relay)**
- **Frame Relay DE interworking**
- **Internal SNMP MIB counters**

Flexible Architectures

- **Multi-peer host**
- **Direct switch attachment via reverse UTOPIA**
- **ATM Terminal**
  - Host control
  - Local Bus control
- **Optional local processor**

xBR Traffic Management

- **T.M. 4.1 Service Classes**
  - CBR
  - VBR (single, dual and CLP 0+1 leaky buckets)
  - Real-time VBR
  - ABR
  - UBR
  - GFC (controlled and uncontrolled flows)
  - Guaranteed frame rate (GFR) (guaranteed MCR on UBR VCCs)
- **8 levels of priorities (8 + CBR)**
- **Dynamic per-VCC scheduling**
- **Multiple programmable ABR templates (supplied by Conexant or user)**
- **Scheduler driven by local clock for low-jitter CBR**
- **Internal RM OAM cell feedback path**
- **Virtual FIFO rate matching (source rate matching)**
- **Tunneling**
  - VP tunnels (VCI interleaving on PDU boundaries)
  - CBR tunnels (cells interleaved on UBR with an aggregate CBR limit)

Multi-Queue Segmentation Processing

- **32 transmit queues with optional priority levels**
- **64K VCCs maximum ****
- **AAL5 and AAL3/4 CPCS generation**
- **AAL0 null CPCS (optional use of PTI for PDU demarcation)**
- **ATM cell header generation**
- **Raw cell mode (52 octet)**
- **200 Mbps half duplex**
- **155 Mbps full duplex (with 2-cell PDUs)**
- **Message and streaming status modes**
- **Variable-length transmit FIFO-CDV-host latency matching (1 to 9 cells)**
- **Symmetric Tx and Rx architecture**
  - Buffer descriptors
  - Queues
- **User-defined field circulates back to host (32 bits)**
- **Distributed host or SAR-shared memory segmentation**
- **Simultaneous segmentation and reassembly**
- **Per-PDU control of CLP/PTI (UBR)**
- **Per-PDU control of AAL5 UU field**
- **Virtual Tx FIFO (PCI host)**

ABR Traffic Management

The ABR flow control manager dynamically rate-shapes ABR traffic independently per VCC, based upon network feedback. One or more ABR templates are used to govern the behavior of traffic. Both relative rate (RR) and explicit rate (ER) algorithms are employed when computing a rate adjustment on an ABR VCC. Programmable ABR templates allow rate-shaping policies on groups of VCCs to be tuned for different network applications. The RS8234 automatically generates and processes all resource management (RM) cells. The on-chip hardware, coupled with the user-defined ABR templates, implements all required source and destination behaviors as defined in T.M. 4.1. Optional behaviors such as use-it-or-lose-it, out-of-rate RM cells, host congestion and allowed cell rate (ACR) monitoring are also supported.

Early Packet Discard for Frame Relay and LAN Emulation

The early packet discard (EPD) feature provides a mechanism to discard complete or partial CPCS-PDUs based upon service discard attributes or error conditions. For example, the reassembly coprocessor performs EPD functions for the following conditions: Frame Relay packet discard based on the discard eligibility (DE) field in the received frame and the channel exceeding a user-defined priority threshold; LANE-LECID packet discard to implement echo suppression on multicast data frames on ELAN channels; and for errors like receive FIFO full condition/threshold and various AAL3/4 MIB errors.

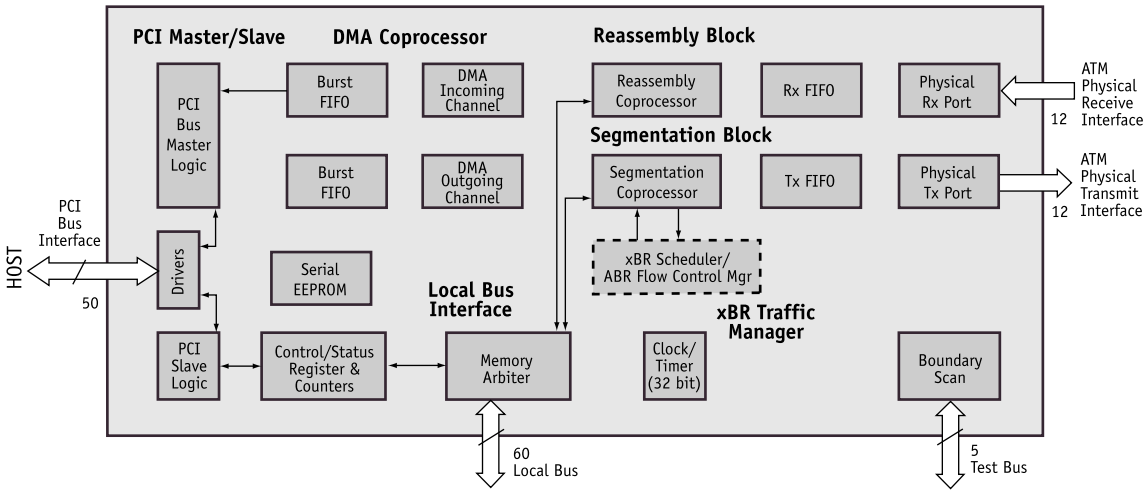

Figure 1. RS8234 functional block diagram

IP and Frame Relay Interworking

The VBR-3, CLPO+1 category includes rate-shaping via the dual leaky bucket GCRA algorithm based on the CLP bit which is used in Frame Relay applications and is recommended by the IETF for use with IP.

UNI or NNI Addressing

The RS8234 handles both UNI (8-bit VPI field) and NNI (12-bit VPI field) addresses.

Virtual Path Networking

The RS8234 can interleave segmentation of numerous VCCs (i.e., separate VC channels) as members of one VP. VP-based traffic shaping is supported. The entire VP is scheduled according to one set of traffic parameters.

CBR Tunneling

The user can delineate up to four CBR pipes (or tunnels) in which to transmit multiple channels. The tunneled VCCs can be further shaped as UBR, VBR or ABR connections.

RS8234EVM (Evaluation Module)

This PCI card is specifically designed to be a full-featured ATM controller based on the RS8250 ATM receiver/transmitter and the RS8234 ServiceSAR. The PHY interface comes configured with an optical OC-3 connection for testing at 155 Mbps.

The PCI interface between the host processor and the local system is controlled by the RS8234 Hardware Programming Interface (RS823xHPI),

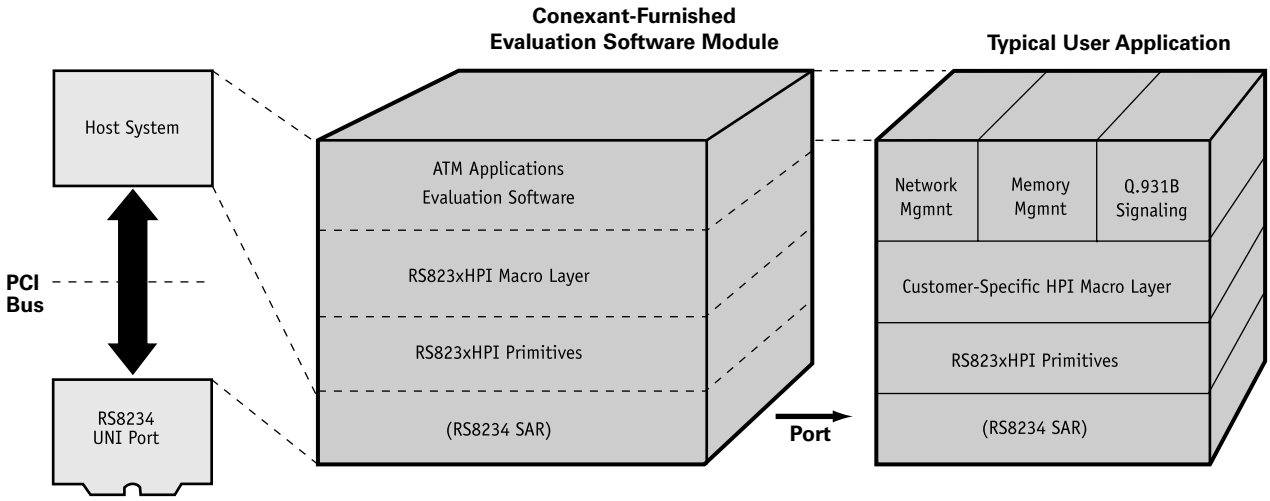

Figure 2. RS8234EVM system software

Multi-Queue Reassembly Processing

- **32 reassembly queues**
- **64K VCCs maximum ****
- **AAL5 and AAL3/4 CPCS checking**
- **AAL0**
  - PTI termination
  - Cell count termination
- **Early packet discard, based on:**
  - Receive buffer underflow
  - Receive status overflow
  - CLP with priority threshold
  - AAL5 max PDU length
  - Rx FIFO full
  - Frame Relay DE with priority threshold
  - LECID filtering for echo suppression
  - Per-VCC firewalls
- **Dynamic channel lookup (NNI or UNI addressing)**
  - Supports full address space
  - Deterministic
  - Flexible VCI count per VPI
  - Optimized for signaling address assignment
- **Message and streaming status modes**
- **Raw cell mode (52 octet)**
- **200 Mbps half duplex**
- **155 Mbps full duplex (with 2-cell PDUs)**
- **Distributed host or SAR shared memory reassembly**
- **8 programmable reassembly hardware time-outs (assignable per VCC)**
- **Global max PDU length for AAL5**
- **Per-VCC buffer firewall (memory usage limit)**
- **Simultaneous reassembly and segmentation**
- **Idle cell filtering**
- **32K duplex VCCs**

High-Performance Host Architecture with Buffer Isolation

- **Write-only control and status**
- **Read multiple command for data transfer**
- **Up to 32 host clients control and status queues**
- **Physical or logical clients**
  - Enables peer-to-peer architecture
- **Descriptor-based buffer chaining**
- **Scatter/gather DMA**
- **Endian neutral**
- **Non-word (byte) aligned host buffer addresses**
- **Automatically detects presence of Tx data or Rx free buffers**
- **Virtual FIFOs (PCI bursts treated as single address)**
- **Hardware indication of BOM**
- **Allows isolation of system resources**
- **Status queue interrupt delay**

Designer Toolkit

- **Evaluation module (RS8234EVM)**
- **Reference schematics**
- **Hardware Programming Interface – RS8234HPI reference source code (C)**

Generous Implementation of OAM-PM Protocols

- **Detection of all F4/F5 OAM flows**
- **Internal PM monitoring and generation for up to 128 VCCs**
- **Optional global OAM Rx/Tx queues**
- **In-line OAM insertion and generation**

Standards-Based I/O

- **33 MHz PCI 2.1**
- **Serial EEPROM to store PCI configuration information**
- **PHY Interfaces**
  - UTOPIA master (Level 1)
  - UTOPIA slave (Level 1)
- **Flexible SAR-shared memory architecture**
- **Optional local control interface**
- **Boundary scan for board-level testing**
- **Source loopback, for diagnostics**
- **Glueless connection to Conexant's RS8250 ATM PHY device**

Electrical/Mechanical

- **388-pin BGA package**
- **3.3V power supply**
- **5V tolerant I/O pads**
- **5V - 3.3V PCI pads**
- **Low power 1.0 W (typical) at full rate**
- **Industrial temperature range**
- **TTL level inputs**
- **CMOS level outputs**

Standards Compliance

- **UNI/NNI 3.1**
- **T.M. 4.1**
- **Bellcore GR-1248**
- **ATM Forum B-ICI V 2.0**
- **I.363**
- **I.610 /GR-1248**
- **AToM MIB (RFC1695)**
- **ILMI MIB**
- **ANSI T1.635**
- **GFC per I.361**
- **SNMP**
- **I^2C Protocol**
- **PCI Revision 2.1**
- **IEEE 1149.1-1990**
- **IEEE 1149.1 supplement B, 1994**

Statistics and Counters

- **Global register counter of # of cells transmitted**
- **Global register counter of # of cells received on active channels**
- **Global register counter of # of cells received on inactive channels**
- **Global register counter of # of AAL5 CPCS-PDUs discarded due to per-channel firewall, etc**
- **RSM per VCC service discard counters (Frame Relay and LANE)**
- **1 programmable interval timer (32 bits with interrupt)**
- **Per-VCC AAL3/4 MIB counters:**
  - # cells with CRC10 errors
  - # cells with MID errors
  - # cells with LI errors
  - # cells with SN errors
  - # cells with BOM or SSM errors
  - # cells with EOM errors

****** Depends on local memory size and device configuration; 32K VCCs typically.

What is ATM?

Asynchronous Transfer Mode (ATM) has emerged as the primary networking technology for next-generation, multi-service communication networks. ATM-enabled services benefit the Internet as well as emerging applications in science, telemedicine and distance learning. Just as the Internet revolutionized worldwide communications, ATM brings new meaning to high-speed networking.

ATM, which uses a fixed-size packet, or cell, is a transport protocol capable of providing a homogeneous network for all traffic types, whether the application is to carry conventional telephony, video entertainment, or data traffic over LANs, MANs or WANs.

The ITU-T and ANSI selected ATM for Broadband-ISDN. SONET/SDH, as specified by the ITU, is intended as the primary transport mechanism for ATM cells in WAN applications. ATM also plays a key role in next-generation consumer applications for high-speed Internet access and wireless access. The ADSL Forum and the Universal ADSL Working Group chose ATM as the network layer protocol for G.lite and G.DMT ADSL.

ATM physical-layer (ATM-PHY) IC devices adapt ATM cells to and from transmission rates ranging from 1.544 Mbps to 2.4 Gbps, via a standard system interface called UTOPIA. ATM-PHY devices perform ATM cell functions (transmission convergence) such as cell scrambling/descrambling, cell delineation (HEC), cell header processing, and cell-rate decoupling as well as rate-specific functions for frame generation/recovery, frame adaptation and clock/data recovery.

Product Features

- **AAL0, AAL5, AAL3/4**
- **Factory-supplied ABR templates (user may configure)**
- **xBR Traffic Manager**
  - CBR
  - VBR (single bucket)
  - VBR (dual bucket)
  - VBR (CLP 0+1)
  - rt-VBR
  - ABR (TM4.0)
  - UBR
  - GFC
  - GFR (guaranteed MCR on UBR VCCs)
- **32K duplex VCCs (non ABR)**
- **PCI 2.1**
- **UTOPIA Level 1**
- **Glueless RS8250 ATM PHY interface**
- **Reference design available**
- **RS8234 evaluation system available**
- **Reference software available (RS823xHPI)**

Applications

- **ATM Uplinks**
  - Routers
  - Ethernet switches
- **ATM Service Adapters**
  - Frame Relay over ATM
  - IP over ATM
  - LAN emulation
- **ATM Servers**
  - File servers
  - Control servers
    - LANE
    - MPOA
    - P-NNI
    - SIG

Ordering Information

Part Number	Description
RS8234EBGD	ATM Enhanced xBR SAR
RS8234/8250EVM	PCI Card implementing the RS8234 SAR as a UNI port *Includes:* RS823xHPI and HPI Macro Layer software, RS8234EVM Schematics, Porting Guide and download instructions, RS823xHPI specification

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