S29GLxxxN MirrorBit™ Flash Family
S29GL512N, S29GL256N, S29GL128N
512 Megabit, 256 Megabit, and 128 Megabit, 3.0 Volt-only Page Mode Flash Memory featuring 110 nm MirrorBit process technology

Datasheet

ADVANCE INFORMATION

Distinctive Characteristics

Architectural Advantages

- **Single power supply operation**
  - 3 volt read, erase, and program operations
- **Enhanced VersatileI/O™ control**
  - All input levels (address, control, and DQ input levels) and outputs are determined by voltage on V_{IO} input. V_{IO} range is 1.65 to V_{CC}
- **Manufactured on 110 nm MirrorBit process technology**
- **SecSi™ (Secured Silicon) Sector region**
  - 128-word/256-byte sector for permanent, secure identification through an 8-word/16-byte random Electronic Serial Number, accessible through a command sequence
  - May be programmed and locked at the factory or by the customer
- **Flexible sector architecture**
  - S29GL512N: Five hundred twelve 64 Kword (128 Kbyte) sectors
  - S29GL256N: Two hundred fifty-six 64 Kword (128 Kbyte) sectors
  - S29GL128N: One hundred twenty-eight 64 Kword (128 Kbyte) sectors
- **Compatibility with JEDEC standards**
  - Provides pinout and software compatibility for single-power supply flash, and superior inadvertent write protection
- **100,000 erase cycles per sector typical**
- **20-year data retention typical**

Performance Characteristics

- **High performance**
  - 80 ns access time (S29GL128N, S29GL256N), 90 ns access time (S29GL512N)
  - 8-word/16-byte page read buffer
  - 25 ns page read times
  - 16-word/32-byte write buffer reduces overall programming time for multiple-word updates
- **Low power consumption (typical values at 3.0 V, 5 MHz)**
  - 25 mA typical active read current;
  - 50 mA typical erase/program current
  - 1 µA typical standby mode current
- **Package options**
  - 56-pin TSOP
  - 64-ball Fortified BGA

Software & Hardware Features

- **Software features**
  - Program Suspend & Resume: read other sectors before programming operation is completed
  - Erase Suspend & Resume: read/program other sectors before an erase operation is completed
  - Data# polling & toggle bits provide status
  - Unlock Bypass Program command reduces overall multiple-word or byte programming time
  - CFI (Common Flash Interface) compliant: allows host system to identify and accommodate multiple flash devices
- **Hardware features**
  - Advanced Sector Protection
  - WP#/ACC input accelerates programming time (when high voltage is applied) for greater throughput during system production. Protects first or last sector regardless of sector protection settings
  - Hardware reset input (RESET#) resets device
  - Ready/Busy# output (RY/BY#) detects program or erase cycle completion

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This document contains information on a product under development at FASL LLC. The information is intended to help you evaluate this product. FASL LLC reserves the right to change or discontinue work on this proposed product without notice.

General Description

The S29GL512/256/128N family of devices are 3.0V single power flash memory manufactured using 110 nm MirrorBit technology. The S29GL512N is a 512 Mbit, organized as 33,554,432 words or 67,108,864 bytes. The S29GL256N is a 256 Mbit, organized as 16,777,216 words or 33,554,432 bytes. The S29GL128N is a 128 Mbit, organized as 8,388,608 words or 16,777,216 bytes. The devices have a 16-bit wide data bus that can also function as an 8-bit wide data bus by using the BYTE# input. The device can be programmed either in the host system or in standard EPROM programmers.

Access times as fast as 80 ns (S29GL128N, S29GL256N) or 90 ns (S29GL512N) are available. Note that each access time has a specific operating voltage range (V_{CC}) and an I/O voltage range (V_{IO}), as specified in the Product Selector Guide and the Ordering Information (512 Mb) sections. The devices are offered in a 56-pin TSOP or 64-ball Fortified BGA package. Each device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

Each device requires only a **single 3.0 volt power supply** for both read and write functions. In addition to a V_{CC} input, a high-voltage **accelerated program (**WP#/**ACC)** input provides shorter programming times through increased current. This feature is intended to facilitate factory throughput during system production, but may also be used in the field if desired.

The devices are entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the device using standard microprocessor write timing. Write cycles also internally latch addresses and data needed for the programming and erase operations.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Device programming and erasure are initiated through command sequences. Once a program or erase operation has begun, the host system need only poll the DQ7 (Data# Polling) or DQ6 (toggle) **status bits** or monitor the **Ready/Busy# (RY/BY#)** output to determine whether the operation is complete. To facilitate programming, an **Unlock Bypass** mode reduces command sequence overhead by requiring only two write cycles to program data instead of four.

The **Enhanced VersatileI/O™** (V_{IO}) control allows the host system to set the voltage levels that the device generates and tolerates on all input levels (address, chip control, and DQ input levels) to the same voltage level that is asserted on the V_{IO} pin. This allows the device to operate in a 1.8 V or 3 V system environment as required.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. **Persistent Sector Protection** provides in-system, command-enabled protection of any combination of sectors using a single power supply at V_{CC}. **Password Sector Protection** prevents unauthorized write and erase operations in any combination of sectors through a user-defined 64-bit password.

The **Erase Suspend/Erase Resume** feature allows the host system to pause an erase operation in a given sector to read or program any other sector and then complete the erase operation. The **Program Suspend/Program Resume** feature enables the host system to pause a program operation in a given sector to read any other sector and then complete the program operation.

The **hardware RESET# pin** terminates any operation in progress and resets the device, after which it is then ready for a new operation. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the host system to read boot-up firmware from the Flash memory device.

The device reduces power consumption in the **standby mode** when it detects specific voltage levels on CE# and RESET#, or when addresses have been stable for a specified period of time.

The **SecSi™ (Secured Silicon) Sector** provides a 128-word/256-byte area for code or data that can be permanently protected. Once this sector is protected, no further changes within the sector can occur.

The **Write Protect (WP#/ACC)** feature protects the first or last sector by asserting a logic low on the WP# pin.

MirrorBit flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via hot-hole assisted erase. The data is programmed using hot electron injection.

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Product Selector Guide

S29GL5I2N

Part Number		S29GL512N			
Speed Option V_{CC} = 2.7–3.6 V	V_{IO} = 2.7–3.6 V	**90**	**10**		
	V_{IO} = 1.65–1.95 V			**10**	**11**
Max. Access Time (ns)		90	100	100	110
Max. CE# Access Time (ns)		90	100	100	110
Max. Page access time (ns)		25	25	35	35
Max. OE# Access Time (ns)		25	25	35	35

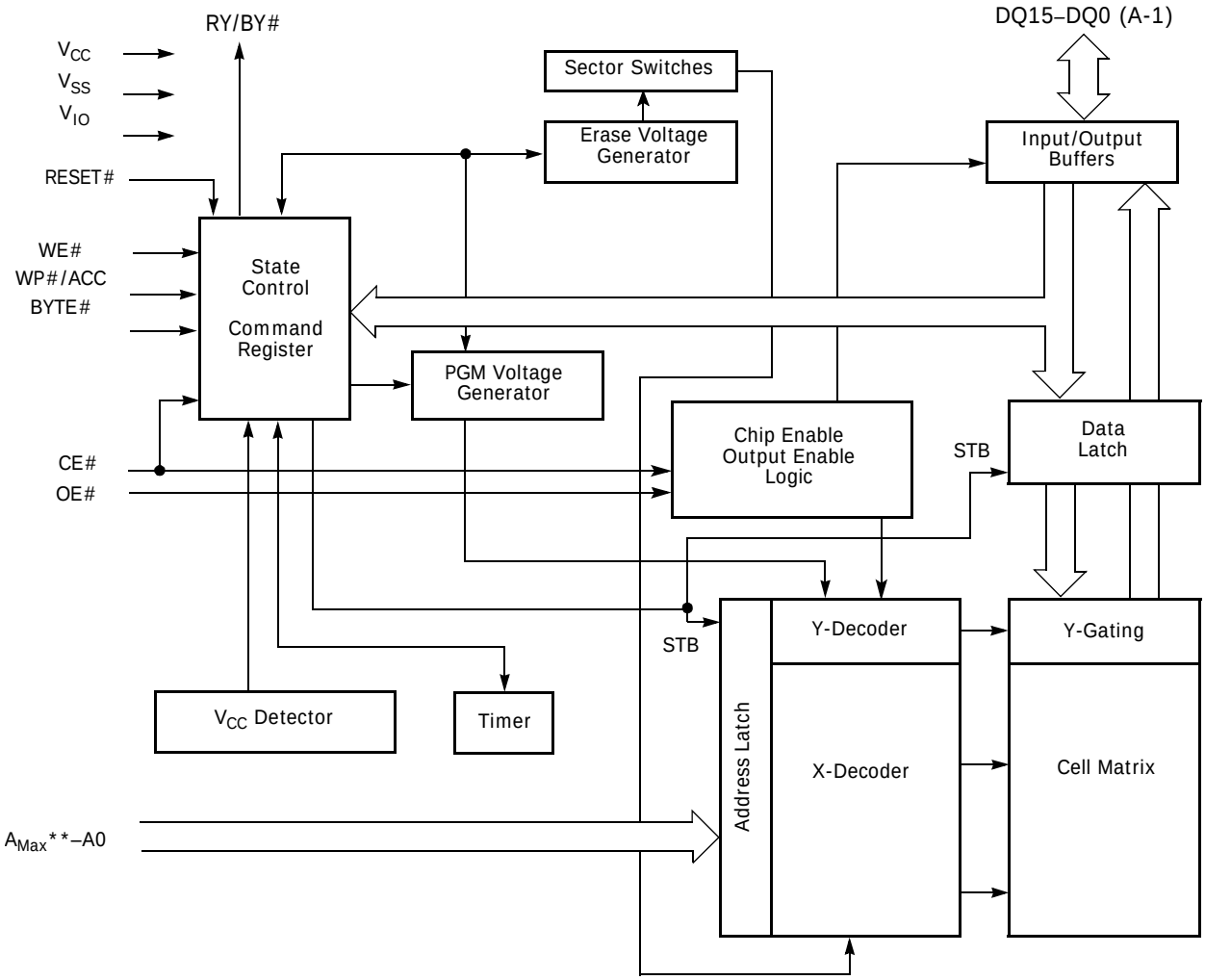
S29GL256N

Part Number		S29GL256N			
Speed Option V_{CC} = 2.7–3.6 V	V_{IO} = 2.7–3.6 V	**80**	**90**		
	V_{IO} = 1.65–1.95 V			**90**	**10**
Max. Access Time (ns)		80	90	90	100
Max. CE# Access Time (ns)		80	90	90	100
Max. Page access time (ns)		25	25	35	35
Max. OE# Access Time (ns)		25	25	35	35

S29GLI28N

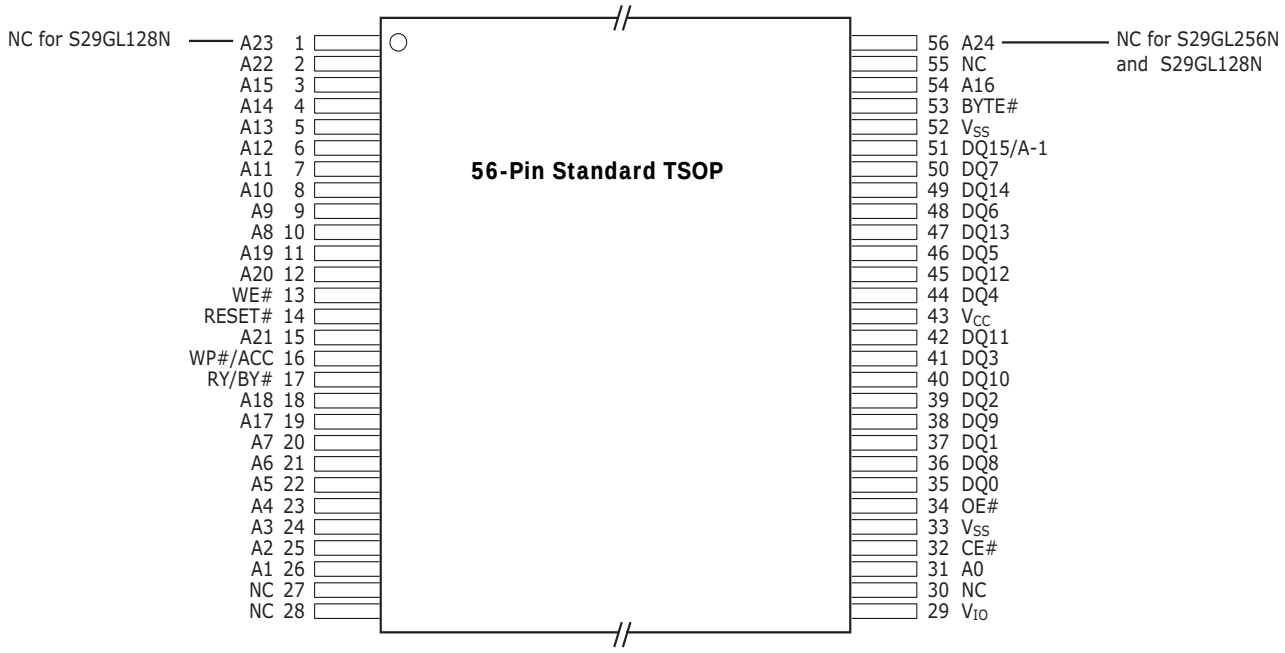
Part Number		S29GL128N			
Speed Option V_{CC} = 2.7–3.6 V	V_{IO} = 2.7–3.6 V	**80**	**90**		
	V_{IO} = 1.65–1.95 V			**90**	**10**
Max. Access Time (ns)		80	90	90	100
Max. CE# Access Time (ns)		80	90	90	100
Max. Page access time (t_{PACC})		25	25	35	35
Max. OE# Access Time (ns)		25	25	35	35

Block Diagram



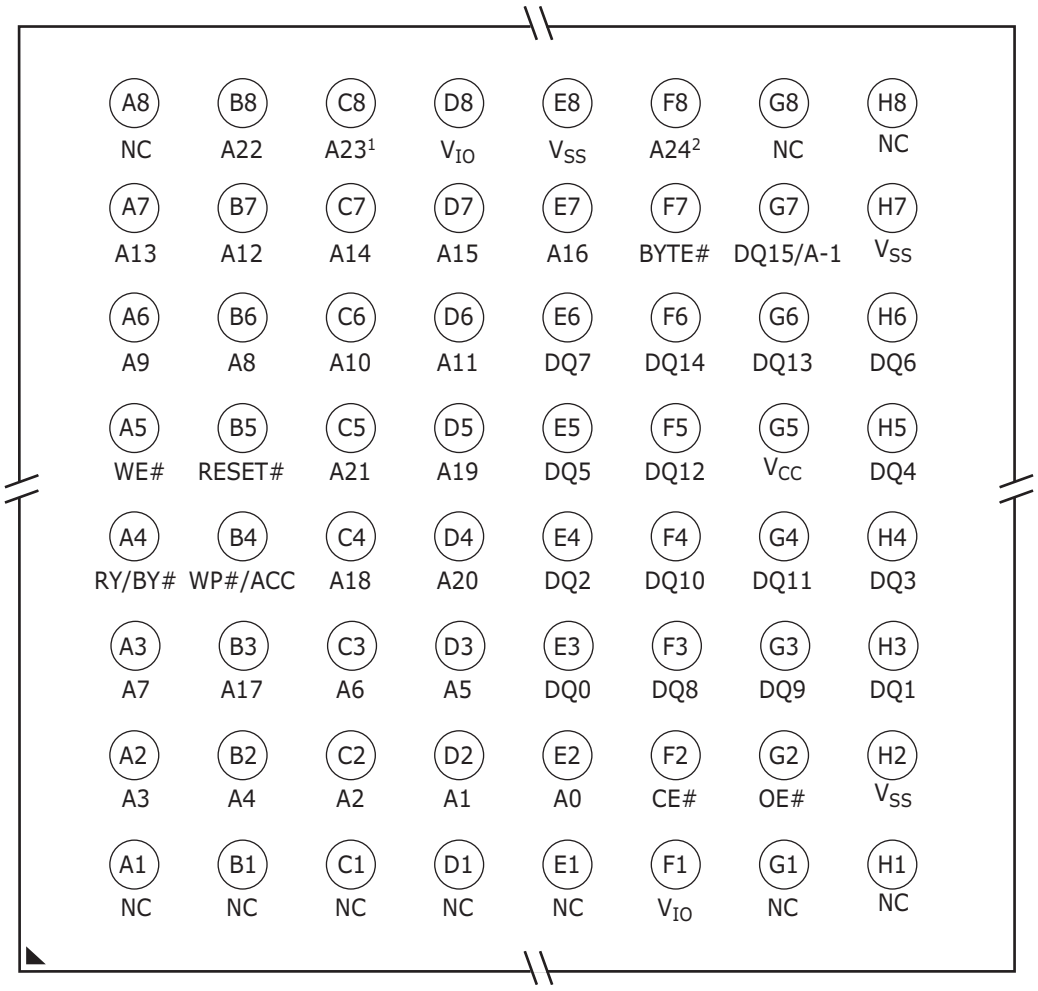
*** A_{Max} GL512N = A24, A_{Max} GL256N = A23, A_{Max} GL128N = A22*

Connection Diagrams



Connection Diagrams

64-ball Fortified BGA
Top View, Balls Facing Down



Note:

1. *Ball C8 is NC on S29GL128N*
2. *Ball F8 is NC on S29GL256N and S29GL128N*

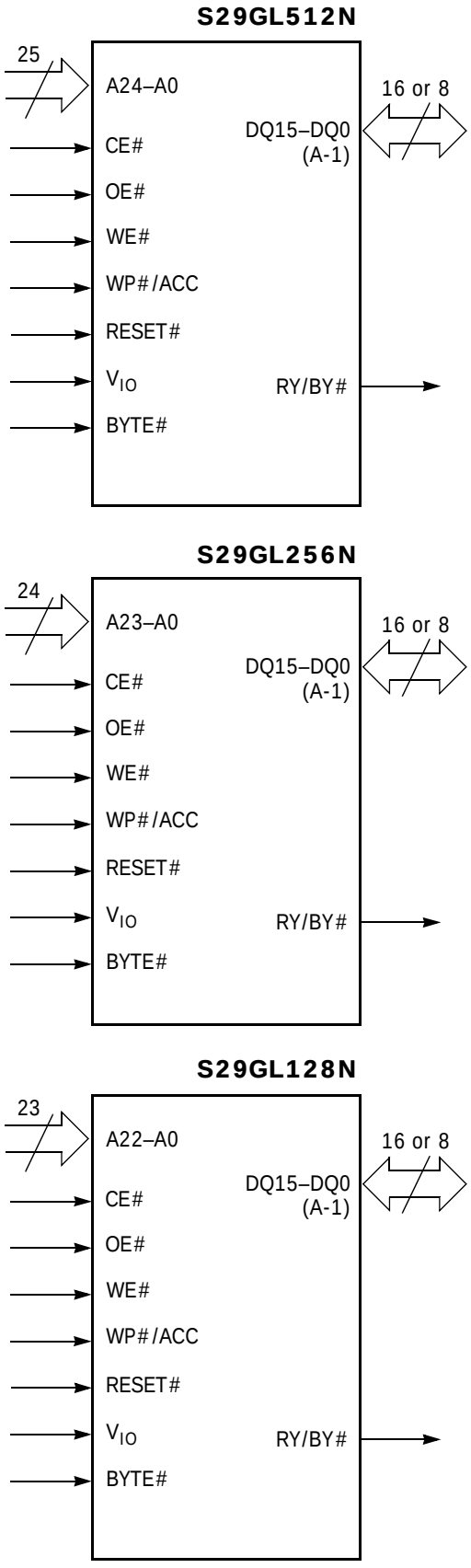
Special Package Handling Instructions

Special handling is required for Flash Memory products in molded packages (TSOP, BGA). The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

PIN DESCRIPTION

A24–A0	=	25 Address inputs (512 Mb)
A23–A0	=	24 Address inputs (256 Mb)
A22–A0	=	23 Address inputs (128 Mb)
DQ14–DQ0	=	15 Data inputs/outputs
DQ15/A-1	=	DQ15 (Data input/output, word mode), A-1 (LSB Address input, byte mode)
CE#	=	Chip Enable input
OE#	=	Output Enable input
WE#	=	Write Enable input
WP#/ACC	=	Hardware Write Protect input; Acceleration input
RESET#	=	Hardware Reset Pin input
BYTE#	=	Selects 8-bit or 16-bit mode
RY/BY#	=	Ready/Busy output
V_{CC}	=	3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
V_{IO}	=	Output Buffer power
V_{SS}	=	Device Ground
NC	=	Pin Not Connected Internally

LOGIC SYMBOL



Ordering Information (512 Mb)

The ordering part number is formed by a valid combination of the following:

S29GL512N 10 F A I 00 0

PACKING TYPE
0 = Tray (standard; see note 1)
3 = 13" Tape and Reel

MODEL NUMBER (V_{IO} range, protection when WP# =V_{IL})
01 = V_{IO} = 2.7 to 3.6 V, highest address sector protected
02 = V_{IO} = 2.7 to 3.6 V, lowest address sector protected$_L$
V1 = V_{IO} = 1.65 to 1.95 V, highest address sector protected
V2 = V_{IO} = 1.65 to 1.95 V, lowest address sector protected

TEMPERATURE RANGE
I = Industrial (–40°C to +85°C)

PACKAGE MATERIALS SET
A = Standard
F = Pb-free

PACKAGE TYPE
T = Thin Small Outline Package (TSOP) Standard Pinout
F = Fortified Ball Grid Array, 1.0 mm pitch package

SPEED OPTION
90 = 90 ns
10 = 100 ns
11 = 110 ns

DEVICE NUMBER/DESCRIPTION
S29GL512N
3.0 Volt-only, 512 Megabit (32 M x 16-Bit/64 M x 8-Bit) Page-Mode Flash Memory
Manufactured on 110 nm MirrorBit™ process technology

S29GL512N Valid Combinations					Package Description	
512 Mb	Speed (ns)	Package & Temperature	Model Number	Pack Type		
S29GL512N	90, 10	TAI, TFI FAI, FFI	01, 02	0, 3 (Note 1)	TS056 (Note 2)	TSOP
	10, 11		V1, V2		LAA064 (Note 3)	Fortified BGA

Notes:
1. *Type 0 is standard. Specify other options as required.*
2. *TSOP package marking omits packing type designator from ordering part number.*
3. *BGA package marking omits leading "S29" and packing type designator from ordering part number.*

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Ordering Information (256 Mb)

The ordering part number is formed by a valid combination of the following:

S29GL256N 90 T A I 00 0

PACKING TYPE
0 = Tray (standard; see note 1)
3 = 13” Tape and Reel

MODEL NUMBER (V_{IO} range, protection when WP# =V_{IL})
01 = V_{IO} = 2.7 to 3.6 V, highest address sector protected
02 = V_{IO} = 2.7 to 3.6 V, lowest address sector protected
V1 = V_{IO} = 1.65 to 1.95 V, highest address sector protected
V2 = V_{IO} = 1.65 to 1.95 V, lowest address sector protected

TEMPERATURE RANGE
I = Industrial (–40°C to +85°C)

PACKAGE MATERIALS SET
A = Standard
F = Pb-free

PACKAGE TYPE
T = Thin Small Outline Package (TSOP) Standard Pinout
F = Fortified Ball Grid Array, 1.0 mm pitch package

SPEED OPTION
80 = 80 ns
90 = 90 ns
10 = 100 ns

DEVICE NUMBER/DESCRIPTION
S29GL256N
3.0 Volt-only, 256 Megabit (16 M x 16-Bit/64 M x 8-Bit) Page-Mode Flash Memory
Manufactured on 110 nm MirrorBit™ process technology

S29GL512N Valid Combinations					Package Description	
256 Mb	Speed (ns)	Package & Temperature	Model Number	Pack Type		
S29GL256N	80, 90	TAI, TFI FAI, FFI	01, 02	0, 2 (Note 1)	TS056 (Note 2)	TSOP
	90, 10		V1, V2		LAA064 (Note 3)	Fortified BGA

Notes:
1. *Type 0 is standard. Specify other options as required.*
2. *TSOP package marking omits packing type designator from ordering part number.*
3. *BGA package marking omits leading “S29” and packing type designator from ordering part number.*

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Ordering Information (I28 Mb)

The ordering part number is formed by a valid combination of the following:

S29GLI28N 90 T A I 00 0

PACKING TYPE
0 = Tray (standard; see note 1)
3 = 13” Tape and Reel

MODEL NUMBER (V_{IO} range, protection when WP# =V_{IL})
01 = V_{IO} = 2.7 to 3.6 V, highest address sector protected
02 = V_{IO} = 2.7 to 3.6 V, lowest address sector protected$_L$
V1 = V_{IO} = 1.65 to 1.95 V, highest address sector protected
V2 = V_{IO} = 1.65 to 1.95 V, lowest address sector protected

TEMPERATURE RANGE
I = Industrial (–40°C to +85°C)

PACKAGE MATERIALS SET
A = Standard
F = Pb-free

PACKAGE TYPE
T = Thin Small Outline Package (TSOP) Standard Pinout
F = Fortified Ball Grid Array, 1.0 mm pitch package

SPEED OPTION
80 = 80 ns
90 = 90 ns
10 = 100 ns

DEVICE NUMBER/DESCRIPTION
S29GL128N
3.0 Volt-only, 512 Megabit (32 M x 16-Bit/64 M x 8-Bit) Page-Mode Flash Memory
Manufactured on 110 nm MirrorBit™ process technology

S29GL512N Valid Combinations					Package Description	
128 Mb	**Speed (ns)**	**Package & Temperature**	**Model Number**	**Pack Type**		
S29GL128N	80, 90	TAI, TFI FAI, FFI	01, 02	0, 3 (Note 1)	TS056 (Note 2)	TSOP
	90, 10		V1, V2		LAA064 (Note 3)	Fortified BGA

Notes:
1. *Type 0 is standard. Specify other options as required.*
2. *TSOP package marking omits packing type designator from ordering part number.*
3. *BGA package marking omits leading “S29” and packing type designator from ordering part number.*

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table I. Device Bus Operations

Operation	CE#	OE#	WE #	RESET#	WP# / ACC	Addresses (Note 2)	DQ0–DQ7	DQ8–DQ15	
								BYTE# = V_{IH}	BYTE# = V_{IL}
Read	L	L	H	H	X	A_{IN}	D_{OUT}	D_{OUT}	DQ8–DQ14 = High-Z, DQ15 = A-1
Write (Program/Erase)	L	H	L	H	Note 2	A_{IN}	(Note 3)	(Note 3)	
Accelerated Program	L	H	L	H	V_{HH}	A_{IN}	(Note 3)	(Note 3)	
Standby	V_{CC} ± 0.3 V	X	X	V_{CC} ± 0.3 V	H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	X	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	X	X	High-Z	High-Z	High-Z

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 11.5–12.5 V, V_{HH} = 11.5–12.5V, X = Don't Care, SA = Sector Address, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out*

Notes:

1. *Addresses are AMax:A0 in word mode; A_{Max}:A-1 in byte mode. Sector addresses are A_{Max}:A16 in both modes.*
2. *If WP# = V_{IL}, the first or last sector group remains protected. If WP# = V_{IH}, the first or last sector will be protected or unprotected as determined by the method described in "Write Protect (WP#)". All sectors are unprotected when shipped from the factory (The SecSi Sector may be factory protected depending on version ordered.)*
3. *D_{IN} or D_{OUT} as required by command sequence, data polling, or sector protect algorithm (see Figure 2).*

Word/Byte Configuration

The BYTE# pin controls whether the device data I/O pins operate in the byte or word configuration. If the BYTE# pin is set at logic '1', the device is in word configuration, DQ0–DQ15 are active and controlled by CE# and OE#.

If the BYTE# pin is set at logic '0', the device is in byte configuration, and only data I/O pins DQ0–DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8–DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

VersatileIO™ (V_{IO}) Control

The **VersatileIO**™ (V_{IO}) control allows the host system to set the voltage levels that the device generates and tolerates on CE# and DQ I/Os to the same voltage

level that is asserted on V_{IO}. See Ordering Information for V_{IO} options on this device.

For example, a $V_{I/O}$ of 1.65–3.6 volts allows for I/O at the 1.8 or 3 volt levels, driving and receiving signals to and from other 1.8 or 3 V devices on the same data bus.

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See “Reading Array Data” for more information. Refer to the AC Read-Only Operations table for timing specifications and to Figure 11 for the timing diagram. Refer to the DC Characteristics table for the active current specification on reading array data.

Page Mode Read

The device is capable of fast page mode read and is compatible with the page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. The page size of the device is 8 words/16 bytes. The appropriate page is selected by the higher address bits A(max)–A3. Address bits A2–A0 in word mode (A2–A-1 in byte mode) determine the specific word within a page. This is an asynchronous operation; the microprocessor supplies the specific word location.

The random or initial page access is equal to t_{ACC} or t_{CE} and subsequent page read accesses (as long as the locations specified by the microprocessor falls within that page) is equivalent to t_{PACC}. When CE# is de-asserted and reasserted for a subsequent access, the access time is t_{ACC} or t_{CE}. Fast page mode accesses are obtained by keeping the “read-page addresses” constant and changing the “intra-read page” addresses.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. The “Word/Byte Program Command Sequence” section has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 2 indicates the address space that each sector occupies.

Refer to the DC Characteristics table for the active current specification for the write mode. The AC Characteristics section contains timing specification tables and timing diagrams for write operations.

Write Buffer

Write Buffer Programming allows the system write to a maximum of 16 words/32 bytes in one programming operation. This results in faster effective programming time than the standard programming algorithms. See “Write Buffer” for more information.

Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This is one of two functions provided by the WP#/ACC pin. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts V_{HH} on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sector groups, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the WP#/ACC pin returns the device to normal operation. *Note that the WP#/ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result. WP# has an internal pullup; when unconnected, WP# is at V_{IH}.*

Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the “Autoselect Mode” section on page 44 and “Autoselect Command Sequence” section on page 58 sections for more information.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at V_{IO} ± 0.3 V. (Note that this is a more restricted voltage range than V_{IH}.) If CE# and RESET# are held at V_{IH}, but not within V_{IO} ± 0.3 V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

Refer to the “DC Characteristics” section on page 86 for the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# con-

trol signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. Refer to the "DC Characteristics" section on page 86 for the automatic sleep mode current specification.

RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS}±0.3 V, the device draws CMOS standby current (I_{CC5}). If RESET# is held at V_{IL} but not within V_{SS}±0.3 V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

Refer to the AC Characteristics tables for RESET# parameters and to Figure 13 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Table 2. Sector Address Table–S29GL5I2N

Sector	A24–A16									Sector Size (Kbytes/ Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA0	0	0	0	0	0	0	0	0	0	128/64	0000000–001FFFF	0000000–000FFFF
SA1	0	0	0	0	0	0	0	0	1	128/64	0020000–003FFFF	0010000–001FFFF
SA2	0	0	0	0	0	0	0	1	0	128/64	0040000–005FFFF	0020000–002FFFF
SA3	0	0	0	0	0	0	0	1	1	128/64	0060000–007FFFF	0030000–003FFFF
SA4	0	0	0	0	0	0	1	0	0	128/64	0080000–009FFFF	0040000–004FFFF
SA5	0	0	0	0	0	0	1	0	1	128/64	00A0000–00BFFFF	0050000–005FFFF
SA6	0	0	0	0	0	0	1	1	0	128/64	00C0000–00DFFFF	0060000–006FFFF
SA7	0	0	0	0	0	0	1	1	1	128/64	00E0000–00FFFFF	0070000–007FFFF
SA8	0	0	0	0	0	1	0	0	0	128/64	0100000–011FFFF	0080000–008FFFF
SA9	0	0	0	0	0	1	0	0	1	128/64	0120000–013FFFF	0090000–009FFFF
SA10	0	0	0	0	0	1	0	1	0	128/64	0140000–015FFFF	00A0000–00AFFFF
SA11	0	0	0	0	0	1	0	1	1	128/64	0160000–017FFFF	00B0000–00BFFFF
SA12	0	0	0	0	0	1	1	0	0	128/64	0180000–019FFFF	00C0000–00CFFFF
SA13	0	0	0	0	0	1	1	0	1	128/64	01A0000–01BFFFF	00D0000–00DFFFF

Table 2. Sector Address Table–S29GL5I2N (Continued)

Sector	A24–A16									Sector Size (Kbytes/ Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA14	0	0	0	0	0	1	1	1	0	128/64	01C0000–01DFFFF	00E0000–00EFFFF
SA15	0	0	0	0	0	1	1	1	1	128/64	01E0000–01FFFFF	00F0000–00FFFFF
SA16	0	0	0	0	1	0	0	0	0	128/64	0200000–021FFFF	0100000–010FFFF
SA17	0	0	0	0	1	0	0	0	1	128/64	0220000–023FFFF	0110000–011FFFF
SA18	0	0	0	0	1	0	0	1	0	128/64	0240000–025FFFF	0120000–012FFFF
SA19	0	0	0	0	1	0	0	1	1	128/64	0260000–027FFFF	0130000–013FFFF
SA20	0	0	0	0	1	0	1	0	0	128/64	0280000–029FFFF	0140000–014FFFF
SA21	0	0	0	0	1	0	1	0	1	128/64	02A0000–02BFFFF	0150000–015FFFF
SA22	0	0	0	0	1	0	1	1	0	128/64	02C0000–02DFFFF	0160000–016FFFF
SA23	0	0	0	0	1	0	1	1	1	128/64	02E0000–02FFFFF	0170000–017FFFF
SA24	0	0	0	0	1	1	0	0	0	128/64	0300000–031FFFF	0180000–018FFFF
SA25	0	0	0	0	1	1	0	0	1	128/64	0320000–033FFFF	0190000–019FFFF
SA26	0	0	0	0	1	1	0	1	0	128/64	0340000–035FFFF	01A0000–01AFFFF
SA27	0	0	0	0	1	1	0	1	1	128/64	0360000–037FFFF	01B0000–01BFFFF
SA28	0	0	0	0	1	1	1	0	0	128/64	0380000–039FFFF	01C0000–01CFFFF
SA29	0	0	0	0	1	1	1	0	1	128/64	03A0000–03BFFFF	01D0000–01DFFFF
SA30	0	0	0	0	1	1	1	1	0	128/64	03C0000–03DFFFF	01E0000–01EFFFF
SA31	0	0	0	0	1	1	1	1	1	128/64	03E0000–0EFFFFF	01F0000–01FFFFF
SA32	0	0	0	1	0	0	0	0	0	128/64	0400000–041FFFF	0200000–020FFFF
SA33	0	0	0	1	0	0	0	0	1	128/64	0420000–043FFFF	0210000–021FFFF
SA34	0	0	0	1	0	0	0	1	0	128/64	0440000–045FFFF	0220000–022FFFF
SA35	0	0	0	1	0	0	0	1	1	128/64	0460000–047FFFF	0230000–023FFFF
SA36	0	0	0	1	0	0	1	0	0	128/64	0480000–049FFFF	0240000–024FFFF
SA37	0	0	0	1	0	0	1	0	1	128/64	04A0000–04BFFFF	0250000–025FFFF
SA38	0	0	0	1	0	0	1	1	0	128/64	04C0000–04DFFFF	0260000–026FFFF
SA39	0	0	0	1	0	0	1	1	1	128/64	04E0000–04FFFFF	0270000–027FFFF
SA40	0	0	0	1	0	1	0	0	0	128/64	0500000–051FFFF	0280000–028FFFF
SA41	0	0	0	1	0	1	0	0	1	128/64	0520000–053FFFF	0290000–029FFFF
SA42	0	0	0	1	0	1	0	1	0	128/64	0540000–055FFFF	02A0000–02AFFFF
SA43	0	0	0	1	0	1	0	1	1	128/64	0560000–057FFFF	02B0000–02BFFFF
SA44	0	0	0	1	0	1	1	0	0	128/64	0580000–059FFFF	02C0000–02CFFFF
SA45	0	0	0	1	0	1	1	0	1	128/64	05A0000–05BFFFF	02D0000–02DFFFF
SA46	0	0	0	1	0	1	1	1	0	128/64	05C0000–05DFFFF	02E0000–02EFFFF
SA47	0	0	0	1	0	1	1	1	1	128/64	05E0000–05FFFFF	02F0000–02FFFFF
SA48	0	0	0	1	1	0	0	0	0	128/64	0600000–061FFFF	0300000–030FFFF

Table 2. Sector Address Table–S29GL5I2N (Continued)

Sector	A24–A16									Sector Size (Kbytes/ Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA49	0	0	0	1	1	0	0	0	1	128/64	0620000–063FFFF	0310000–031FFFF
SA50	0	0	0	1	1	0	0	1	0	128/64	0640000–065FFFF	0320000–032FFFF
SA51	0	0	0	1	1	0	0	1	1	128/64	0660000–067FFFF	0330000–033FFFF
SA52	0	0	0	1	1	0	1	0	0	128/64	0680000–069FFFF	0340000–034FFFF
SA53	0	0	0	1	1	0	1	0	1	128/64	06A0000–06BFFFF	0350000–035FFFF
SA54	0	0	0	1	1	0	1	1	0	128/64	06C0000–06DFFFF	0360000–036FFFF
SA55	0	0	0	1	1	0	1	1	1	128/64	06E0000–06FFFFF	0370000–037FFFF
SA56	0	0	0	1	1	1	0	0	0	128/64	0700000–071FFFF	0380000–038FFFF
SA57	0	0	0	1	1	1	0	0	1	128/64	0720000–073FFFF	0390000–039FFFF
SA58	0	0	0	1	1	1	0	1	0	128/64	0740000–075FFFF	03A0000–03AFFFF
SA59	0	0	0	1	1	1	0	1	1	128/64	0760000–077FFFF	03B0000–03BFFFF
SA60	0	0	0	1	1	1	1	0	0	128/64	0780000–079FFFF	03C0000–03CFFFF
SA61	0	0	0	1	1	1	1	0	1	128/64	07A0000–07BFFFF	03D0000–03DFFFF
SA62	0	0	0	1	1	1	1	1	0	128/64	07C0000–07DFFFF	03E0000–03EFFFF
SA63	0	0	0	1	1	1	1	1	1	128/64	07E0000–07FFFFF	03F0000–03FFFFF
SA64	0	0	1	0	0	0	0	0	0	128/64	0800000–081FFFF	0400000–040FFFF
SA65	0	0	1	0	0	0	0	0	1	128/64	0820000–083FFFF	0410000–041FFFF
SA66	0	0	1	0	0	0	0	1	0	128/64	0840000–085FFFF	0420000–042FFFF
SA67	0	0	1	0	0	0	0	1	1	128/64	0860000–087FFFF	0430000–043FFFF
SA68	0	0	1	0	0	0	1	0	0	128/64	0880000–089FFFF	0440000–044FFFF
SA69	0	0	1	0	0	0	1	0	1	128/64	08A0000–08BFFFF	0450000–045FFFF
SA70	0	0	1	0	0	0	1	1	0	128/64	08C0000–08DFFFF	0460000–046FFFF
SA71	0	0	1	0	0	0	1	1	1	128/64	08E0000–08FFFFF	0470000–047FFFF
SA72	0	0	1	0	0	1	0	0	0	128/64	0900000–091FFFF	0480000–048FFFF
SA73	0	0	1	0	0	1	0	0	1	128/64	0920000–093FFFF	0490000–049FFFF
SA74	0	0	1	0	0	1	0	1	0	128/64	0940000–095FFFF	04A0000–04AFFFF
SA75	0	0	1	0	0	1	0	1	1	128/64	0960000–097FFFF	04B0000–04BFFFF
SA76	0	0	1	0	0	1	1	0	0	128/64	0980000–099FFFF	04C0000–04CFFFF
SA77	0	0	1	0	0	1	1	0	1	128/64	09A0000–09BFFFF	04D0000–04DFFFF
SA78	0	0	1	0	0	1	1	1	0	128/64	09C0000–09DFFFF	04E0000–04EFFFF
SA79	0	0	1	0	0	1	1	1	1	128/64	09E0000–09FFFFF	04F0000–04FFFFF
SA80	0	0	1	0	1	0	0	0	0	128/64	0A00000–0A1FFFF	0500000–050FFFF
SA81	0	0	1	0	1	0	0	0	1	128/64	0A20000–0A3FFFF	0510000–051FFFF
SA82	0	0	1	0	1	0	0	1	0	128/64	0A40000–0A5FFFF	0520000–052FFFF
SA83	0	0	1	0	1	0	0	1	1	128/64	0A60000–0A7FFFF	0530000–053FFFF

Table 2. Sector Address Table–S29GL5I2N (Continued)

Sector	A24–A16									Sector Size (Kbytes/ Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA84	0	0	1	0	1	0	1	0	0	128/64	0A80000–0A9FFFF	0540000–054FFFF
SA85	0	0	1	0	1	0	1	0	1	128/64	0AA0000–0ABFFFF	0550000–055FFFF
SA86	0	0	1	0	1	0	1	1	0	128/64	0AC0000–0ADFFFF	0560000–056FFFF
SA87	0	0	1	0	1	0	1	1	1	128/64	0AE0000–0AFFFFF	0570000–057FFFF
SA88	0	0	1	0	1	1	0	0	0	128/64	0B00000–0B1FFFF	0580000–058FFFF
SA89	0	0	1	0	1	1	0	0	1	128/64	0B20000–0B3FFFF	0590000–059FFFF
SA90	0	0	1	0	1	1	0	1	0	128/64	0B40000–0B5FFFF	05A0000–05AFFFF
SA91	0	0	1	0	1	1	0	1	1	128/64	0B60000–0B7FFFF	05B0000–05BFFFF
SA92	0	0	1	0	1	1	1	0	0	128/64	0B80000–0B9FFFF	05C0000–05CFFFF
SA93	0	0	1	0	1	1	1	0	1	128/64	0BA0000–0BBFFFF	05D0000–05DFFFF
SA94	0	0	1	0	1	1	1	1	0	128/64	0BC0000–0BDFFFF	05E0000–05EFFFF
SA95	0	0	1	0	1	1	1	1	1	128/64	0BE0000–0BFFFFF	05F0000–05FFFFF
SA96	0	0	1	1	0	0	0	0	0	128/64	0C00000–0C1FFFF	0600000–060FFFF
SA97	0	0	1	1	0	0	0	0	1	128/64	0C20000–0C3FFFF	0610000–061FFFF
SA98	0	0	1	1	0	0	0	1	0	128/64	0C40000–0C5FFFF	0620000–062FFFF
SA99	0	0	1	1	0	0	0	1	1	128/64	0C60000–0C7FFFF	0630000–063FFFF
SA100	0	0	1	1	0	0	1	0	0	128/64	0C80000–0C9FFFF	0640000–064FFFF
SA101	0	0	1	1	0	0	1	0	1	128/64	0CA0000–0CBFFFF	0650000–065FFFF
SA102	0	0	1	1	0	0	1	1	0	128/64	0CC0000–0CDFFFF	0660000–066FFFF
SA103	0	0	1	1	0	0	1	1	1	128/64	0CE0000–0CFFFFF	0670000–067FFFF
SA104	0	0	1	1	0	1	0	0	0	128/64	0D00000–0D1FFFF	0680000–068FFFF
SA105	0	0	1	1	0	1	0	0	1	128/64	0D20000–0D3FFFF	0690000–069FFFF
SA106	0	0	1	1	0	1	0	1	0	128/64	0D40000–0D5FFFF	06A0000–06AFFFF
SA107	0	0	1	1	0	1	0	1	1	128/64	0D60000–0D7FFFF	06B0000–06BFFFF
SA108	0	0	1	1	0	1	1	0	0	128/64	0D80000–0D9FFFF	06C0000–06CFFFF
SA109	0	0	1	1	0	1	1	0	1	128/64	0DA0000–0DBFFFF	06D0000–06DFFFF
SA110	0	0	1	1	0	1	1	1	0	128/64	0DC0000–0DDFFFF	06E0000–06EFFFF
SA111	0	0	1	1	0	1	1	1	1	128/64	0DE0000–0DFFFFF	06F0000–06FFFFF
SA112	0	0	1	1	1	0	0	0	0	128/64	0E00000–0E1FFFF	0700000–070FFFF
SA113	0	0	1	1	1	0	0	0	1	128/64	0E20000–0E3FFFF	0710000–071FFFF
SA114	0	0	1	1	1	0	0	1	0	128/64	0E40000–0E5FFFF	0720000–072FFFF
SA115	0	0	1	1	1	0	0	1	1	128/64	0E60000–0E7FFFF	0730000–073FFFF
SA116	0	0	1	1	1	0	1	0	0	128/64	0E80000–0E9FFFF	0740000–074FFFF
SA117	0	0	1	1	1	0	1	0	1	128/64	0EA0000–0EBFFFF	0750000–075FFFF
SA118	0	0	1	1	1	0	1	1	0	128/64	0EC0000–0EDFFFF	0760000–076FFFF

Table 2. Sector Address Table–S29GL5I2N (Continued)

Sector	A24–A16									Sector Size (Kbytes/ Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA119	0	0	1	1	1	0	1	1	1	128/64	0EE0000–0EFFFFF	0770000–077FFFF
SA120	0	0	1	1	1	1	0	0	0	128/64	0F00000–0F1FFFF	0780000–078FFFF
SA121	0	0	1	1	1	1	0	0	1	128/64	0F20000–0F3FFFF	0790000–079FFFF
SA122	0	0	1	1	1	1	0	1	0	128/64	0F40000–0F5FFFF	07A0000–07AFFFF
SA123	0	0	1	1	1	1	0	1	1	128/64	0F60000–0F7FFFF	07B0000–07BFFFF
SA124	0	0	1	1	1	1	1	0	0	128/64	0F80000–0F9FFFF	07C0000–07CFFFF
SA125	0	0	1	1	1	1	1	0	1	128/64	0FA0000–0FBFFFF	07D0000–07DFFFF
SA126	0	0	1	1	1	1	1	1	0	128/64	0FC0000–0FDFFFF	07E0000–07EFFFF
SA127	0	0	1	1	1	1	1	1	1	128/64	0FE0000–0FFFFFF	07F0000–07FFFFF
SA128	0	1	0	0	0	0	0	0	0	128/64	1000000–101FFFF	0800000–080FFFF
SA129	0	1	0	0	0	0	0	0	1	128/64	1020000–103FFFF	0810000–081FFFF
SA130	0	1	0	0	0	0	0	1	0	128/64	1040000–105FFFF	0820000–082FFFF
SA131	0	1	0	0	0	0	0	1	1	128/64	1060000–017FFFF	0830000–083FFFF
SA132	0	1	0	0	0	0	1	0	0	128/64	1080000–109FFFF	0840000–084FFFF
SA133	0	1	0	0	0	0	1	0	1	128/64	10A0000–10BFFFF	0850000–085FFFF
SA134	0	1	0	0	0	0	1	1	0	128/64	10C0000–10DFFFF	0860000–086FFFF
SA135	0	1	0	0	0	0	1	1	1	128/64	10E0000–10FFFFF	0870000–087FFFF
SA136	0	1	0	0	0	1	0	0	0	128/64	1100000–111FFFF	0880000–088FFFF
SA137	0	1	0	0	0	1	0	0	1	128/64	1120000–113FFFF	0890000–089FFFF
SA138	0	1	0	0	0	1	0	1	0	128/64	1140000–115FFFF	08A0000–08AFFFF
SA139	0	1	0	0	0	1	0	1	1	128/64	1160000–117FFFF	08B0000–08BFFFF
SA140	0	1	0	0	0	1	1	0	0	128/64	1180000–119FFFF	08C0000–08CFFFF
SA141	0	1	0	0	0	1	1	0	1	128/64	11A0000–11BFFFF	08D0000–08DFFFF
SA142	0	1	0	0	0	1	1	1	0	128/64	11C0000–11DFFFF	08E0000–08EFFFF
SA143	0	1	0	0	0	1	1	1	1	128/64	11E0000–11FFFFF	08F0000–08FFFFF
SA144	0	1	0	0	1	0	0	0	0	128/64	1200000–121FFFF	0900000–090FFFF
SA145	0	1	0	0	1	0	0	0	1	128/64	1220000–123FFFF	0910000–091FFFF
SA146	0	1	0	0	1	0	0	1	0	128/64	1240000–125FFFF	0920000–092FFFF
SA147	0	1	0	0	1	0	0	1	1	128/64	1260000–127FFFF	0930000–093FFFF
SA148	0	1	0	0	1	0	1	0	0	128/64	1280000–129FFFF	0940000–094FFFF
SA149	0	1	0	0	1	0	1	0	1	128/64	12A0000–12BFFFF	0950000–095FFFF
SA150	0	1	0	0	1	0	1	1	0	128/64	12C0000–12DFFFF	0960000–096FFFF
SA151	0	1	0	0	1	0	1	1	1	128/64	12E0000–12FFFFF	0970000–097FFFF
SA152	0	1	0	0	1	1	0	0	0	128/64	1300000–131FFFF	0980000–098FFFF
SA153	0	1	0	0	1	1	0	0	1	128/64	1320000–133FFFF	0990000–099FFFF

Table 2. Sector Address Table–S29GL5I2N (Continued)

Sector	A24–A16									Sector Size (Kbytes/ Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA154	0	1	0	0	1	1	0	1	0	128/64	1340000–135FFFF	09A0000–09AFFFF
SA155	0	1	0	0	1	1	0	1	1	128/64	1360000–137FFFF	09B0000–09BFFFF
SA156	0	1	0	0	1	1	1	0	0	128/64	1380000–139FFFF	09C0000–09CFFFF
SA157	0	1	0	0	1	1	1	0	1	128/64	13A0000–13BFFFF	09D0000–09DFFFF
SA158	0	1	0	0	1	1	1	1	0	128/64	13C0000–13DFFFF	09E0000–09EFFFF
SA159	0	1	0	0	1	1	1	1	1	128/64	13E0000–13FFFFF	09F0000–09FFFFF
SA160	0	1	0	1	0	0	0	0	0	128/64	1400000–141FFFF	0A00000–0A0FFFF
SA161	0	1	0	1	0	0	0	0	1	128/64	1420000–143FFFF	0A10000–0A1FFFF
SA162	0	1	0	1	0	0	0	1	0	128/64	1440000–145FFFF	0A20000–0A2FFFF
SA163	0	1	0	1	0	0	0	1	1	128/64	1460000–147FFFF	0A30000–0A3FFFF
SA164	0	1	0	1	0	0	1	0	0	128/64	1480000–149FFFF	0A40000–0A4FFFF
SA165	0	1	0	1	0	0	1	0	1	128/64	14A0000–14BFFFF	0A50000–0A5FFFF
SA166	0	1	0	1	0	0	1	1	0	128/64	14C0000–14DFFFF	0A60000–0A6FFFF
SA167	0	1	0	1	0	0	1	1	1	128/64	14E0000–14FFFFF	0A70000–0A7FFFF
SA168	0	1	0	1	0	1	0	0	0	128/64	1500000–151FFFF	0A80000–0A8FFFF
SA169	0	1	0	1	0	1	0	0	1	128/64	1520000–153FFFF	0A90000–0A9FFFF
SA170	0	1	0	1	0	1	0	1	0	128/64	1540000–155FFFF	0AA0000–0AAFFFF
SA171	0	1	0	1	0	1	0	1	1	128/64	1560000–157FFFF	0AB0000–0ABFFFF
SA172	0	1	0	1	0	1	1	0	0	128/64	1580000–159FFFF	0AC0000–0ACFFFF
SA173	0	1	0	1	0	1	1	0	1	128/64	15A0000–15BFFFF	0AD0000–0ADFFFF
SA174	0	1	0	1	0	1	1	1	0	128/64	15C0000–15DFFFF	0AE0000–0AEFFFF
SA175	0	1	0	1	0	1	1	1	1	128/64	15E0000–15FFFFF	0AF0000–0AFFFFF
SA176	0	1	0	1	1	0	0	0	0	128/64	160000–161FFFF	0B00000–0B0FFFF
SA177	0	1	0	1	1	0	0	0	1	128/64	1620000–163FFFF	0B10000–0B1FFFF
SA178	0	1	0	1	1	0	0	1	0	128/64	1640000–165FFFF	0B20000–0B2FFFF
SA179	0	1	0	1	1	0	0	1	1	128/64	1660000–167FFFF	0B30000–0B3FFFF
SA180	0	1	0	1	1	0	1	0	0	128/64	1680000–169FFFF	0B40000–0B4FFFF
SA181	0	1	0	1	1	0	1	0	1	128/64	16A0000–16BFFFF	0B50000–0B5FFFF
SA182	0	1	0	1	1	0	1	1	0	128/64	16C0000–16DFFFF	0B60000–0B6FFFF
SA183	0	1	0	1	1	0	1	1	1	128/64	16E0000–16FFFFF	0B70000–0B7FFFF
SA184	0	1	0	1	1	1	0	0	0	128/64	1700000–171FFFF	0B80000–0B8FFFF
SA185	0	1	0	1	1	1	0	0	1	128/64	1720000–173FFFF	0B90000–0B9FFFF
SA186	0	1	0	1	1	1	0	1	0	128/64	1740000–175FFFF	0BA0000–0BAFFFF
SA187	0	1	0	1	1	1	0	1	1	128/64	1760000–177FFFF	0BB0000–0BBFFFF
SA188	0	1	0	1	1	1	1	0	0	128/64	1780000–179FFFF	0BC0000–0BCFFFF

Table 2. Sector Address Table–S29GL5I2N (Continued)

Sector	A24–A16									Sector Size (Kbytes/ Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA189	0	1	0	1	1	1	1	0	1	128/64	17A0000–17BFFFF	0BD0000–0BDFFFF
SA190	0	1	0	1	1	1	1	1	0	128/64	17C0000–17DFFFF	0BE0000–0BEFFFF
SA191	0	1	0	1	1	1	1	1	1	128/64	17E0000–17FFFFF	0BF0000–0BFFFFF
SA192	0	1	1	0	0	0	0	0	0	128/64	1800000–181FFFF	0C00000–0C0FFFF
SA193	0	1	1	0	0	0	0	0	1	128/64	1820000–183FFFF	0C10000–0C1FFFF
SA194	0	1	1	0	0	0	0	1	0	128/64	1840000–185FFFF	0C20000–0C2FFFF
SA195	0	1	1	0	0	0	0	1	1	128/64	1860000–187FFFF	0C30000–0C3FFFF
SA196	0	1	1	0	0	0	1	0	0	128/64	1880000–189FFFF	0C40000–0C4FFFF
SA197	0	1	1	0	0	0	1	0	1	128/64	18A0000–18BFFFF	0C50000–0C5FFFF
SA198	0	1	1	0	0	0	1	1	0	128/64	18C0000–18DFFFF	0C60000–0C6FFFF
SA199	0	1	1	0	0	0	1	1	1	128/64	18E0000–18FFFFF	0C70000–0C7FFFF
SA200	0	1	1	0	0	1	0	0	0	128/64	1900000–191FFFF	0C80000–0C8FFFF
SA201	0	1	1	0	0	1	0	0	1	128/64	1920000–193FFFF	0C90000–0C9FFFF
SA202	0	1	1	0	0	1	0	1	0	128/64	1940000–195FFFF	0CA0000–0CAFFFF
SA203	0	1	1	0	0	1	0	1	1	128/64	1960000–197FFFF	0CB0000–0CBFFFF
SA204	0	1	1	0	0	1	1	0	0	128/64	1980000–199FFFF	0CC0000–0CCFFFF
SA205	0	1	1	0	0	1	1	0	1	128/64	19A0000–19BFFFF	0CD0000–0CDFFFF
SA206	0	1	1	0	0	1	1	1	0	128/64	19C0000–19DFFFF	0CE0000–0CEFFFF
SA207	0	1	1	0	0	1	1	1	1	128/64	19E0000–19FFFFF	0CF0000–0CFFFFF
SA208	0	1	1	0	1	0	0	0	0	128/64	1A00000–1A1FFFF	0D00000–0D0FFFF
SA209	0	1	1	0	1	0	0	0	1	128/64	1A20000–1A3FFFF	0D10000–0D1FFFF
SA210	0	1	1	0	1	0	0	1	0	128/64	1A40000–1A5FFFF	0D20000–0D2FFFF
SA211	0	1	1	0	1	0	0	1	1	128/64	1A60000–1A7FFFF	0D30000–0D3FFFF
SA212	0	1	1	0	1	0	1	0	0	128/64	1A80000–1A9FFFF	0D40000–0D4FFFF
SA213	0	1	1	0	1	0	1	0	1	128/64	1AA0000–1ABFFFF	0D50000–0D5FFFF
SA214	0	1	1	0	1	0	1	1	0	128/64	1AC0000–1ADFFFF	0D60000–0D6FFFF
SA215	0	1	1	0	1	0	1	1	1	128/64	1AE0000–1AFFFFF	0D70000–0D7FFFF
SA216	0	1	1	0	1	1	0	0	0	128/64	1B00000–1B1FFFF	0D80000–0D8FFFF
SA217	0	1	1	0	1	1	0	0	1	128/64	1B20000–1B3FFFF	0D90000–0D9FFFF
SA218	0	1	1	0	1	1	0	1	0	128/64	1B40000–1B5FFFF	0DA0000–0DAFFFF
SA219	0	1	1	0	1	1	0	1	1	128/64	1B60000–1B7FFFF	0DB0000–0DBFFFF
SA220	0	1	1	0	1	1	1	0	0	128/64	1B80000–1B9FFFF	0DC0000–0DCFFFF
SA221	0	1	1	0	1	1	1	0	1	128/64	1BA0000–1BBFFFF	0DD0000–0DDFFFF
SA222	0	1	1	0	1	1	1	1	0	128/64	1BC0000–1BDFFFF	0DE0000–0DEFFFF
SA223	0	1	1	0	1	1	1	1	1	128/64	1BE0000–1BFFFFF	0DF0000–0DFFFFF

Table 2. Sector Address Table–S29GL5I2N (Continued)

Sector	A24–A16									Sector Size (Kbytes/ Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA224	0	1	1	1	0	0	0	0	0	128/64	1C00000–1C1FFFF	0E00000–0E0FFFF
SA225	0	1	1	1	0	0	0	0	1	128/64	1C20000–1C3FFFF	0E10000–0E1FFFF
SA226	0	1	1	1	0	0	0	1	0	128/64	1C40000–1C5FFFF	0E20000–0E2FFFF
SA227	0	1	1	1	0	0	0	1	1	128/64	1C60000–1C7FFFF	0E30000–0E3FFFF
SA228	0	1	1	1	0	0	1	0	0	128/64	1C80000–1C9FFFF	0E40000–0E4FFFF
SA229	0	1	1	1	0	0	1	0	1	128/64	1CA0000–1CBFFFF	0E50000–0E5FFFF
SA230	0	1	1	1	0	0	1	1	0	128/64	1CC0000–1CDFFFF	0E60000–0E6FFFF
SA231	0	1	1	1	0	0	1	1	1	128/64	1CE0000–1CFFFFF	0E70000–0E7FFFF
SA232	0	1	1	1	0	1	0	0	0	128/64	1D00000–1D1FFFF	0E80000–0E8FFFF
SA233	0	1	1	1	0	1	0	0	1	128/64	1D20000–1D3FFFF	0E90000–0E9FFFF
SA234	0	1	1	1	0	1	0	1	0	128/64	1D40000–1D5FFFF	0EA0000–0EAFFFF
SA235	0	1	1	1	0	1	0	1	1	128/64	1D60000–1D7FFFF	0EB0000–0EBFFFF
SA236	0	1	1	1	0	1	1	0	0	128/64	1D80000–1D9FFFF	0EC0000–0ECFFFF
SA237	0	1	1	1	0	1	1	0	1	128/64	1DA0000–1DBFFFF	0ED0000–0EDFFFF
SA238	0	1	1	1	0	1	1	1	0	128/64	1DC0000–1DDFFFF	0EE0000–0EEFFFF
SA239	0	1	1	1	0	1	1	1	1	128/64	1DE0000–1DFFFFF	0EF0000–0EFFFFF
SA240	0	1	1	1	1	0	0	0	0	128/64	1E00000–1E1FFFF	0F00000–0F0FFFF
SA241	0	1	1	1	1	0	0	0	1	128/64	1E20000–1E3FFFF	0F10000–0F1FFFF
SA242	0	1	1	1	1	0	0	1	0	128/64	1E40000–1E5FFFF	0F20000–0F2FFFF
SA243	0	1	1	1	1	0	0	1	1	128/64	1E60000–1E7FFFF	0F30000–0F3FFFF
SA244	0	1	1	1	1	0	1	0	0	128/64	1E80000–1E9FFFF	0F40000–0F4FFFF
SA245	0	1	1	1	1	0	1	0	1	128/64	1EA0000–1EBFFFF	0F50000–0F5FFFF
SA246	0	1	1	1	1	0	1	1	0	128/64	1EC0000–1EDFFFF	0F60000–0F6FFFF
SA247	0	1	1	1	1	0	1	1	1	128/64	1EE0000–1EFFFFF	0F70000–0F7FFFF
SA248	0	1	1	1	1	1	0	0	0	128/64	1F00000–1F1FFFF	0F80000–0F8FFFF
SA249	0	1	1	1	1	1	0	0	1	128/64	1F20000–1F3FFFF	0F90000–0F9FFFF
SA250	0	1	1	1	1	1	0	1	0	128/64	1F40000–1F5FFFF	0FA0000–0FAFFFF
SA251	0	1	1	1	1	1	0	1	1	128/64	1F60000–1F7FFFF	0FB0000–0FBFFFF
SA252	0	1	1	1	1	1	1	0	0	128/64	1F80000–1F9FFFF	0FC0000–0FCFFFF
SA253	0	1	1	1	1	1	1	0	1	128/64	1FA0000–1FBFFFF	0FD0000–0FDFFFF
SA254	0	1	1	1	1	1	1	1	0	128/64	1FC0000–1FDFFFF	0FE0000–0FEFFFF
SA255	0	1	1	1	1	1	1	1	1	128/64	1FE0000–1FFFFFF	0FF0000–0FFFFFF
SA256	1	0	0	0	0	0	0	0	0	128/64	2000000–201FFFF	1000000–100FFFF
SA257	1	0	0	0	0	0	0	0	1	128/64	2020000–203FFFF	1010000–101FFFF
SA258	1	0	0	0	0	0	0	1	0	128/64	2040000–205FFFF	1020000–102FFFF

Table 2. Sector Address Table–S29GL5I2N (Continued)

Sector	A24–A16									Sector Size (Kbytes/ Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA259	1	0	0	0	0	0	0	1	1	128/64	2060000–207FFFF	1030000–103FFFF
SA260	1	0	0	0	0	0	1	0	0	128/64	2080000–209FFFF	1040000–104FFFF
SA261	1	0	0	0	0	0	1	0	1	128/64	20A0000–20BFFFF	1050000–105FFFF
SA262	1	0	0	0	0	0	1	1	0	128/64	20C0000–20DFFFF	1060000–106FFFF
SA263	1	0	0	0	0	0	1	1	1	128/64	20E0000–20FFFFF	1070000–107FFFF
SA264	1	0	0	0	0	1	0	0	0	128/64	2100000–211FFFF	1080000–108FFFF
SA265	1	0	0	0	0	1	0	0	1	128/64	2120000–213FFFF	1090000–109FFFF
SA266	1	0	0	0	0	1	0	1	0	128/64	2140000–215FFFF	10A0000–10AFFFF
SA267	1	0	0	0	0	1	0	1	1	128/64	2160000–217FFFF	10B0000–10BFFFF
SA268	1	0	0	0	0	1	1	0	0	128/64	2180000–219FFFF	10C0000–10CFFFF
SA269	1	0	0	0	0	1	1	0	1	128/64	21A0000–21BFFFF	10D0000–10DFFFF
SA270	1	0	0	0	0	1	1	1	0	128/64	21C0000–21DFFFF	10E0000–10EFFFF
SA271	1	0	0	0	0	1	1	1	1	128/64	21E0000–21FFFFF	10F0000–10FFFFF
SA272	1	0	0	0	1	0	0	0	0	128/64	2200000–221FFFF	1100000–110FFFF
SA273	1	0	0	0	1	0	0	0	1	128/64	2220000–223FFFF	1110000–111FFFF
SA274	1	0	0	0	1	0	0	1	0	128/64	2240000–225FFFF	1120000–112FFFF
SA275	1	0	0	0	1	0	0	1	1	128/64	2260000–227FFFF	1130000–113FFFF
SA276	1	0	0	0	1	0	1	0	0	128/64	2280000–229FFFF	1140000–114FFFF
SA277	1	0	0	0	1	0	1	0	1	128/64	22A0000–22BFFFF	1150000–115FFFF
SA278	1	0	0	0	1	0	1	1	0	128/64	22C0000–22DFFFF	1160000–116FFFF
SA279	1	0	0	0	1	0	1	1	1	128/64	22E0000–22FFFFF	1170000–117FFFF
SA280	1	0	0	0	1	1	0	0	0	128/64	2300000–231FFFF	1180000–118FFFF
SA281	1	0	0	0	1	1	0	0	1	128/64	2320000–233FFFF	1190000–119FFFF
SA282	1	0	0	0	1	1	0	1	0	128/64	2340000–235FFFF	11A0000–11AFFFF
SA283	1	0	0	0	1	1	0	1	1	128/64	2360000–237FFFF	11B0000–11BFFFF
SA284	1	0	0	0	1	1	1	0	0	128/64	2380000–239FFFF	11C0000–11CFFFF
SA285	1	0	0	0	1	1	1	0	1	128/64	23A0000–23BFFFF	11D0000–11DFFFF
SA286	1	0	0	0	1	1	1	1	0	128/64	23C0000–23DFFFF	11E0000–11EFFFF
SA287	1	0	0	0	1	1	1	1	1	128/64	23E0000–23FFFFF	11F0000–11FFFFF
SA288	1	0	0	1	0	0	0	0	0	128/64	2400000–241FFFF	1200000–120FFFF
SA289	1	0	0	1	0	0	0	0	1	128/64	2420000–243FFFF	1210000–121FFFF
SA290	1	0	0	1	0	0	0	1	0	128/64	2440000–245FFFF	1220000–122FFFF
SA291	1	0	0	1	0	0	0	1	1	128/64	2460000–247FFFF	1230000–123FFFF
SA292	1	0	0	1	0	0	1	0	0	128/64	2480000–249FFFF	1240000–124FFFF
SA293	1	0	0	1	0	0	1	0	1	128/64	24A0000–24BFFFF	1250000–125FFFF

Table 2. Sector Address Table–S29GL5I2N (Continued)

Sector	A24–A16									Sector Size (Kbytes/ Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA294	1	0	0	1	0	0	1	1	0	128/64	24C0000–24DFFFF	1260000–126FFFF
SA295	1	0	0	1	0	0	1	1	1	128/64	24E0000–24FFFFF	1270000–127FFFF
SA296	1	0	0	1	0	1	0	0	0	128/64	2500000–251FFFF	1280000–128FFFF
SA297	1	0	0	1	0	1	0	0	1	128/64	2520000–253FFFF	1290000–129FFFF
SA298	1	0	0	1	0	1	0	1	0	128/64	2540000–255FFFF	12A0000–12AFFFF
SA299	1	0	0	1	0	1	0	1	1	128/64	2560000–257FFFF	12B0000–12BFFFF
SA300	1	0	0	1	0	1	1	0	0	128/64	2580000–259FFFF	12C0000–12CFFFF
SA301	1	0	0	1	0	1	1	0	1	128/64	25A0000–25BFFFF	12D0000–12DFFFF
SA302	1	0	0	1	0	1	1	1	0	128/64	25C0000–25DFFFF	12E0000–12EFFFF
SA303	1	0	0	1	0	1	1	1	1	128/64	25E0000–25FFFFF	12F0000–12FFFFF
SA304	1	0	0	1	1	0	0	0	0	128/64	2600000–261FFFF	1300000–130FFFF
SA305	1	0	0	1	1	0	0	0	1	128/64	2620000–263FFFF	1310000–131FFFF
SA306	1	0	0	1	1	0	0	1	0	128/64	2640000–265FFFF	1320000–132FFFF
SA307	1	0	0	1	1	0	0	1	1	128/64	2660000–267FFFF	1330000–133FFFF
SA308	1	0	0	1	1	0	1	0	0	128/64	2680000–269FFFF	1340000–134FFFF
SA309	1	0	0	1	1	0	1	0	1	128/64	26A0000–26BFFFF	1350000–135FFFF
SA310	1	0	0	1	1	0	1	1	0	128/64	26C0000–26DFFFF	1360000–136FFFF
SA311	1	0	0	1	1	0	1	1	1	128/64	26E0000–26FFFFF	1370000–137FFFF
SA312	1	0	0	1	1	1	0	0	0	128/64	2700000–271FFFF	1380000–138FFFF
SA313	1	0	0	1	1	1	0	0	1	128/64	2720000–273FFFF	1390000–139FFFF
SA314	1	0	0	1	1	1	0	1	0	128/64	2740000–275FFFF	13A0000–13AFFFF
SA315	1	0	0	1	1	1	0	1	1	128/64	2760000–277FFFF	13B0000–13BFFFF
SA316	1	0	0	1	1	1	1	0	0	128/64	2780000–279FFFF	13C0000–13CFFFF
SA317	1	0	0	1	1	1	1	0	1	128/64	27A0000–27BFFFF	13D0000–13DFFFF
SA318	1	0	0	1	1	1	1	1	0	128/64	27C0000–27DFFFF	13E0000–13EFFFF
SA319	1	0	0	1	1	1	1	1	1	128/64	27E0000–27FFFFF	13F0000–13FFFFF
SA320	1	0	1	0	0	0	0	0	0	128/64	2800000–281FFFF	1400000–140FFFF
SA321	1	0	1	0	0	0	0	0	1	128/64	2820000–283FFFF	1410000–141FFFF
SA322	1	0	1	0	0	0	0	1	0	128/64	2840000–285FFFF	1420000–142FFFF
SA323	1	0	1	0	0	0	0	1	1	128/64	2860000–287FFFF	1430000–143FFFF
SA324	1	0	1	0	0	0	1	0	0	128/64	2880000–289FFFF	1440000–144FFFF
SA325	1	0	1	0	0	0	1	0	1	128/64	28A0000–28BFFFF	1450000–145FFFF
SA326	1	0	1	0	0	0	1	1	0	128/64	28C0000–28DFFFF	1460000–146FFFF
SA327	1	0	1	0	0	0	1	1	1	128/64	28E0000–28FFFFF	1470000–147FFFF
SA328	1	0	1	0	0	1	0	0	0	128/64	2900000–291FFFF	1480000–148FFFF

Table 2. Sector Address Table–S29GL5I2N (Continued)

Sector	A24–A16									Sector Size (Kbytes/ Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA329	1	0	1	0	0	1	0	0	1	128/64	2920000–293FFFF	1490000–149FFFF
SA330	1	0	1	0	0	1	0	1	0	128/64	2940000–295FFFF	14A0000–14AFFFF
SA331	1	0	1	0	0	1	0	1	1	128/64	2960000–297FFFF	14B0000–14BFFFF
SA332	1	0	1	0	0	1	1	0	0	128/64	2980000–299FFFF	14C0000–14CFFFF
SA333	1	0	1	0	0	1	1	0	1	128/64	29A0000–29BFFFF	14D0000–14DFFFF
SA334	1	0	1	0	0	1	1	1	0	128/64	29C0000–29DFFFF	14E0000–14EFFFF
SA335	1	0	1	0	0	1	1	1	1	128/64	29E0000–29FFFFF	14F0000–14FFFFF
SA336	1	0	1	0	1	0	0	0	0	128/64	2A00000–2A1FFFF	1500000–150FFFF
SA337	1	0	1	0	1	0	0	0	1	128/64	2A20000–2A3FFFF	1510000–151FFFF
SA338	1	0	1	0	1	0	0	1	0	128/64	2A40000–2A5FFFF	1520000–152FFFF
SA339	1	0	1	0	1	0	0	1	1	128/64	2A60000–2A7FFFF	1530000–153FFFF
SA340	1	0	1	0	1	0	1	0	0	128/64	2A80000–2A9FFFF	1540000–154FFFF
SA341	1	0	1	0	1	0	1	0	1	128/64	2AA0000–2ABFFFF	1550000–155FFFF
SA342	1	0	1	0	1	0	1	1	0	128/64	2AC0000–2ADFFFF	1560000–156FFFF
SA343	1	0	1	0	1	0	1	1	1	128/64	2AE00000–2EFFFFF	1570000–157FFFF
SA344	1	0	1	0	1	1	0	0	0	128/64	2B00000–2B1FFFF	1580000–158FFFF
SA345	1	0	1	0	1	1	0	0	1	128/64	2B20000–2B3FFFF	1590000–159FFFF
SA346	1	0	1	0	1	1	0	1	0	128/64	2B40000–2B5FFFF	15A0000–15AFFFF
SA347	1	0	1	0	1	1	0	1	1	128/64	2B60000–2B7FFFF	15B0000–15BFFFF
SA348	1	0	1	0	1	1	1	0	0	128/64	2B80000–2B9FFFF	15C0000–15CFFFF
SA349	1	0	1	0	1	1	1	0	1	128/64	2BA0000–2BBFFFF	15D0000–15DFFFF
SA350	1	0	1	0	1	1	1	1	0	128/64	2BC0000–2DFFFFF	15E0000–15EFFFF
SA351	1	0	1	0	1	1	1	1	1	128/64	2BE0000–2BFFFFF	15F0000–15FFFFF
SA352	1	0	1	1	0	0	0	0	0	128/64	2C00000–2C1FFFF	1600000–160FFFF
SA353	1	0	1	1	0	0	0	0	1	128/64	2C20000–2C3FFFF	1610000–161FFFF
SA354	1	0	1	1	0	0	0	1	0	128/64	2C40000–2C5FFFF	1620000–162FFFF
SA355	1	0	1	1	0	0	0	1	1	128/64	2C60000–2C7FFFF	1630000–163FFFF
SA356	1	0	1	1	0	0	1	0	0	128/64	2C80000–2C9FFFF	1640000–164FFFF
SA357	1	0	1	1	0	0	1	0	1	128/64	2CA0000–2CBFFFF	1650000–165FFFF
SA358	1	0	1	1	0	0	1	1	0	128/64	2CC0000–2CDFFFF	1660000–166FFFF
SA359	1	0	1	1	0	0	1	1	1	128/64	2CE0000–2CFFFFF	1670000–167FFFF
SA360	1	0	1	1	0	1	0	0	0	128/64	2D00000–2D1FFFF	1680000–168FFFF
SA361	1	0	1	1	0	1	0	0	1	128/64	2D20000–2D3FFFF	1690000–169FFFF
SA362	1	0	1	1	0	1	0	1	0	128/64	2D40000–2D5FFFF	16A0000–16AFFFF
SA363	1	0	1	1	0	1	0	1	1	128/64	2D60000–2D7FFFF	16B0000–16BFFFF

Table 2. Sector Address Table–S29GL5I2N (Continued)

Sector	A24–A16									Sector Size (Kbytes/ Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA364	1	0	1	1	0	1	1	0	0	128/64	2D80000–2D9FFFF	16C0000–16CFFFF
SA365	1	0	1	1	0	1	1	0	1	128/64	2DA0000–2DBFFFF	16D0000–16DFFFF
SA366	1	0	1	1	0	1	1	1	0	128/64	2DC0000–2DDFFFF	16E0000–16EFFFF
SA367	1	0	1	1	0	1	1	1	1	128/64	2DE0000–2DFFFFF	16F0000–16FFFFF
SA368	1	0	1	1	1	0	0	0	0	128/64	2E00000–2E1FFFF	1700000–170FFFF
SA369	1	0	1	1	1	0	0	0	1	128/64	2E20000–2E3FFFF	1710000–171FFFF
SA370	1	0	1	1	1	0	0	1	0	128/64	2E40000–2E5FFFF	1720000–172FFFF
SA371	1	0	1	1	1	0	0	1	1	128/64	2E60000–2E7FFFF	1730000–173FFFF
SA372	1	0	1	1	1	0	1	0	0	128/64	2E80000–2E9FFFF	1740000–174FFFF
SA373	1	0	1	1	1	0	1	0	1	128/64	2EA0000–2EBFFFF	1750000–175FFFF
SA374	1	0	1	1	1	0	1	1	0	128/64	2EC0000–2EDFFFF	1760000–176FFFF
SA375	1	0	1	1	1	0	1	1	1	128/64	2EE0000–2EFFFFF	1770000–177FFFF
SA376	1	0	1	1	1	1	0	0	0	128/64	2F00000–2F1FFFF	1780000–178FFFF
SA377	1	0	1	1	1	1	0	0	1	128/64	2F20000–2F3FFFF	1790000–179FFFF
SA378	1	0	1	1	1	1	0	1	0	128/64	2F40000–2F5FFFF	17A0000–17AFFFF
SA379	1	0	1	1	1	1	0	1	1	128/64	2F60000–2F7FFFF	17B0000–17BFFFF
SA380	1	0	1	1	1	1	1	0	0	128/64	2F80000–2F9FFFF	17C0000–17CFFFF
SA381	1	0	1	1	1	1	1	0	1	128/64	2FA0000–2FBFFFF	17D0000–17DFFFF
SA382	1	0	1	1	1	1	1	1	0	128/64	2FC0000–2FDFFFF	17E0000–17EFFFF
SA383	1	0	1	1	1	1	1	1	1	128/64	3FE0000–3FFFFFF	17F0000–17FFFFF
SA384	1	1	0	0	0	0	0	0	0	128/64	3000000–301FFFF	1800000–180FFFF
SA385	1	1	0	0	0	0	0	0	1	128/64	3020000–303FFFF	1810000–181FFFF
SA386	1	1	0	0	0	0	0	1	0	128/64	3040000–305FFFF	1820000–182FFFF
SA387	1	1	0	0	0	0	0	1	1	128/64	3060000–307FFFF	1830000–183FFFF
SA388	1	1	0	0	0	0	1	0	0	128/64	3080000–309FFFF	1840000–184FFFF
SA389	1	1	0	0	0	0	1	0	1	128/64	30A0000–30BFFFF	1850000–185FFFF
SA390	1	1	0	0	0	0	1	1	0	128/64	30C0000–30DFFFF	1860000–186FFFF
SA391	1	1	0	0	0	0	1	1	1	128/64	30E0000–30FFFFF	1870000–187FFFF
SA392	1	1	0	0	0	1	0	0	0	128/64	3100000–311FFFF	1880000–188FFFF
SA393	1	1	0	0	0	1	0	0	1	128/64	3120000–313FFFF	1890000–189FFFF
SA394	1	1	0	0	0	1	0	1	0	128/64	3140000–315FFFF	18A0000–18AFFFF
SA395	1	1	0	0	0	1	0	1	1	128/64	3160000–317FFFF	18B0000–18BFFFF
SA396	1	1	0	0	0	1	1	0	0	128/64	3180000–319FFFF	18C0000–18CFFFF
SA397	1	1	0	0	0	1	1	0	1	128/64	31A0000–31BFFFF	18D0000–18DFFFF
SA398	1	1	0	0	0	1	1	1	0	128/64	31C0000–31DFFFF	18E0000–18EFFFF

Table 2. Sector Address Table–S29GL5I2N (Continued)

Sector	A24–A16									Sector Size (Kbytes/ Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA399	1	1	0	0	0	1	1	1	1	128/64	31E0000–31FFFFF	18F0000–18FFFFF
SA400	1	1	0	0	1	0	0	0	0	128/64	3200000–321FFFF	1900000–190FFFF
SA401	1	1	0	0	1	0	0	0	1	128/64	3220000–323FFFF	1910000–191FFFF
SA402	1	1	0	0	1	0	0	1	0	128/64	3240000–325FFFF	1920000–192FFFF
SA403	1	1	0	0	1	0	0	1	1	128/64	3260000–327FFFF	1930000–193FFFF
SA404	1	1	0	0	1	0	1	0	0	128/64	3280000–329FFFF	1940000–194FFFF
SA405	1	1	0	0	1	0	1	0	1	128/64	32A0000–32BFFFF	1950000–195FFFF
SA406	1	1	0	0	1	0	1	1	0	128/64	32C0000–32DFFFF	1960000–196FFFF
SA407	1	1	0	0	1	0	1	1	1	128/64	32E0000–32FFFFF	1970000–197FFFF
SA408	1	1	0	0	1	1	0	0	0	128/64	3300000–331FFFF	1980000–198FFFF
SA409	1	1	0	0	1	1	0	0	1	128/64	3320000–333FFFF	1990000–199FFFF
SA410	1	1	0	0	1	1	0	1	0	128/64	3340000–335FFFF	19A0000–19AFFFF
SA411	1	1	0	0	1	1	0	1	1	128/64	3360000–337FFFF	19B0000–19BFFFF
SA412	1	1	0	0	1	1	1	0	0	128/64	3380000–339FFFF	19C0000–19CFFFF
SA413	1	1	0	0	1	1	1	0	1	128/64	33A0000–33BFFFF	19D0000–19DFFFF
SA414	1	1	0	0	1	1	1	1	0	128/64	33C0000–33DFFFF	19E0000–19EFFFF
SA415	1	1	0	0	1	1	1	1	1	128/64	33E0000–33FFFFF	19F0000–19FFFFF
SA416	1	1	0	1	0	0	0	0	0	128/64	3400000–341FFFF	1A00000–1A0FFFF
SA417	1	1	0	1	0	0	0	0	1	128/64	3420000–343FFFF	1A10000–1A1FFFF
SA418	1	1	0	1	0	0	0	1	0	128/64	3440000–345FFFF	1A20000–1A2FFFF
SA419	1	1	0	1	0	0	0	1	1	128/64	3460000–347FFFF	1A30000–1A3FFFF
SA420	1	1	0	1	0	0	1	0	0	128/64	3480000–349FFFF	1A40000–1A4FFFF
SA421	1	1	0	1	0	0	1	0	1	128/64	34A0000–34BFFFF	1A50000–1A5FFFF
SA422	1	1	0	1	0	0	1	1	0	128/64	34C0000–34DFFFF	1A60000–1A6FFFF
SA423	1	1	0	1	0	0	1	1	1	128/64	34E0000–34FFFFF	1A70000–1A7FFFF
SA424	1	1	0	1	0	1	0	0	0	128/64	3500000–351FFFF	1A80000–1A8FFFF
SA425	1	1	0	1	0	1	0	0	1	128/64	3520000–353FFFF	1A90000–1A9FFFF
SA426	1	1	0	1	0	1	0	1	0	128/64	3540000–355FFFF	1AA0000–1AAFFFF
SA427	1	1	0	1	0	1	0	1	1	128/64	3560000–357FFFF	1AB0000–1ABFFFF
SA428	1	1	0	1	0	1	1	0	0	128/64	3580000–359FFFF	1AC0000–1ACFFFF
SA429	1	1	0	1	0	1	1	0	1	128/64	35A0000–35BFFFF	1AD0000–1ADFFFF
SA430	1	1	0	1	0	1	1	1	0	128/64	35C0000–35DFFFF	1AE0000–1AEFFFF
SA431	1	1	0	1	0	1	1	1	1	128/64	35E0000–35FFFFF	1AF0000–1AFFFFF
SA432	1	1	0	1	1	0	0	0	0	128/64	3600000–361FFFF	1B00000–1B0FFFF
SA433	1	1	0	1	1	0	0	0	1	128/64	3620000–363FFFF	1B10000–1B1FFFF

Table 2. Sector Address Table–S29GL5I2N (Continued)

Sector	A24–A16									Sector Size (Kbytes/ Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA434	1	1	0	1	1	0	0	1	0	128/64	3640000–365FFFF	1B20000–1B2FFFF
SA435	1	1	0	1	1	0	0	1	1	128/64	3660000–367FFFF	1B30000–1B3FFFF
SA436	1	1	0	1	1	0	1	0	0	128/64	3680000–369FFFF	1B40000–1B4FFFF
SA437	1	1	0	1	1	0	1	0	1	128/64	36A0000–36BFFFF	1B50000–1B5FFFF
SA438	1	1	0	1	1	0	1	1	0	128/64	36C0000–36DFFFF	1B60000–1B6FFFF
SA439	1	1	0	1	1	0	1	1	1	128/64	36E0000–36FFFFF	1B70000–1B7FFFF
SA440	1	1	0	1	1	1	0	0	0	128/64	3700000–371FFFF	1B80000–1B8FFFF
SA441	1	1	0	1	1	1	0	0	1	128/64	3720000–373FFFF	1B90000–1B9FFFF
SA442	1	1	0	1	1	1	0	1	0	128/64	3740000–375FFFF	1BA0000–1BAFFFF
SA443	1	1	0	1	1	1	0	1	1	128/64	3760000–377FFFF	1BB0000–1BBFFFF
SA444	1	1	0	1	1	1	1	0	0	128/64	3780000–379FFFF	1BC0000–1BCFFFF
SA445	1	1	0	1	1	1	1	0	1	128/64	37A0000–37BFFFF	1BD0000–1BDFFFF
SA446	1	1	0	1	1	1	1	1	0	128/64	37C0000–37DFFFF	1BE0000–1BEFFFF
SA447	1	1	0	1	1	1	1	1	1	128/64	37E0000–37FFFFF	1BF0000–1BFFFFF
SA448	1	1	1	0	0	0	0	0	0	128/64	3800000–381FFFF	1C00000–1C0FFFF
SA449	1	1	1	0	0	0	0	0	1	128/64	3820000–383FFFF	1C10000–1C1FFFF
SA450	1	1	1	0	0	0	0	1	0	128/64	3840000–385FFFF	1C20000–1C2FFFF
SA451	1	1	1	0	0	0	0	1	1	128/64	3860000–387FFFF	1C30000–1C3FFFF
SA452	1	1	1	0	0	0	1	0	0	128/64	3880000–389FFFF	1C40000–1C4FFFF
SA453	1	1	1	0	0	0	1	0	1	128/64	38A0000–38BFFFF	1C50000–1C5FFFF
SA454	1	1	1	0	0	0	1	1	0	128/64	38C0000–38DFFFF	1C60000–1C6FFFF
SA455	1	1	1	0	0	0	1	1	1	128/64	38E0000–38FFFFF	1C70000–1C7FFFF
SA456	1	1	1	0	0	1	0	0	0	128/64	3900000–391FFFF	1C80000–1C8FFFF
SA457	1	1	1	0	0	1	0	0	1	128/64	3920000–393FFFF	1C90000–1C9FFFF
SA458	1	1	1	0	0	1	0	1	0	128/64	3940000–395FFFF	1CA0000–1CAFFFF
SA459	1	1	1	0	0	1	0	1	1	128/64	3960000–397FFFF	1CB0000–1CBFFFF
SA460	1	1	1	0	0	1	1	0	0	128/64	3980000–399FFFF	1CC0000–1CCFFFF
SA461	1	1	1	0	0	1	1	0	1	128/64	39A0000–39BFFFF	1CD0000–1CDFFFF
SA462	1	1	1	0	0	1	1	1	0	128/64	39C0000–39DFFFF	1CE0000–1CEFFFF
SA463	1	1	1	0	0	1	1	1	1	128/64	39E0000–39FFFFF	1CF0000–1CFFFFF
SA464	1	1	1	0	1	0	0	0	0	128/64	3A00000–3A1FFFF	1D00000–1D0FFFF
SA465	1	1	1	0	1	0	0	0	1	128/64	3A20000–3A3FFFF	1D10000–1D1FFFF
SA466	1	1	1	0	1	0	0	1	0	128/64	3A40000–3A5FFFF	1D20000–1D2FFFF
SA467	1	1	1	0	1	0	0	1	1	128/64	3A60000–3A7FFFF	1D30000–1D3FFFF
SA468	1	1	1	0	1	0	1	0	0	128/64	3A80000–3A9FFFF	1D40000–1D4FFFF

Table 2. Sector Address Table–S29GL5I2N (Continued)

Sector	A24–A16									Sector Size (Kbytes/ Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA469	1	1	1	0	1	0	1	0	1	128/64	3AA0000–3ABFFFF	1D50000–1D5FFFF
SA470	1	1	1	0	1	0	1	1	0	128/64	3AC0000–3ADFFFF	1D60000–1D6FFFF
SA471	1	1	1	0	1	0	1	1	1	128/64	3AE0000–3AFFFFF	1D70000–1D7FFFF
SA472	1	1	1	0	1	1	0	0	0	128/64	3B00000–3B1FFFF	1D80000–1D8FFFF
SA473	1	1	1	0	1	1	0	0	1	128/64	3B20000–3B3FFFF	1D90000–1D9FFFF
SA474	1	1	1	0	1	1	0	1	0	128/64	3B40000–3B5FFFF	1DA0000–1DAFFFF
SA475	1	1	1	0	1	1	0	1	1	128/64	3B60000–3B7FFFF	1DB0000–1DBFFFF
SA476	1	1	1	0	1	1	1	0	0	128/64	3B80000–3B9FFFF	1DC0000–1DCFFFF
SA477	1	1	1	0	1	1	1	0	1	128/64	3BA0000–3BBFFFF	1DD0000–1DDFFFF
SA478	1	1	1	0	1	1	1	1	0	128/64	3BC0000–3BDFFFF	1DE0000–1DEFFFF
SA479	1	1	1	0	1	1	1	1	1	128/64	3BE0000–3BFFFFF	1DF0000–1DFFFFF
SA480	1	1	1	1	0	0	0	0	0	128/64	3C00000–3C1FFFF	1E00000–1E0FFFF
SA481	1	1	1	1	0	0	0	0	1	128/64	3C20000–3C3FFFF	1E10000–1E1FFFF
SA482	1	1	1	1	0	0	0	1	0	128/64	3C40000–3C5FFFF	1E20000–1E2FFFF
SA483	1	1	1	1	0	0	0	1	1	128/64	3C60000–3C7FFFF	1E30000–1E3FFFF
SA484	1	1	1	1	0	0	1	0	0	128/64	3C80000–3C9FFFF	1E40000–1E4FFFF
SA485	1	1	1	1	0	0	1	0	1	128/64	3CA0000–3CBFFFF	1E50000–1E5FFFF
SA486	1	1	1	1	0	0	1	1	0	128/64	3CC0000–3CDFFFF	1E60000–1E6FFFF
SA487	1	1	1	1	0	0	1	1	1	128/64	3CE0000–3CFFFFF	1E70000–1E7FFFF
SA488	1	1	1	1	0	1	0	0	0	128/64	3D00000–3D1FFFFF	1E80000–1E8FFFF
SA489	1	1	1	1	0	1	0	0	1	128/64	3D20000–3D3FFFF	1E90000–1E9FFFF
SA490	1	1	1	1	0	1	0	1	0	128/64	3D40000–3D5FFFF	1EA0000–1EAFFFF
SA491	1	1	1	1	0	1	0	1	1	128/64	3D60000–3D7FFFF	1EB0000–1EBFFFF
SA492	1	1	1	1	0	1	1	0	0	128/64	3D80000–3D9FFFF	1EC0000–1ECFFFF
SA493	1	1	1	1	0	1	1	0	1	128/64	3DA0000–3DBFFFF	1ED0000–1EDFFFF
SA494	1	1	1	1	0	1	1	1	0	128/64	3DC0000–3DDFFFF	1EE0000–1EEFFFF
SA495	1	1	1	1	0	1	1	1	1	128/64	3DE0000–3DFFFFF	1EF0000–1EFFFFF
SA496	1	1	1	1	1	0	0	0	0	128/64	3E00000–3E1FFFF	1F00000–1F0FFFF
SA497	1	1	1	1	1	0	0	0	1	128/64	3E20000–3E3FFFF	1F10000–1F1FFFF
SA498	1	1	1	1	1	0	0	1	0	128/64	3E40000–3E5FFFF	1F20000–1F2FFFF
SA499	1	1	1	1	1	0	0	1	1	128/64	3E60000–3E7FFFF	1F30000–1F3FFFF
SA500	1	1	1	1	1	0	1	0	0	128/64	3E80000–3E9FFFF	1F40000–1F4FFFF
SA501	1	1	1	1	1	0	1	0	1	128/64	3EA0000–3EBFFFF	1F50000–1F5FFFF
SA502	1	1	1	1	1	0	1	1	0	128/64	3EC00000–3EDFFFF	1F60000–1F6FFFF
SA503	1	1	1	1	1	0	1	1	1	128/64	3EE0000–3EFFFFF	1F70000–1F7FFFF

Table 2. Sector Address Table–S29GL5I2N (Continued)

Sector	A24–A16									Sector Size (Kbytes/ Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA504	1	1	1	1	1	1	0	0	0	128/64	3F00000–3F1FFFF	1F80000–1F8FFFF
SA505	1	1	1	1	1	1	0	0	1	128/64	3F20000–3F3FFFF	1F90000–1F9FFFF
SA506	1	1	1	1	1	1	0	1	0	128/64	3F40000–3F5FFFF	1FA0000–1FAFFFF
SA507	1	1	1	1	1	1	0	1	1	128/64	3F60000–3F7FFFF	1FB0000–1FBFFFF
SA508	1	1	1	1	1	1	1	0	0	128/64	3F80000–3F9FFFF	1FC0000–1FCFFFF
SA509	1	1	1	1	1	1	1	0	1	128/64	3FA0000–3FBFFFF	1FD0000–1FDFFFF
SA510	1	1	1	1	1	1	1	1	0	128/64	3FC0000–3FDFFFF	1FE0000–1FEFFFF
SA511	1	1	1	1	1	1	1	1	1	128/64	3FE0000–3FFFFFF	1FF0000–1FFFFFF

Table 3. Sector Address Table–S29GL256N

Sector	A23–A16								Sector Size (Kbytes/ Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA0	0	0	0	0	0	0	0	0	128/64	0000000–001FFFF	0000000–000FFFF
SA1	0	0	0	0	0	0	0	1	128/64	0020000–003FFFF	0010000–001FFFF
SA2	0	0	0	0	0	0	1	0	128/64	0040000–005FFFF	0020000–002FFFF
SA3	0	0	0	0	0	0	1	1	128/64	0060000–007FFFF	0030000–003FFFF
SA4	0	0	0	0	0	1	0	0	128/64	0080000–009FFFF	0040000–004FFFF
SA5	0	0	0	0	0	1	0	1	128/64	00A0000–00BFFFF	0050000–005FFFF
SA6	0	0	0	0	0	1	1	0	128/64	00C0000–00DFFFF	0060000–006FFFF
SA7	0	0	0	0	0	1	1	1	128/64	00E0000–00FFFFF	0070000–007FFFF
SA8	0	0	0	0	1	0	0	0	128/64	0100000–011FFFF	0080000–008FFFF
SA9	0	0	0	0	1	0	0	1	128/64	0120000–013FFFF	0090000–009FFFF
SA10	0	0	0	0	1	0	1	0	128/64	0140000–015FFFF	00A0000–00AFFFF
SA11	0	0	0	0	1	0	1	1	128/64	0160000–017FFFF	00B0000–00BFFFF
SA12	0	0	0	0	1	1	0	0	128/64	0180000–019FFFF	00C0000–00CFFFF
SA13	0	0	0	0	1	1	0	1	128/64	01A0000–01BFFFF	00D0000–00DFFFF
SA14	0	0	0	0	1	1	1	0	128/64	01C0000–01DFFFF	00E0000–00EFFFF
SA15	0	0	0	0	1	1	1	1	128/64	01E0000–01FFFFF	00F0000–00FFFFF
SA16	0	0	0	1	0	0	0	0	128/64	0200000–021FFFF	0100000–010FFFF
SA17	0	0	0	1	0	0	0	1	128/64	0220000–023FFFF	0110000–011FFFF
SA18	0	0	0	1	0	0	1	0	128/64	0240000–025FFFF	0120000–012FFFF
SA19	0	0	0	1	0	0	1	1	128/64	0260000–027FFFF	0130000–013FFFF
SA20	0	0	0	1	0	1	0	0	128/64	0280000–029FFFF	0140000–014FFFF
SA21	0	0	0	1	0	1	0	1	128/64	02A0000–02BFFFF	0150000–015FFFF

Table 3. Sector Address Table–S29GL256N (Continued)

Sector	A23–A16								Sector Size (Kbytes/ Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA22	0	0	0	1	0	1	1	0	128/64	02C0000–02DFFFF	0160000–016FFFF
SA23	0	0	0	1	0	1	1	1	128/64	02E0000–02FFFFF	0170000–017FFFF
SA24	0	0	0	1	1	0	0	0	128/64	0300000–031FFFF	0180000–018FFFF
SA25	0	0	0	1	1	0	0	1	128/64	0320000–033FFFF	0190000–019FFFF
SA26	0	0	0	1	1	0	1	0	128/64	0340000–035FFFF	01A0000–01AFFFF
SA27	0	0	0	1	1	0	1	1	128/64	0360000–037FFFF	01B0000–01BFFFF
SA28	0	0	0	1	1	1	0	0	128/64	0380000–039FFFF	01C0000–01CFFFF
SA29	0	0	0	1	1	1	0	1	128/64	03A0000–03BFFFF	01D0000–01DFFFF
SA30	0	0	0	1	1	1	1	0	128/64	03C0000–03DFFFF	01E0000–01EFFFF
SA31	0	0	0	1	1	1	1	1	128/64	03E0000–03FFFFF	01F0000–01FFFFF
SA32	0	0	1	0	0	0	0	0	128/64	0400000–041FFFF	0200000–020FFFF
SA33	0	0	1	0	0	0	0	1	128/64	0420000–043FFFF	0210000–021FFFF
SA34	0	0	1	0	0	0	1	0	128/64	0440000–045FFFF	0220000–022FFFF
SA35	0	0	1	0	0	0	1	1	128/64	0460000–047FFFF	0230000–023FFFF
SA36	0	0	1	0	0	1	0	0	128/64	0480000–049FFFF	0240000–024FFFF
SA37	0	0	1	0	0	1	0	1	128/64	04A0000–04BFFFF	0250000–025FFFF
SA38	0	0	1	0	0	1	1	0	128/64	04C0000–04DFFFF	0260000–026FFFF
SA39	0	0	1	0	0	1	1	1	128/64	04E0000–04FFFFF	0270000–027FFFF
SA40	0	0	1	0	1	0	0	0	128/64	0500000–051FFFF	0280000–028FFFF
SA41	0	0	1	0	1	0	0	1	128/64	0520000–053FFFF	0290000–029FFFF
SA42	0	0	1	0	1	0	1	0	128/64	0540000–055FFFF	02A0000–02AFFFF
SA43	0	0	1	0	1	0	1	1	128/64	0560000–057FFFF	02B0000–02BFFFF
SA44	0	0	1	0	1	1	0	0	128/64	0580000–059FFFF	02C0000–02CFFFF
SA45	0	0	1	0	1	1	0	1	128/64	05A0000–05BFFFF	02D0000–02DFFFF
SA46	0	0	1	0	1	1	1	0	128/64	05C0000–05DFFFF	02E0000–02EFFFF
SA47	0	0	1	0	1	1	1	1	128/64	05E0000–05FFFFF	02F0000–02FFFFF
SA48	0	0	1	1	0	0	0	0	128/64	0600000–061FFFF	0300000–030FFFF
SA49	0	0	1	1	0	0	0	1	128/64	0620000–063FFFF	0310000–031FFFF
SA50	0	0	1	1	0	0	1	0	128/64	0640000–065FFFF	0320000–032FFFF
SA51	0	0	1	1	0	0	1	1	128/64	0660000–067FFFF	0330000–033FFFF
SA52	0	0	1	1	0	1	0	0	128/64	0680000–069FFFF	0340000–034FFFF
SA53	0	0	1	1	0	1	0	1	128/64	06A0000–06BFFFF	0350000–035FFFF
SA54	0	0	1	1	0	1	1	0	128/64	06C0000–06DFFFF	0360000–036FFFF
SA55	0	0	1	1	0	1	1	1	128/64	06E0000–06FFFFF	0370000–037FFFF
SA56	0	0	1	1	1	0	0	0	128/64	0700000–071FFFF	0380000–038FFFF

Table 3. Sector Address Table–S29GL256N (Continued)

Sector	A23–A16								Sector Size (Kbytes/ Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA57	0	0	1	1	1	0	0	1	128/64	0720000–073FFFF	0390000–039FFFF
SA58	0	0	1	1	1	0	1	0	128/64	0740000–075FFFF	03A0000–03AFFFF
SA59	0	0	1	1	1	0	1	1	128/64	0760000–077FFFF	03B0000–03BFFFF
SA60	0	0	1	1	1	1	0	0	128/64	0780000–079FFFF	03C0000–03CFFFF
SA61	0	0	1	1	1	1	0	1	128/64	07A0000–7BFFFF	03D0000–03DFFFF
SA62	0	0	1	1	1	1	1	0	128/64	07C0000–07DFFFF	03E0000–03EFFFF
SA63	0	0	1	1	1	1	1	1	128/64	07E0000–07FFFFF0	03F0000–03FFFFF
SA64	0	1	0	0	0	0	0	0	128/64	0800000–081FFFF	0400000–040FFFF
SA65	0	1	0	0	0	0	0	1	128/64	0820000–083FFFF	0410000–041FFFF
SA66	0	1	0	0	0	0	1	0	128/64	0840000–085FFFF	0420000–042FFFF
SA67	0	1	0	0	0	0	1	1	128/64	0860000–087FFFF	0430000–043FFFF
SA68	0	1	0	0	0	1	0	0	128/64	0880000–089FFFF	0440000–044FFFF
SA69	0	1	0	0	0	1	0	1	128/64	08A0000–08BFFFF	0450000–045FFFF
SA70	0	1	0	0	0	1	1	0	128/64	08C0000–08DFFFF	0460000–046FFFF
SA71	0	1	0	0	0	1	1	1	128/64	08E0000–08FFFFF	0470000–047FFFF
SA72	0	1	0	0	1	0	0	0	128/64	0900000–091FFFF	0480000–048FFFF
SA73	0	1	0	0	1	0	0	1	128/64	0920000–093FFFF	0490000–049FFFF
SA74	0	1	0	0	1	0	1	0	128/64	0940000–095FFFF	04A0000–04AFFFF
SA75	0	1	0	0	1	0	1	1	128/64	0960000–097FFFF	04B0000–04BFFFF
SA76	0	1	0	0	1	1	0	0	128/64	0980000–099FFFF	04C0000–04CFFFF
SA77	0	1	0	0	1	1	0	1	128/64	09A0000–09BFFFF	04D0000–04DFFFF
SA78	0	1	0	0	1	1	1	0	128/64	09C0000–09DFFFF	04E0000–04EFFFF
SA79	0	1	0	0	1	1	1	1	128/64	09E0000–09FFFFF	04F0000–04FFFFF
SA80	0	1	0	1	0	0	0	0	128/64	0A00000–0A1FFFF	0500000–050FFFF
SA81	0	1	0	1	0	0	0	1	128/64	0A20000–0A3FFFF	0510000–051FFFF
SA82	0	1	0	1	0	0	1	0	128/64	0A40000–045FFFF	0520000–052FFFF
SA83	0	1	0	1	0	0	1	1	128/64	0A60000–0A7FFFF	0530000–053FFFF
SA84	0	1	0	1	0	1	0	0	128/64	0A80000–0A9FFFF	0540000–054FFFF
SA85	0	1	0	1	0	1	0	1	128/64	0AA0000–0ABFFFF	0550000–055FFFF
SA86	0	1	0	1	0	1	1	0	128/64	0AC0000–0ADFFFF	0560000–056FFFF
SA87	0	1	0	1	0	1	1	1	128/64	0AE0000–AEFFFFF	0570000–057FFFF
SA88	0	1	0	1	1	0	0	0	128/64	0B00000–0B1FFFF	0580000–058FFFF
SA89	0	1	0	1	1	0	0	1	128/64	0B20000–0B3FFFF	0590000–059FFFF
SA90	0	1	0	1	1	0	1	0	128/64	0B40000–0B5FFFF	05A0000–05AFFFF
SA91	0	1	0	1	1	0	1	1	128/64	0B60000–0B7FFFF	05B0000–05BFFFF

Table 3. Sector Address Table–S29GL256N (Continued)

Sector	A23–A16								Sector Size (Kbytes/ Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA92	0	1	0	1	1	1	0	0	128/64	0B80000–0B9FFFF	05C0000–05CFFFF
SA93	0	1	0	1	1	1	0	1	128/64	0BA0000–0BBFFFF	05D0000–05DFFFF
SA94	0	1	0	1	1	1	1	0	128/64	0BC0000–0BDFFFF	05E0000–05EFFFF
SA95	0	1	0	1	1	1	1	1	128/64	0BE0000–0BFFFFF	05F0000–05FFFFF
SA96	0	1	1	0	0	0	0	0	128/64	0C00000–0C1FFFF	0600000–060FFFF
SA97	0	1	1	0	0	0	0	1	128/64	0C20000–0C3FFFF	0610000–061FFFF
SA98	0	1	1	0	0	0	1	0	128/64	0C40000–0C5FFFF	0620000–062FFFF
SA99	0	1	1	0	0	0	1	1	128/64	0C60000–0C7FFFF	0630000–063FFFF
SA100	0	1	1	0	0	1	0	0	128/64	0C80000–0C9FFFF	0640000–064FFFF
SA101	0	1	1	0	0	1	0	1	128/64	0CA0000–0CBFFFF	0650000–065FFFF
SA102	0	1	1	0	0	1	1	0	128/64	0CC0000–0CDFFFF	0660000–066FFFF
SA103	0	1	1	0	0	1	1	1	128/64	0CE0000–0CFFFFF	0670000–067FFFF
SA104	0	1	1	0	1	0	0	0	128/64	0D00000–0D1FFFF	0680000–068FFFF
SA105	0	1	1	0	1	0	0	1	128/64	0D20000–0D3FFFF	0690000–069FFFF
SA106	0	1	1	0	1	0	1	0	128/64	0D40000–0D5FFFF	06A0000–06AFFFF
SA107	0	1	1	0	1	0	1	1	128/64	0D60000–0D7FFFF	06B0000–06BFFFF
SA108	0	1	1	0	1	1	0	0	128/64	0D80000–0D9FFFF	06C0000–06CFFFF
SA109	0	1	1	0	1	1	0	1	128/64	0DA0000–0DBFFFF	06D0000–06DFFFF
SA110	0	1	1	0	1	1	1	0	128/64	0DC0000–0DDFFFF	06E0000–06EFFFF
SA111	0	1	1	0	1	1	1	1	128/64	0DE0000–0DFFFFF	06F0000–06FFFFF
SA112	0	1	1	1	0	0	0	0	128/64	0E00000–0E1FFFF	0700000–070FFFF
SA113	0	1	1	1	0	0	0	1	128/64	0E20000–0E3FFFF	0710000–071FFFF
SA114	0	1	1	1	0	0	1	0	128/64	0E40000–0E5FFFF	0720000–072FFFF
SA115	0	1	1	1	0	0	1	1	128/64	0E60000–0E7FFFF	0730000–073FFFF
SA116	0	1	1	1	0	1	0	0	128/64	0E80000–0E9FFFF	0740000–074FFFF
SA117	0	1	1	1	0	1	0	1	128/64	0EA0000–0EBFFFF	0750000–075FFFF
SA118	0	1	1	1	0	1	1	0	128/64	0EC0000–0EDFFFF	0760000–076FFFF
SA119	0	1	1	1	0	1	1	1	128/64	0EE0000–0EFFFFF	0770000–077FFFF
SA120	0	1	1	1	1	0	0	0	128/64	0F00000–0F1FFFF	0780000–078FFFF
SA121	0	1	1	1	1	0	0	1	128/64	0F20000–0F3FFFF	0790000–079FFFF
SA122	0	1	1	1	1	0	1	0	128/64	0F40000–0F5FFFF	07A0000–07AFFFF
SA123	0	1	1	1	1	0	1	1	128/64	0F60000–0F7FFFF	07B0000–07BFFFF
SA124	0	1	1	1	1	1	0	0	128/64	0F80000–0F9FFFF	07C0000–07CFFFF
SA125	0	1	1	1	1	1	0	1	128/64	0FA0000–0FBFFFF	07D0000–07DFFFF
SA126	0	1	1	1	1	1	1	0	128/64	0FC0000–0FDFFFF	07E0000–07EFFFF

Table 3. Sector Address Table–S29GL256N (Continued)

Sector	A23–A16								Sector Size (Kbytes/ Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA127	0	1	1	1	1	1	1	1	128/64	0FE0000–0FFFFFF	07F0000–07FFFFF
SA128	1	0	0	0	0	0	0	0	128/64	1000000–101FFFF	0800000–080FFFF
SA129	1	0	0	0	0	0	0	1	128/64	1020000–103FFFF	0810000–081FFFF
SA130	1	0	0	0	0	0	1	0	128/64	1040000–105FFFF	0820000–082FFFF
SA131	1	0	0	0	0	0	1	1	128/64	1060000–107FFFF	0830000–083FFFF
SA132	1	0	0	0	0	1	0	0	128/64	1080000–109FFFF	0840000–084FFFF
SA133	1	0	0	0	0	1	0	1	128/64	10A0000–10BFFFF	0850000–085FFFF
SA134	1	0	0	0	0	1	1	0	128/64	10C0000–10DFFFF	0860000–086FFFF
SA135	1	0	0	0	0	1	1	1	128/64	10E0000–10FFFFF	0870000–087FFFF
SA136	1	0	0	0	1	0	0	0	128/64	1100000–111FFFF	0880000–088FFFF
SA137	1	0	0	0	1	0	0	1	128/64	1120000–113FFFF	0890000–089FFFF
SA138	1	0	0	0	1	0	1	0	128/64	1140000–115FFFF	08A0000–08AFFFF
SA139	1	0	0	0	1	0	1	1	128/64	1160000–117FFFF	08B0000–08BFFFF
SA140	1	0	0	0	1	1	0	0	128/64	1180000–119FFFF	08C0000–08CFFFF
SA141	1	0	0	0	1	1	0	1	128/64	11A0000–11BFFFF	08D0000–08DFFFF
SA142	1	0	0	0	1	1	1	0	128/64	11C0000–11DFFFF	08E0000–08EFFFF
SA143	1	0	0	0	1	1	1	1	128/64	11E0000–11FFFFF	08F0000–08FFFFF
SA144	1	0	0	1	0	0	0	0	128/64	1200000–121FFFF	0900000–090FFFF
SA145	1	0	0	1	0	0	0	1	128/64	1220000–123FFFF	0910000–091FFFF
SA146	1	0	0	1	0	0	1	0	128/64	1240000–125FFFF	0920000–092FFFF
SA147	1	0	0	1	0	0	1	1	128/64	1260000–127FFFF	0930000–093FFFF
SA148	1	0	0	1	0	1	0	0	128/64	1280000–129FFFF	0940000–094FFFF
SA149	1	0	0	1	0	1	0	1	128/64	12A0000–12BFFFF	0950000–095FFFF
SA150	1	0	0	1	0	1	1	0	128/64	12C0000–12DFFFF	0960000–096FFFF
SA151	1	0	0	1	0	1	1	1	128/64	12E0000–12FFFFF	0970000–097FFFF
SA152	1	0	0	1	1	0	0	0	128/64	1300000–131FFFF	0980000–098FFFF
SA153	1	0	0	1	1	0	0	1	128/64	1320000–133FFFF	0990000–099FFFF
SA154	1	0	0	1	1	0	1	0	128/64	1340000–135FFFF	09A0000–09AFFFF
SA155	1	0	0	1	1	0	1	1	128/64	1360000–137FFFF	09B0000–09BFFFF
SA156	1	0	0	1	1	1	0	0	128/64	1380000–139FFFF	09C0000–09CFFFF
SA157	1	0	0	1	1	1	0	1	128/64	13A0000–13BFFFF	09D0000–09DFFFF
SA158	1	0	0	1	1	1	1	0	128/64	13C0000–13DFFFF	09E0000–09EFFFF
SA159	1	0	0	1	1	1	1	1	128/64	13E0000–13FFFFF	09F0000–09FFFFF
SA160	1	0	1	0	0	0	0	0	128/64	1400000–141FFFF	0A00000–0A0FFFF
SA161	1	0	1	0	0	0	0	1	128/64	1420000–143FFFF	0A10000–0A1FFFF

Table 3. Sector Address Table–S29GL256N (Continued)

Sector	A23–A16								Sector Size (Kbytes/ Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA162	1	0	1	0	0	0	1	0	128/64	1440000–145FFFF	0A20000–0A2FFFF
SA163	1	0	1	0	0	0	1	1	128/64	1460000–147FFFF	0A30000–0A3FFFF
SA164	1	0	1	0	0	1	0	0	128/64	1480000–149FFFF	0A40000–0A4FFFF
SA165	1	0	1	0	0	1	0	1	128/64	14A0000–14BFFFF	0A50000–0A5FFFF
SA166	1	0	1	0	0	1	1	0	128/64	14C0000–14DFFFF	0A60000–0A6FFFF
SA167	1	0	1	0	0	1	1	1	128/64	14E0000–14FFFFF	0A70000–0A7FFFF
SA168	1	0	1	0	1	0	0	0	128/64	1500000–151FFFF	0A80000–0A8FFFF
SA169	1	0	1	0	1	0	0	1	128/64	1520000–153FFFF	0A90000–0A9FFFF
SA170	1	0	1	0	1	0	1	0	128/64	1540000–155FFFF	0AA0000–0AAFFFF
SA171	1	0	1	0	1	0	1	1	128/64	1560000–157FFFF	0AB0000–0ABFFFF
SA172	1	0	1	0	1	1	0	0	128/64	1580000–159FFFF	0AC0000–0ACFFFF
SA173	1	0	1	0	1	1	0	1	128/64	15A0000–15BFFFF	0AD0000–0ADFFFF
SA174	1	0	1	0	1	1	1	0	128/64	15C0000–15DFFFF	0AE0000–0AEFFFF
SA175	1	0	1	0	1	1	1	1	128/64	15E0000–15FFFFF	0AF0000–0AFFFFF
SA176	1	0	1	1	0	0	0	0	128/64	1600000–161FFFF	0B00000–0B0FFFF
SA177	1	0	1	1	0	0	0	1	128/64	1620000–163FFFF	0B10000–0B1FFFF
SA178	1	0	1	1	0	0	1	0	128/64	1640000–165FFFFF	0B20000–0B2FFFF
SA179	1	0	1	1	0	0	1	1	128/64	1660000–167FFFF	0B30000–0B3FFFF
SA180	1	0	1	1	0	1	0	0	128/64	1680000–169FFFF	0B40000–0B4FFFF
SA181	1	0	1	1	0	1	0	1	128/64	16A0000–16BFFFF	0B50000–0B5FFFF
SA182	1	0	1	1	0	1	1	0	128/64	16C0000–16DFFFF	0B60000–0B6FFFF
SA183	1	0	1	1	0	1	1	1	128/64	16E0000–16FFFFF	0B70000–0B7FFFF
SA184	1	0	1	1	1	0	0	0	128/64	1700000–171FFFF	0B80000–0B8FFFF
SA185	1	0	1	1	1	0	0	1	128/64	1720000–173FFFF	0B90000–0B9FFFF
SA186	1	0	1	1	1	0	1	0	128/64	1740000–175FFFF	0BA0000–0BAFFFF
SA187	1	0	1	1	1	0	1	1	128/64	1760000–177FFFF	0BB0000–0BBFFFF
SA188	1	0	1	1	1	1	0	0	128/64	1780000–179FFFF	0BC0000–0BCFFFF
SA189	1	0	1	1	1	1	0	1	128/64	17A0000–17BFFFF	0BD0000–0BDFFFF
SA190	1	0	1	1	1	1	1	0	128/64	17C0000–17DFFFF	0BE0000–0BEFFFF
SA191	1	0	1	1	1	1	1	1	128/64	17E0000–17FFFFF	0BF0000–0BFFFFF
SA192	1	1	0	0	0	0	0	0	128/64	1800000–181FFFF	0C00000–0C0FFFF
SA193	1	1	0	0	0	0	0	1	128/64	1820000–183FFFF	0C10000–0C1FFFF
SA194	1	1	0	0	0	0	1	0	128/64	1840000–185FFFF	0C20000–0C2FFFF
SA195	1	1	0	0	0	0	1	1	128/64	1860000–187FFFF	0C30000–0C3FFFF
SA196	1	1	0	0	0	1	0	0	128/64	1880000–189FFFF	0C40000–0C4FFFF

Table 3. Sector Address Table–S29GL256N (Continued)

Sector	A23–A16								Sector Size (Kbytes/ Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA197	1	1	0	0	0	1	0	1	128/64	18A0000–18BFFFF	0C50000–0C5FFFF
SA198	1	1	0	0	0	1	1	0	128/64	18C0000–18DFFFF	0C60000–0C6FFFF
SA199	1	1	0	0	0	1	1	1	128/64	18E0000–18FFFFF	0C70000–0C7FFFF
SA200	1	1	0	0	1	0	0	0	128/64	1900000–191FFFF	0C80000–0C8FFFF
SA201	1	1	0	0	1	0	0	1	128/64	1920000–193FFFF	0C90000–0C9FFFF
SA202	1	1	0	0	1	0	1	0	128/64	1940000–195FFFF	0CA0000–0CAFFFF
SA203	1	1	0	0	1	0	1	1	128/64	1960000–197FFFF	0CB0000–0CBFFFF
SA204	1	1	0	0	1	1	0	0	128/64	1980000–199FFFF	0CC0000–0CCFFFF
SA205	1	1	0	0	1	1	0	1	128/64	19A0000–19BFFFF	0CD0000–0CDFFFF
SA206	1	1	0	0	1	1	1	0	128/64	19C0000–19DFFFF	0CE0000–0CEFFFF
SA207	1	1	0	0	1	1	1	1	128/64	19E0000–19FFFF	0CF0000–0CFFFFF
SA208	1	1	0	1	0	0	0	0	128/64	1A00000–1A1FFFF	0D00000–0D0FFFF
SA209	1	1	0	1	0	0	0	1	128/64	1A20000–1A3FFFF	0D10000–0D1FFFF
SA210	1	1	0	1	0	0	1	0	128/64	1A40000–1A5FFFF	0D20000–0D2FFFF
SA211	1	1	0	1	0	0	1	1	128/64	1A60000–1A7FFFF	0D30000–0D3FFFF
SA212	1	1	0	1	0	1	0	0	128/64	1A80000–1A9FFFF	0D40000–0D4FFFF
SA213	1	1	0	1	0	1	0	1	128/64	1AA0000–1ABFFFF	0D50000–0D5FFFF
SA214	1	1	0	1	0	1	1	0	128/64	1AC0000–1ADFFFF	0D60000–0D6FFFF
SA215	1	1	0	1	0	1	1	1	128/64	1AE0000–1AFFFFF	0D70000–0D7FFFF
SA216	1	1	0	1	1	0	0	0	128/64	1B00000–1B1FFFF	0D80000–0D8FFFF
SA217	1	1	0	1	1	0	0	1	128/64	1B20000–1B3FFFF	0D90000–0D9FFFF
SA218	1	1	0	1	1	0	1	0	128/64	1B40000–1B5FFFF	0DA0000–0DAFFFF
SA219	1	1	0	1	1	0	1	1	128/64	1B60000–1B7FFFF	0DB0000–0DBFFFF
SA220	1	1	0	1	1	1	0	0	128/64	1B80000–1B9FFFF	0DC0000–0DCFFFF
SA221	1	1	0	1	1	1	0	1	128/64	1BA0000–1BBFFFF	0DD0000–0DDFFFF
SA222	1	1	0	1	1	1	1	0	128/64	1BC0000–1BDFFFF	0DE0000–0DEFFFF
SA223	1	1	0	1	1	1	1	1	128/64	1BE0000–1BFFFFF	0DF0000–0DFFFFF
SA224	1	1	1	0	0	0	0	0	128/64	1C00000–1C1FFFF	0E00000–0E0FFFF
SA225	1	1	1	0	0	0	0	1	128/64	1C20000–1C3FFFF	0E10000–0E1FFFF
SA226	1	1	1	0	0	0	1	0	128/64	1C40000–1C5FFFF	0E20000–0E2FFFF
SA227	1	1	1	0	0	0	1	1	128/64	1C60000–1C7FFFF	0E30000–0E3FFFF
SA228	1	1	1	0	0	1	0	0	128/64	1C80000–1C9FFFF	0E40000–0E4FFFF
SA229	1	1	1	0	0	1	0	1	128/64	1CA0000–1CBFFFF	0E50000–0E5FFFF
SA230	1	1	1	0	0	1	1	0	128/64	1CC0000–1CDFFFF	0E60000–0E6FFFF
SA231	1	1	1	0	0	1	1	1	128/64	1CE0000–1CFFFFF	0E70000–0E7FFFF

Table 3. Sector Address Table–S29GL256N (Continued)

Sector	A23–A16								Sector Size (Kbytes/ Kwords)	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA232	1	1	1	0	1	0	0	0	128/64	1D00000–1D1FFFF	0E80000–0E8FFFF
SA233	1	1	1	0	1	0	0	1	128/64	1D20000–1D3FFFF	0E90000–0E9FFFF
SA234	1	1	1	0	1	0	1	0	128/64	1D40000–1D5FFFF	0EA0000–0EAFFFF
SA235	1	1	1	0	1	0	1	1	128/64	1D60000–1D7FFFF	0EB0000–0EBFFFF
SA236	1	1	1	0	1	1	0	0	128/64	1D80000–1D9FFFF	0EC0000–0ECFFFF
SA237	1	1	1	0	1	1	0	1	128/64	1DA0000–1DBFFFF	0ED0000–0EDFFFF
SA238	1	1	1	0	1	1	1	0	128/64	1DC0000–1DDFFFF	0EE0000–0EEFFFF
SA239	1	1	1	0	1	1	1	1	128/64	1DE0000–1DFFFFF	0EF0000–0EFFFFF
SA240	1	1	1	1	0	0	0	0	128/64	1E00000–1E1FFFF	0F00000–0F0FFFF
SA241	1	1	1	1	0	0	0	1	128/64	1E20000–1E3FFFF	0F10000–0F1FFFF
SA242	1	1	1	1	0	0	1	0	128/64	1E40000–1E5FFFF	0F20000–0F2FFFF
SA243	1	1	1	1	0	0	1	1	128/64	1E60000–137FFFF	0F30000–0F3FFFF
SA244	1	1	1	1	0	1	0	0	128/64	1E80000–1E9FFFF	0F40000–0F4FFFF
SA245	1	1	1	1	0	1	0	1	128/64	1EA0000–1EBFFFF	0F50000–0F5FFFF
SA246	1	1	1	1	0	1	1	0	128/64	1EC0000–1EDFFFF	0F60000–0F6FFFF
SA247	1	1	1	1	0	1	1	1	128/64	1EE0000–1EFFFFF	0F70000–0F7FFFF
SA248	1	1	1	1	1	0	0	0	128/64	1F00000–1F1FFFF	0F80000–0F8FFFF
SA249	1	1	1	1	1	0	0	1	128/64	1F20000–1F3FFFF	0F90000–0F9FFFF
SA250	1	1	1	1	1	0	1	0	128/64	1F40000–1F5FFFF	0FA0000–0FAFFFF
SA251	1	1	1	1	1	0	1	1	128/64	1F60000–1F7FFFF	0FB0000–0FBFFFF
SA252	1	1	1	1	1	1	0	0	128/64	1F80000–1F9FFFF	0FC0000–0FCFFFF
SA253	1	1	1	1	1	1	0	1	128/64	1FA0000–1FBFFFF	0FD0000–0FDFFFF
SA254	1	1	1	1	1	1	1	0	128/64	1FC0000–1FDFFFF	0FE0000–0FEFFFF
SA255	1	1	1	1	1	1	1	1	128/64	1FE0000–1FFFFFF	0FF0000–0FFFFFF

Table 4. Sector Address Table–S29GLI28N

Sector	A22–A16						Sector Size (Kbytes/ Kwords)	8-Bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA0	0	0	0	0	0	0	128/64	0000000–001FFFF	0000000–000FFFF
SA1	0	0	0	0	0	1	128/64	0020000–003FFFF	0010000–001FFFF
SA2	0	0	0	0	1	0	128/64	0040000–005FFFF	0020000–002FFFF
SA3	0	0	0	0	1	1	128/64	0060000–007FFFF	0030000–003FFFF
SA4	0	0	0	1	0	0	128/64	0080000–009FFFF	0040000–004FFFF
SA5	0	0	0	1	0	1	128/64	00A0000–00BFFFF	0050000–005FFFF

Table 4. Sector Address Table–S29GLI28N (Continued)

Sector	A22–A16						Sector Size (Kbytes/ Kwords)	8-Bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA6	0	0	0	1	1	0	128/64	00C0000–00DFFFF	0060000–006FFFF
SA7	0	0	0	1	1	1	128/64	00E0000–00FFFFF	0070000–007FFFF
SA8	0	0	1	0	0	0	128/64	0100000–011FFFF	0080000–008FFFF
SA9	0	0	1	0	0	1	128/64	0120000–013FFFF	0090000–009FFFF
SA10	0	0	1	0	1	0	128/64	0140000–015FFFF	00A0000–00AFFFF
SA11	0	0	1	0	1	1	128/64	0160000–017FFFF	00B0000–00BFFFF
SA12	0	0	1	1	0	0	128/64	0180000–019FFFF	00C0000–00CFFFF
SA13	0	0	1	1	0	1	128/64	01A0000–01BFFFF	00D0000–00DFFFF
SA14	0	0	1	1	1	0	128/64	01C0000–01DFFFF	00E0000–00EFFFF
SA15	0	0	1	1	1	1	128/64	01E0000–01FFFFF	00F0000–00FFFFF
SA16	0	1	0	0	0	0	128/64	0200000–021FFFF	0100000–010FFFF
SA17	0	1	0	0	0	1	128/64	0220000–023FFFF	0110000–011FFFF
SA18	0	1	0	0	1	0	128/64	0240000–025FFFF	0120000–012FFFF
SA19	0	1	0	0	1	1	128/64	0260000–027FFFF	0130000–013FFFF
SA20	0	1	0	1	0	0	128/64	0280000–029FFFF	0140000–014FFFF
SA21	0	1	0	1	0	1	128/64	02A0000–02BFFFF	0150000–015FFFF
SA22	0	1	0	1	1	0	128/64	02C0000–02DFFFF	0160000–016FFFF
SA23	0	1	0	1	1	1	128/64	02E0000–02FFFFF	0170000–017FFFF
SA24	0	1	1	0	0	0	128/64	0300000–031FFFF	0180000–018FFFF
SA25	0	1	1	0	0	1	128/64	0320000–033FFFF	0190000–019FFFF
SA26	0	1	1	0	1	0	128/64	0340000–035FFFF	01A0000–01AFFFF
SA27	0	1	1	0	1	1	128/64	0360000–037FFFF	01B0000–01BFFFF
SA28	0	1	1	1	0	0	128/64	0380000–039FFFF	01C0000–01CFFFF
SA29	0	1	1	1	0	1	128/64	03A0000–03BFFFF	01D0000–01DFFFF
SA30	0	1	1	1	1	0	128/64	03C0000–03DFFFF	01E0000–01EFFFF
SA31	0	1	1	1	1	1	128/64	03E0000–03FFFFF	01F0000–01FFFFF
SA32	1	0	0	0	0	0	128/64	0400000–041FFFF	0200000–020FFFF
SA33	1	0	0	0	0	1	128/64	0420000–043FFFF	0210000–021FFFF
SA34	1	0	0	0	1	0	128/64	0440000–045FFFF	0220000–022FFFF
SA35	1	0	0	0	1	1	128/64	0460000–047FFFF	0230000–023FFFF
SA36	1	0	0	1	0	0	128/64	0480000–049FFFF	0240000–024FFFF
SA37	1	0	0	1	0	1	128/64	04A0000–04BFFFF	0250000–025FFFF
SA38	1	0	0	1	1	0	128/64	04C0000–04DFFFF	0260000–026FFFF
SA39	1	0	0	1	1	1	128/64	04E0000–04FFFFF	0270000–027FFFF
SA40	1	0	1	0	0	0	128/64	0500000–051FFFF	0280000–028FFFF

Table 4. Sector Address Table–S29GLI28N (Continued)

Sector	A22–A16						Sector Size (Kbytes/ Kwords)	8-Bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA41	1	0	1	0	0	1	128/64	0520000–053FFFF	0290000–029FFFF
SA42	1	0	1	0	1	0	128/64	0540000–055FFFF	02A0000–02AFFFF
SA43	1	0	1	0	1	1	128/64	0560000–057FFFF	02B0000–02BFFFF
SA44	1	0	1	1	0	0	128/64	0580000–059FFFF	02C0000–02CFFFF
SA45	1	0	1	1	0	1	128/64	05A0000–05BFFFF	02D0000–02DFFFF
SA46	1	0	1	1	1	0	128/64	05C0000–05DFFFF	02E0000–02EFFFF
SA47	1	0	1	1	1	1	128/64	05E0000–05FFFFF	02F0000–02FFFFF
SA48	1	1	0	0	0	0	128/64	0600000–061FFFF	0300000–030FFFF
SA49	1	1	0	0	0	1	128/64	0620000–063FFFF	0310000–031FFFF
SA50	1	1	0	0	1	0	128/64	0640000–065FFFF	0320000–032FFFF
SA51	1	1	0	0	1	1	128/64	0660000–067FFFF	0330000–033FFFF
SA52	1	1	0	1	0	0	128/64	0680000–069FFFF	0340000–034FFFF
SA53	1	1	0	1	0	1	128/64	06A0000–06BFFFF	0350000–035FFFF
SA54	1	1	0	1	1	0	128/64	06C0000–06DFFFF	0360000–036FFFF
SA55	1	1	0	1	1	1	128/64	06E0000–06FFFFF	0370000–037FFFF
SA56	1	1	1	0	0	0	128/64	0700000–071FFFF	0380000–038FFFF
SA57	1	1	1	0	0	1	128/64	0720000–073FFFF	0390000–039FFFF
SA58	1	1	1	0	1	0	128/64	0740000–075FFFF	03A0000–03AFFFF
SA59	1	1	1	0	1	1	128/64	0760000–077FFFF	03B0000–03BFFFF
SA60	1	1	1	1	0	0	128/64	0780000–079FFFF	03C0000–03CFFFF
SA61	1	1	1	1	0	1	128/64	07A0000–07BFFFF	03D0000–03DFFFF
SA62	1	1	1	1	1	0	128/64	07C0000–07DFFFF	03E0000–03EFFFF
SA63	1	1	1	1	1	1	128/64	07E0000–07FFFFF	03F0000–03FFFFF
SA64	0	0	0	0	0	0	128/64	0800000–081FFFF	0400000–040FFFF
SA65	0	0	0	0	0	1	128/64	0820000–083FFFF	0410000–041FFFF
SA66	0	0	0	0	1	0	128/64	0840000–085FFFF	0420000–042FFFF
SA67	0	0	0	0	1	1	128/64	0860000–087FFFF	0430000–043FFFF
SA68	0	0	0	1	0	0	128/64	0880000–089FFFF	0440000–044FFFF
SA69	0	0	0	1	0	1	128/64	08A0000–08BFFFF	0450000–045FFFF
SA70	0	0	0	1	1	0	128/64	08C0000–08DFFFF	0460000–046FFFF
SA71	0	0	0	1	1	1	128/64	08E0000–08FFFFF	0470000–047FFFF
SA72	0	0	1	0	0	0	128/64	0900000–091FFFF	0480000–048FFFF
SA73	0	0	1	0	0	1	128/64	0920000–093FFFF	0490000–049FFFF
SA74	0	0	1	0	1	0	128/64	0940000–095FFFF	04A0000–04AFFFF
SA75	0	0	1	0	1	1	128/64	0960000–097FFFF	04B0000–04BFFFF

Table 4. Sector Address Table–S29GLI28N (Continued)

Sector	A22–A16						Sector Size (Kbytes/ Kwords)	8-Bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA76	0	0	1	1	0	0	128/64	0980000–099FFFF	04C0000–04CFFFF
SA77	0	0	1	1	0	1	128/64	09A0000–09BFFFF	04D0000–04DFFFF
SA78	0	0	1	1	1	0	128/64	09C0000–09DFFFF	04E0000–04EFFFF
SA79	0	0	1	1	1	1	128/64	09E0000–09FFFFF	04F0000–04FFFFF
SA80	0	1	0	0	0	0	128/64	0A00000–0A1FFFF	0500000–050FFFF
SA81	0	1	0	0	0	1	128/64	0A20000–0A3FFFF	0510000–051FFFF
SA82	0	1	0	0	1	0	128/64	0A40000–0A5FFFF	0520000–052FFFF
SA83	0	1	0	0	1	1	128/64	0A60000–0A7FFFF	0530000–053FFFF
SA84	0	1	0	1	0	0	128/64	0A80000–0A9FFFF	0540000–054FFFF
SA85	0	1	0	1	0	1	128/64	0AA0000–0ABFFFF	0550000–055FFFF
SA86	0	1	0	1	1	0	128/64	0AC0000–0ADFFFF	0560000–056FFFF
SA87	0	1	0	1	1	1	128/64	0AE0000–0AFFFFF	0570000–057FFFF
SA88	0	1	1	0	0	0	128/64	0B00000–0B1FFFF	0580000–058FFFF
SA89	0	1	1	0	0	1	128/64	0B20000–0B3FFFF	0590000–059FFFF
SA90	0	1	1	0	1	0	128/64	0B40000–0B5FFFF	05A0000–05AFFFF
SA91	0	1	1	0	1	1	128/64	0B60000–0B7FFFF	05B0000–05BFFFF
SA92	0	1	1	1	0	0	128/64	0B80000–0B9FFFF	05C0000–05CFFFF
SA93	0	1	1	1	0	1	128/64	0BA0000–0BBFFFF	05D0000–05DFFFF
SA94	0	1	1	1	1	0	128/64	0BC0000–0BDFFFF	05E0000–05EFFFF
SA95	0	1	1	1	1	1	128/64	0BE0000–0BFFFFF	05F0000–05FFFFF
SA96	1	0	0	0	0	0	128/64	0C00000–0C1FFFF	0600000–060FFFF
SA97	1	0	0	0	0	1	128/64	0C20000–0C3FFFF	0610000–061FFFF
SA98	1	0	0	0	1	0	128/64	0C40000–0C5FFFF	0620000–062FFFF
SA99	1	0	0	0	1	1	128/64	0C60000–0C7FFFF	0630000–063FFFF
SA100	1	0	0	1	0	0	128/64	0C80000–0C9FFFF	0640000–064FFFF
SA101	1	0	0	1	0	1	128/64	0CA0000–0CBFFFF	0650000–065FFFF
SA102	1	0	0	1	1	0	128/64	0CC0000–0CDFFFF	0660000–066FFFF
SA103	1	0	0	1	1	1	128/64	0CE0000–0CFFFFF	0670000–067FFFF
SA104	1	0	1	0	0	0	128/64	0D00000–0D1FFFF	0680000–068FFFF
SA105	1	0	1	0	0	1	128/64	0D20000–0D3FFFF	0690000–069FFFF
SA106	1	0	1	0	1	0	128/64	0D40000–0D5FFFF	06A0000–06AFFFF
SA107	1	0	1	0	1	1	128/64	0D60000–0D7FFFF	06B0000–06BFFFF
SA108	1	0	1	1	0	0	128/64	0D80000–0D9FFFF	06C0000–06CFFFF
SA109	1	0	1	1	0	1	128/64	0DA0000–0DBFFFF	06D0000–06DFFFF
SA110	1	0	1	1	1	0	128/64	0DC0000–0DDFFFF	06E0000–06EFFFF

Table 4. Sector Address Table–S29GLI28N (Continued)

Sector	A22–A16						Sector Size (Kbytes/ Kwords)	8-Bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA111	1	0	1	1	1	1	128/64	0DE0000–0DFFFFF	06F0000–06FFFFF
SA112	1	1	0	0	0	0	128/64	0E00000–0E1FFFF	0700000–070FFFF
SA113	1	1	0	0	0	1	128/64	0E20000–0E3FFFF	0710000–071FFFF
SA114	1	1	0	0	1	0	128/64	0E40000–0E5FFFF	0720000–072FFFF
SA115	1	1	0	0	1	1	128/64	0E60000–0E7FFFF	0730000–073FFFF
SA116	1	1	0	1	0	0	128/64	0E80000–0E9FFFF	0740000–074FFFF
SA117	1	1	0	1	0	1	128/64	0EA0000–0EBFFFF	0750000–075FFFF
SA118	1	1	0	1	1	0	128/64	0EC0000–0EDFFFF	0760000–076FFFF
SA119	1	1	0	1	1	1	128/64	0EE0000–0EFFFFF	0770000–077FFFF
SA120	1	1	1	0	0	0	128/64	0F00000–0F1FFFF	0780000–078FFFF
SA121	1	1	1	0	0	1	128/64	0F20000–0F3FFFF	0790000–079FFFF
SA122	1	1	1	0	1	0	128/64	0F40000–0F5FFFF	07A0000–07AFFFF
SA123	1	1	1	0	1	1	128/64	0F60000–0F7FFFF	07B0000–07BFFFF
SA124	1	1	1	1	0	0	128/64	0F80000–0F9FFFF	07C0000–07CFFFF
SA125	1	1	1	1	0	1	128/64	0FA0000–0FBFFFF	07D0000–07DFFFF
SA126	1	1	1	1	1	0	128/64	0FC0000–0FDFFFF	07E0000–07EFFFF
SA127	1	1	1	1	1	1	128/64	0FE0000–0FFFFFF	07F0000–07FFFFF

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector group protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires VID on address pin A9. Address pins A6, A3, A2, A1, and A0 must be as shown in Table 5. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Table 2). Table 5 shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 12 and Table 13. This method does not require V_{ID}. Refer to the Autoselect Command Sequence section for more information.

Table 5. Autoselect Codes, (High Voltage Method)

Description		CE#	OE#	WE #	A22 to A15	A14 to A10	A9	A8 to A7	A6	A5 to A4	A3 to A2	A1	A0	DQ8 to DQ15		DQ7 to DQ0
														BYTE#= V_{IH}	BYTE# = V_{IL}	
Manufacturer ID: Spansion Product		L	L	H	X	X	V_{ID}	X	L	X	L	L	L	00	X	01h
Device ID S29GL512N	Cycle 1	L	L	H	X	X	V_{ID}	X	L	X	L	L	H	22	X	7Eh
	Cycle 2										H	H	L	22	X	23h
	Cycle 3										H	H	H	22	X	01h
Device ID S29GL256N	Cycle 1	L	L	H	X	X	V_{ID}	X	L	X	L	L	H	22	X	7Eh
	Cycle 2										H	H	L	22	X	22h
	Cycle 3										H	H	H	22	X	01h
Device ID S29GL128N	Cycle 1	L	L	H	X	X	V_{ID}	X	L	X	L	L	H	22	X	7Eh
	Cycle 2										H	H	L	22	X	21h
	Cycle 3										H	H	H	22	X	01h
Sector Group Protection Verification		L	L	H	SA	X	V_{ID}	X	L	X	L	H	L	X	X	01h (protected), 00h (unprotected)
SecSi Sector Indicator Bit (DQ7), WP# protects highest address sector		L	L	H	X	X	V_{ID}	X	L	X	L	H	H	X	X	98h (factory locked), 18h (not factory locked)
SecSi Sector Indicator Bit (DQ7), WP# protects lowest address sector		L	L	H	X	X	V_{ID}	X	L	X	L	H	H	X	X	88h (factory locked), 08h (not factory locked)

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care.*

Sector Protection

The device features several levels of sector protection, which can disable both the program and erase operations in certain sectors or sector groups:

Persistent Sector Protection

A command sector protection method that replaces the old 12 V controlled protection method.

Password Sector Protection

A highly sophisticated protection method that requires a password before changes to certain sectors or sector groups are permitted

WP# Hardware Protection

A write protect pin that can prevent program or erase operations in the outermost sectors.

The WP# Hardware Protection feature is always available, independent of the software managed protection method chosen.

Selecting a Sector Protection Mode

All parts default to operate in the Persistent Sector Protection mode. The customer must then choose if the Persistent or Password Protection method is most desirable. There are two one-time programmable non-volatile bits that define which sector protection method will be used. If the customer decides to continue

using the Persistent Sector Protection method, they must set the **Persistent Sector Protection Mode Locking Bit**. This will permanently set the part to operate only using Persistent Sector Protection. If the customer decides to use the password method, they must set the **Password Mode Locking Bit**. This will permanently set the part to operate only using password sector protection.

It is important to remember that setting either the **Persistent Sector Protection Mode Locking Bit** or the **Password Mode Locking Bit** permanently selects the protection mode. It is not possible to switch between the two methods once a locking bit has been set. **It is important that one mode is explicitly selected when the device is first programmed, rather than relying on the default mode alone.** This is so that it is not possible for a system program or virus to later set the Password Mode Locking Bit, which would cause an unexpected shift from the default Persistent Sector Protection Mode into the Password Protection Mode.

The device is shipped with all sectors unprotected. The factory offers the option of programming and protecting sectors at the factory prior to shipping the device through the ExpressFlash™ Service. Contact your sales representative for details.

It is possible to determine whether a sector is protected or unprotected. See “Autoselect Command Sequence” section on page 58 for details.

Advanced Sector Protection

Advanced Sector Protection features several levels of sector protection, which can disable both the program and erase operations in certain sectors.

Persistent Sector Protection is a method that replaces the old 12V controlled protection method.

Password Sector Protection is a highly sophisticated protection method that requires a password before changes to certain sectors are permitted.

Advanced Sector Protection is available when ACC = V_{HH}.

Lock Register

The Lock Register consists of 3 bits (DQ2, DQ1, and DQ0). These DQ2, DQ1, DQ0 bits of the Lock Register are programmable by the user. Users are not allowed to program both DQ2 and DQ1 bits of the Lock Register to the 00 state. If the user tries to program DQ2 and DQ1 bits of the Lock Register to the 00 state, the device will abort the Lock Register back to the default 11 state. The programming time of the Lock Register is same as the typical word programming time without utilizing the Write Buffer of the device. During a Lock Register programming sequence execution, the DQ6 Toggle Bit I will toggle until the programming of the Lock Register has completed to indicate programming status. All Lock Register bits are readable to allow users to verify Lock Register statuses. Initial access delay is required to read the Lock Register.

The Customer SecSi Sector Protection Bit is DQ0, Persistent Protection Mode Lock Bit is DQ1, and Password Protection Mode Lock Bit is DQ2 are accessible by all users. Each of these bits are non-volatile. DQ15-DQ3 are reserved and must be 1's when the user tries to program the DQ2, DQ1, and DQ0 bits of the Lock Register. The user is not required to program DQ2, DQ1 and DQ0 bits of the Lock Register at the same time. This allows users to lock the SecSi Sector and then set the device either permanently into Password Protection Mode or Persistent Protection Mode and then lock the SEcSi Sector at separate instances and time frames.

- SecSi Sector Protection allows the user to lock the SecSi Sector area
- Persistent Protection Mode Lock Bit allows the user to set the device permanently to operate in the Persistent Protection Mode
- Password Protection Mode Lock Bit allows the user to set the device permanently to operate in the Password Protection Mode

Table 6. Lock Register

DQ15-3	DQ2	DQ1	DQ0
Don't Care	Password Protection Mode Lock Bit	Persistent Protection Mode Lock Bit	SecSi Sector Protection Bit

Persistent Sector Protection

The Persistent Sector Protection method replaces the old 12 V controlled protection method while at the same time enhancing flexibility by providing three different sector protection states:

- **Dynamically Locked**-The sector is protected and can be changed by a simple command
- **Persistently Locked**-A sector is protected and cannot be changed
- **Unlocked**-The sector is unprotected and can be changed by a simple command

In order to achieve these states, three types of "bits" are going to be used:

Dynamic Protection Bit (DYB)

A volatile protection bit is assigned for each sector. After power-up or hardware reset, the contents of all DYB bits are in the "unprotected state" if the DYB Lock Bit of the "Lock Register" is not programmed. If the DYB Lock Bit of the "Lock Register" is programmed, all DYB bits will power-up or hardware reset to the "protected state". Each DYB is individually modifiable through the DYB Set Command and DYB Clear Command. When the parts are first shipped, all of the Persistent Protect Bits (PPB) are cleared into the unprotected state. The DYB bits and PPB Lock bit are defaulted to power up in the cleared state or unprotected state - meaning the all PPB bits are changeable.

The Protection State for each sector is determined by the logical OR of the PPB and the DYB related to that sector. For the sectors that have the PPB bits cleared, the DYB bits control whether or not the sector is protected or unprotected. By issuing the DYB Set and DYB Clear command sequences, the DYB bits will be protected or unprotected, thus placing each sector in the protected or unprotected state. These are the so-called Dynamic Locked or Unlocked states. They are called dynamic states because it is very easy to switch back and forth between the protected and un-protected conditions. This allows software to easily protect sectors against inadvertent changes yet does not prevent the easy removal of protection when changes are needed.

The DYB bits maybe set or cleared as often as needed. The PPB bits allow for a more static, and difficult to change, level of protection. The PPB bits retain their state across power cycles because they are Non-Volatile. Individual PPB bits are set with a program command but must all be cleared as a group through an erase command.

The PPB Lock Bit adds an additional level of protection. Once all PPB bits are programmed to the desired settings, the PPB Lock Bit may be set to the "freeze

state". Setting the PPB Lock Bit to the "freeze state" disables all program and erase commands to the Non-Volatile PPB bits. In effect, the PPB Lock Bit locks the PPB bits into their current state. The only way to clear the PPB Lock Bit to the "unfreeze state" is to go through a power cycle, or hardware reset. The Software Reset command will not clear the PPB Lock Bit to the "unfreeze state". System boot code can determine if any changes to the PPB bits are needed e.g. to allow new system code to be downloaded. If no changes are needed then the boot code can set the PPB Lock Bit to disable any further changes to the PPB bits during system operation.

The WP# write protect pin adds a final level of hardware protection. When this pin is low it is not possible to change the contents of the WP# protected sectors. These sectors generally hold system boot code. So, the WP# pin can prevent any changes to the boot code that could override the choices made while setting up sector protection during system initialization.

It is possible to have sectors that have been persistently locked, and sectors that are left in the dynamic state. The sectors in the dynamic state are all unprotected. If there is a need to protect some of them, a simple DYB Set command sequence is all that is necessary. The DYB Set and DYB Clear commands for the dynamic sectors switch the DYB bits to signify protected and unprotected, respectively. If there is a need to change the status of the persistently locked sectors, a few more steps are required. First, the PPB Lock Bit must be disabled to the "unfreeze state" by either putting the device through a power-cycle, or hardware reset. The PPB bits can then be changed to reflect the desired settings. Setting the PPB Lock Bit once again to the "freeze state" will lock the PPB bits, and the device operates normally again.

Note: to achieve the best protection, it's recommended to execute the PPB Lock Bit Set command early in the boot code, and protect the boot code by holding WP# = V_{IL}.

Persistent Protection Bit (PPB)

A single Persistent (non-volatile) Protection Bit is assigned to each sector. If a PPB is programmed to the protected state through the "PPB Program" command, that sector will be protected from program or erase operations will be read-only. If a PPB requires erasure, all of the sector PPB bits must first be erased in parallel through the "All PPB Erase" command. The "All PPB Erase" command will preprogrammed all PPB bits prior to PPB erasing. All PPB bits erase in parallel, unlike programming where individual PPB bits are programmable. The PPB bits have the same endurance as the flash memory.

Programming the PPB bit requires the typical word programming time without utilizing the Write Buffer. During a PPB bit programming and A11 PPB bit erasing sequence execution, the DQ6 Toggle Bit I will toggle until the programming of the PPB bit or erasing of all PPB bits has completed to indicate programming and erasing status. Erasing all of the PPB bits at once requires typical sector erase time. During the erasing of all PPB bits, the DQ3 Sector Erase Timer bit will output a 1 to indicate the erasure of all PPB bits are in progress. When the erasure of all PPB bits has completed, the DQ3 Sector Erase Timer bit will output a 0 to indicate that all PPB bits have been erased. Reading the PPB Status bit requires the initial access time of the device.

Persistent Protection Bit Lock (PPB Lock Bit)

A global volatile bit. When set to the “freeze state”, the PPB bits cannot be changed. When cleared to the “unfreeze state”, the PPB bits are changeable. There is only one PPB Lock Bit per device. The PPB Lock Bit is cleared to the “unfreeze state” after power-up or hardware reset. There is no command sequence to unlock or “unfreeze” the PPB Lock Bit.

Configuring the PPB Lock Bit to the freeze state requires approximately 100ns. Reading the PPB Lock Status bit requires the initial access time of the device.

Table 7. Sector Protection Schemes

Protection States			Sector State
DYB Bit	PPB Bit	PPB Lock Bit	
Unprotect	Unprotect	Unfreeze	Unprotected – PPB and DYB are changeable
Unprotect	Unprotect	Freeze	Unprotected – PPB not changeable, DYB is changeable
Unprotect	Protect	Unfreeze	Protected – PPB and DYB are changeable
Unprotect	Protect	Freeze	Protected – PPB not changeable, DYB is changeable
Protect	Unprotect	Unfreeze	Protected – PPB and DYB are changeable
Protect	Unprotect	Freeze	Protected – PPB not changeable, DYB is changeable
Protect	Protect	Unfreeze	Protected – PPB and DYB are changeable
Protect	Protect	Freeze	Protected – PPB not changeable, DYB is changeable

Table 7 contains all possible combinations of the DYB bit, PPB bit, and PPB Lock Bit relating to the status of the sector. In summary, if the PPB bit is set, and the PPB Lock Bit is set, the sector is protected and the protection cannot be removed until the next power cycle or hardware reset clears the PPB Lock Bit to “unfreeze state”. If the PPB bit is cleared, the sector can be dynamically locked or unlocked. The DYB bit then controls whether or not the sector is protected or unprotected. If the user attempts to program or erase a protected sector, the device ignores the command and returns to read mode. A program command to a protected sector enables status polling for approximately 1 µs before the device returns to read mode without having modified the contents of the protected sector. An erase command to a protected sector enables status polling for approximately 50 µs after which the device returns to read mode without having erased the protected sector. The programming of the DYB bit, PPB bit, and PPB Lock Bit for a given sector can be verified by writing a DYB Status Read, PPB Status Read, and PPB Lock Status Read commands to the device.

The Autoselect Sector Protection Verification outputs the OR function of the DYB bit and PPB bit per sector basis. When the OR function of the DYB bit and PPB bit is a 1, the sector is either protected by DYB or PPB or both. When the OR function of the DYB bit and PPB bit is a 0, the sector is unprotected through both the DYB and PPB.

Persistent Protection Mode Lock Bit

Like the Password Protection Mode Lock Bit, a Persistent Protection Mode Lock Bit exists to guarantee that the device remain in software sector protection. Once programmed, the Persistent Protection Mode Lock Bit prevents programming of

the Password Protection Mode Lock Bit. This guarantees that a hacker could not place the device in Password Protection Mode. The Password Protection Mode Lock Bit resides in the “Lock Register”.

Password Sector Protection

The Password Sector Protection method allows an even higher level of security than the Persistent Sector Protection method. There are two main differences between the Persistent Sector Protection and the Password Sector Protection methods:

- When the device is first powered on, or comes out of a reset cycle, the PPB Lock Bit is set to the locked state, or the freeze state, rather than cleared to the unlocked state, or the unfreeze state.
- The only means to clear and unfreeze the PPB Lock Bit is by writing a unique 64-bit Password to the device.

The Password Sector Protection method is otherwise identical to the Persistent Sector Protection method.

A 64-bit password is the only additional tool utilized in this method.

The password is stored in a one-time programmable (OTP) region outside of the flash memory. Once the Password Protection Mode Lock Bit is set, the password is permanently set with no means to read, program, or erase it. The password is used to clear and unfreeze the PPB Lock Bit. The Password Unlock command must be written to the flash, along with a password. The flash device internally compares the given password with the pre-programmed password. If they match, the PPB Lock Bit is cleared to the “unfreezed state”, and the PPB bits can be altered. If they do not match, the flash device does nothing. There is a built-in 2 µs delay for each “password check” after the valid 64-bit password has been entered for the PPB Lock Bit to be cleared to the “unfreezed state”. This delay is intended to thwart any efforts to run a program that tries all possible combinations in order to crack the password.

Password and Password Protection Mode Lock Bit

In order to select the Password Sector Protection method, the customer must first program the password. The factory recommends that the password be somehow correlated to the unique Electronic Serial Number (ESN) of the particular flash device. Each ESN is different for every flash device; therefore each password should be different for every flash device. While programming in the password region, the customer may perform Password Read operations. Once the desired password is programmed in, the customer must then set the Password Protection Mode Lock Bit. This operation achieves two objectives:

1. It permanently sets the device to operate using the Password Protection Mode. It is not possible to reverse this function.
2. It also disables all further commands to the password region. All program, and read operations are ignored.

Both of these objectives are important, and if not carefully considered, may lead to unrecoverable errors. The user must be sure that the Password Sector Protection method is desired when programming the Password Protection Mode Lock Bit. More importantly, the user must be sure that the password is correct when the Password Protection Mode Lock Bit is programmed. Due to the fact that read operations are disabled, there is no means to read what the password is afterwards. If the password is lost after programming the Password Protection Mode

Lock Bit, there will be no way to clear and unfreeze the PPB Lock Bit. The Password Protection Mode Lock Bit, once programmed, prevents reading the 64-bit password on the DQ bus and further password programming. The Password Protection Mode Lock Bit is not erasable. Once Password Protection Mode Lock Bit is programmed, the Persistent Protection Mode Lock Bit is disabled from programming, guaranteeing that no changes to the protection scheme are allowed.

64-bit Password

The 64-bit Password is located in its own memory space and is accessible through the use of the Password Program and Password Read commands. The password function works in conjunction with the Password Protection Mode Lock Bit, which when programmed, prevents the Password Read command from reading the contents of the password on the pins of the device.

Persistent Protection Bit Lock (PPB Lock Bit)

A global volatile bit. The PPB Lock Bit is a volatile bit that reflects the state of the Password Protection Mode Lock Bit after power-up reset. If the Password Protection Mode Lock Bit is also programmed after programming the Password, the Password Unlock command must be issued to clear and unfreeze the PPB Lock Bit after a hardware reset (RESET# asserted) or a power-up reset. Successful execution of the Password Unlock command clears and unfreezes the PPB Lock Bit, allowing for sector PPB bits to be modified. Without issuing the Password Unlock command, while asserting RESET#, taking the device through a power-on reset, or issuing the PPB Lock Bit Set command sets the PPB Lock Bit to a the “freeze state”.

If the Password Protection Mode Lock Bit is not programmed, the device defaults to Persistent Protection Mode. In the Persistent Protection Mode, the PPB Lock Bit is cleared to the “unfreeze state” after power-up or hardware reset. The PPB Lock Bit is set to the “freeze state” by issuing the PPB Lock Bit Set command. Once set to the “freeze state” the only means for clearing the PPB Lock Bit to the “unfreeze state” is by issuing a hardware or power-up reset. The Password Unlock command is ignored in Persistent Protection Mode.

Reading the PPB Lock Bit requires a 200ns access time.

SecSi (Secured Silicon) Sector Flash Memory Region

The SecSi (Secured Silicon) Sector feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The SecSi Sector is 256 bytes in length, and uses a SecSi Sector Indicator Bit (DQ7) to indicate whether or not the SecSi Sector is locked when shipped from the factory. This bit is permanently set at the factory and cannot be changed, which prevents cloning of a factory locked part. This ensures the security of the ESN once the product is shipped to the field.

The factory offers the device with the SecSi Sector either customer lockable (standard shipping option) or factory locked (contact an AMD sales representative for ordering information). The customer-lockable version is shipped with the SecSi Sector unprotected, allowing customers to program the sector after receiving the device. The customer-lockable version also has the SecSi Sector Indicator Bit permanently set to a “0.” The factory-locked version is always protected when shipped from the factory, and has the SecSi (Secured Silicon) Sector Indicator Bit permanently set to a “1.” Thus, the SecSi Sector Indicator Bit prevents customer-lockable devices from being used to replace devices that are factory locked. *Note*

that the ACC function and unlock bypass modes are not available when the SecSi Sector is enabled.

The SecSi sector address space in this device is allocated as follows:

SecSi Sector Address Range	Customer Lockable	ESN Factory Locked	ExpressFlash Factory Locked
000000h–000007h	Determined by customer	ESN	ESN or determined by customer
000008h–00007Fh		Unavailable	Determined by customer

The system accesses the SecSi Sector through a command sequence (see "Write Protect (WP#)"). After the system has written the Enter SecSi Sector command sequence, it may read the SecSi Sector by using the addresses normally occupied by the first sector (SA0). This mode of operation continues until the system issues the Exit SecSi Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to sector SA0.

Customer Lockable: SecSi Sector NOT Programmed or Protected At the Factory

Unless otherwise specified, the device is shipped such that the customer may program and protect the 256-byte SecSi sector.

The system may program the SecSi Sector using the write-buffer, accelerated and/or unlock bypass methods, in addition to the standard programming command sequence. See Command Definitions.

Programming and protecting the SecSi Sector must be used with caution since, once protected, there is no procedure available for unprotecting the SecSi Sector area and none of the bits in the SecSi Sector memory space can be modified in any way.

The SecSi Sector area can be protected using one of the following procedures:

- Write the three-cycle Enter SecSi Sector Region command sequence, and then follow the in-system sector protect algorithm as shown in Figure 2, except that *RESET# may be at either* V_{IH} *or* V_{ID}. This allows in-system protection of the SecSi Sector without raising any device pin to a high voltage. Note that this method is only applicable to the SecSi Sector.
- To verify the protect/unprotect status of the SecSi Sector, follow the algorithm shown in Figure 1.

Once the SecSi Sector is programmed, locked and verified, the system must write the Exit SecSi Sector Region command sequence to return to reading and writing within the remainder of the array.

Factory Locked: SecSi Sector Programmed and Protected At the Factory

In devices with an ESN, the SecSi Sector is protected when the device is shipped from the factory. The SecSi Sector cannot be modified in any way. An ESN Factory Locked device has an 16-byte random ESN at addresses 000000h–000007h. Please contact your sales representative for details on ordering ESN Factory Locked devices.

Customers may opt to have their code programmed by the factory through the ExpressFlash service (Express Flash Factory Locked). The devices are then shipped from the factory with the SecSi Sector permanently locked. Contact your sales representative for details on using the ExpressFlash service.

Write Protect (WP#)

The Write Protect function provides a hardware method of protecting the first or last sector group without using V_{ID}. Write Protect is one of two functions provided by the WP#/ACC input.

If the system asserts V_{IL} on the WP#/ACC pin, the device disables program and erase functions in the first or last sector group independently of whether those sector groups were protected or unprotected using the method described in"Advanced Sector Protection" section on page 46. Note that if WP#/ACC is at V_{IL} when the device is in the standby mode, the maximum input load current is increased. See the table in "DC Characteristics" section on page 86.

If the system asserts V_{IH} on the WP#/ACC pin, the device reverts to whether the first or last sector was previously set to be protected or unprotected using the method described in "Sector Group Protection and Unprotection". *Note that WP# has an internal pullup; when unconnected, WP# is at V_{IH}.*

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Tables 16 and 17 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to the read mode. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

Common Flash Memory Interface (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can

then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h, any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 8-11. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 8–11. The system must write the reset command to return the device to reading array data.

For further information, please refer to the CFI Specification and CFI Publication 100, available via the World Wide Web at http://www.amd.com/flash/cfi. Alternatively, contact your sales representative for copies of these documents.

Table 8. CFI Query Identification String

Addresses (x16)	Addresses (x8)	Data	Description
10h 11h 12h	20h 22h 24h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
13h 14h	26h 28h	0002h 0000h	Primary OEM Command Set
15h 16h	2Ah 2Ch	0040h 0000h	Address for Primary Extended Table
17h 18h	2Eh 30h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	32h 34h	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 9. System Interface String

Addresses (x16)	Addresses (x8)	Data	Description
1Bh	36h	0027h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	38h	0036h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	3Ah	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	3Ch	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	3Eh	0007h	Typical timeout per single byte/word write 2^N µs
20h	40h	0007h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	42h	000Ah	Typical timeout per individual block erase 2^N ms
22h	44h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	46h	0001h	Max. timeout for byte/word write 2^N times typical
24h	48h	0005h	Max. timeout for buffer write 2^N times typical
25h	4Ah	0004h	Max. timeout per individual block erase 2^N times typical
26h	4Ch	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 10. Device Geometry Definition

Addresses (x16)	Addresses (x8)	Data	Description
27h	4Eh	001Ah 0019h 0018h	Device Size = 2^N byte 1A = 512 Mb, 19 = 256 Mb, 18 = 128 Mb
28h 29h	50h 52h	0002h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	54h 56h	0005h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	58h	0001h	Number of Erase Block Regions within device (01h = uniform device, 02h = boot device)
2Dh 2Eh 2Fh 30h	5Ah 5Ch 5Eh 60h	00xxh 000xh 0000h 000xh	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100) 00FFh, 001h, 0000h, 0002h = 512 Mb 00FFh, 0000h, 0000h, 0002h = 256 Mb 007Fh, 0000h, 0000h, 0002h = 128 Mb
31h 32h 33h 34h	60h 64h 66h 68h	0000h 0000h 0000h 0000h	Erase Block Region 2 Information (refer to CFI publication 100)
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0000h 0000h 0000h 0000h	Erase Block Region 3 Information (refer to CFI publication 100)
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	0000h 0000h 0000h 0000h	Erase Block Region 4 Information (refer to CFI publication 100)

Table II. Primary Vendor-Specific Extended Query

Addresses (x16)	Addresses (x8)	Data	Description
40h 41h 42h	80h 82h 84h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	86h	0031h	Major version number, ASCII
44h	88h	0033h	Minor version number, ASCII
45h	8Ah	0010h	Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Process Technology (Bits 7-2) 0100b = 110 nm MirrorBit
46h	8Ch	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	8Eh	0001h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	90h	0000h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	92h	0008h	Sector Protect/Unprotect scheme 0008h = Advanced Sector Protection
4Ah	94h	0000h	Simultaneous Operation 00 = Not Supported, X = Number of Sectors in Bank
4Bh	96h	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	98h	0002h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	9Ah	00B5h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	9Ch	00C5h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	9Eh	00xxh	WP# Protection 04h = Uniform sectors bottom WP# protect, 05h = Uniform sectors top WP# protect
50h	A0h	0001h	Program Suspend 00h = Not Supported, 01h = Supported

Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. Table 12 and Table 13 define the valid register command sequences. *Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state.* A reset command is then required to return the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the AC Characteristics section for timing diagrams.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See the Erase Suspend/Erase Resume Commands section for more information.

The system *must* issue the reset command to return the device to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the device is in the autoselect mode. See the next section, Reset Command, for more information.

See also Requirements for Reading Array Data in the Device Bus Operations section for more information. The Read-Only Operations–"AC Characteristics" section on page 88 provides the read parameters, and Figure 11 shows the timing diagram.

Reset Command

Writing the reset command resets the device to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to the read mode. If the program command sequence is written while the device is in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If the device entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to the read mode (or erase-suspend-read mode if the device was in Erase Suspend).

Note that if DQ1 goes high during a Write Buffer Programming operation, the system must write the Write-to-Buffer-Abort Reset command sequence to reset the device for the next operation.

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. Table 12 and Table 13 show the address and data requirements. This method is an alternative to that shown in Table 5, which is intended for PROM programmers

and requires V_{ID} on address pin A9. The autoselect command sequence may be written to an address that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the autoselect command. The device then enters the autoselect mode. The system may read at any address any number of times without initiating another autoselect command sequence:

- A read cycle at address XX00h returns the manufacturer code.
- Three read cycles at addresses 01h, 0Eh, and 0Fh return the device code.
- A read cycle to an address containing a sector address (SA), and the address 02h on A7–A0 in word mode returns 01h if the sector is protected, or 00h if it is unprotected.

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the device was previously in Erase Suspend).

Enter SecSi Sector/Exit SecSi Sector Command Sequence

The SecSi Sector region provides a secured data area containing an 8-word/16-byte random Electronic Serial Number (ESN). The system can access the SecSi Sector region by issuing the three-cycle Enter SecSi Sector command sequence. The device continues to access the SecSi Sector region until the system issues the four-cycle Exit SecSi Sector command sequence. The Exit SecSi Sector command sequence returns the device to normal operation. Table 12 and Table 13 show the address and data requirements for both command sequences. See also "SecSi (Secured Silicon) Sector Flash Memory Region" for further information. *Note that the ACC function and unlock bypass modes are not available when the SecSi Sector is enabled.*

Word Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 12 and Table 13 show the address and data requirements for the word program command sequence.

When the Embedded Program algorithm is complete, the device then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7 or DQ6. Refer to the Write Operation Status section for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. ***Note that the SecSi Sector, autoselect, and CFI functions are unavailable when a program operation is in progress.*** Note that a **hardware reset** immediately terminates the program operation. The program command sequence should be reinitiated once the device has returned to the read mode, to ensure data integrity.

Programming is allowed in any sequence of address locations and across sector boundaries. Programming to the same word address multiple times without intervening erases (incremental bit programming) requires a modified programming method. For such application requirements, please contact your local Spansion representative. Word programming is supported for backward

compatibility with existing Flash driver software and for occassional writng of individual words. Use of Write Buffer Programming is strongly recommended for general programming use when more than a few words are to be programmed. The effective word programming time using Write Buffer Programming is much shorter than the single word programming time. **Any word cannot be programmed from "0" back to a "1."** Attempting to do so may cause the device to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still "0." Only erase operations can convert a "0" to a "1."

Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 12 and Table 13 show the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. (See Table 12 and Table 13).

Write Buffer Programming

Write Buffer Programming allows the system write to a maximum of 16 words/32 bytes in one programming operation. This results in faster effective programming time than the standard programming algorithms. The Write Buffer Programming command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the Write Buffer Load command written at the Sector Address in which programming will occur. The fourth cycle writes the sector address and the number of word locations, minus one, to be programmed. For example, if the system will program 6 unique address locations, then 05h should be written to the device. This tells the device how many write buffer addresses will be loaded with data and therefore when to expect the Program Buffer to Flash command. The number of locations to program cannot exceed the size of the write buffer or the operation will abort.

The fifth cycle writes the first address location and data to be programmed. The write-buffer-page is selected by address bits A_{MAX}–A_4. All subsequent address/data pairs must fall within the selected-write-buffer-page. The system then writes the remaining address/data pairs into the write buffer. Write buffer locations may be loaded in any order.

The write-buffer-page address must be the same for all address/data pairs loaded into the write buffer. (This means Write Buffer Programming cannot be performed across multiple write-buffer pages. This also means that Write Buffer Programming cannot be performed across multiple sectors. If the system attempts to load programming data outside of the selected write-buffer page, the operation will abort.)

Note that if a Write Buffer address location is loaded multiple times, the address/data pair counter will be decremented for every data load operation. The host system must therefore account for loading a write-buffer location more than once. The counter decrements for each data load operation, not for each unique write-buffer-address location. Note also that if an address location is loaded more than once into the buffer, the final data loaded for that address will be programmed.

Once the specified number of write buffer locations have been loaded, the system must then write the Program Buffer to Flash command at the sector address. Any other address and data combination aborts the Write Buffer Programming operation. The device then begins programming. Data polling should be used while monitoring the last address location loaded into the write buffer. DQ7, DQ6, DQ5, and DQ1 should be monitored to determine the device status during Write Buffer Programming.

The write-buffer programming operation can be suspended using the standard program suspend/resume commands. Upon successful completion of the Write Buffer Programming operation, the device is ready to execute the next command.

The Write Buffer Programming Sequence can be aborted in the following ways:

- Load a value that is greater than the page buffer size during the Number of Locations to Program step.
- Write to an address in a sector different than the one specified during the Write-Buffer-Load command.
- Write an Address/Data pair to a different write-buffer-page than the one selected by the Starting Address during the write buffer data loading stage of the operation.
- Write data other than the Confirm Command after the specified number of data load cycles.

The abort condition is indicated by DQ1 = 1, DQ7 = DATA# (for the last address location loaded), DQ6 = toggle, and DQ5=0. A Write-to-Buffer-Abort Reset command sequence must be written to reset the device for the next operation. Note that the full 3-cycle Write-to-Buffer-Abort Reset command sequence is required when using Write-Buffer-Programming features in Unlock Bypass mode.

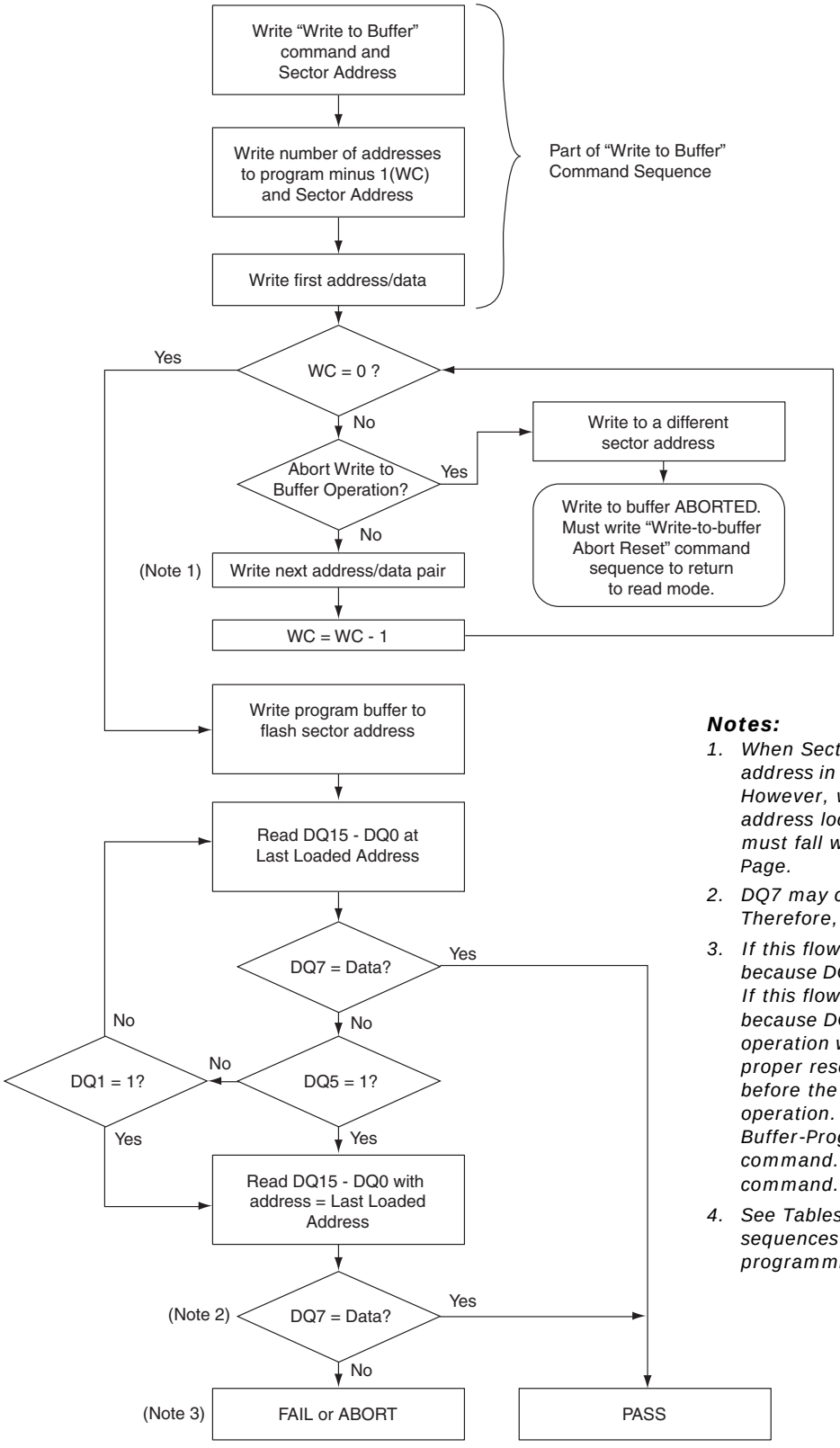
Write buffer programming is allowed in any sequence. Note that the SecSi sector, autoselect, and CFI functions are unavailable when a program operation is in progress. This flash device is capable of handling multiple write buffer programming operations on the same write buffer address range without intervening erases. For applications requiring incremental bit programming, a modified programming method is required, please contact your local Spansion representative. **Any bit in a write buffer address range cannot be programmed from "0" back to a "1."** Attempting to do so may cause the device to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still "0." Only erase operations can convert a "0" to a "1."

Accelerated Program

The device offers accelerated program operations through the WP#/ACC pin. When the system asserts V_{HH} on the WP#/ACC pin, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the WP#/ACC pin to accelerate the operation. *Note that the* WP#/*ACC pin must not*

be at V_{HH} for operations other than accelerated programming, or device damage may result. WP# has an internal pullup; when unconnected, WP# is at V_{IH}.

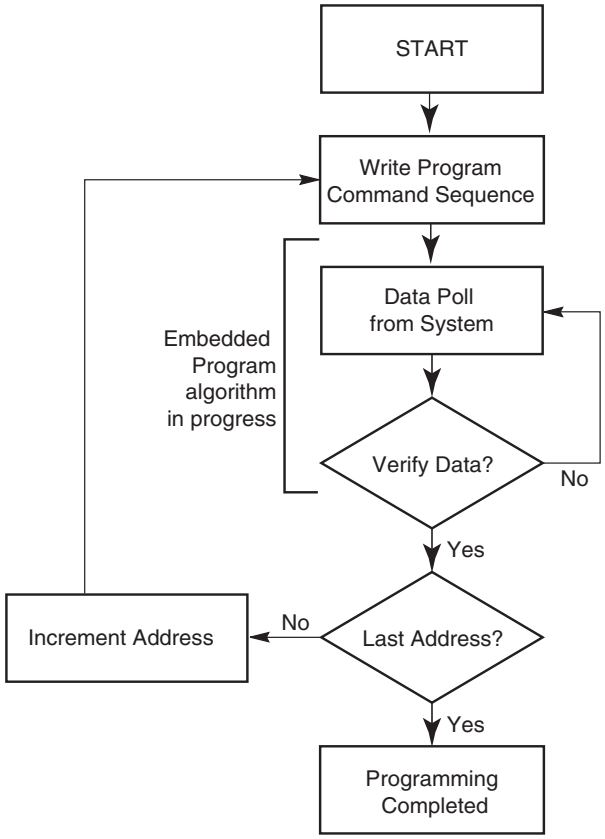
Figure 3 illustrates the algorithm for the program operation. Refer to the Erase and Program Operations–"AC Characteristics" section on page 88 section for parameters, and Figure 14 for timing diagrams.



Notes:

1. *When Sector Address is specified, any address in the selected sector is acceptable. However, when loading Write-Buffer address locations with data, all addresses must fall within the selected Write-Buffer Page.*
2. *DQ7 may change simultaneously with DQ5. Therefore, DQ7 should be verified.*
3. *If this flowchart location was reached because DQ5= "1", then the device FAILED. If this flowchart location was reached because DQ1= "1", then the Write to Buffer operation was ABORTED. In either case, the proper reset command must be written before the device can begin another operation. If DQ1=1, write the Write-Buffer-Programming-Abort-Reset command. if DQ5=1, write the Reset command.*
4. *See Tables 16 and 17 for command sequences required for write buffer programming.*

Figure I. Write Buffer Programming Operation



Note: *See Table 12 and Table 13 for program command sequence.*

Figure 2. Program Operation

Program Suspend/Program Resume Command Sequence

The Program Suspend command allows the system to interrupt a programming operation or a Write to Buffer programming operation so that data can be read from any non-suspended sector. When the Program Suspend command is written during a programming process, the device halts the program operation within 15 µs maximum (5µs typical) and updates the status bits. Addresses are not required when writing the Program Suspend command.

After the programming operation has been suspended, the system can read array data from any non-suspended sector. The Program Suspend command may also be issued during a programming operation while an erase is suspended. In this case, data may be read from any addresses not in Erase Suspend or Program Suspend. If a read is needed from the SecSi Sector area (One-time Program area), then user must use the proper command sequences to enter and exit this region. *Note that the SecSi Sector autoselect, and CFI functions are unavailable when program operation is in progress.*

The system may also write the autoselect command sequence when the device is in the Program Suspend mode. The system can read as many autoselect codes as required. When the device exits the autoselect mode, the device reverts to the Program Suspend mode, and is ready for another valid operation. See Autoselect Command Sequence for more information.

After the Program Resume command is written, the device reverts to programming. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See Write Operation Status for more information.

The system must write the Program Resume command (address bits are don't care) to exit the Program Suspend mode and continue the programming operation. Further writes of the Resume command are ignored. Another Program Suspend command can be written after the device has resume programming.

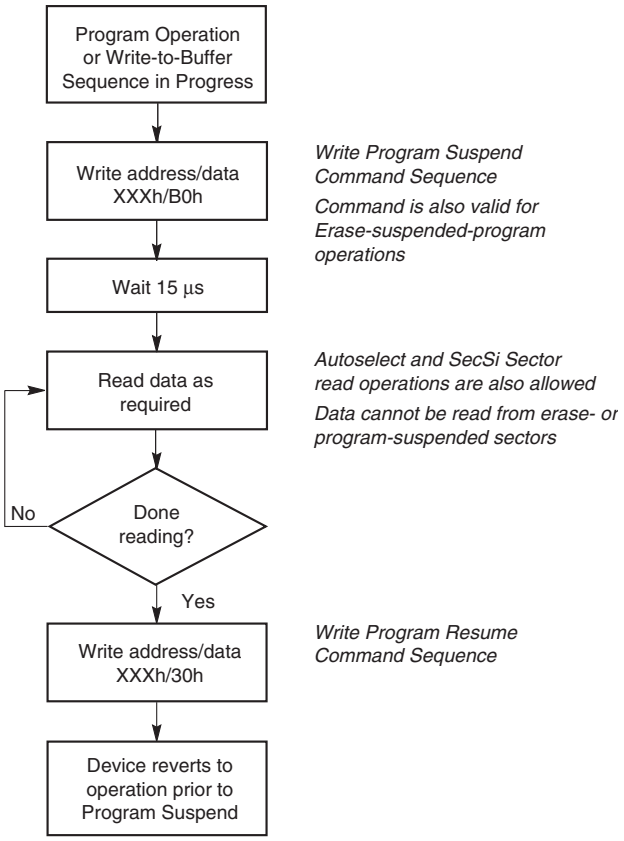


Figure 3. Program Suspend/Program Resume

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 12 and Table 13 show the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, the device returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. Refer to the Write Operation Status section for information on these status bits.

Any commands written during the chip erase operation are ignored, including erase suspend commands. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

Figure 4 illustrates the algorithm for the erase operation. ***Note that the SecSi Sector, autoselect, and CFI functions are unavailable when an erase operation in is progress.*** Refer to the Erase and Program Operations table in the AC Characteristics section for parameters, and Figure 16 section for timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 12 and Table 13 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

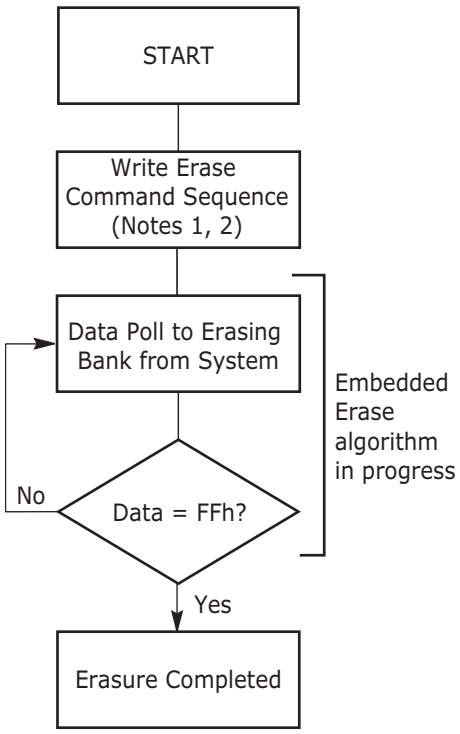
After the command sequence is written, a sector erase time-out of 50 µs occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. **Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to the read mode.** ***Note that the SecSi Sector, autoselect, and CFI functions are unavailable when an erase operation in is progress.*** The system must rewrite the command sequence and any additional addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out (See the section on DQ3: Sector Erase Timer.). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by reading DQ7, DQ6, or DQ2 in the erasing sector. Refer to the Write Operation Status section for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

Figure 4 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations table in the AC Characteristics section for parameters, and Figure 16 section for timing diagrams.



Notes:

1. *See Table 12 and Table 13 for program command sequence.*
2. *See the section on DQ3 for information on the sector erase timer.*

Figure 4. Erase Operation

Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

When the Erase Suspend command is written during the sector erase operation, the device requires a typical of 5 µs (maximum of 20 µs) to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the device enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to the Write Operation Status section for information on these status bits.

After an erase-suspended program operation is complete, the device returns to the erase-suspend-read mode. The system can determine the status of the pro-

gram operation using the DQ7 or DQ6 status bits, just as in the standard word program operation. Refer to the Write Operation Status section for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. Refer to the Autoselect Mode section and “Autoselect Command Sequence” section on page 58 sections for details.

To resume the sector erase operation, the system must write the Erase Resume command. The address of the erase-suspended sector is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing. It is important to allow an intervalof at least 5 ns between Erase Resume and Erase Suspend.

Lock Register Command Set Definitions

The Lock Register Command Set permits the user to one-time program the SecSi Sector Protection Bit, Persistent Protection Mode Lock Bit, and Password Protection Mode Lock Bit. The Lock Register bits are all readable after an initial access delay.

The **Lock Register Command Set Entry** command sequence must be issued prior to any of the following commands listed, to enable proper command execution.

Note that issuing the **Lock Register Command Set Entry** command **disables reads and writes for the flash memory**.

- Lock Register Program Command
- Lock Register Read Command

The **Lock Register Command Set Exit** command must be issued after the execution of the commands to reset the device to read mode. Otherwise the device will hang. If this happens, the flash device must be reset. Please refer to RESET# for more information. It is important to note that the device will be in either Persistent Protection mode or Password Protection mode depending on the mode selected prior to the device hang.

For either the SecSi Sector to be locked, or the device to be permanently set to the Persistent Protection Mode or the Password Protection Mode, the associated Lock Register bits must be programmed. **Note that the Persistent Protection Mode Lock Bit and Password Protection Mode Lock Bit can never be programmed together at the same time. If so, the Lock Register Program operation will abort**.

The Lock Register Command Set Exit command must be initiated to re-enable reads and writes to the main memory.

Password Protection Command Set Definitions

The Password Protection Command Set permits the user to program the 64-bit password, verify the programming of the 64-bit password, and then later unlock the device by issuing the valid 64-bit password.

The **Password Protection Command Set Entry** command sequence must be issued prior to any of the commands listed following to enable proper command execution.

Note that issuing the **Password Protection Command Set Entry** command **disabled reads and writes the main memory.**

- **Password Program Command**
- **Password Read Command**
- **Password Unlock Command**

The Password Program command permits programming the password that is used as part of the hardware protection scheme. The actual password is 64-bits long. There is no special addressing order required for programming the password. **The password is programmed in 8-bit or 16-bit portions. Each portion requires a Password Program Command.**

Once the Password is written and verified, the Password Protection Mode Lock Bit in the "Lock Register" must be programmed in order to prevent verification. The Password Program command is only capable of programming "0"s. Programming a "1" after a cell is programmed as a "0" results in a time-out by the Embedded Program Algorithm™ with the cell remaining as a "0". The password is all F's when shipped from the factory. All 64-bit password combinations are valid as a password.

The Password Read command is used to verify the Password. The Password is verifiable only when the Password Protection Mode Lock Bit in the "Lock Register" is not programmed. If the Password Protection Mode Lock Bit in the "Lock Register" is programmed and the user attempts to read the Password, the device will always drive all F's onto the DQ databus.

The lower two address bits (A1–A0) for word mode and (A1–A-1) for by byte mode are valid during the Password Read, Password Program, and Password Unlock commands. **Writing a "1" to any other address bits (A_{MAX}-A2) will abort the Password Read and Password Program commands.**

The Password Unlock command is used to clear the PPB Lock Bit to the "unfreeze state" so that the PPB bits can be modified. The exact password must be entered in order for the unlocking function to occur. **This 64-bit Password Unlock command sequence will take at least 2 µs to process each time to prevent a hacker from running through the all 64-bit combinations in an attempt to correctly match the password. If another password unlock is issued before the 64-bit password check execution window is completed, the command will be ignored. If the wrong address or data is given during password unlock command cycle, the device may enter the write-to-buffer abort state. In order to exit the write-to-abort state, the write-to-buffer-abort-reset command must be given. Otherwise the device will hang.**

The Password Unlock function is accomplished by writing Password Unlock command and data to the device to perform the clearing of the PPB Lock Bit to the "unfreeze state". The password is 64 bits long. A1 and A0 are used for matching in word mode and A1, A0, A-1 in byte mode. Writing the Password Unlock command does not need to be address order specific. An example sequence is starting with the lower address A1-A0=00, followed by A1-A0=01, A1-A0=10, and A1-A0=11 if the device is configured to operate in word mode.

Approximately 2 µs is required for unlocking the device after the valid 64-bit password is given to the device. It is the responsibility of the microprocessor to keep track of the entering the portions of the 64-bit password with the Password Unlock command, the order, and when to read the PPB Lock bit to confirm successful password unlock. In order to re-lock the device into the Password Protection Mode, the PPB Lock Bit Set command can be re-issued.

The **Password Protection Command Set Exit** command must be issued after the execution of the commands listed previously to reset the device to read mode. Otherwise the device will hang.
Note that issuing the **Password Protection Command Set Exit command re-enables reads and writes for the main memory.**

Non-Volatile Sector Protection Command Set Definitions

The Non-Volatile Sector Protection Command Set permits the user to program the Persistent Protection Bits (PPB bits), erase all of the Persistent Protection Bits (PPB bits), and read the logic state of the Persistent Protection Bits (PPB bits).

The **Non-Volatile Sector Protection Command Set Entry** command sequence must be issued prior to any of the commands listed following to enable proper command execution.

Note that issuing the **Non-Volatile Sector Protection Command Set Entry** command **disables reads and writes for the main memory**.

- PPB Program Command

The PPB Program command is used to program, or set, a given PPB bit. Each PPB bit is individually programmed (but is bulk erased with the other PPB bits). The specific sector address (A24-A16 for S29GL512N, A23-A16 for S29GL256N, A22-A16 for S29GL128N) is written at the same time as the program command. If the PPB Lock Bit is set to the “freeze state”, the PPB Program command will not execute and the command will time-out without programming the PPB bit.

- All PPB Erase Command

The All PPB Erase command is used to erase all PPB bits in bulk. There is no means for individually erasing a specific PPB bit. Unlike the PPB program, no specific sector address is required. However, when the All PPB Erase command is issued, all Sector PPB bits are erased in parallel. If the PPB Lock Bit is set to “freeze state”, the ALL PPB Erase command will not execute and the command will time-out without erasing the PPB bits.

The device will preprogram all PPB bits prior to erasing when issuing the All PPB Erase command. Also note that the total number of PPB program/erase cycles has the same endurance as the flash memory array.

- PPB Status Read Command

The programming state of the PPB for a given sector can be verified by writing a PPB Status Read Command to the device. This requires an initial access time latency.

The **Non-Volatile Sector Protection Command Set Exit** command must be issued after the execution of the commands listed previously to reset the device to read mode.

Note that issuing the **Non-Volatile Sector Protection Command Set Exit** command **re-enables reads and writes for the main memory**.

Global Volatile Sector Protection Freeze Command Set

The Global Volatile Sector Protection Freeze Command Set permits the user to set the PPB Lock Bit and reading the logic state of the PPB Lock Bit.

The **Global Volatile Sector Protection Freeze Command Set Entry** command sequence must be issued prior to any of the commands listed following to enable proper command execution.

Reads and writes from the main memory are allowed.

- PPB Lock Bit Set Command

The PPB Lock Bit Set command is used to set the PPB Lock Bit to the “freeze state” if it is cleared either at reset or if the Password Unlock command was successfully executed. There is no PPB Lock Bit Clear command. Once the PPB Lock Bit is set to the “freeze state”, it cannot be cleared unless the device is taken through a power-on clear (for Persistent Protection Mode) or the Password Unlock command is executed (for Password Protection Mode). If the Password Protection Mode Lock Bit is programmed, the PPB Lock Bit status is reflected as set to the “freeze state”, even after a power-on reset cycle.

- PPB Lock Bit Status Read Command

The programming state of the PPB Lock Bit can be verified by executing a PPB Lock Bit Status Read command to the device.

The **Global Volatile Sector Protection Freeze Command Set Exit** command must be issued after the execution of the commands listed previously to reset the device to read mode.

Volatile Sector Protection Command Set

The Volatile Sector Protection Command Set permits the user to set the Dynamic Protection Bit (DYB) to the “protected state”, clear the Dynamic Protection Bit (DYB) to the “unprotected state”, and read the logic state of the Dynamic Protection Bit (DYB).

The **Volatile Sector Protection Command Set Entry** command sequence must be issued prior to any of the commands listed following to enable proper command execution.

Note that issuing the **Volatile Sector Protection Command Set Entry** command **disables reads for the bank selected with the command**. **Reads and Writes for other banks excluding that bank are allowed**.

- DYB Set Command
- DYB Clear Command

The DYB Set and DYB Clear commands are used to protect or unprotect a DYB for a given sector. The high order address bits are issued at the same time as the code 00h or 01h on DQ7-DQ0. All other DQ data bus pins are ignored during the data write cycle. The DYB bits are modifiable at any time, regardless of the state of the PPB bit or PPB Lock Bit. The DYB bits are cleared to the “unprotected state” at power-up or hardware reset.

—DYB Status Read Command

The programming state of the DYB bit for a given sector can be verified by writing a DYB Status Read command to the device. This requires an initial access delay.

The **Volatile Sector Protection Command Set Exit** command must be issued after the execution of the commands listed previously to reset the device to read mode.

Note that issuing the **Volatile Sector Protection Command Set Exit command re-enables reads and writes to the main memory**.

SecSi Sector Entry Command

The SecSi Sector Entry command allows the following commands to be executed

- Read from SecSi Sector

- Program to SecSi Sector

Once the SecSi Sector Entry Command is issued, the SecSi Sector Exit command has to be issued to exit SecSi Sector Mode.

SecSi Sector Exit Command

The SecSi Sector Exit command may be issued to exit the SecSi Sector Mode.

Command Definitions

Table 12. S29GL512N, S29GL256N, S29GL128N Command Definitions, x16

Command (Notes)		Cycles	Bus Cycles (Notes 2–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (6)		1	RA	RD										
Reset (7)		1	XXX	F0										
Autoselect (Note 8)	Manufacturer ID	4	555	AA	2AA	55	555	90	X00	01				
	Device ID	4	555	AA	2AA	55	555	90	X01	227E	X0E	Note 17	X0F	Note 17
	Sector Protect Verify	4	555	AA	2AA	55	555	90	(SA) X02	XX00				
										XX01				
	Secure Device Verify (9)	4	555	AA	2AA	55	555	90	X03	Note 10				
CFI Query (11)		1	55	98										
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Write to Buffer		3	555	AA	2AA	55	SA	25	SA	WC	PA	PD	WBL	PD
Program Buffer to Flash (confirm)		1	SA	29										
Write-to-Buffer-Abort Reset (16)		3	555	AA	2AA	55	555	F0						
Unlock Bypass		3	555	AA	2AA	55	555	20						
Unlock Bypass Program (12)		2	XXX	A0	PA	PD								
Unlock Bypass Sector Erase (12)		2	XXX	80	SA	30								
Unlock Bypass Chip Erase (12)		2	XXX	80	XXX	10								
Unlock Bypass Reset (13)		2	XXX	90	XXX	00								
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase Suspend/Program Suspend (14)		1	XXX	B0										
Erase Resume/Program Resume (15)		1	XXX	30										
Sector Command Definitions														
SecSi™ SEctor	SecSi Sector Entry	3	555	AA	2AA	55	555	88						
	SecSi Sector Exit (18)	4	555	AA	2AA	55	555	90	XX	00				
Lock Register Command Set Definitions														
Lock Register	Lock Register Command Set Entry	3	555	AA	2AA	55	555	40						
	Lock Register Bits Program (22)	2	XXX	A0	XXX	Data								
	Lock Register Bits Read (22)	1	00	Data										
	Lock Register Command Set Exit (18, 23)	2	XXX	90	XXX	00								
Password Protection Command Set Definitions														

Command (Notes)		Cycles	Bus Cycles (Notes 2–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Password	Password Protection Command Set Entry	3	555	AA	2AA	55	555	60						
	Password Program (20)	2	XXX	A0	PWA x	PWD x								
	Password Read (19)	4	XXX	PWD 0	01	PWD 1	02	PWD 2	03	PWD 3				
	Password Unlock (19)	7	00	25	00	03	00	PWD 0	01	PWD 1	02	PWD 2	03	PWD 3
			00	29										
	Password Protection Command Set Exit (18, 23)	2	XXX	90	XXX	00								
Non-Volatile Sector Protection Command Set Definitions														
PPB	Nonvolatile Sector Protection Command Set Entry	3	555	AA	2AA	55	555	C0						
	PPB Program (24, 25)	2	XXX	A0	SA	00								
	All PPB Erase	2	XXX	80	00	30								
	PPB Status Read (25)	1	SA	RD (0)										
	Non-Volatile Sector Protection Command Set Exit (18)	2	XXX	90	XXX	00								
Global Non-Volatile Sector Protection Freeze Command Set Definitions														
PPB Lock Bit	Global Non-Volatile Sector Protection Freeze Command Set Entry	3	555	AA	2AA	55	555	50						
	PPB Lock Bit Set (25)	2	XXX	A0	XXX	00								
	PPB Lock Status Read (25)	1	XXX	RD (0)										
	Global Non-Volatile Sector Protection Freeze Command Set Exit (18)	2	XXX	90	XXX	00								
Volatile Sector Protection Command Set Definitions														
DYB	Volatile Sector Protection Command Set Entry	3	555	AA	2AA	55	555	E0						
	DYB Set (24, 25)	2	XXX	A0	SA	00								
	DYB Clear (25)	2	XXX	A0	SA	01								
	DYB Status Read (25)	1	SA	RD (0)										
	Volatile Sector Protection Command Set Exit (18)	2	XXX	90	XXX	00								

Legend:

X = Don't care

RA = Address of the memory to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of the WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A_{max}–A16 uniquely select any sector.

WBL = Write Buffer Location. The address must be within the same write buffer page as PA.

WC = Word Count is the number of write buffer locations to load minus 1.

PWD = Password

PWD_X = Password word0, word1, word2, and word3.

DATA = Lock Register Contents: PD(0) = SecSi Sector Protection Bit, PD(1) = Persistent Protection Mode Lock Bit, PD(2) = Password Protection Mode Lock Bit.

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the read cycle, and the 4th, 5th, and 6th cycle of the autoselect command sequence, all bus cycles are write cycles.*
4. *Data bits DQ15-DQ8 are don't cares for unlock and command cycles.*
5. *Address bits A_{MAX}:A16 are don't cares for unlock and command cycles, unless SA or PA required. (A_{MAX} is the Highest Address pin.).*
6. *No unlock or command cycles required when reading array data.*
7. *The Reset command is required to return to reading array data when device is in the autoselect mode, or if DQ5 goes high (while the device is providing status data).*
8. *The fourth, fifth, and sixth cycle of the autoselect command sequence is a read cycle.*
9. *The data is 00h for an unprotected sector and 01h for a protected sector. See "Autoselect Command Sequence" for more information. This is same as PPB Status Read except that the protect and unprotect statuses are inverted here.*
10. *The data value for DQ7 is "1" for a serialized and protected OTP region and "0" for an unserialized and unprotected SecSi™Sector region. See "SecSi™Sector Flash Memory Region" for more information. For S29GLVxxxNH: XX18h/18h = Not Factory Locked. XX98h/98h = Factory Locked. For S29GLxxxNL: XX08h/08h = Not Factory Locked. XX88h/88h = Factory Locked.*
11. *Command is valid when device is ready to read array data or when device is in autoselect mode.*
12. *The Unlock-Bypass command is required prior to the Unlock-Bypass-Program command.*
13. *The Unlock-Bypass-Reset command is required to return to reading array data when the device is in the unlock bypass mode.*
14. *The system may read and program/program suspend in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
15. *The Erase Resume/Program Resume command is valid only during the Erase Suspend/Program Suspend modes.*
16. *Issue this command sequence to return to READ mode after detecting device is in a Write-to-Buffer-Abort state. NOTE: the full command sequence is required if resetting out of ABORT while using Unlock Bypass Mode.*
17. *S29GL512NH/L = 2223h/23h, 220h/01h; S29GL256NH/L = 2222h/22h, 2201h/01h; S29GL128NH/L = 2221h/21h, 2201h/01h.*
18. *The Exit command returns the device to reading the array.*
19. *Note that the password portion can be entered or read in any order as long as the entire 64-bit password is entered or read.*
20. *For PWDx, only one portion of the password can be programmed per each "A0" command.*
21. *The All PPB Erase command embeds programming of all PPB bits before erasure.*
22. *All Lock Register bits are one-time programmable. Note that the program state = "0" and the erase state = "1". Also note that of both the Persistent Protection Mode Lock Bit and the Password Protection Mode Lock Bit cannot be programmed at the same time or the Lock Register Bits Program operation will abort and return the device to read mode. Lock Register bits that are reserved for future use will default to "1's". The Lock Register is shipped out as "FFFF's" before Lock Register Bit program execution.*
23. *If any of the Entry command was initiated, an Exit command must be issued to reset the device into read mode. Otherwise the device will hang.*
24. *If ACC = V_{HH}, sector protection will match when ACC = V_{IH}*
25. *Protected State = "00h", Unprotected State = "01h".*

Table 13. S29GL512N, S29GL256N, S29GL128N Command Definitions, x8

Command (Notes)		Cycles	Bus Cycles (Notes 2–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (6)		1	RA	RD										
Reset (7)		1	XXX	F0										
Autoselect	Manufacturer ID	4	AAA	AA	555	55	AAA	90	X00	01				
	Device ID	4	AAA	AA	555	55	AAA	90	X02	XX7E	X1C	Note 17	X1E	Note 17
	Sector Protect Verify	4	AAA	AA	555	55	AAA	90	(SA) X04	00				
										01				
	Secure Device Verify (9)	4	AAA	AA	555	55	AAA	90	X06	Note 10				
CFI Query (11)		1	AA	98										
Write to Buffer		3	AAA	AA	555	55	SA	25	SA	WC	PA	PD	WBL	PD
Program Buffer to Flash (confirm)		1	SA	29										
Write-to-Buffer-Abort Reset (16)		3	AAA	AA	PA	55	555	F0						
Chip Erase		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10
Sector Erase		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	SA	30
Erase Suspend/Program Suspend (14)		1	XXX	B0										
Erase Resume/Program Resume (15)		1	XXX	30										
SecSi Sector Command Definitions														
SecSi™ SEctor	SecSi Sector Entry	3	AAA	AA	555	55	AAA	88						
	SecSi Sector Exit (18)	4	AAA	AA	555	55	AAA	90	XX	00				
Lock Register Command Set Definitions														
Lock Register	Lock Register Command Set Entry	3	AAA	AA	555	55	AAA	40						
	Lock Register Bits Program (22)	2	XXX	A0	XXX	Data								
	Lock Register Bits Read (22)	1	00	Data										
	Lock Register Command Set Exit (18, 23)	2	XXX	90	XXX	00								
Password Protection Command Set Definitions														
Password	Password Protection Command Set Entry	3	AAA	AA	555	55	AAA	60						
	Password Program (20)	2	XXX	A0	PWA x	PWD x								
	Password Read (19)	8	00	PWD 0	01	PWD 1	02	PWD 2	03	PWD 3	04	PWD 4	05	PWD 5
			06	PWD 6	07	PWD 7								
	Password Unlock (19)	11	00	25	00	03	00	PWD 0	01	PWD 1	02	PWD 2	03	PWD 3
			04	PWD 4	05	PWD 5	06	PWD 6	07	PWD 7	00	29		
	Password Protection Command Set Exit (18, 23)	2	XXX	90	XXX	00								

Command (Notes)		Cycles	Bus Cycles (Notes 2–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Non-Volatile Sector Protection Command Set Definitions														
PPB	Nonvolatile Sector Protection Command Set Entry	3	AAA	AA	55	55	AAA	C0						
	PPB Program (24, 25)	2	XXX	A0	SA	00								
	All PPB Erase	2	XXX	80	00	30								
	PPB Status Read (25)	1	SA	RD (0)										
	Non-Volatile Sector Protection Command Set Exit (18)	2	XXX	90	XXX	00								
Global Non-Volatile Sector Protection Freeze Command Set Definitions														
PPB Lock Bit	Global Non-Volatile Sector Protection Freeze Command Set Entry	3	AAA	AA	555	55	AAA	50						
	PPB Lock Bit Set (25)	2	XXX	A0	XXX	00								
	PPB Lock Status Read (25)	1	XXX	RD (0)										
	Global Non-Volatile Sector Protection Freeze Command Set Exit (18)	2	XXX	90	XXX	00								
Volatile Sector Protection Command Set Definitions														
DYB	Volatile Sector Protection Command Set Entry	3	AAA	AA	555	55	AAA	E0						
	DYB Set (24, 25)	2	XXX	A0	SA	00								
	DYB Clear (25)	2	XXX	A0	SA	01								
	DYB Status Read (25)	1	SA	RD (0)										
	Volatile Sector Protection Command Set Exit (18)	2	XXX	90	XXX	00								

Legend:

X = Don't care

RA = Address of the memory to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of the WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A_{max}–A16 uniquely select any sector.

WBL = Write Buffer Location. The address must be within the same write buffer page as PA.

WC = Word Count is the number of write buffer locations to load minus 1.

PWD = Password

PWD_x = Password word0, word1, word2, word3. word 4, word 5, word 6, and word 7.

DATA = Lock Register Contents: PD(0) = SecSi Sector Protection Bit, PD(1) = Persistent Protection Mode Lock Bit, PD(2) = Password Protection Mode Lock Bit.

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the read cycle, and the 4th, 5th, and 6th cycle of the autoselect command sequence, all bus cycles are write cycles.*

4. *Data bits DQ15-DQ8 are don't cares for unlock and command cycles.*
5. *Address bits A_{MAX}:A16 are don't cares for unlock and command cycles, unless SA or PA required. (A_{MAX} is the Highest Address pin.).*
6. *No unlock or command cycles required when reading array data.*
7. *The Reset command is required to return to reading array data when device is in the autoselect mode, or if DQ5 goes high (while the device is providing status data).*
8. *The fourth, fifth, and sixth cycle of the autoselect command sequence is a read cycle.*
9. *The data is 00h for an unprotected sector and 01h for a protected sector. See "Autoselect Command Sequence" for more information. This is same as PPB Status Read except that the protect and unprotect statuses are inverted here.*
10. *The data value for DQ7 is "1" for a serialized and protected OTP region and "0" for an unserialized and unprotected SecSi™ Sector region. See "SecSi™ Sector Flash Memory Region" for more information. For S29GLxxxNH.: XX18h/18h = Not Factory Locked. XX98h/98h = Factory Locked. For S29GLxxxNL: XX08h/08h = Not Factory Locked. XX88h/88h = Factory Locked.*
11. *Command is valid when device is ready to read array data or when device is in autoselect mode.*
12. *The system may read and program/program suspend in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
13. *The Erase Resume/Program Resume command is valid only during the Erase Suspend/Program Suspend modes.*
14. *Issue this command sequence to return to READ mode after detecting device is in a Write-to-Buffer-Abort state. NOTE: the full command sequence is required if resetting out of ABORT while using Unlock Bypass Mode.*
15. *S29GL512NH/L = 2223h/23h, 220h/01h; S29GL256NH/L = 2222h/22h, 2201h/01h; S29GL128NH/L = 2221h/21h, 2201h/01h.*
16. *The Exit command returns the device to reading the array.*
17. *Note that the password portion can be entered or read in any order as long as the entire 64-bit password is entered or read.*
18. *For PWDx, only one portion of the password can be programmed per each "A0" command.*
19. *The All PPB Erase command embeds programming of all PPB bits before erasure.*
20. *All Lock Register bits are one-time programmable. Note that the program state = "0" and the erase state = "1". Also note that of both the Persistent Protection Mode Lock Bit and the Password Protection Mode Lock Bit cannot be programmed at the same time or the Lock Register Bits Program operation will abort and return the device to read mode. Lock Register bits that are reserved for future use will default to "1's". The Lock Register is shipped out as "FFFF's" before Lock Register Bit program execution.*
21. *If any of the Entry command was initiated, an Exit command must be issued to reset the device into read mode. Otherwise the device will hang.*
22. *If ACC = V_{HH}, sector protection will match when ACC = V_{IH}*

Protected State = "00h", Unprotected State = "01h".

Write Operation Status

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 19 and the following subsections describe the function of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. The device also provides a hardware-based output signal, RY/BY#, to determine whether an Embedded Program or Erase operation is in progress or has been completed.

Note that all Write Operation Status DQ bits are valid only after 4 µs delay.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a pro-

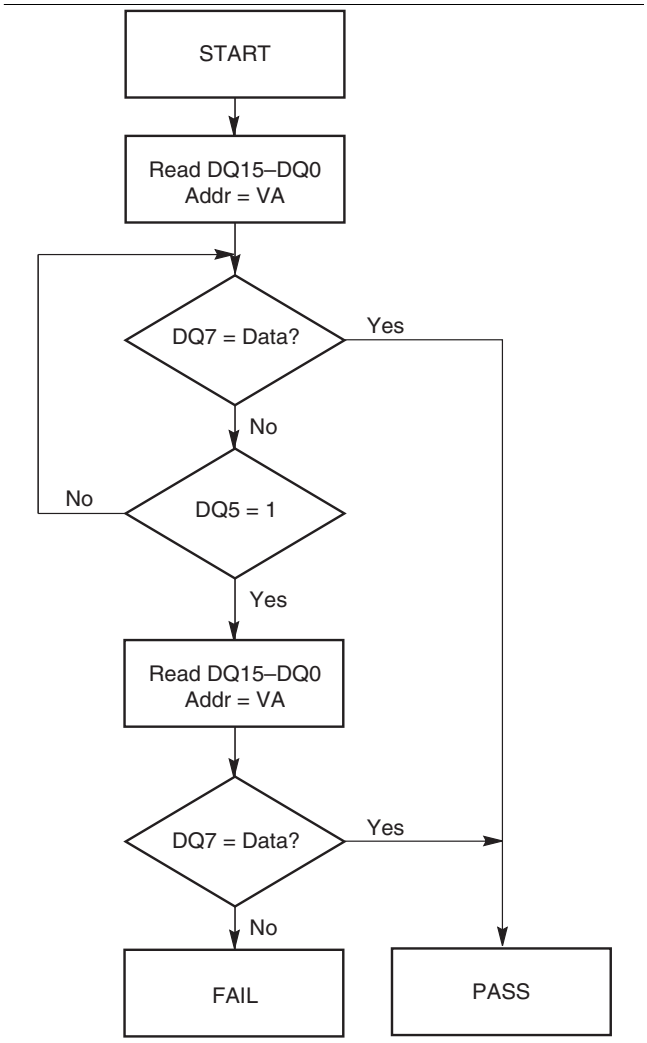
gram address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then the device returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a “1” on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the device returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ0–DQ6 may be still invalid. Valid data on DQ0–DQ7 will appear on successive read cycles.

Table 14 shows the outputs for Data# Polling on DQ7. Figure 5 shows the Data# Polling algorithm. Figure 17 in the AC Characteristics section shows the Data# Polling timing diagram.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.*

Figure 5. Data# Polling Algorithm

RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin which indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is in the read mode, the standby mode, or in the erase-suspend-read mode. Table 14 shows the outputs for RY/BY#.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, DQ6 stops toggling.

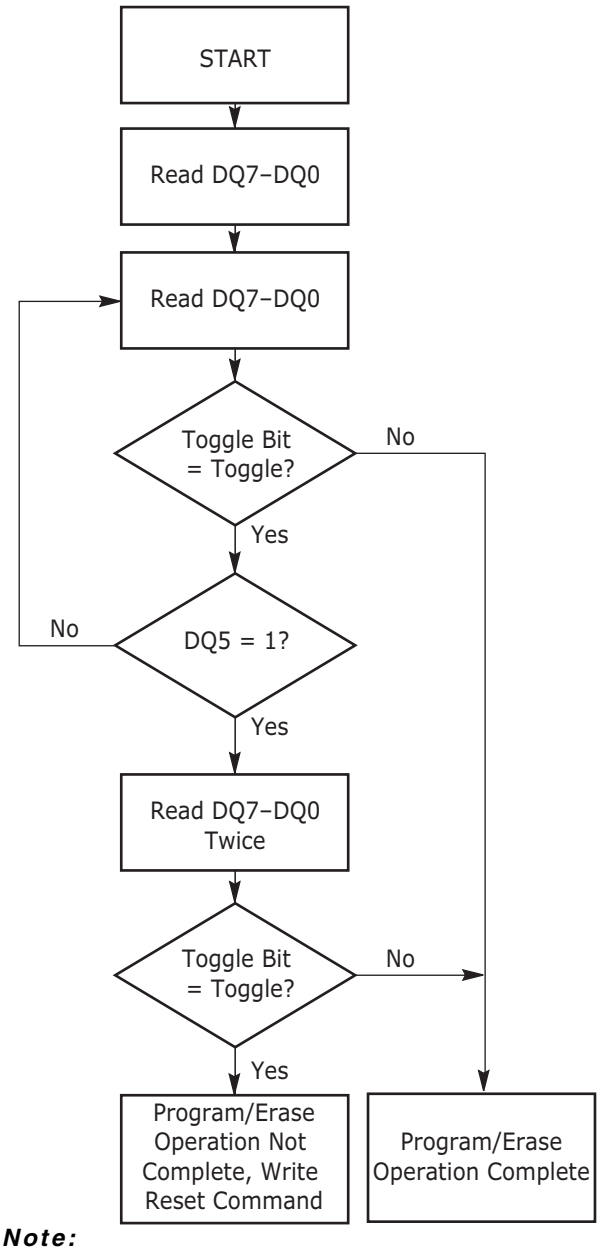
After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 14 shows the outputs for Toggle Bit I on DQ6. Figure 6 shows the toggle bit algorithm. Figure 18 in the “AC Characteristics” section shows the toggle bit timing diagrams. Figure 19 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on DQ2: Toggle Bit II.



Note:
The system should recheck the toggle bit even if DQ5 = "1" because the toggle bit may stop toggling as DQ5 changes to "1." See the subsections on DQ6 and DQ2 for more information.

Figure 6. Toggle Bit Algorithm

DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the

read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 14 to compare outputs for DQ2 and DQ6.

Figure 6 shows the toggle bit algorithm in flowchart form, and the section "DQ2: Toggle Bit II" explains the algorithm. See also the RY/BY#: Ready/Busy# subsection. Figure 18 shows the toggle bit timing diagram. Figure 19 shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 6 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 6).

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program, erase, or write-to-buffer time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1," indicating that the program or erase cycle was not successfully completed.

The device may output a "1" on DQ5 if the system tries to program a "1" to a location that was previously programmed to "0." **Only an erase operation can change a "0" back to a "1."** Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a "1."

In all these cases, the system must write the reset command to return the device to the reading the array (or to erase-suspend-read if the device was previously in the erase-suspend-program mode).

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command.

When the time-out period is complete, DQ3 switches from a “0” to a “1.” If the time between additional sector erase commands from the system can be assumed to be less than 50 µs, the system need not monitor DQ3. See also the Sector Erase Command Sequence section.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is “1,” the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is “0,” the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 14 shows the status of DQ3 relative to the other status bits.

DQI: Write-to-Buffer Abort

DQ1 indicates whether a Write-to-Buffer operation was aborted. Under these conditions DQ1 produces a “1”. The system must issue the Write-to-Buffer-Abort-Reset command sequence to return the device to reading array data. See Write Buffer section for more details.

Table I4. Write Operation Status

Status			DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	DQ1	RY/BY#
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle	0	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	N/A	0
Program Suspend Mode	Program-Suspend Read	Program-Suspended Sector	Invalid (not allowed)						1
		Non-Program Suspended Sector	Data						1
Erase Suspend Mode	Erase-Suspend Read	Erase-Suspended Sector	1	No toggle	0	N/A	Toggle	N/A	1
		Non-Erase Suspended Sector	Data						1
	Erase-Suspend-Program (Embedded Program)		DQ7#	Toggle	0	N/A	N/A	N/A	0
Write-to-Buffer	Busy (Note 3)		DQ7#	Toggle	0	N/A	N/A	0	0
	Abort (Note 4)		DQ7#	Toggle	0	N/A	N/A	1	0

Notes:

1. *DQ5 switches to ‘1’ when an Embedded Program, Embedded Erase, or Write-to-Buffer operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*
3. *The Data# Polling algorithm should be used to monitor the last loaded write-buffer address location.*
4. *DQ1 switches to ‘1’ when the device has aborted the write-to-buffer operation*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature, Plastic Packages . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –65°C to +125°C

Voltage with Respect to Ground:

V_{CC} (Note 1) . . . . . –0.5 V to +4.0 V

V_{IO} . . . . . –0.5 V to +4.0 V

A9, OE#, ACC and RESET# (Note 2) . . . . . –0.5 V to +12.5 V

All other pins (Note 1) . . . . . –0.5 V to +12.5 V

Output Short Circuit Current (Note 3) 200 mA

Notes:

1. *Minimum DC voltage on input or I/Os is –0.5 V. During voltage transitions, inputs or I/Os may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 7. Maximum DC voltage on input or I/Os is V_{CC} + 0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See Figure 8.*
2. *Minimum DC input voltage on pins A9, OE#, ACC, and RESET# is –0.5 V. During voltage transitions, A9, OE#, ACC, and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 7. Maximum DC input voltage on pin A9, OE#, ACC, and RESET# is +12.5 V which may overshoot to +14.0V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
4. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

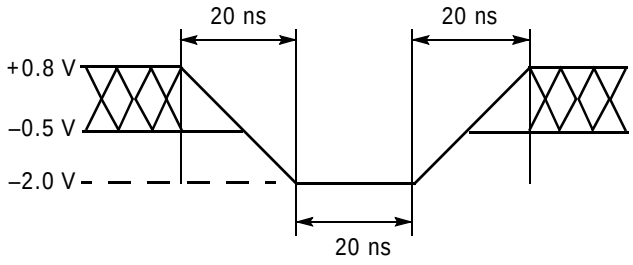


Figure 7. Maximum Negative Overshoot Waveform

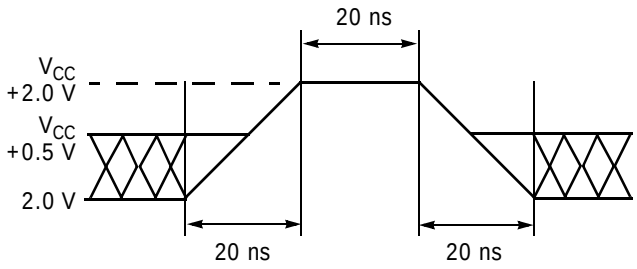


Figure 8. Maximum Positive Overshoot Waveform

Operating Ranges

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . –40°C to +85°C

Supply Voltages

V_{CC} . . . . . +2.7 V to +3.6 V

V_{IO} (Note 2) . . . . . +1.65 V to +1.95 V or +2.7 to + 3.6 V

Notes:

1. *Operating ranges define those limits between which the functionality of the device is guaranteed.*
2. *See Ordering Information (256 Mb) section for valid V_{CC}/V_{IO} range combinations. The I/Os will not operate at 3 V when V_{IO}=1.8 V.*

DC Characteristics

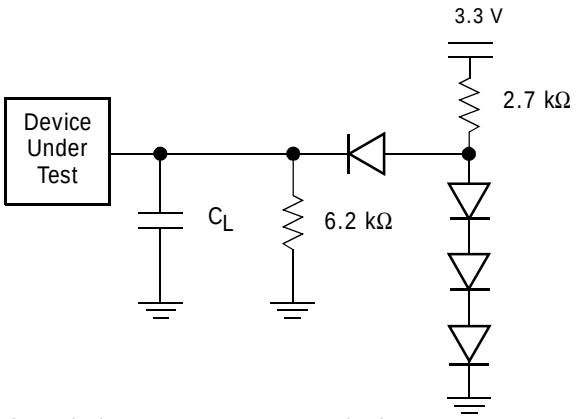
CMOS Compatible

Parameter Symbol	Parameter Description (Notes)	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Load Current (1)	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$			±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC\ max}$; A9 = 12.5 V			35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$			±1.0	µA
I_{IO1}	V_{IO} Active Read Current (Switching Current)	V_{IO} = 1.8 V, CE# = V_{IL}, OE# = V_{IL}, WE# = V_{IL}, *f* = 5 MHz		5	10	µA
I_{IO2}	V_{IO} Non-Active Output	CE# = V_{IL}, OE# = V_{IH}		0.2	10	mA
I_{CC1}	V_{CC} Active Read Current (1)	CE# = V_{IL}, OE# = V_{IH}, V_{CC} = V_{CCmax}, *f* = 5 MHz, Byte Mode		25	30	mA
		CE# = V_{IL}, OE# = V_{IH}, V_{CC} = V_{CCmax}, *f* = 5 MHz, Word Mode		25	30	
I_{CC2}	V_{CC} Initial Page Read Current (1)	CE# = V_{IL}, OE# = V_{IH}, V_{CC} = V_{CCmax}		50	60	mA
I_{CC3}	V_{CC} *Intra-Page Read Current* (1)	CE# = V_{IL}, OE# = V_{IH}, V_{CC} = V_{CCmax}		10	20	mA
I_{CC4}	V_{CC} Active Erase/Program Current (2, 3)	CE# = V_{IL}, OE# = V_{IH}, V_{CC} = V_{CCmax}		50	70	mA
I_{CC5}	V_{CC} Standby Current	CE#, RESET# = V_{SS} ± 0.3 V, OE# = V_{IH}, V_{CC} = V_{CCmax} V_{IL} = V_{SS} + 0.3 V/-0.1V,		1	5	µA
I_{CC6}	V_{CC} Reset Current	V_{CC} = V_{CCmax}; V_{IL} = V_{SS} + 0.3 V/-0.1V, RESET# = V_{SS} ± 0.3 V		1	5	µA
I_{CC7}	Automatic Sleep Mode (4)	V_{CC} = V_{CCmax} V_{IH} = V_{CC} ± 0.3 V, V_{IL} = V_{SS} + 0.3 V/-0.1V, WP#/ACC = V_{IH}		1	5	µA
I_{ACC}	ACC Accelerated Program Current	CE# = V_{IL}, OE# = V_{IH}, V_{CC} = V_{CCmax}, WP#/ACC = V_{IH}	WP#/ACC pin	10	20	mA
			V_{CC} pin	30	60	
V_{IL}	Input Low Voltage (5)		–0.1		0.3 x V_{IO}	V
V_{IH}	Input High Voltage (5)		0.7 x V_{IO}		V_{IO} + 0.3	V
V_{HH}	Voltage for ACC Erase/Program Acceleration	V_{CC} = 2.7 –3.6 V	11.5		12.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 2.7 –3.6 V	11.5		12.5	V
V_{OL}	Output Low Voltage (5)	I_{OL} = 100 µA			0.15 x V_{IO}	V
V_{OH}	Output High Voltage (5)	I_{OH} = 100 µA	0.85 x V_{IO}			V
V_{LKO}	Low V_{CC} Lock-Out Voltage (3)		2.3		2.5	V

Notes:

1. *The I_{CC} current listed is typically less than TBD mA/MHz, with OE# at V_{IH}.*
2. *I_{CC} active while Embedded Erase or Embedded Program or Write Buffer Programming is in progress.*
3. *Not 100% tested.*
4. *Automatic sleep mode enables the lower power mode when addresses remain stable tor t_{ACC} + 30 ns.*
5. *V_{IO} = 1.65–1.95 V or 2.7–3.6 V*
6. *V_{CC} = 3 V and V_{IO} = 3V or 1.8V. When V_{IO} is at 1.8V, I/O pins cannot operate at 3V.*

Test Conditions



Note: *Diodes are IN3064 or equivalent.*

Figure 9. Test Setup

Note: *Diodes are IN3064 or equivalent*

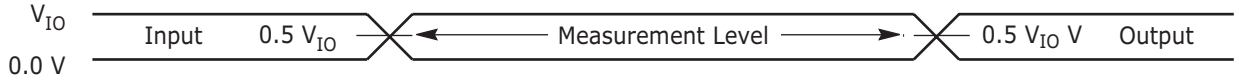
Table 15. Test Specifications

Test Condition	All Speeds	Unit
Output Load	1 TTL gate	
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0–V_{IO}	V
Input timing measurement reference levels (See Note)	0.5V_{IO}	V
Output timing measurement reference levels	0.5 V_{IO}	V

Note: *If V_{IO} < V_{CC}, the reference level is 0.5 V_{IO}.*

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)



Note: *If V_{IO} < V_{CC}, the input measurement reference level is 0.5 V_{IO}.*

Figure 10. Input Waveforms and Measurement Levels

AC Characteristics

Read-Only Operations–S29GL5I2N Only

Parameter		Description		Test Setup		Speed Options				Unit
JEDEC	Std.					90	100	100	110	
t_{AVAV}	t_{RC}	Read Cycle Time		$V_{IO} = V_{CC} = 3$ V	Min	90	100			ns
				$V_{IO} = 2.5$ V, $V_{CC} = 3$ V (Note 1)		100	110			
				$V_{IO} = 1.8$ V, $V_{CC} = 3$ V				100	110	ns
t_{AVQV}	t_{ACC}	Address to Output Delay (Note 2)		$V_{IO} = V_{CC} = 3$ V	Max	90	100			ns
				$V_{IO} = 2.5$ V, $V_{CC} = 3$ V (Note 1)		100	110			
				$V_{IO} = 1.8$ V, $V_{CC} = 3$ V				100	110	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay (Note 3)		$V_{IO} = V_{CC} = 3$ V	Max	90	105			ns
				$V_{IO} = 2.5$ V, $V_{CC} = 3$ V (Note 1)		100	110			
				$V_{IO} = 1.8$ V, $V_{CC} = 3$ V				100	110	ns
	t_{PACC}	Page Access Time			Max	25	25	35	35	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	25	25	35	35	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)			Max	20				ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)			Max	20				ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First			Min	0				ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0				ns
			Toggle and Data# Polling		Min	10				ns
	t_{CEH}	Chip Enable Hold Time	Read		Min	35				ns

Notes:

1. *Not 100% tested.*
2. *CE#, OE# = V_{IL}*
3. *OE# = V_{IL}*
4. *See Figure 9 and Table 15 for test specifications.*
5. *Unless otherwise indicated, AC specifications for 90 ns and 100 ns speed options are tested with $V_{IO} = V_{CC} = 3$ V. AC specifications for 100 ns and 110 ns speed options are tested with $V_{IO} = 1.8$ V and $V_{CC} = 3.0$ V.*

AC Characteristics

Read-Only Operations–S29GL256N Only

Parameter		Description		Test Setup		Speed Options				Unit
JEDEC	Std.					80	90	90	100	
t_{AVAV}	t_{RC}	Read Cycle Time		$V_{IO} = V_{CC} = 3$ V	Min	80	90			ns
				$V_{IO} = 2.5$ V, $V_{CC} = 3$ V (Note 1)		90	100			
				$V_{IO} = 1.8$ V, $V_{CC} = 3$ V				90	100	ns
t_{AVQV}	t_{ACC}	Address to Output Delay (Note 2)		$V_{IO} = V_{CC} = 3$ V	Max	80	90			ns
				$V_{IO} = 2.5$ V, $V_{CC} = 3$ V (Note 1)		90	100			
				$V_{IO} = 1.8$ V, $V_{CC} = 3$ V				90	100	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay (Note 3)		$V_{IO} = V_{CC} = 3$ V	Max	80	90			ns
				$V_{IO} = 2.5$ V, $V_{CC} = 3$ V (Note 1)		90	100			
				$V_{IO} = 1.8$ V, $V_{CC} = 3$ V				90	100	ns
	t_{PACC}	Page Access Time			Max	25	25	35	35	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	25	25	35	35	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)			Max	20				ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)			Max	20				ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First			Min	0				ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0				ns
			Toggle and Data# Polling		Min	10				ns
	t_{CEH}	Chip Enable Hold Time	Read		Min	35				ns

Notes:

1. *Not 100% tested.*
2. *CE#, OE# = V_{IL}*
3. *OE# = V_{IL}*
4. *See Figure 9 and Table 15 for test specifications.*
5. *Unless otherwise indicated, AC specifications for 80 ns and 90 ns speed options are tested with $V_{IO} = V_{CC} = 3$ V. AC specifications for 90 ns and 100 ns speed options are tested with $V_{IO} = 1.8$ V and $V_{CC} = 3.0$ V.*

AC Characteristics

Read-Only Operations–S29GLI28N Only

Parameter		Description		Test Setup		Speed Options				Unit
JEDEC	Std.					80	90	90	100	
t_{AVAV}	t_{RC}	Read Cycle Time		$V_{IO} = V_{CC} = 3$ V	Min	80	90			ns
				$V_{IO} = 2.5$ V, $V_{CC} = 3$ V (Note 1)		90	100			
				$V_{IO} = 1.8$ V, $V_{CC} = 3$ V				90	100	ns
t_{AVQV}	t_{ACC}	Address to Output Delay (Note 2)		$V_{IO} = V_{CC} = 3$ V	Max	80	90			ns
				$V_{IO} = 2.5$ V, $V_{CC} = 3$ V (Note 1)		90	100			
				$V_{IO} = 1.8$ V, $V_{CC} = 3$ V				90	100	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay (Note 3)		$V_{IO} = V_{CC} = 3$ V	Max	80	90			ns
				$V_{IO} = 2.5$ V, $V_{CC} = 3$ V (Note 1)		90	100			
				$V_{IO} = 1.8$ V, $V_{CC} = 3$ V				90	100	ns
	t_{PACC}	Page Access Time			Max	25	25	35	35	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	25	25	35	35	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)			Max	20				ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)			Max	20				ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First			Min	0				ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0				ns
			Toggle and Data# Polling		Min	10				ns
	tCEH	Chip Enable Hold Time	Read		Min	35				ns

Notes:

1. *Not 100% tested.*
2. *CE#, OE# = V_{IL}*
3. *OE# = V_{IL}*
4. *See Figure 9 and Table 15 for test specifications.*
5. *Unless otherwise indicated, AC specifications for 80 ns and 90 ns speed options are tested with $V_{IO} = V_{CC} = 3$ V. AC specifications for 90 ns and 100 ns speed options are tested with $V_{IO} = 1.8$ V and $V_{CC} = 3.0$ V.*

AC Characteristics

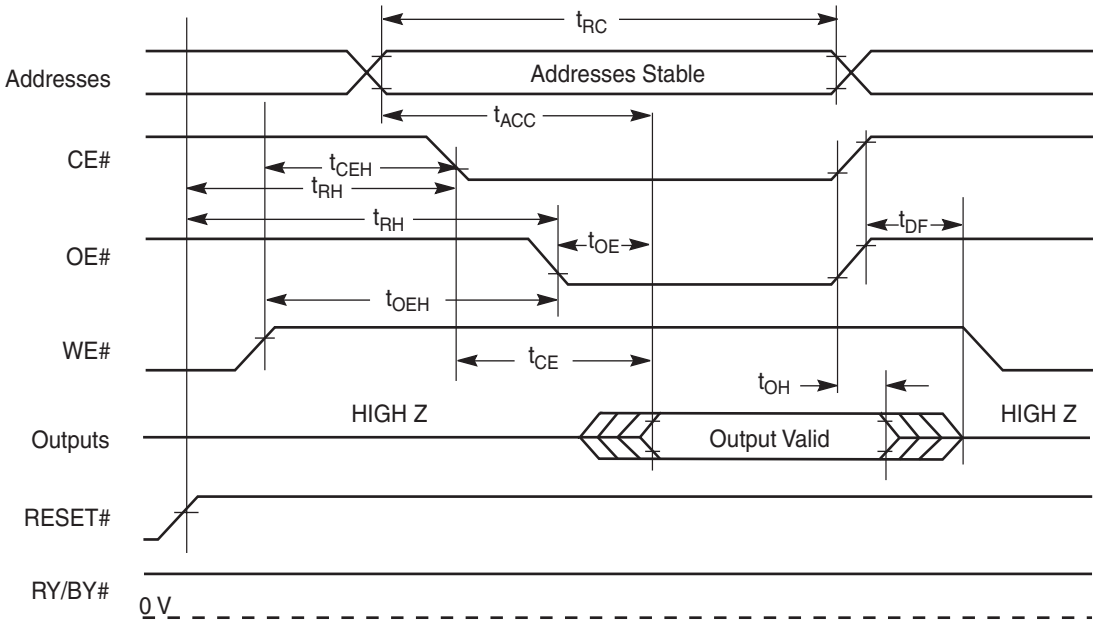
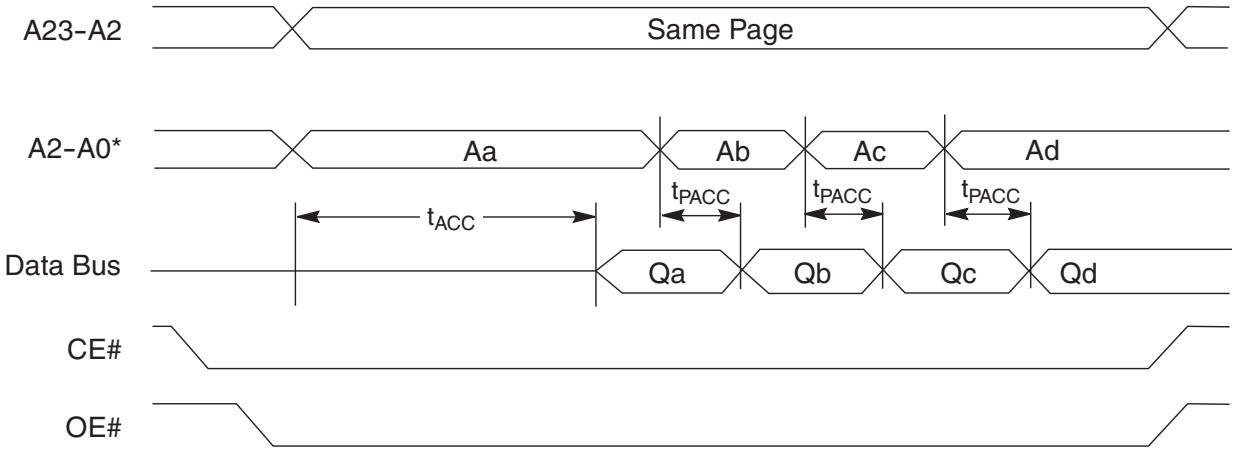


Figure II. Read Operation Timings



** Figure shows word mode. Addresses are A2–A-1 for byte mode.*

Figure I2. Page Read Timings

AC Characteristics

Hardware Reset (RESET#)

Parameter		Description		All Speed Options	Unit
JEDEC	Std.				
	t_{Ready}	RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note)	Max	1	ms
	t_{Ready}	RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note)	Max	1	ms
	t_{RP}	RESET# Pulse Width	Min	1	ms
	t_{RH}	Reset High Time Before Read (See Note)	Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	20	µs
	t_{RB}	RY/BY# Recovery Time	Min	0	ns

Note: *Not 100% tested. If ramp rate is equal to or faster than 1V/100µs with a falling edge of the RESET# pin initiated, the RESET# pin needs to be held low only for 100µs for power-up..*

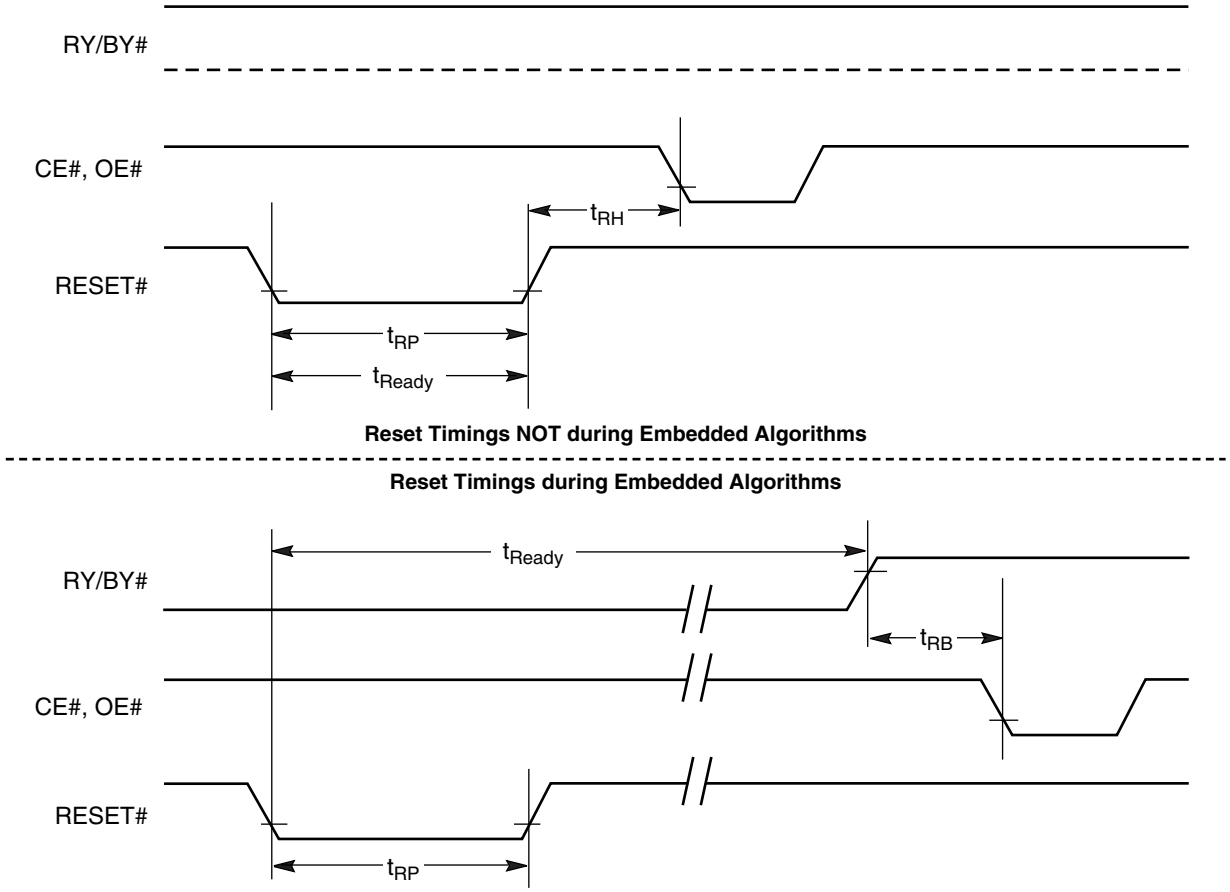


Figure 13. Reset Timings

AC Characteristics

Erase and Program Operations–S29GL5I2N Only

Parameter		Description			Speed Options				Unit
JEDEC	Std.				90	100	100	110	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	90	100	100	110	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0				ns
	t_{ASO}	Address Setup Time to OE# low during toggle bit polling		Min	15				ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	45				ns
	t_{AHT}	Address Hold Time From CE# or OE# high during toggle bit polling		Min	0				ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	45				ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0				ns
	t_{OEPH}	Output Enable High during toggle bit polling		Min	20				ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0				ns
t_{ELWL}	t_{CS}	CE# Setup Time		Min	0				ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0				ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	35				ns
t_{WHDL}	t_{WPH}	Write Pulse Width High		Min	30				ns
t_{WHWH1}	t_{WHWH1}	Write Buffer Program Operation (Notes 2, 3)		Typ	240				µs
		Effective Write Buffer Program Operation (Notes 2, 4)	Per Word	Typ	15				µs
		Accelerated Effective Write Buffer Program Operation (Notes 2, 4)	Per Word	Typ	13.5				µs
		Program Operation (Note 2)	Word	Typ	60				µs
		Accelerated Programming Operation (Note 2)	Word	Typ	54				µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	1.0				sec
	t_{VHH}	V_{HH} Rise and Fall Time (Note 1)		Min	250				ns
	t_{VCS}	V_{CC} Setup Time (Note 1)		Min	50				µs

Notes:

1. *Not 100% tested.*
2. *See the "Erase and Programming Performance" section for more information.*
3. *For 1–16 words/1–32 bytes programmed.*
4. *Effective write buffer specification is based upon a 16-word/32-byte write buffer operation.*
5. *Unless otherwise indicated, AC specifications for 90 ns and 100 ns speed options are tested with V_{IO} = V_{CC} = 3 V. AC specifications for 100 ns and 110 ns speed options are tested with V_{IO} = 1.8 V and V_{CC} = 3.0 V.*

AC Characteristics

Erase and Program Operations–S29GL256N Only

Parameter		Description			Speed Options				Unit
JEDEC	Std.				80	90	90	100	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	80	90	90	100	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0				ns
	t_{ASO}	Address Setup Time to OE# low during toggle bit polling		Min	15				ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	45				ns
	t_{AHT}	Address Hold Time From CE# or OE# high during toggle bit polling		Min	0				ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	45				ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0				ns
	t_{OEPH}	Output Enable High during toggle bit polling		Min	20				ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0				ns
t_{ELWL}	t_{CS}	CE# Setup Time		Min	0				ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0				ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	35				ns
t_{WHDL}	t_{WPH}	Write Pulse Width High		Min	30				ns
t_{WHWH1}	t_{WHWH1}	Write Buffer Program Operation (Notes 2, 3)		Typ	240				µs
		Effective Write Buffer Program Operation (Notes 2, 4)	Per Word	Typ	15				µs
		Accelerated Effective Write Buffer Program Operation (Notes 2, 4)	Per Word	Typ	13.5				µs
		Program Operation (Note 2)	Word	Typ	60				µs
		Accelerated Programming Operation (Note 2)	Word	Typ	54				µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	1.0				sec
	t_{VHH}	V_{HH} Rise and Fall Time (Note 1)		Min	250				ns
	t_{VCS}	V_{CC} Setup Time (Note 1)		Min	50				µs

Notes:

1. *Not 100% tested.*
2. *See the "Erase and Programming Performance" section for more information.*
3. *For 1–16 words/1–32 bytes programmed.*
4. *Effective write buffer specification is based upon a 16-word/32-byte write buffer operation.*
5. *Unless otherwise indicated, AC specifications for 80 ns and 90 ns speed options are tested with V_{IO} = V_{CC} = 3 V. AC specifications for 90 ns and 100 ns speed options are tested with V_{IO} = 1.8 V and V_{CC} = 3.0 V.*

AC Characteristics

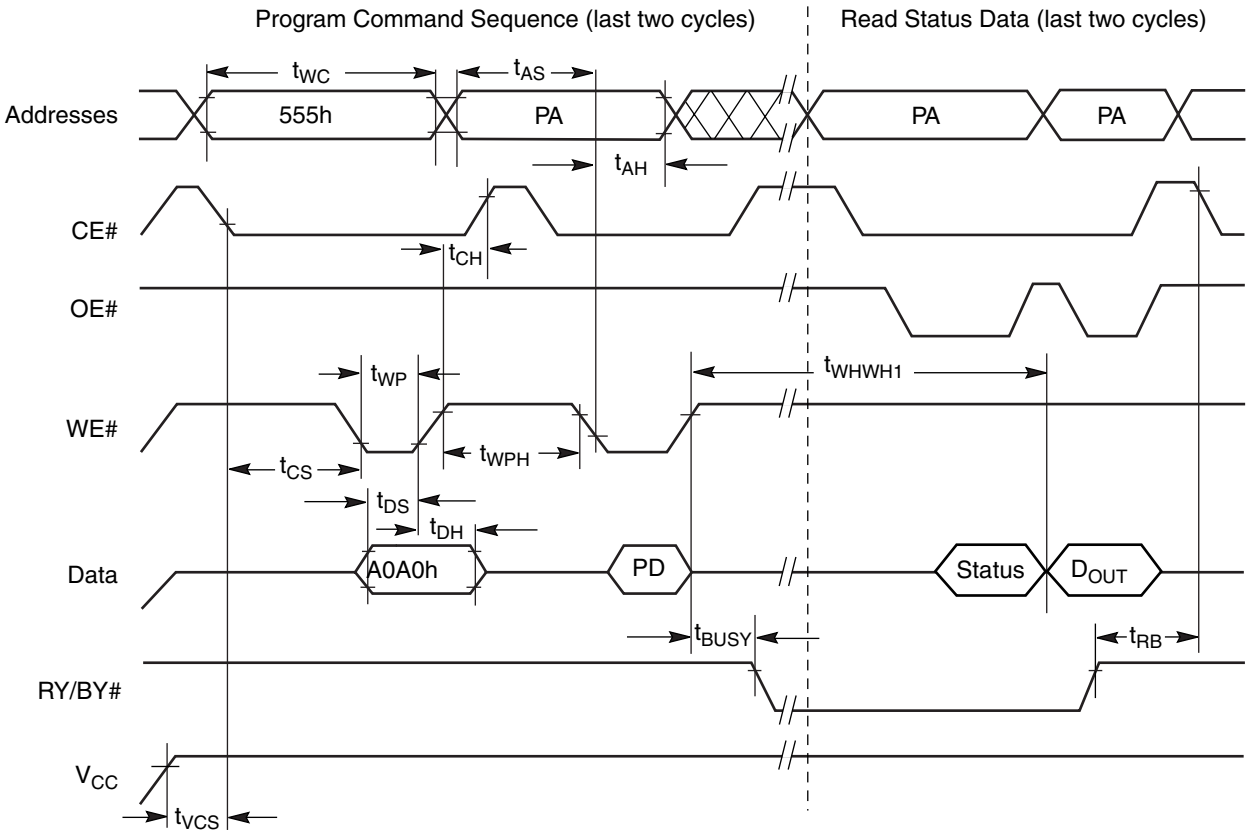
Erase and Program Operations–S29GLI28N Only

Parameter		Description			Speed Options				Unit
JEDEC	Std.				80	90	90	100	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	80	90	90	100	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0				ns
	t_{ASO}	Address Setup Time to OE# low during toggle bit polling		Min	15				ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	45				ns
	t_{AHT}	Address Hold Time From CE# or OE# high during toggle bit polling		Min	0				ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	45				ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0				ns
	t_{OEPH}	Output Enable High during toggle bit polling		Min	20				ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0				ns
t_{ELWL}	t_{CS}	CE# Setup Time		Min	0				ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0				ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	35				ns
t_{WHDL}	t_{WPH}	Write Pulse Width High		Min	30				ns
t_{WHWH1}	t_{WHWH1}	Write Buffer Program Operation (Notes 2, 3)		Typ	240				µs
		Effective Write Buffer Program Operation (Notes 2, 4)	Per Word	Typ	15				µs
		Accelerated Effective Write Buffer Program Operation (Notes 2, 4)	Per Word	Typ	13.5				µs
		Program Operation (Note 2)	Word	Typ	60				µs
		Accelerated Programming Operation (Note 2)	Word	Typ	54				µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	1.0				sec
	t_{VHH}	V_{HH} Rise and Fall Time (Note 1)		Min	250				ns
	t_{VCS}	V_{CC} Setup Time (Note 1)		Min	50				µs

Notes:

1. *Not 100% tested.*
2. *See the "Erase and Programming Performance" section for more information.*
3. *For 1–16 words/1–32 bytes programmed.*
4. *Effective write buffer specification is based upon a 16-word/32-byte write buffer operation.*
5. *Unless otherwise indicated, AC specifications for 80 ns and 90 ns speed options are tested with V_{IO} = V_{CC} = 3 V. AC specifications for 90 ns and 100 ns speed options are tested with V_{IO} = 1.8 V and V_{CC} = 3.0 V.*

AC Characteristics



Notes:

1. *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*
2. *Illustration shows device in word mode.*

Figure 14. Program Operation Timings

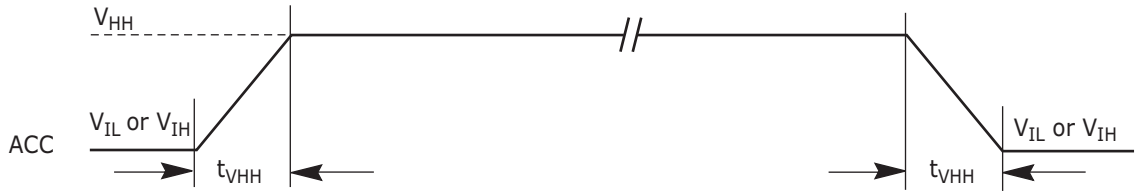
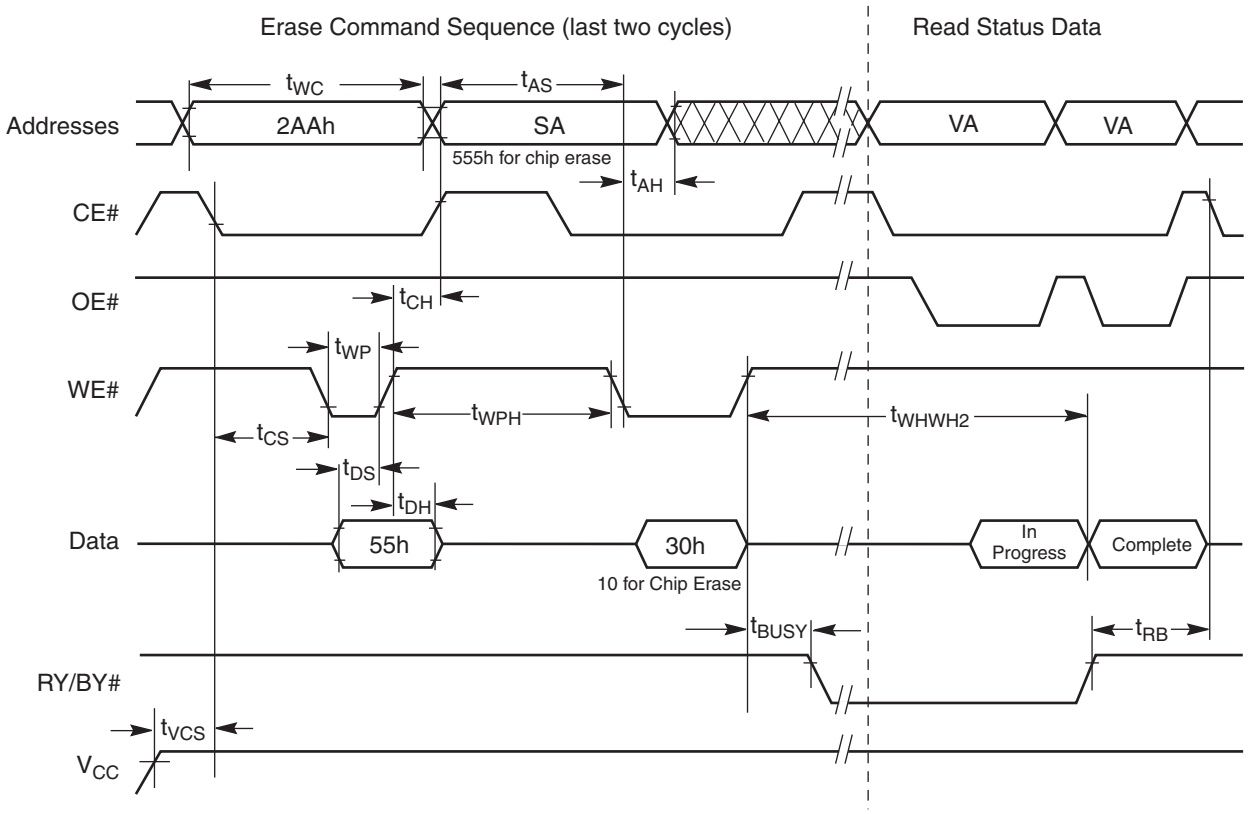


Figure 15. Accelerated Program Timing Diagram

Notes:

1. *Not 100% tested.*
2. *CE#, OE# = V_{IL}*
3. *OE# = V_{IL}*
4. *See Figure 9 and Table 15 for test specifications.*

AC Characteristics

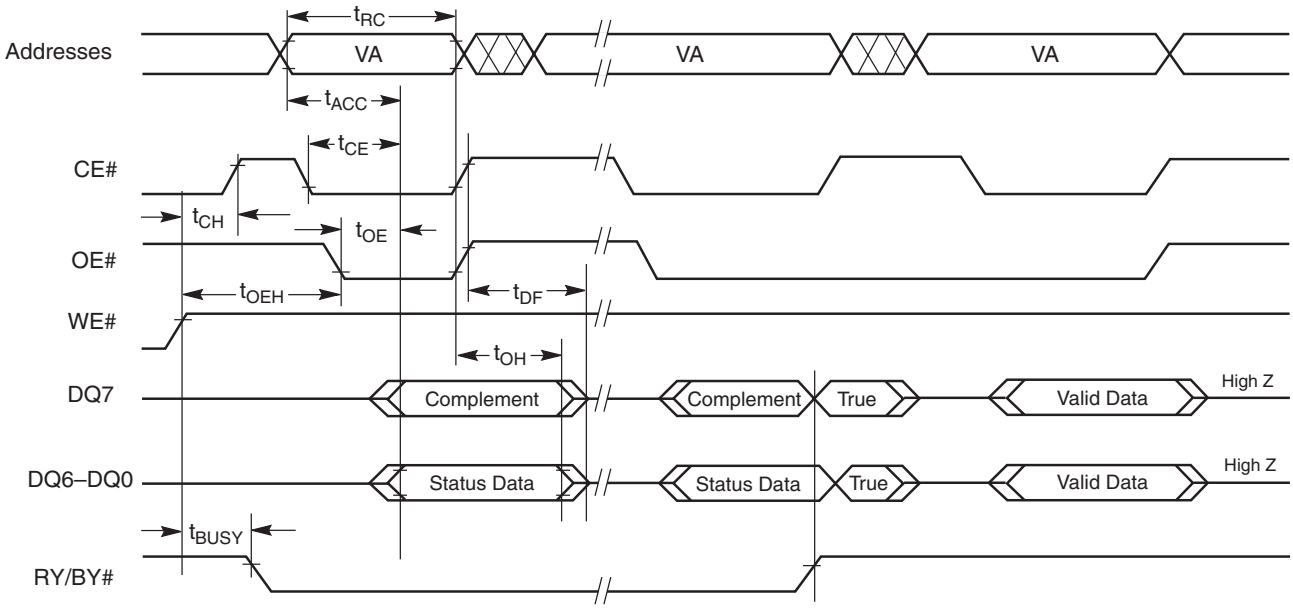


Notes:

1. *SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see "Write Operation Status".*
2. *These waveforms are for the word mode.*

Figure 16. Chip/Sector Erase Operation Timings

AC Characteristics

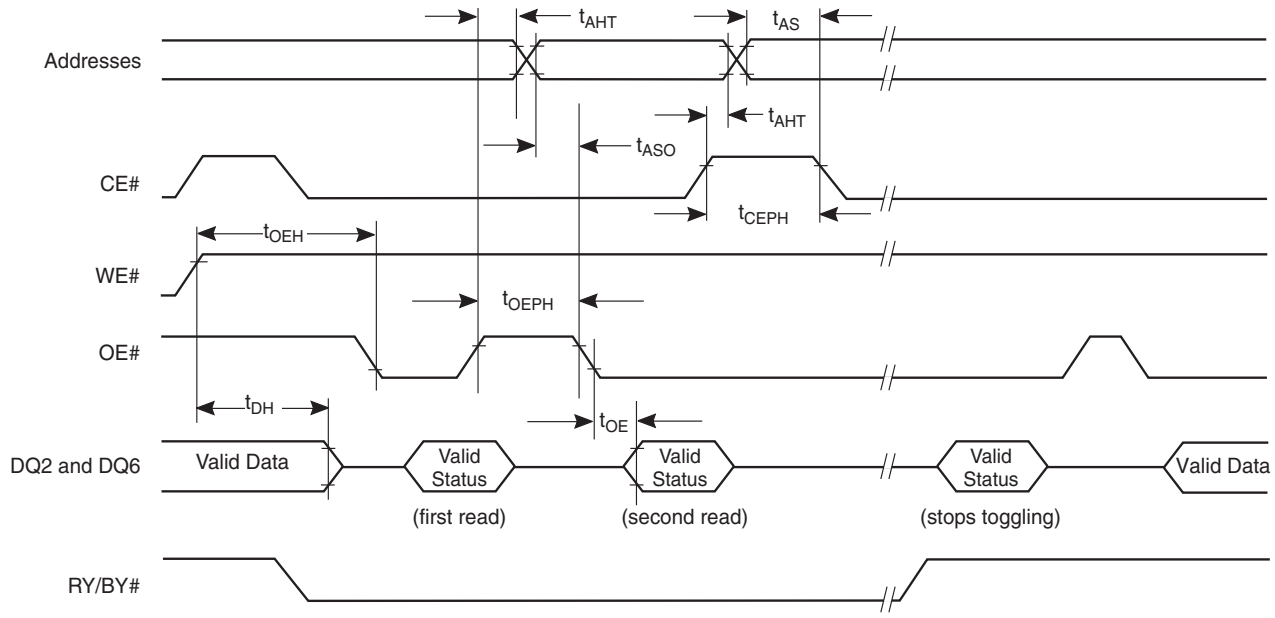


Note:

1. *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.*
2. *t_{OE} for data polling is 45 ns when V_{IO} = 1.65 to 2.7 V and is 35 ns when V_{IO} = 2.7 to 3.6 V*

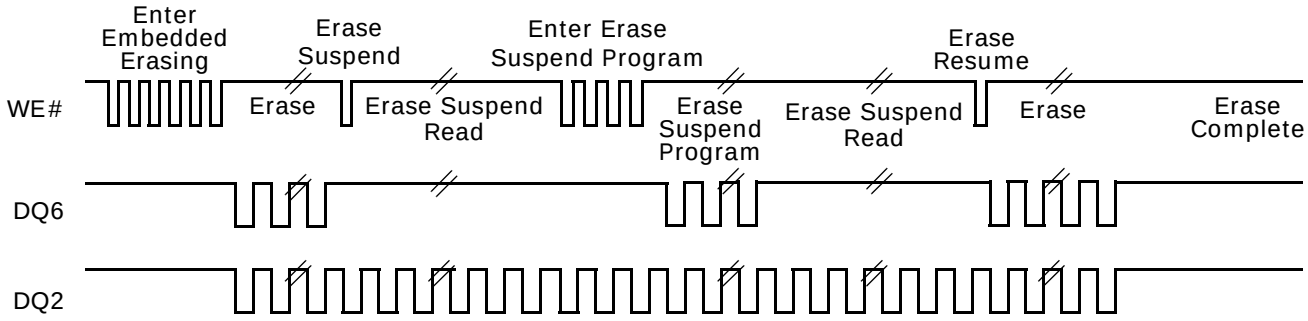
Figure 17. Data# Polling Timings (During Embedded Algorithms)

AC Characteristics



Note: *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle*

Figure 18. Toggle Bit Timings (During Embedded Algorithms)



Note: *DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE# to toggle DQ2 and DQ6.*

Figure 19. DQ2 vs. DQ6

AC Characteristics

Alternate CE# Controlled Erase and Program Operations–S29GL5I2N Only

Parameter		Description			Speed Options				Unit
JEDEC	Std.				90	100	100	110	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	90	100	100	110	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0				ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	45				ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	45				ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0				ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0				ns
t_{WLEL}	t_{WS}	WE# Setup Time		Min	0				ns
t_{EHWH}	t_{WH}	WE# Hold Time		Min	0				ns
t_{ELEH}	t_{CP}	CE# Pulse Width		Min	45				ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High		Min	30				ns
t_{WHWH1}	t_{WHWH1}	Write Buffer Program Operation (Notes 2, 3)		Typ	240				µs
		Effective Write Buffer Program Operation (Notes 2, 4)	Per Word	Typ	15				µs
		Effective Accelerated Write Buffer Program Operation (Notes 2, 4)	Per Word	Typ	13.5				µs
		Program Operation (Note 2)	Word	Typ	60				µs
		Accelerated Programming Operation (Note 2)	Word	Typ	54				µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	1.0				sec

Notes:

1. *Not 100% tested.*
2. *See the "AC Characteristics" section for more information.*
3. *For 1–16 words/1–32 bytes programmed.*
4. *Effective write buffer specification is based upon a 16-word/32-byte write buffer operation.*
5. *Unless otherwise indicated, AC specifications for 90 ns and 100 ns speed options are tested with V_{IO} = V_{CC} = 3 V. AC specifications for 100 ns and 110 ns speed options are tested with V_{IO} = 1.8 V and V_{CC} = 3.0 V.*

AC Characteristics

Alternate CE# Controlled Erase and Program Operations–S29GL256N Only

Parameter		Description			Speed Options				Unit
JEDEC	Std.				80	90	90	100	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	80	90	90	100	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0				ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	45				ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	45				ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0				ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0				ns
t_{WLEL}	t_{WS}	WE# Setup Time		Min	0				ns
t_{EHWH}	t_{WH}	WE# Hold Time		Min	0				ns
t_{ELEH}	t_{CP}	CE# Pulse Width		Min	45				ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High		Min	30				ns
t_{WHWH1}	t_{WHWH1}	Write Buffer Program Operation (Notes 2, 3)		Typ	240				µs
		Effective Write Buffer Program Operation (Notes 2, 4)	Per Word	Typ	15				µs
		Effective Accelerated Write Buffer Program Operation (Notes 2, 4)	Per Word	Typ	13.5				µs
		Program Operation (Note 2)	Word	Typ	60				µs
		Accelerated Programming Operation (Note 2)	Word	Typ	54				µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	1.0				sec

Notes:

1. *Not 100% tested.*
2. *See the "AC Characteristics" section for more information.*
3. *For 1–16 words/1–32 bytes programmed.*
4. *Effective write buffer specification is based upon a 16-word/32-byte write buffer operation.*
5. *Unless otherwise indicated, AC specifications for 80 ns and 90 ns speed options are tested with V_{IO} = V_{CC} = 3 V. AC specifications for 90 ns and 100 ns speed options are tested with V_{IO} = 1.8 V and V_{CC} = 3.0 V.*

AC Characteristics

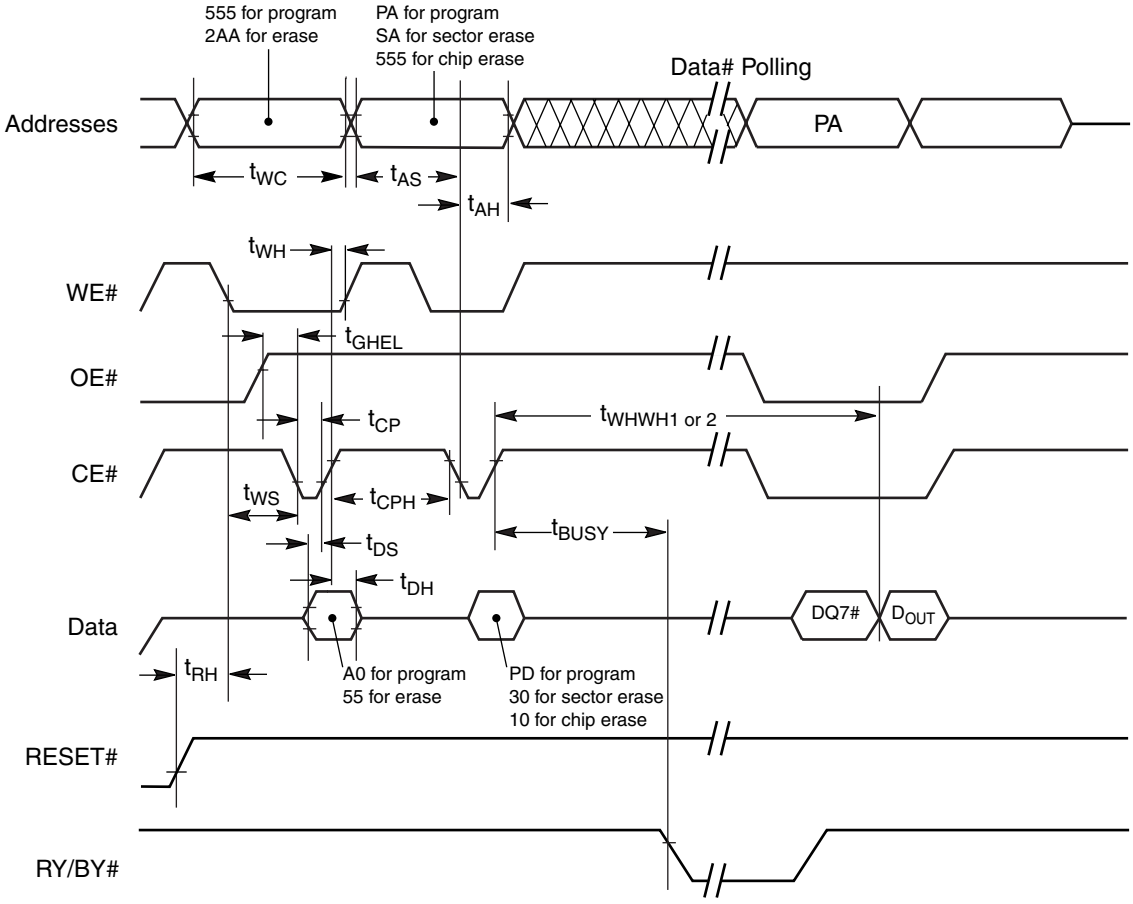
Alternate CE# Controlled Erase and Program Operations–S29GLI28N Only

Parameter		Description			Speed Options				Unit
JEDEC	Std.				80	90	90	100	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	80	90	90	100	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0				ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	45				ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	45				ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0				ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0				ns
t_{WLEL}	t_{WS}	WE# Setup Time		Min	0				ns
t_{EHWH}	t_{WH}	WE# Hold Time		Min	0				ns
t_{ELEH}	t_{CP}	CE# Pulse Width		Min	45				ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High		Min	30				ns
t_{WHWH1}	t_{WHWH1}	Write Buffer Program Operation (Notes 2, 3)		Typ	240				µs
		Effective Write Buffer Program Operation (Notes 2, 4)	Per Word	Typ	15				µs
		Effective Accelerated Write Buffer Program Operation (Notes 2, 4)	Per Word	Typ	13.5				µs
		Program Operation (Note 2)	Word	Typ	60				µs
		Accelerated Programming Operation (Note 2)	Word	Typ	54				µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	1.0				sec

Notes:

1. *Not 100% tested.*
2. *See the "AC Characteristics" section for more information.*
3. *For 1–16 words/1–32 bytes programmed.*
4. *Effective write buffer specification is based upon a 16-word/32-byte write buffer operation.*
5. *Unless otherwise indicated, AC specifications for 80 ns and 90 ns speed options are tested with V_{IO} = V_{CC} = 3 V. AC specifications for 90 ns and 100 ns speed options are tested with V_{IO} = 1.8 V and V_{CC} = 3.0 V.*

AC Characteristics



Notes:

1. *Figure indicates last two bus cycles of a program or erase operation.*
2. *PA = program address, SA = sector address, PD = program data.*
3. *DQ7# is the complement of the data written to the device. D_{OUT} is the data written to the device.*
4. *Waveforms are for the word mode.*

Figure 20. Alternate CE# Controlled Write (Erase/Program) Operation Timings

Erase And Programming Performance

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time		1	3.5	sec	Excludes 00h programming prior to erasure (Note 5)
Chip Erase Time	S29GL128N	128	256	sec	
	S29GL256N	256	512		
	S29GL512N	512	1024		
Total Write Buffer Time (Note 3)		240		µs	Excludes system level overhead (Note 6)
Total Accelerated Effective Write Buffer Programming Time (Note 3)		200		µs	
Chip Program Time	S29GL128N	123		sec	
	S29GL256N	246			
	S29GL512N	492			

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 3.0 V V_{CC}, 10,000 cycles, checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 3.0 V, 1,000,000 cycles.*
3. *Effective write buffer specification is based upon a 16-word write buffer operation.*
4. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most words program faster than the maximum program times listed.*
5. *In the pre-programming step of the Embedded Erase algorithm, all bits are programmed to 00h before erasure.*
6. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 17 for further information on command definitions.*

TSOP Pin and BGA Package Capacitance

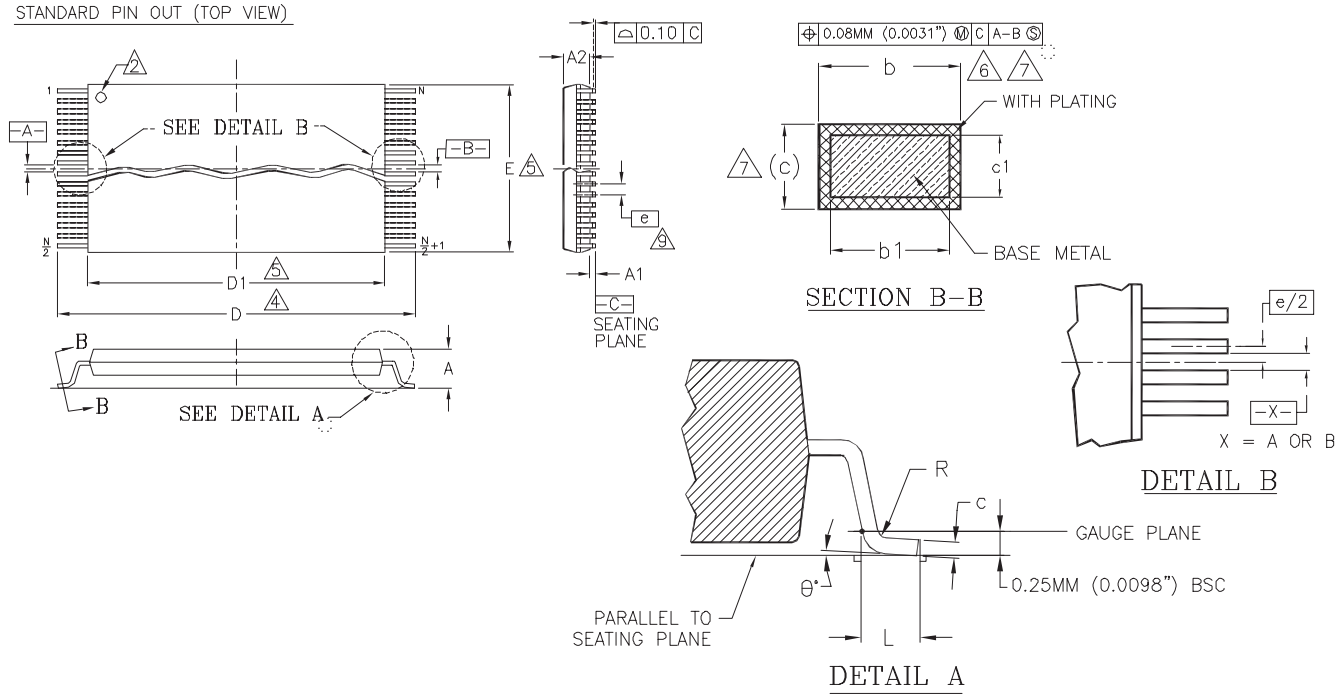
Parameter Symbol	Parameter Description	Test Setup		Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	TSOP	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	TSOP	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	TSOP	7.5	9	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

Physical Dimensions

TS056—56-Pin Standard Thin Small Outline Package (TSOP)



PACKAGE	TS 56		
JEDEC	MO-142 (B) EC		
SYMBOL	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.05	---	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	---	0.16
c	0.10	---	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	13.90	14.00	14.10
e	0.50 BASIC		
L	0.50	0.60	0.70
Ø	0°	-	8°
R	0.08	---	0.20
N	56		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982.)
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. TO BE DETERMINED AT THE SEATING PLANE -C- . THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
4. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15 mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08 mm TOTAL IN EXCESS OF b DIMENSION AT MAX MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07 mm.
6. THESE DIMESIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
7. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.
8. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

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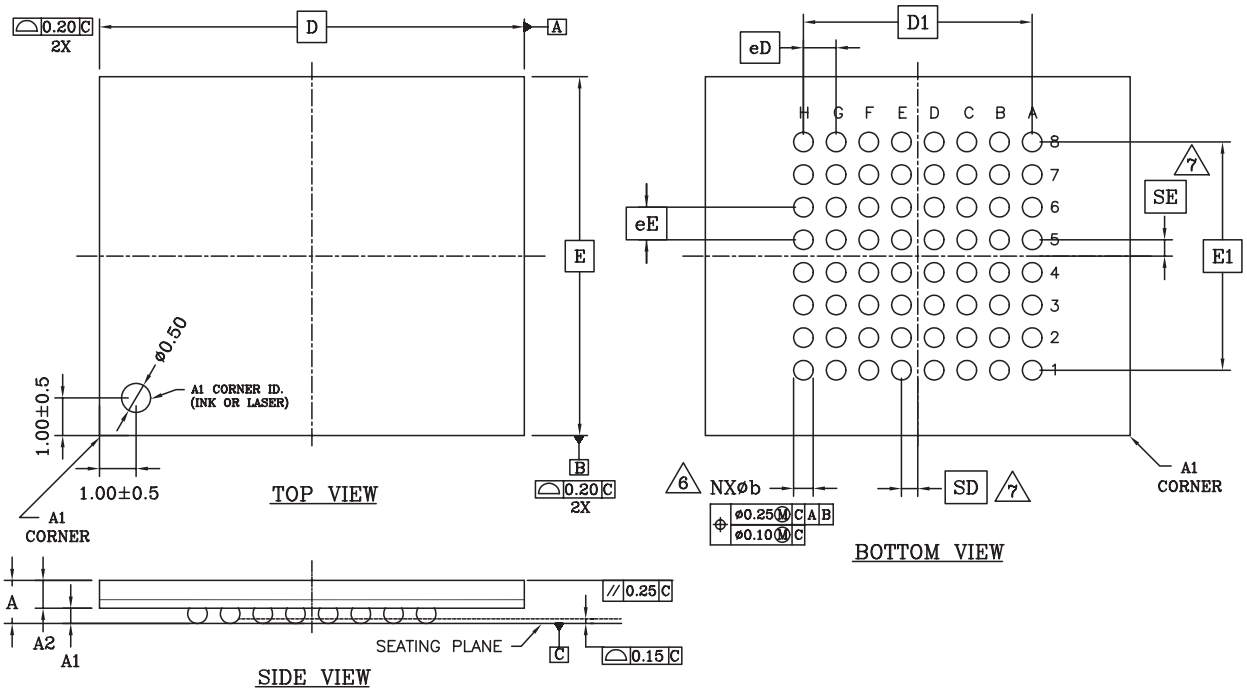
Physical Dimensions

LAA064—64-Ball Fortified Ball Grid Array (FBGA)



PACKAGE	LAA 064			
JEDEC	N/A			
	13.00x11.00 mm PACKAGE			
SYMBOL	MIN.	NOM.	MAX.	NOTE
A	–	–	1.40	PROFILE HEIGHT
A1	0.40	–	–	STANDOFF
A2	0.60	–	–	BODY THICKNESS
D	13.00 BSC.			BODY SIZE
E	11.00 BSC.			BODY SIZE
D1	7.00 BSC.			MATRIX FOOTPRINT
E1	7.00 BSC.			MATRIX FOOTPRINT
MD	8			MATRIX SIZE D DIRECTION
ME	8			MATRIX SIZE E DIRECTION
N	64			BALL COUNT
øb	0.50	0.60	0.70	BALL DIAMETER
eD	1.00 BSC.			BALL PITCH – D DIRECTION
eE	1.00 BSC.			BALL PITCH – E DIRECTION
SD/SE	0.50 BSC.			SOLDER BALL PLACEMENT
	A1–A8, K1–K8			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M–1994 .
2. ALL DIMENSIONS ARE IN MILLIMETERS .
3. BALL POSITION DESIGNATION PER JESD 95–1, SPP–010 (EXCEPT AS NOTED).
4. e REPRESENTS THE SOLDER BALL GRID PITCH .
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM "C".
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = 0.000.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "X" IN THE PACKAGE VARIATIONS DENOTES PART IS UNDER QUALIFICATION.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

Revision Summary

Revision A (September 2, 2003)

Initial Release.

Revision A+1 (October 16, 2003)

Global

Added LAA064 package.

Distinctive Characteristics, Performance Characteristics

Clarified fifth bullet information.

Added RTSOP to Package Options.

Distinctive Characteristics, Software and Hardware Features

Clarified “Password Sector Protection” to “Advanced Sector Protection”

Connection Diagrams

Removed Note.

Ordering Information

Modified Package codes

Device Bus Operations, Table 1

Modified Table, removed Note.

Sector Address Tables

All address ranges doubled in all sector address tables.

Sector Protection

Lock Register: Corrected text to reflect 3 bits instead of 4.

Table 6, Lock Register: Corrected address range from DQ15-5 to DQ15-3; removed DQ4 and DQ3; Corrected DQ15-3 Lock Register to Don’t Care.

Table 7, Sector Protection Schemes: Corrected Sector States.

Command Definitions

Table 12, Command Definitions, x16

Nonvolatile Sector Protection Command Set Entry Second Cycle Address corrected from 55 to 2AA.

Legend: Clarified PWDx, DATA

Notes: Clarified Note 19.

Table 13, Command Definitions, x8

Password Read and Unlock Addresses and Data corrected.

Legend: Clarified PWDx, DATA

Notes: Clarified Note 19.

Test Conditions

Table 15, Test Specifications and Figure 10, Input Waveforms and Measurement Levels: Corrected Input Pulse Levels to 0.0–VIO; corrected Input timing measurement reference levels to $0.5V_{IO}$.

Revision A+2 (January 22, 2004)

Lock Register

Corrected and added new text for SecSi Sector Protection Bit, Persistent Protection Mode Lock Bit, and Password Protection Mode Lock Bit.

Persistent Sector Protection

Persistent Protection Bit (PPB): Added the second paragraph text about programming the PPB bit.

Persistent Protection Bit Lock (PPB Lock Bit): Added the second paragraph text about configuring the PPB Lock Bit, and fourth paragraph on Autoselect Sector Protection Verification.

Added PPB Lock Bit requirement of 200ns access time.

Password Sector Protection

Corrected 1 µs (built-in delay for each password check) to 2 µs.

Lock Register Command Set Definitions

Added new information for this section.

Password Protection Command Set Definitions

Added new information for this section.

Non-Volatile Sector Protection Command Set Definitions

Added new information for this section.

Global Volatile Sector Protection Freeze Command Set

Added new information for this section.

Volatile Sector Protection Command Set

Added new information for this section.

SecSi Sector Entry Command

Added new information for this section.

SecSi Sector Exit Command

Added new information for this section.

Revision A+3 (March 2, 2004)

Connection Diagrams

Removed 56-pin reverse TSOP diagram.

Ordering Information

Updated the Standard Products for the S29GL512/256/128N devices and modified the valid combinations tables.

Word Program Command Sequence

Added new information to this section.

Lock Register Command Set Definitions

Added new information to this section.

Table 13

Updated this table.

Revision A+4 (May 13, 2004)

Global

Removed references to RTSOP.

Distinctive Characteristics

Removed 16-word/32-byte page read buffer from Performance Characteristics.

Changed Low power consumption to 25 mA typical active read current and removed 10 mA typical intrapage active read current.

Ordering Information

Changed formatting of pages.

Changed model numbers from 00,01,02,03 to 01, 02, V1, V2.

Table 1, "Device Bus Operations"

Combined WP# and ACC columns.

Table 8, "CFI Query Identification String", Table 9, "System Interface String", Table 10, "Device Geometry Definition", and Table 11, "Primary Vendor-Specific Extended Query

Added Address (x8) column.

Word Program Command Sequence

Added text to fourth paragraph.

Figure 1, "Write Buffer Programming Operation,"

Added note references and removed DQ15 and DQ13.

Figure 3, "Program Suspend/Program Resume,"

Changed field to read XXXh/B0h and XXXh/30h.

Password Protection Command Set Definitions

Replaced all text.

Table 12, "S29GL512N, S29GL256N, S29GL128N Command Definitions, x16"

Changed the first cycle address of CFI Query to 55.

Table 13, "S29GL512N, S29GL256N, S29GL128N Command Definitions, x8"

Changed the third cycle data Device ID to 90.

Removed Unlock Bypass Reset.

Removed Note 12 and 13.

Figure 5, "Data# Polling Algorithm,"

Removed DQ15 and DQ13.

Absoulte Maximum Ratings

Removed VCC from "All other pins" with respect to Ground.

CMOS Compatible

Changed the Max of I_{CC4} to 70 mA

Added V_{IL} to the Test conditions of I_{CC5}, I_{CC6}, and I_{CC7}

Change the Min of V_{IL} to - 0.1 V.

Updated note 5.

Read-Only Operations–S29GL128N Only

Added t_{CEH} parameter to table.

Figure 11, “Read Operation Timings,”
Added t_{CEH} to figure.

Figure 12, “Page Read Timings,”
Change A1-A0 to A2-A0.

Erase and Program Operations
Updated t_{WHWH1} and t_{WHWH2} with values.

Figure 16, “Chip/Sector Erase Operation Timings,”
Changed 5555h to 55h and 3030h to 30h.

Figure 17, “Data# Polling Timings (During Embedded Algorithms),”
Removed DQ15 and DQ14-DQ8

Added Note 2

Figure 18, “Toggle Bit Timings (During Embedded Algorithms),”
Changed DQ6 & DQ14/DQ2 & DQ10 to DQ2 and DQ6.

Alternate CE# Controlled Erase and Program Operations
Updated t_{WHWH1} and t_{WHWH2} with values.

Latchup Characteristics
Removed Table.

Erase and Programming Performance
Updated TBD with values.

Updated Note 1 and 2.

Physical Dimensions
Removed the reverse pinout information and note 3.

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