S29NS-N MirrorBit™ Flash Family

S29NS256N, S29NS128N, S29NS064N
256/128/64 Megabit (16/8/4M x 16-bit), CMOS 1.8 Volt-only Simultaneous Read/Write, Multiplexed, Burst Mode Flash Memory

Data Sheet *(Advance Information)*

Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. Each product described herein may be designated as Advance Information, Preliminary, or Full Production. See *Notice On Data Sheet Designations* for definitions.

Publication Number S29NS-N_00 **Revision** A **Amendment** 12 **Issue Date** June 13, 2006

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Spansion LLC issues data sheets with Advance Information or Preliminary designations to advise readers of product information or intended specifications throughout the product life cycle, including development, qualification, initial production, and full production. In all cases, however, readers are encouraged to verify that they have the latest information before finalizing their design. The following descriptions of Spansion data sheet designations are presented here to highlight their presence and definitions.

Advance Information

The Advance Information designation indicates that Spansion LLC is developing one or more specific products, but has not committed any design to production. Information presented in a document with this designation is likely to change, and in some cases, development on the product may discontinue. Spansion LLC therefore places the following conditions upon Advance Information content:

> "This document contains information on one or more products under development at Spansion LLC. The information is intended to help you evaluate this product. Do not design in this product without contacting the factory. Spansion LLC reserves the right to change or discontinue work on this proposed product without notice."

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The Preliminary designation indicates that the product development has progressed such that a commitment to production has taken place. This designation covers several aspects of the product life cycle, including product qualification, initial production, and the subsequent phases in the manufacturing process that occur before full production is achieved. Changes to the technical specifications presented in a Preliminary document should be expected while keeping these aspects of production under consideration. Spansion places the following conditions upon Preliminary content:

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Combination

Some data sheets contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document distinguishes these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with the DC Characteristics table and the AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion LLC applies the following conditions to documents in this category:

> "This document states the current technical specifications regarding the Spansion product(s) described herein. Spansion LLC deems the products to have been in sufficient production volume such that subsequent versions of this document are not expected to change. However, typographical or specification corrections, or modifications to the valid combinations offered may occur."

Questions regarding these document designations may be directed to your local AMD or Fujitsu sales office.

S29NS-N MirrorBit™ Flash Family

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256/128/64 Megabit (16/8/4M x 16-bit), CMOS 1.8 Volt-only Simultaneous Read/Write, Multiplexed, Burst Mode Flash Memory

Data Sheet *(Advance Information)*

Distinctive Characteristics

- **Single 1.8V read, program and erase (1.70V to 1.95V)**
- **VersatileIO™ Feature**
  - Device generates data output voltages and tolerates data input voltages as determined by the voltage on the V_{CCQ} pin
  - 1.8V compatible I/O signals
- **Multiplexed Data and Address for reduced I/O count**
  - A15–A0 multiplexed as DQ15–DQ0
  - Addresses are latched by AVD# control input when CE# low
- **Simultaneous Read/Write operation**
  - Data can be continuously read from one bank while executing erase/program functions in other bank
  - Zero latency between read and write operations
- **Read access times at 80/66 MHz**
  - Burst access times of 9/11 ns at industrial temperature range
  - Asynchronous random access times of 80 ns
  - Synchronous random access times of 80 ns
- **Burst length**
  - Continuous linear burst
  - 8/16/32 word linear burst with wrap around
  - 8/16/32 word linear burst without wrap around
- **Secured Silicon Sector region**
  - 256 words accessible through a command sequence
  - 128 words for the Factory Secured Silicon Sector
  - 128 words for the Customer Secured Silicon Sector
- **Power dissipation (typical values: 8 bits switching, C_L = 30 pF) @ 80 MHz**
  - Continuous Burst Mode Read: 28 mA (at 66MHz)
  - Simultaneous Operation: 50 mA
  - Program/Erase: 19 mA
  - Standby mode: 20 µA
- **Sector Architecture**
  - Four 16 K word sectors (S29NS256N and S29NS128N) and four 8K word sectors (S29NS064N) in upper-most address range
  - Two-hundred-fifty-five 64-Kword sectors (S29NS256N), one-hundred-twenty-seven 64-Kword sectors (S29NS128N) and one hundred twenty-seven 32Kword sectors (S29NS064N)
  - Sixteen banks (S29NS128N and S29NS256N) and eight banks (S29NS064N)
- **High Performance**
  - Typical word programming time of 40 µs
  - Typical effective word programming time of 9.4 µs utilizing a 32-Word Write Buffer at V_{CC} Level
  - Typical effective word programming time of 6 µs utilizing a 32-Word Write Buffer at ACC Level
  - Typical sector erase time of 150 ms for 16 Kword sectors and 800 ms sector erase time for 64 Kword sectors

Security features

- **Persistent Sector Protection**
  - A command sector protection method to lock combinations of individual sectors to prevent program or erase operations within that sector
  - Sectors can be locked and unlocked in-system at V_{CC} level
- **Password Sector Protection**
  - A sophisticated sector protection method to lock combinations of individual sectors to prevent program or erase operations within that sector using a user-defined 64-bit password
- **Hardware Sector Protection**
  - WP# protects the two highest sectors
  - All sectors locked when ACC = V_{IL}
- **Handshaking feature**
  - Provides host system with minimum possible latency by monitoring RDY
- **Supports Common Flash Memory Interface (CFI)**
- **Software command set compatible with JEDEC 42.4 standards**
  - Backwards compatible with Am29F and Am29LV families
- **Manufactured on 110 nm MirrorBit™ process technology**
- **Cycling endurance: 100,000 cycles per sector typical**
- **Data retention: 20 years typical**
- **Data# Polling and toggle bits**
  - Provides a software method of detecting program and erase operation completion
- **Erase Suspend/Resume**
  - Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Program Suspend/Resume**
  - Suspends a programming operation to read data from a sector other than the one being programmed, then resume the programming operation
- **Unlock Bypass Program command**
  - Reduces overall programming time when issuing multiple program command sequences
- **Packages**
  - 48-ball Very Thin FBGA (S29NS256N)
  - 44-ball Very Thin FBGA (S29NS128N, S29NS064N)

Publication Number S29NS-N_00 **Revision** A **Amendment** 12 **Issue Date** June 13, 2006

1. General Description

The S29NS256N, S29NS128N and S29NS064N are 256 Mb, 128 Mb and 64Mb (respectively), 1.8 Volt-only, Simultaneous Read/Write, Burst Mode Flash memory devices, organized as 16,777,216, 8,388,608, and 4,194,304 words of 16 bits each. These devices use a single V_{CC} of 1.70 to 1.95 V to read, program, and erase the memory array. A 9.0-volt ACC, may be used for faster program performance if desired. These devices can also be programmed in standard EPROM programmers.

The devices are offered at the following speeds:

Clock Speed	Burst Access (ns)	Synch. Initial Access (ns)	Asynch. Initial Access (ns)	Output Loading
80 MHz	9	80	80	30 pF
66 MHz	11.0	80	80	

The devices operate within the temperature range of −25°C to +85°C, and are offered in Very Thin FBGA packages.

1.1 Simultaneous Read/Write Operations with Zero Latency

The Simultaneous Read/Write architecture provides **simultaneous operation** by dividing the memory space into sixteen banks. The device allows a host system to program or erase in one bank, then immediately and simultaneously read from another bank, with zero latency. This releases the system from waiting for the completion of program or erase operations. The devices are structured as shown in the following tables:

S29NS256N			
Bank 0-14 Sectors		Bank 15 Sectors	
Quantity	Size	Quantity	Size
240	64 Kwords	4	16 Kwords
		15	64 Kwords
240 Mb total		16 Mb total	

S29NS128N			
Bank 0-14 Sectors		Bank 15 Sectors	
Quantity	Size	Quantity	Size
120	64 Kwords	4	16 Kwords
		7	64 Kwords
120 Mb total		8 Mb total	

S29NS064N			
Bank 0-6 Sectors		Bank 7 Sectors	
Quantity	Size	Quantity	Size
112	32 Kwords	4	8 Kwords
		15	32 Kwords
56 Mbits		8 Mbits	

The VersatileIO™ (V_{IO}) control allows the host system to set the voltage levels that the device generates at its data outputs and the voltages tolerated at its data inputs to the same voltage level that is asserted on the V_{CCQ} pin.

The devices use Chip Enable (CE#), Write Enable (WE#), Address Valid (AVD#) and Output Enable (OE#) to control asynchronous read and write operations. For burst operations, the devices additionally require Ready (RDY) and Clock (CLK). This implementation allows easy interface with minimal glue logic to microprocessors/microcontrollers for high performance read operations.

The devices offer complete compatibility with the **JEDEC 42.4 single-power-supply Flash command set standard**. Commands are written to the command register using standard microprocessor write timings. Reading data out of the device are similar to reading from other Flash or EPROM devices.

The host system can detect whether a program or erase operation is complete by using the device **status bit** DQ7 (Data# Polling) and DQ6/DQ2 (toggle bits). After a program or erase cycle has been completed, the device automatically returns to reading array data.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The devices are fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The devices also offer three types of data protection at the sector level. **Persistent Sector Protection** provides in-system, command-enabled protection of any combination of sectors using a single power supply at V_{CC}. **Password Sector Protection** prevents unauthorized write and erase operations in any combination of sectors through a user-defined 64-bit password. When at V_{IL}, **WP#** locks the highest two sectors. Finally, when ACC is at V_{IL}, all sectors are locked.

The devices offer two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both modes.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm - an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The **Unlock Bypass** mode facilitates faster program times by requiring only two write cycles to program data instead of four. Additionally, **Write Buffer Programming** is available on this family of devices. This feature provides superior programming performance by grouping locations being programmed.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm - an internal algorithm that automatically preprograms the array (if it is not already fully programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The **Program Suspend/Program Resume** feature enables the user to put program on hold to read data from any sector that is not selected for programming. If a read is needed from the Persistent Protection area, Dynamic Protection area, or the CFI area, after an program suspend, then the user must use the proper command sequence to enter and exit this region. The program suspend/resume functionality is also available when programming in erase suspend (1 level depth only).

The **Erase Suspend/Erase Resume** feature enables the user to put erase on hold to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved. If a read is needed from the Persistent Protection area, Dynamic Protection area, or the CFI area, after an erase suspend, then the user must use the proper command sequence to enter and exit this region.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read boot-up firmware from the Flash memory device.

The host system can detect whether a memory array program or erase operation is complete by using the device status bit DQ7 (Data# Polling), DQ6/DQ2 (toggle bits), DQ5 (exceeded timing limit), DQ3 (sector erase start timeout state indicator), and DQ1 (write to buffer abort). After a program or erase cycle has been completed, the device automatically returns to reading array data.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. **The device is fully erased when shipped from the factory**.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The device also offers two types of data protection at the sector level. When at V_{IL}, **WP#** locks the two outermost boot sectors at the top of memory.

When the ACC pin = V_{IL}, the entire flash memory array is protected.

Spansion LLC Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector. The data is programmed using hot electron injection.

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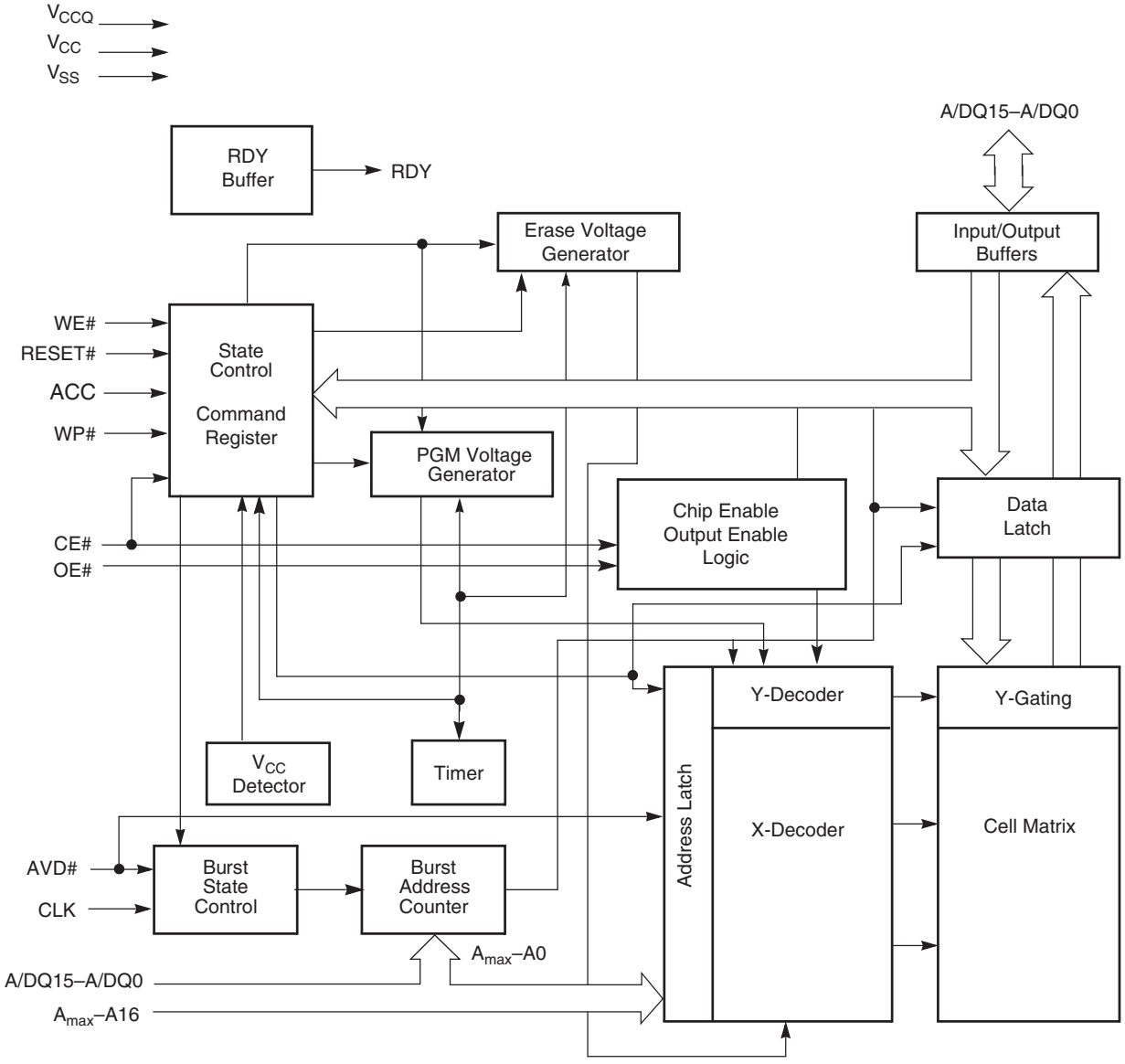
2. Product Selector Guide

Description	S29NS256N, S29NS128N, S29NS064N	
Burst Frequency	**80 MHz**	**66 MHz**
Max Initial Synchronous Access Time, ns (T_{IACC})	80	80
Max Burst Access Time, ns (T_{BACC})	9	11.0
Max Asynchronous Access Time, ns (T_{ACC})	80	80
Max CE# Access Time, ns (T_{CE})		
Max OE# Access Time, ns (T_{OE})	9	11.0

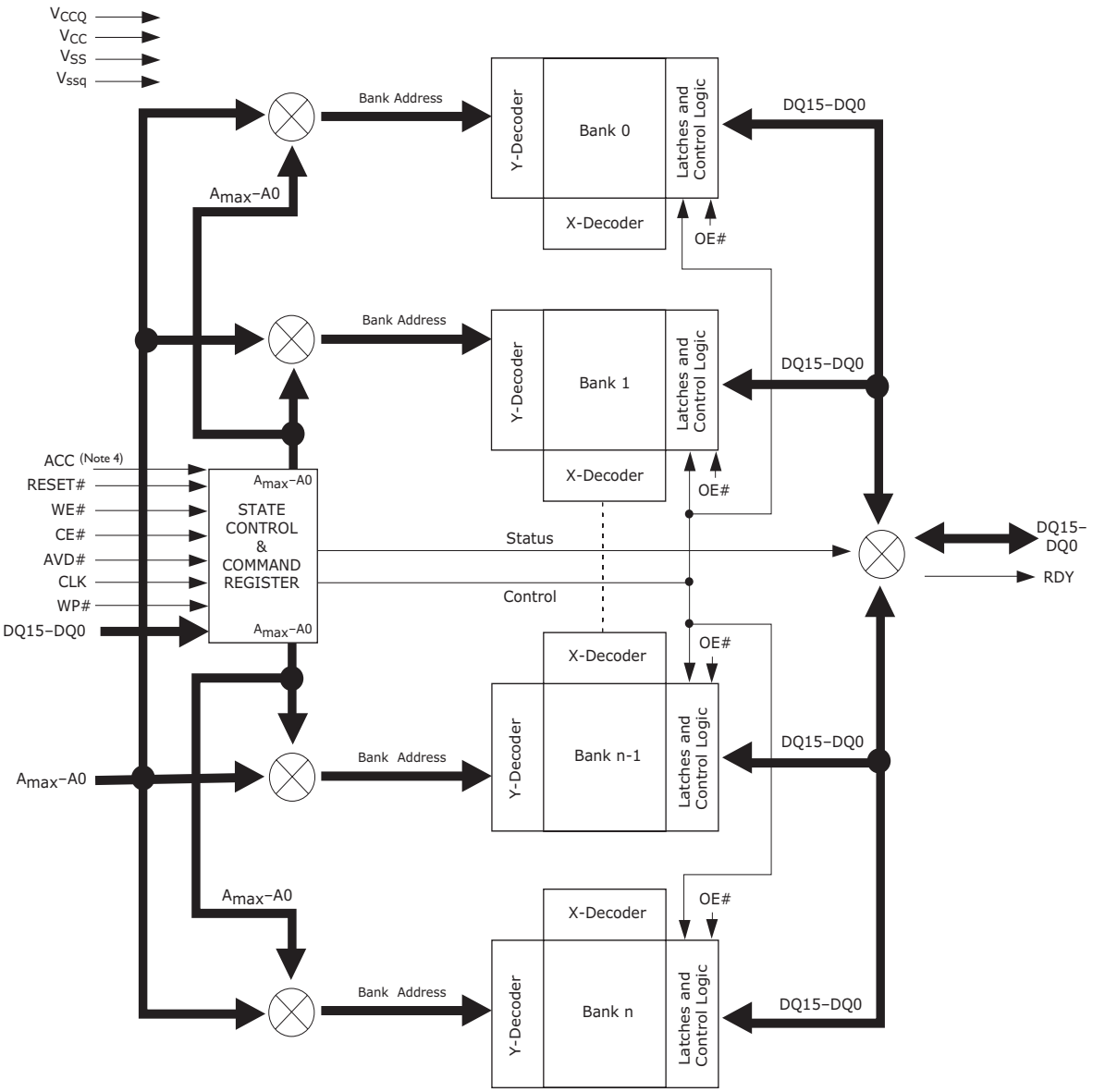
3. Block Diagram



Note

A_{max} indicates the highest order address bit. A_{max} equals A23 for NS256N, and A22 for NS128N and A21 for S29NS064N.

4. Block Diagram of Simultaneous Operation Circuit

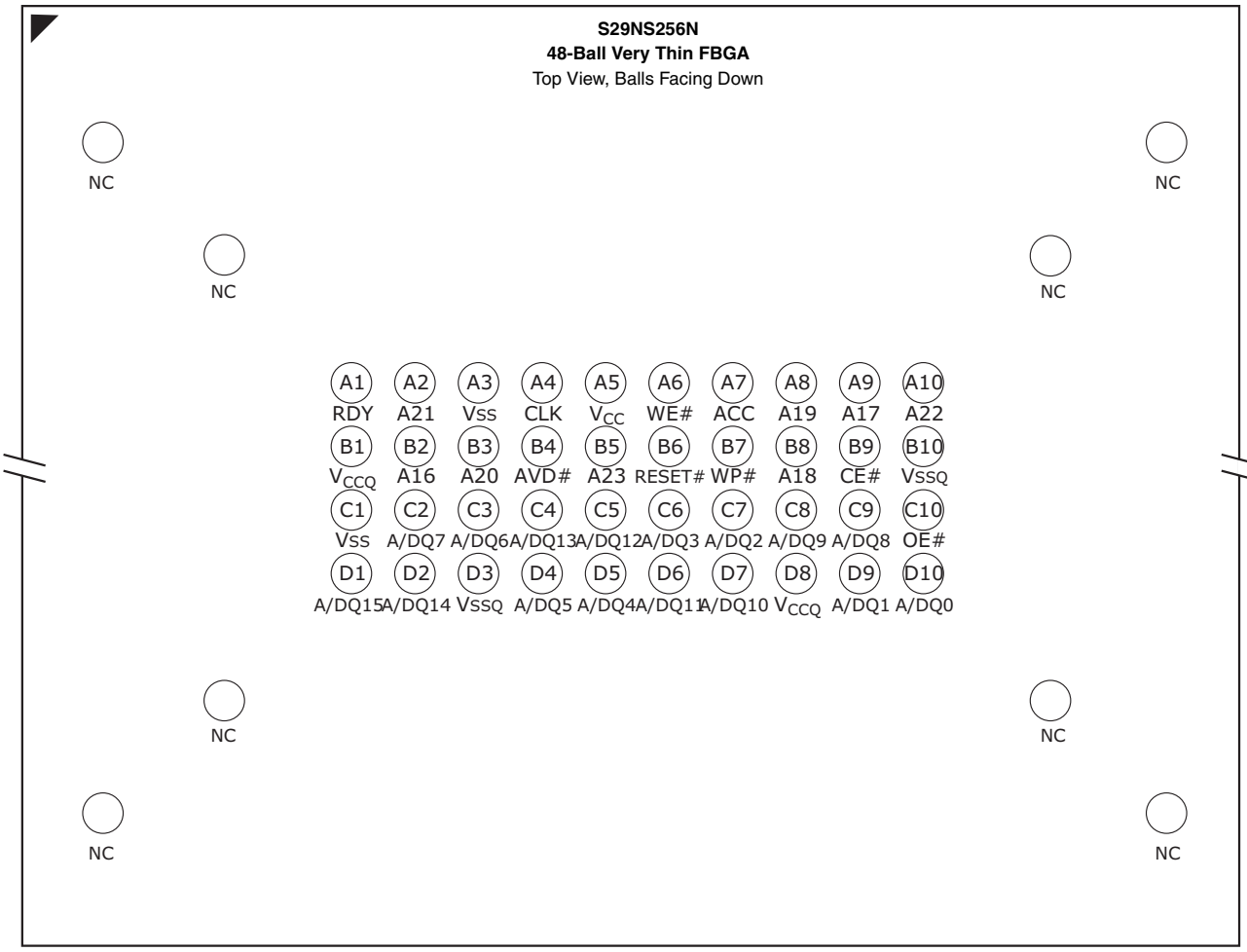


Notes

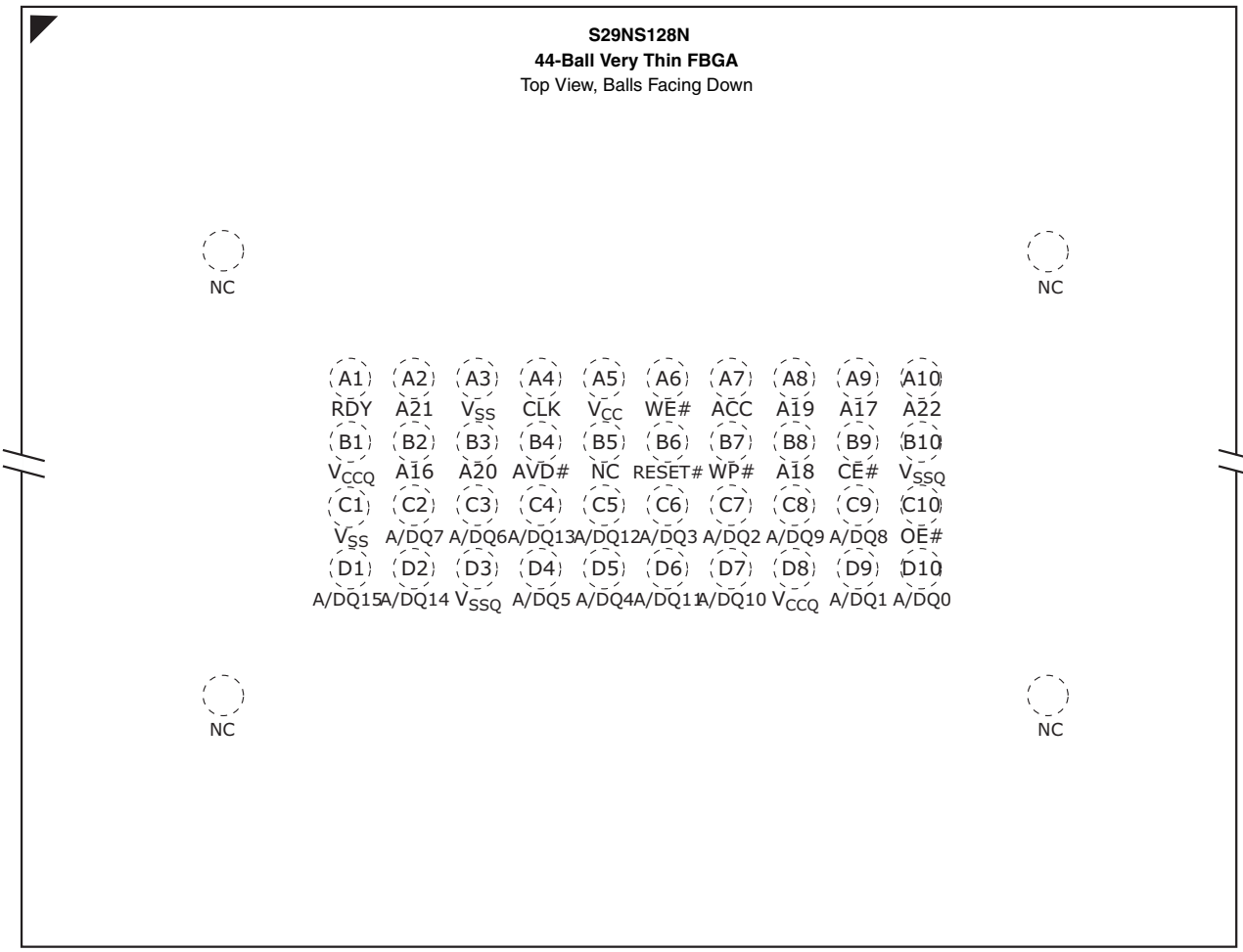
1. *A15–A0 are multiplexed with DQ15–DQ0.*
2. *Amax indicates the highest order address bit. A23 (NS256N), A22 (NS128N), and A21 (NS064N).*
3. *n = 15 for NS256N and NS128N, n = 7 for NS064N.*

5. Connection Diagram

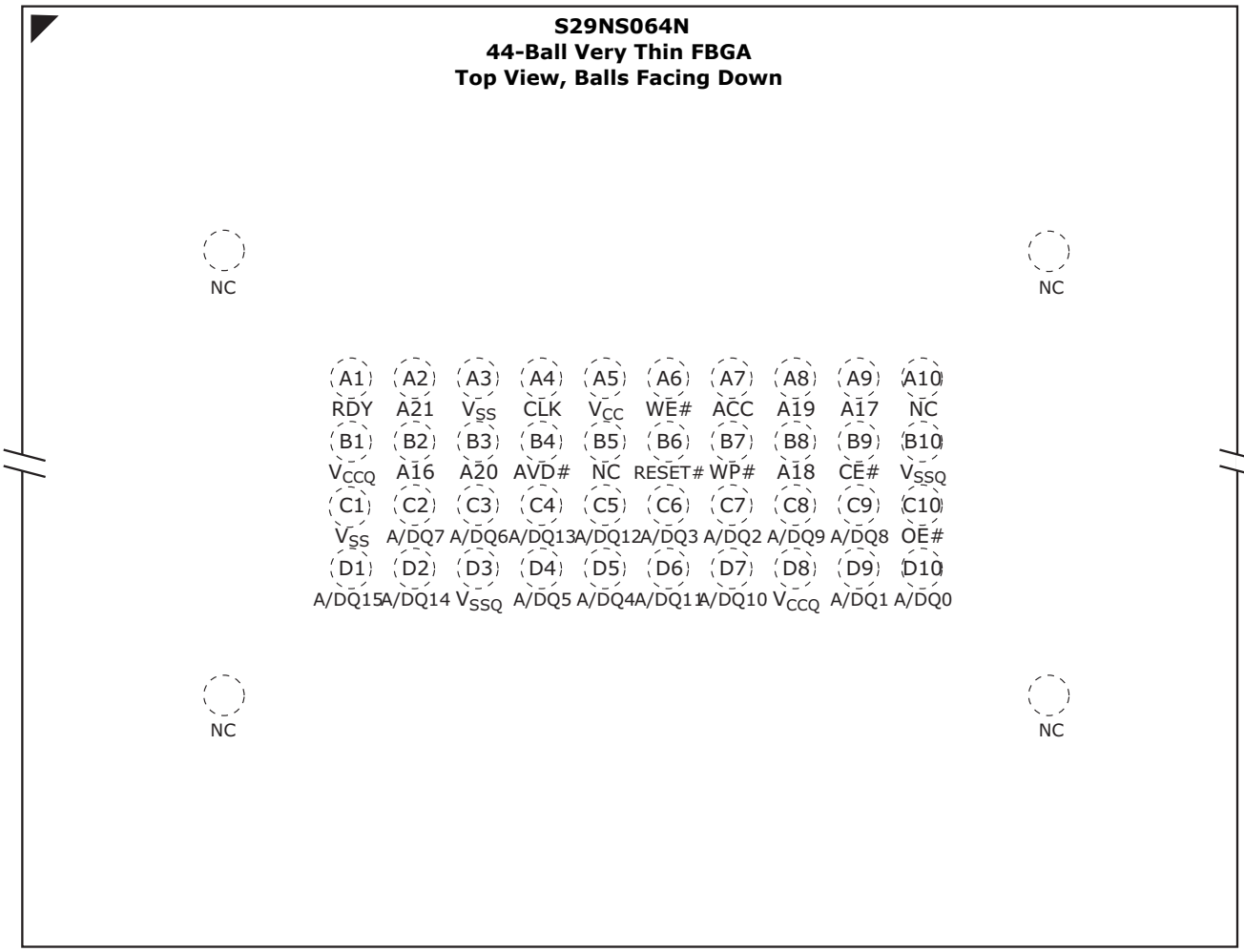
5.1 S29NS256N – 48-Ball Very Thin FBGA Connection Diagram



5.2 S29NS128N – 48-Ball Very Thin FBGA Connection Diagram



5.3 S29NS064N – 44-Ball Very Thin FBGA Connection Diagram



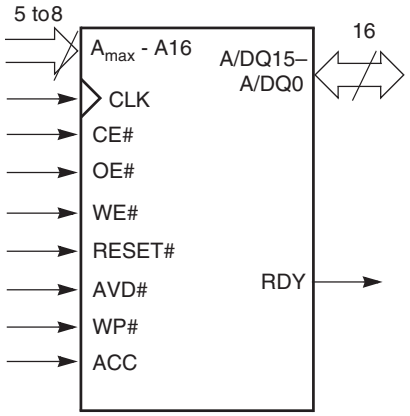
5.4 Special Package Handling Instructions

Special handling is required for Flash Memory products in FBGA packages.The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

6. Input/Output Descriptions

A23–A16	=	Address Inputs, S29NS256N
A22–A16	=	Address Inputs, S29NS128N
A21-A16	=	Address Inputs, S29NS064N
A/DQ15–A/DQ0	=	Multiplexed Address/Data input/output
CE#	=	Chip Enable Input. Asynchronous relative to CLK for the Burst mode
OE#	=	Output Enable Input. Asynchronous relative to CLK for the Burst mode
WE#	=	Write Enable Input
V_{CC}	=	Device Power Supply (1.70V–1.95V)
V_{CCQ}	=	Input/Output Power Supply (1.70V–1.95V)
V_{SS}	=	Ground
V_{SSQ}	=	Input/Output Ground
NC	=	No Connect; not connected internally
RDY	=	Ready output; indicates the status of the Burst read. V_{OL}= data invalid. V_{OH} = data valid
CLK	=	The first rising edge of CLK in conjunction with AVD# low latches address input and activates burst mode operation. After the initial word is output, subsequent rising edges of CLK increment the internal address counter. CLK should remain low during asynchronous access
AVD#	=	Address Valid input. Indicates to device that the valid address is present on the address inputs (address bits A15–A0 are multiplexed, address bits Amax–A16 are address only) V_{IL} = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched on rising edge of CLK. V_{IH}= device ignores address inputs
RESET#	=	Hardware reset input. V_{IL}= device resets and returns to reading array data
WP#	=	Hardware write protect input. V_{IL} = disables writes to SA257–258 (S29NS256N), SA129–130 (S29NS128N) or SA129-130 (S29NS064N). Should be at V_{IH} for all other conditions
ACC	=	At 9V, accelerates programming; automatically places device in unlock bypass mode. At V_{IL}, disables program and erase functions. Should be at V_{IH} for all other conditions

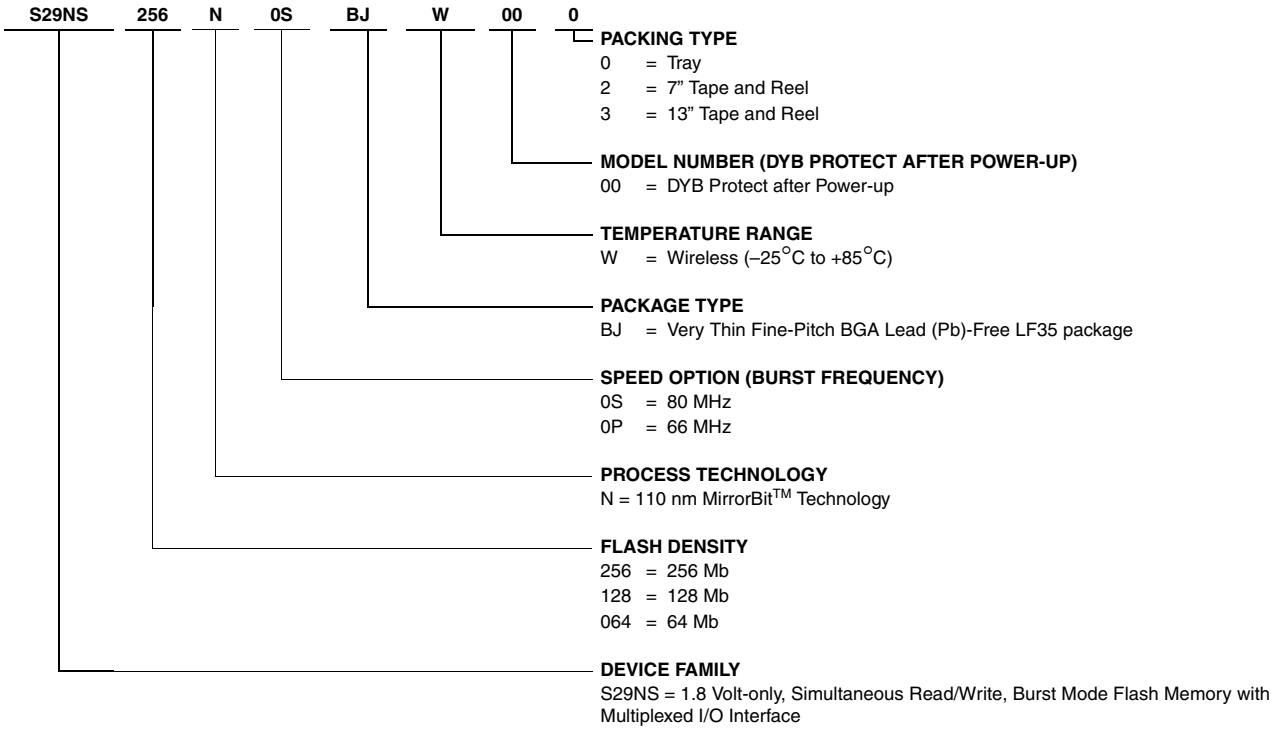
6.1 Logic Symbol



A_{max} indicates the highest order address bit.

7. Ordering Information

The order number (Valid Combination) is formed by the following:



7.1 Valid Combinations

Consult the local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

S29NSxxxN Valid Combinations				Package Marking	Speed Options (MHz)	Package Type
Base Ordering Part Number	Package & Temperature	Model Number	Packing Type (Note 1, 2)			
S29NS256N	BJW	00	0, 2, 3 (Note 1)	NS256N0SBJW00	80	48-ball FBGA 10mm x 11mm VCD048
				NS256N0PBJW00	66	
S29NS128N	BJW	00	0, 2, 3 (Note 1)	NS128N0SBJW00	80	44-ball FBGA 9.2mm x 8.0mm VDD044
				NS128N0PBJW00	66	
S29NS064N	BJW	00	0, 2, 3 (Note 1)	NS064N0SBJW00	80	44-ball FBGA 7.7mm x 6.2mm VDE044
				NS064N0PBJW00	66	

Notes

1. *Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading “S” and packing type designator from ordering part number.*

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

8. Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 8.1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 8.1 Device Bus Operations

Operation	CE#	OE#	WE#	A_{max}–16	A/DQ15–0	RESET#	CLK	AVD#
Asynchronous Read	L	L	H	Addr In	I/O	H	L	
Write	L	H	L	Addr In	I/O	H	H/L	
Standby (CE#)	H	X	X	X	HIGH Z	H	H/L	X
Hardware Reset	X	X	X	X	HIGH Z	L	X	X
Burst Read Operations								
Load Starting Burst Address	L	H	H	Addr In	Addr In	H		
Advance Burst to next address with appropriate Data presented on the Data Bus	L	L	H	X	Burst Data Out	H		H
Terminate current Burst read cycle	H	X	H	X	HIGH Z	H		X
Terminate current Burst read cycle via RESET#	X	X	H	X	HIGH Z	L	X	X
Terminate current Burst read cycle and start new Burst read cycle	L	H	H	X	I/O	H		

Legend

L = Logic 0, H = Logic 1, X = Don't Care.

Note

Terminating the current Burst cycle is determined by the falling edge of AVD#, while starting a new Burst read cycle is determined by the rising edge of AVD#.

8.1 VersatileIO™ (V_{IO}) Control

The VersatileIO (V_{IO}) control allows the host system to set the voltage levels that the device generates at its data outputs and the voltages tolerated at its data inputs to the same voltage level that is asserted on the V_{CCQ} pin.

8.2 Requirements for Asynchronous Read Operation (Non-Burst)

To read data from the memory array, the system must assert a valid address on A_{max}–A16 and A/DQ15–A/DQ0 while AVD# and CE# are at V_{IL}. WE# should remain at V_{IH}. Note that CLK must remain at V_{IL} during asynchronous read operations. The rising edge of AVD# latches the address, after which the system can drive OE# to V_{IL}. The data will appear on A/DQ15–A/DQ0. (See Figure 19.4 on page 67.) Since the memory array is divided into banks, each bank remains enabled for read access until the command register contents are altered.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from the stable addresses and stable CE# to valid data at the outputs. The output enable access time (t_{OE}) is the delay from the falling edge of OE# to valid data at the output.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition.

8.3 Requirements for Synchronous (Burst) Read Operation

The device is capable of seven different burst read modes: continuous burst read; 8-, 16-, and 32-word linear burst reads with wrap around; and 8-, 16-, and 32-word linear burst reads without wrap around.

8.3.1 Continuous Burst

When the device first powers up, it is enabled for asynchronous read operation. The device is automatically enabled for burst mode and addresses are latched on the first rising edge of CLK input, while AVD# is held low for one clock cycle.

Prior to activating the clock signal, the system should determine how many wait states are desired for the initial word (t_{IACC}) of each burst session. The system would then write the Set Configuration Register command sequence.

The initial word is output t_{IACC} after the rising edge of the first CLK cycle. Subsequent words are output t_{BACC} after the rising edge of each successive clock cycle, which automatically increments the internal address counter. **Note that the device has a fixed internal address boundary that occurs every 128 words, starting at address 00007Fh. The transition from the highest address 7FFFFFh to 000000h is also a boundary crossing**. During a boundary crossing, there is a no additional latency between the valid read at address 00007F and the valid read at address 000080 (or between addresses offset from these values by the same multiple of 128 words) for frequencies equal to or lower than 66 Mhz. For frequencies higher than 66 Mhz, there is a latency of 1 cycle.

During the time the device is outputting data with the starting burst address not divisible by four, additional waits are required. The RDY output indicates this condition to the system by deasserting.

Table 8.2 through Table 8.5 shows the address latency as a function of variable wait states.

Table 8.2 Address Latency for 7, 6, and 5 Wait States

Word										
0	7, 6, and 5 ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	1 ws	D4	D5	D6	D7	D8
2		D2	D3	1 ws	1 ws	D4	D5	D6	D7	D8
3		D3	1 ws	1 ws	1 ws	D4	D5	D6	D7	D8

Table 8.3 Address Latency for 4 Wait States

Word										
0	4 ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	D4	D5	D6	D7	D8	D9
2		D2	D3	1 ws	D4	D5	D6	D7	D8	D9
3		D3	1 ws	1 ws	D4	D5	D6	D7	D8	D9

Table 8.4 Address Latency for 3 Wait States

Word										
0	3 ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	D4	D5	D6	D7	D8	D9
2		D2	D3	D4	D5	D6	D7	D8	D9	D10
3		D3	1 ws	D4	D5	D6	D7	D8	D9	D10

Table 8.5 Address Latency for 2 Wait States

Word										
0	2 ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	D4	D5	D6	D7	D8	D9
2		D2	D3	D4	D5	D6	D7	D8	D9	D10
3		D3	D4	D5	D6	D7	D8	D9	D10	D11

Table 8.6 through Table 8.8 show the address/boundary crossing latency for variable wait state if a boundary crossing occurs during initial access

Table 8.6 Address/Boundary Crossing Latency for 7, 6, and 5 Wait States

Word										
0	7, 6, and 5 ws	D0	D1	D2	D3	1 ws	D4	D5	D6	D7
1		D1	D2	D3	1 ws	1 ws	D4	D5	D6	D7
2		D2	D3	1 ws	1 ws	1 ws	D4	D5	D6	D7
3		D3	1 ws	1 ws	1 ws	1 ws	D4	D5	D6	D7

Table 8.7 Address/Boundary Crossing Latency for 4 Wait States

Word										
0	4 ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	1 ws	D4	D5	D6	D7	D8
2		D2	D3	1 ws	1 ws	D4	D5	D6	D7	D8
3		D3	1 ws	1 ws	1 ws	D4	D5	D6	D7	D8

Figure 8.1 Address/Boundary Crossing Latency for 3 Wait States

Word										
0	3 ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	D4	D5	D6	D7	D8	D9
2		D2	D3	1 ws	D4	D5	D6	D7	D8	D9
3		D3	1 ws	1 ws	D4	D5	D6	D7	D8	D9

Table 8.8 Address/Boundary Crossing Latency for 2 Wait States

Word										
0	2 ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	D4	D5	D6	D7	D8	D9
2		D2	D3	D4	D5	D6	D7	D8	D9	D10
3		D3	1 ws	D4	D5	D6	D7	D8	D9	D10

The device will continue to output continuous, sequential burst data, wrapping around to address 000000h after it reaches the highest addressable memory location, until the system asserts CE# high, RESET# low, or AVD# low in conjunction with a new address. See Table 8.1 on page 14. The reset command does *not* terminate the burst read operation.

If the host system crosses a 128 word line boundary while reading in burst mode, and the device is not programming or erasing, no additional latency will occur as described above. If the host system crosses the bank boundary while the device is programming or erasing, the device will provide asynchronous read status information. The clock will be ignored. After the host has completed status reads, or the device has completed the program or erase operation, the host can restart a burst operation using a new address and AVD# pulse.

8.3.2 8-, 16-, and 32-Word Linear Burst with Wrap Around

These three modes are of the linear wrap around design, in which a fixed number of words are read from consecutive addresses. In each of these modes, the burst addresses read are determined by the group within which the starting address falls. The groups are sized according to the number of words read in a single burst sequence for a given mode (see Table 8.9.)

Table 8.9 Burst Address Groups

Mode	Group Size	Group Address Ranges
8-word	8 words	0-7h, 8-Fh, 10-17h, 18-1Fh...
16-word	16 words	0-Fh, 10-1Fh, 20-2Fh, 30-3Fh...
32-word	32 words	00-1Fh, 20-3Fh, 40-5Fh, 60-7Fh...

As an example: if the starting address in the 8-word mode is 3Ah, and the burst sequence would be 3A-3B-3C-3D-3E-3F-38-39h. The burst sequence begins with the starting address written to the device, but wraps back to the first address in the selected group. In a similar fashion, the 16-word and 32-word Linear Wrap modes begin their burst sequence on the starting address written to the device, and then wraps back to the first address in the selected address group and terminates the burst read. **Note that in these three burst read modes the address pointer does not cross the boundary that occurs every 128 words; thus, no wait states are inserted (except during the initial access).**

8.3.3 8-, 16-, and 32-Word Linear Burst without Wrap Around

In these modes, a fixed number of words (predefined as 8, 16, or 32 words) are read from consecutive addresses starting with the initial word, which is written to the device. When the address is at the end of the group address range (see Burst Address Groups Table), the burst read operation stops and the RDY output goes low. There is no group limitation and is different from the Linear Burst with Wrap Around.

As an example, for 8-word length Burst Read, if the starting address written to the device is 3A, the burst sequence would be 3A-3B-3C-3D-3E-3F-40-41h, and the read operation will be terminated after all eight words. The 16-word and 32-word modes would operate in a similar fashion and continuously read to the predefined 16 or 32 words accordingly. **Note: In this burst read mode, the address pointer may cross the boundary that occurs every 128 words.**

8.4 Programmable Wait State

The programmable wait state feature indicates to the device the number of additional clock cycles that must elapse after AVD# is driven active before data will be available. Upon power up, the device defaults to the maximum of seven total cycles. The total number of wait states is programmable from two to seven cycles. For further details, see *Set Configuration Register Command Sequence* *on page 37*.

8.5 Configuration Register

The device uses a configuration register to set the various burst parameters: number of wait states, burst read mode, burst length, RDY configuration, and synchronous mode active.

8.6 Handshaking Feature

The handshaking feature allows the host system to simply monitor the RDY signal from the device to determine when the initial word of burst data is ready to be read. The host system should use the configuration register to set the number of wait states for optimal burst mode operation. The initial word of burst data is indicated by the rising edge of RDY after OE# goes low.

8.7 Simultaneous Read/Write Operations with Zero Latency

This device is capable of reading data from one bank of memory while programming or erasing in one of the other banks of memory. An erase operation may also be suspended to read from or program to another location within the same bank (except the sector being erased). Figure 19.13 on page 75 shows how read and write cycles may be initiated for simultaneous operation with zero latency. Refer to the table *DC Characteristics on page 62* for read-while-program and read-while-erase current specifications.

8.8 Writing Commands/Command Sequences

The device has inputs/outputs that accept both address and data information. To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive AVD# and CE# to V_{IL}, and OE# to V_{IH} when providing an address to the device, and drive WE# and CE# to V_{IL}, and OE# to V_{IH}. when writing commands or data.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word, instead of four.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 14-17 indicates the address space that each sector occupies. The device address space is divided into multiple banks. A “bank address” is the address bits required to uniquely select a bank. Similarly, a “sector address” is the address bits required to uniquely select a sector.

Refer to the DC Characteristics table for write mode current specifications. The section *AC Characteristics on page 64* contains timing specification tables and timing diagrams for write operations.

8.9 Accelerated Program and Erase Operations

The device offers accelerated program and erase operation through the ACC function. ACC is primarily intended to allow faster manufacturing throughput at the factory and not to be used in system operations.

If the system asserts V_{HH} on this input, the device automatically enters the aforementioned Unlock Bypass mode and uses the higher voltage on the input to reduce the time required for program and erase operations. The system can then use the abbreviated Embedded Programming command and Write Buffer Load command sequence provided by the Unlock Bypass mode. Note that if a “Write-to-Buffer-Abort Reset” is required while in Unlock Bypass mode, the **full 3-cycle RESET command sequence must be used to reset the device**. Removing V_{HH} from the ACC input, upon completion of the embedded program or erase operation, returns the device to normal operation. Note that sectors must be unlocked prior to raising ACC to V_{HH}. *Note that the ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result. In addition, the ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result*.

When at V_{IL}, ACC locks all sectors. ACC should be at V_{IH} for all other conditions.

8.10 Write Buffer Programming Operation

Write Buffer Programming allows the system to write a maximum of **32** words in one programming operation. This results in a faster effective word programming time than the standard “word” programming algorithms. The Write Buffer Programming command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the Write Buffer Load command written at the Sector Address in which programming will occur. At this point, the system writes the number of “**word locations minus 1**” that will be loaded into the page buffer at the Sector Address in which programming will occur. This tells the device how many write buffer addresses will be loaded with data and therefore when to expect the “Program Buffer to Flash” confirm command. The number of locations to program cannot exceed the size of the write buffer or the operation will abort. (NOTE: The number loaded = the number of locations to program minus 1. For example, if the system will program 6 address locations, then 05h should be written to the device.)

The system then writes the starting address/data combination. This starting address is the first address/data pair to be programmed, and selects the “write-buffer-page” address. All subsequent address/data pairs **must** fall within the “selected-write-buffer-page”, and be loaded in sequential order.

The “write-buffer-page” is selected by using the addresses A_{MAX}-A5 where A_{MAX} is A23 for S29NS256N, A22 for S29NS128N and A21 for S29NS064N.

The “write-buffer-page” addresses **must be the same for all address/data pairs loaded into the write buffer**. (This means Write Buffer Programming **cannot** be performed across multiple “write-buffer-pages”. This also means that Write Buffer Programming **cannot** be performed across multiple sectors. If the system attempts to load programming data outside of the selected “write-buffer-page”, the operation will ABORT.)

After writing the Starting Address/Data pair, the system then writes the remaining address/data pairs into the write buffer. Write buffer locations must be loaded in sequential order.

Note that if a Write Buffer address location is loaded multiple times, the “address/data pair” counter **will be decremented for every data load operation**. Also, the **last data loaded** at a location before the “Program Buffer to Flash” confirm command will be programmed into the device. It is the software’s responsibility to comprehend ramifications of loading a write-buffer location more than once. The counter decrements **for each data load operation**, **NOT for each unique write-buffer-address location**.

Once the specified number of write buffer locations have been loaded, the system must then write the “Program Buffer to Flash” command at the Sector Address. Any other address/data write combinations will abort the Write Buffer Programming operation. The device will then “go busy”. The Data Bar polling techniques should be used while monitoring the **last address location loaded into the write buffer**. This eliminates the need to store an address in memory because the system can load the last address location, issue the program confirm command at the last loaded address location, and then data bar poll at that same address. DQ7, DQ6, DQ5, DQ2, and DQ1 should be monitored to determine the device status during Write Buffer Programming.

The write-buffer “embedded” programming operation can be suspended using the standard suspend/resume commands. Upon successful completion of the Write Buffer Programming operation, the device will return to READ mode.

The Write Buffer Programming Sequence can be ABORTED under any of the following conditions:

- Load a value that is greater than the page buffer size during the “Number of Locations to Program” step.
- Write to an address in a sector different than the one specified during the “Write-Buffer-Load” command.
- Write an Address/Data pair to a different write-buffer-page than the one selected by the “Starting Address” during the “write buffer data loading” stage of the operation.
- Write data other than the “Confirm Command” after the specified number of “data load” cycles.

The ABORT condition is indicated by DQ1 = 1, DQ7 = DATA# (for the “last address location loaded”), DQ6 = TOGGLE, DQ5 = 0. This indicates that the Write Buffer Programming Operation was ABORTED. A “Write-to-Buffer-Abort reset” command sequence is required when using the Write-Buffer-Programming features in Unlock Bypass mode. **Note: The Secured Silicon sector, autoselect, and CFI functions are unavailable when a program operation is in progress**.

Use of the write buffer is strongly recommended for programming when multiple words are to be programmed. Write buffer programming is allowed in any sequence of memory (or address) locations. These flash devices are capable of handling multiple write buffer programming operations on the same write buffer address range without intervening erases. However, programming the same word address multiple times without intervening erases requires a modified programming method. Please contact your local Spansion™ representative for details.

8.11 Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output from the internal register (which is separate from the memory array) on DQ15–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. The autoselect codes can also be accessed in-system.

When verifying sector protection, the sector address must appear on the appropriate highest order address bits. The remaining address bits are don’t care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ15–DQ0. The autoselect codes can also be accessed in-system through the command register. The command sequence is illustrated in Table 11.4, *Command Definitions on page 52*. *Note that if a Bank Address (BA) on address bits A23, A22, A21, and A20 for the NS256N, A22, A21, A20, A19 for the NS128N and A21, A20, and A19 for the NS064N, is asserted during the third write cycle of the autoselect command, the host system can read autoselect data that bank and then immediately read array data from the other bank, without exiting the autoselect mode.*

To access the autoselect codes, the host system must issue the autoselect command via the command register, as shown in Table 11.4, *Command Definitions on page 52*.

8.12 Advanced Sector Protection and Unprotection

This advanced security feature provides an additional level of protection to all sectors against inadvertent program or erase operations.

The advanced sector protection feature disables both programming and erase operations in any sector while the advanced sector unprotection feature re-enables both program and erase operations in previously protected sectors. Sector protection/unprotection can be implemented using either of the two methods

- Hardware method
- Software method

Persistent/Password Sector Protection is achieved by using the software method while the sector protection with WP# pin is achieved by using the hardware method.

All parts default to operate in the Persistent Sector Protection mode. The customer must then choose if the Persistent or Password Protection method is most desirable. There are two one-time programmable non-volatile bits that define which sector protection method will be used.

- Persistent Mode Lock Bit
- Password Mode Lock Bit

If the customer decides to continue using the Persistent Sector Protection method, they must set the **Persistent Mode Lock Bit**. This will permanently set the part to operate only using Persistent Sector Protection. However, if the customer decides to use the Password Sector Protection method, they must set the **Password Mode Lock Bit**. This will permanently set the part to operate only using Password Sector Protection.

It is important to remember that setting either the **Persistent Mode Lock Bit** or the **Password Mode Lock Bit** permanently selects the protection mode. It is not possible to switch between the two methods once a locking bit has been set. **It is important that one mode is explicitly selected when the device is first programmed, rather than relying on the default mode alone. If both are selected to be set at the same time, the operation will abort.** This is done so that it is not possible for a system program or virus to later set the Password Mode Locking Bit, which would cause an unexpected shift from the default Persistent Sector Protection Mode into the Password Sector Protection Mode.

The device is shipped with all sectors unprotected. Spansion offers the option of programming and protecting sectors at the factory prior to shipping the device through Spansion programming services. Contact an Spansion representative for details.

8.13 Sector Protection

The device features several levels of sector protection, which can disable both the program and erase operations in certain sectors.

- Persistent Sector Protection

A software enabled command sector protection method that replaces the old 12 V controlled protection method.

- Password Sector Protection

A highly sophisticated software enabled protection method that requires a password before changes to certain sectors or sector groups are permitted

- WP# Hardware Protection

A write protect pin (WP#) can prevent program or erase operations in the outermost sectors.The WP# Hardware Protection feature is always available, independent of the software managed protection method chosen.

8.14 Persistent Sector Protection

The Persistent Sector Protection method replaces the old 12 V controlled protection method while at the same time enhancing flexibility by providing three different sector protection states:

- **Persistently Locked**—A sector is protected and cannot be changed.
- **Dynamically Locked**—The sector is protected and can be changed by a simple command
- **Unlocked**—The sector is unprotected and can be changed by a simple command

In order to achieve these states, three types of “bits” namely Persistent Protection Bit (PPB), Dynamic Protection Bit (DYB), and Persistent Protection Bit Lock (PPB Lock) are used to achieve the desired sector protection scheme:

8.14.1 Persistent Protection Bit (PPB)

PPB is used to as an advanced security feature to protect individual sectors from being programmed or erased thereby providing additional level of protection. Every sector is assigned a Persistent Protection Bit.

Each PPB is individually programmed through the **PPB Program Command**. However all PPBs are erased in parallel through the **All PPB Erase Command**. Prior to erasing, these bits don’t have to be pre programmed. The Embedded Erase algorithm automatically preprograms and verifies prior to an electrical erase. The system is not required to provide any controls or timings during these operations.

The PPBs retain their state across power cycles because they are Non-Volatile. The PPBs has the same endurance as the flash memory.

8.14.2 Persistent Protection Bit Lock (PPB Lock Bit) in Persistent Sector Protection Mode

PPB Lock Bit is a global volatile bit and provides an additional level of protection to the sectors. When **programmed (set to “0”)**, all the PPBs are locked and hence none of them can be changed. When **erased (cleared to “1”)**, the PPBs are changeable. There is only one PPB Lock Bit in every device. Only a hardware reset or a power-up clears the PPB Lock Bit. It is to be noted that there is no software solution, i.e. command sequence to unlock the PPB Lock Bit.

Once all PPBs are configured to the desired settings, the PPB Lock Bit may be set (programmed to “0”). The PPB Lock Bit is set by issuing the PPB Lock Bit Set Command. Programming or setting the PPB Lock Bit disables program and erase commands to all the PPBs. In effect, the PPB Lock Bit locks the PPBs into their current state. The only way to clear the PPB Lock Bit is to go through a hardware or power-up reset. System boot code can determine if any changes to the PPB are needed e.g. to allow new system code to be downloaded. If no changes are needed then the boot code can disable the PPB Lock Bit to prevent any further changes to the PPBs during system operation.

8.14.3 Dynamic Protection Bit (DYB)

DYB is a security feature used to protect individual sectors from being programmed or erased inadvertently. It is a volatile protection bit and is assigned to each sector. Upon power-up, the contents of all DYBs are set (programmed to “0”). Each DYB can be individually modified through the DYB Set Command or the DYB Clear Command.

The Protection Status for a particular sector is determined by the status of the PPB and the DYB relative to that sector. For the sectors that have the PPBs cleared (erased to “1”), the DYBs control whether or not the sector is protected or unprotected. By issuing the DYB Set or Clear command sequences, the DYBs will be set (programmed to “0”) or cleared (erased to “1”), thus placing each sector in the protected or unprotected state respectively. These states are the so-called Dynamic Locked or Unlocked states due to the fact that they can switch back and forth between the protected and unprotected states. This feature allows software to easily protect sectors against inadvertent changes yet does not prevent the easy removal of protection when changes are needed. The DYBs maybe set (programmed to “0”) or cleared (erased to “1”) as often as needed.

When the parts are first shipped, the PPBs are cleared (erased to “1”) and upon power up or reset, the DYBs are set (programmed to “0”). The PPB Lock Bit defaults to the cleared state (erased to “1”) after power up and the PPBs retain their previous state as they are non-volatile.

Note: Dynamic protection bits revert back to their default values after programming device's "Lock Register."

It is possible to have sectors that have been persistently locked, and sectors that are left in the dynamic state. The sectors in the dynamic state are all unprotected. If there is a need to protect some of them, a simple DYB Set command sequence is all that is necessary. The DYB Set or Clear command for the dynamic sectors signify protected or unprotected state of the sectors respectively. However, if there is a need to change the status of the persistently locked sectors, a few more steps are required. First, the PPB Lock Bit must be cleared by either putting the device through a power-cycle, or hardware reset. The PPBs can then be changed to reflect the desired settings. Setting the PPB Lock Bit once again will lock the PPBs, and the device operates normally again.

Note: To achieve the best protection, it's recommended to execute the PPB Lock Bit Set command early in the boot code, and protect the boot code by holding WP# = V_{IL}. Note that the PPB and DYB bits have the same function when ACC = V_{HH} as they do when ACC = V_{IH}.

Table 8.10 Sector Protection Schemes

DYB	PPB	PPB Lock	Sector State
1	1	1	Sector Unprotected
0	1	1	Sector Protected through DYB
1	0	1	Sector Protected through PPB
0	0	1	Sector Protected through PPB and DYB
1	1	0	Sector Unprotected
0	1	0	Sector Protected through DYB
1	0	0	Sector Protected through PPB
0	0	0	Sector Protected through PPB and DYB

Table 8.10 contains all possible combinations of the DYB, PPB, and PPB Lock relating to the status of the sector.

In summary, if the PPB is set (programmed to "0"), and the PPB Lock is set (programmed to "0"), the sector is protected and the protection can not be removed until the next power cycle clears (erase to "1") the PPB Lock Bit. Once the PPB Lock Bit is cleared (erased to "1"), the sector can be persistently locked or unlocked. Likewise, if both PPB Lock Bit or PPB is cleared (erased to "1") the sector can then be dynamically locked or unlocked. The DYB then controls whether or not the sector is protected or unprotected.

If the user attempts to program or erase a protected sector, the device ignores the command and returns to read mode. A program or erase command to a protected sector enables status polling and returns to read mode without having modified the contents of the protected sector.

The programming of the DYB, PPB, and PPB Lock for a given sector can be verified by writing individual status read commands DYB Status, PPB Status, and PPB Lock Status to the device.

8.15 Persistent Sector Protection Mode Lock Bit

A Persistent Mode Lock Bit exists to guarantee that the device remain in software sector protection. Once programmed (set to "0"), the Persistent Mode Lock Bit prevents programming of the Password Mode Lock Bit. This guarantees that now, a hacker cannot place the device in Password Sector Protection Mode.

8.16 Password Sector Protection

The Password Sector Protection Mode method allows an even higher level of security than the Persistent Sector Protection Mode. There are two main differences between the Persistent Sector Protection Mode and the Password Sector Protection Mode:

- When the device is first powered up, or comes out of a reset cycle, the **PPB Lock Bit is set to the locked state**, rather than cleared to the unlocked state.
- The only means to clear the PPB Lock Bit is by writing a unique **64-bit Password** to the device.

The Password Sector Protection method is otherwise identical to the Persistent Sector Protection method.

A 64-bit password is the only additional tool utilized in this method.

The password is stored in a **one-time programmable (OTP)** region of the flash memory. Once the Password Mode Lock Bit is set, the password is permanently set with no means to read, program, or erase it. The password is used to clear the PPB Lock Bit. The Password Unlock command must be written to the flash, along with a password. The flash device internally compares the given password with the pre-programmed password. If they match, the PPB Lock Bit is cleared, and the PPBs can be altered. If they do not match, the flash device does nothing. There is a built-in 1 µs delay for each “password check.” This delay is intended to thwart any efforts to run a program that tries all possible combinations in order to crack the password.

8.17 64-bit Password

The 64-bit Password is located in a non-erasable region of the FLash and is accessible through the use of the Password Program and Verify commands (see *Password Protection Command Set Definitions* *on page 48*). The password function works in conjunction with the Password Mode Locking Bit, which when set, prevents the Password Verify command from reading the contents of the password on the pins of the device.

8.18 Password Mode Lock Bit

In order to select the Password Sector Protection scheme, the customer must first program the password. Spansion LLC recommends that the password be somehow correlated to the unique Electronic Serial Number (ESN) of the particular flash device. Each ESN is different for every flash device; therefore each password should be different for every flash device. While programming in the password region, the customer may perform Password Verify operations.

Once the desired password is programmed in, the customer must then set the Password Mode Locking Bit. This operation achieves two objectives:

- It permanently sets the device to operate using the Password Sector Protection Mode. It is not possible to reverse this function.
- It also disables *all further commands* to the password region. All program and read operations are ignored.

Both of these objectives are important, and if not carefully considered, may lead to unrecoverable errors. The user must be sure that the Password Sector Protection method is desired when setting the Password Mode Locking Bit. More importantly, the user must be sure that the password is correct when the Password Mode Locking Bit is set. Due to the fact that read operations are disabled, there is no means to verify what the password is afterwards. If the password is lost after setting the Password Mode Lock Bit, there will be no way to clear the PPB Lock Bit.

The Password Mode Lock Bit, once set, prevents reading the 64-bit password on the DQ bus and further password programming. **The Password Mode Lock Bit is not erasable.** Once Password Mode Lock Bit is programmed, the Persistent Mode Lock Bit is disabled from programming, guaranteeing that no changes to the protection scheme are allowed.

8.19 Persistent Protection Bit Lock (PPB Lock Bit) in Password Sector Protection Mode

The Persistent Protection Bit Lock (PPB Lock Bit) is a volatile bit that reflects the state of the Password Mode Lock Bit after power-up reset. If the Password Mode Lock Bit is also set, after a hardware reset (RESET# asserted) or a power-up reset, the ONLY means for clearing the PPB Lock Bit in Password Protection Mode is to issue the Password Unlock command. Successful execution of the Password Unlock command to enter the entire password clears the PPB Lock Bit, allowing for sector PPBs modifications. Asserting RESET#, taking the device through a power-on reset, or issuing the PPB Lock Bit Set command sets the PPB Lock Bit to a “1”.

If the Password Mode Lock Bit is not set (device is operating in the default Persistent Protection Mode). The Password Unlock command is ignored in Persistent Sector Protection Mode.

8.20 Hardware Data Protection Mode

The device offers two types of data protection at the sector level:

1. When WP# is at V_{IL}, the two outermost sectors at the top are locked (device specific).

1. When ACC is at V_{IL}, all sectors are locked.
   SA257 and SA258 are locked (S29NS256N)
   SA129 and SA130 are locked (S29NS128N)
   SA129 and SA130 are locked (S29NS064N)

The write protect pin (WP#) adds a final level of hardware program and erase protection to the boot sectors. The boot sectors are the two sectors containing the highest set of addresses in these top-boot-configured devices. For the none boot option, the WP# hardware feature is not available. **When this pin is low it is not possible to change the contents of these top sectors.** These sectors generally hold system boot code. So, the WP# pin can prevent any changes to the boot code that could override the choices made while setting up sector protection during system initialization.

The following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

8.20.1 Write Protect (WP#)

The Write Protect feature provides a hardware method of protecting the two outermost sectors. This function is provided by the WP# pin and overrides the previously discussed Sector Protection/Unprotection method.

If the system asserts V_{IL} on the WP# pin, the device disables program and erase functions in the “top” boot sectors. If the system asserts V_{IH} on the WP# pin, the device reverts to whether the boot sectors were last set to be protected or unprotected. That is, sector protection or unprotection for these sectors depends on whether they were last protected or unprotected.

8.21 WP# Boot Sector Protection

The WP# signal will be latched at a specific time in the embedded program or erase sequence. To prevent a write to the top two sectors, WP# must be asserted (WP#=V_{IL}) on the last write cycle of the embedded sequence (i.e., 4th write cycle in embedded program, 6th write cycle in embedded erase).

If selecting multiple sectors for erasure: The WP# protection status is latched only on the 6th write cycle of the embedded sector erase command sequence when the first sector is selected. If additional sectors are selected for erasure, they are subject to the WP# status that was latched on the 6th write cycle of the command sequence.

Note that the WP# pin must not be left floating or unconnected; inconsistent behavior of the device may result.

8.22 Low VCC Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to reading array data. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control inputs to prevent unintentional writes when VCC is greater than VLKO.

8.23 Write Pulse “Glitch” Protection

Noise pulses of less than t_{WEP} on WE# do not initiate a write cycle.

8.24 Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

8.24.1 Power-Up Write Inhibit

If WE# = CE# = RESET# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up

8.25 Lock Register

The Lock Register consists of 3 bits. Each of these bits are non-volatile and read-only. DQ15-DQ3 are reserved and are undefined.

Table 8.11 Lock Register

DQ15-DQ3	DQ2	DQ1	DQ0
Undefined	Password Protection Mode Lock Bit	Persistent Protection Mode Lock Bit	Secured Silicon Sector Protection Bit

Note
When the device lock register is programmed (PPB mode lock bit is programmed, password mode lock bit programmed, or the Secured Silicon lock bit is programmed) all DYBs revert to the power-on default state.

8.26 Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# inputs are both held at V_{CC}. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in the *DC Characteristics* table represents the standby current specification.

8.27 Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enters this mode when addresses and clock remain stable for t_{ACC} + 20 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC4} in the *DC Characteristics* table represents the automatic sleep mode current specification.

8.28 RESET#: Hardware Reset Input

The RESET# input provides a hardware method of resetting the device to reading array data. When RESET# is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all outputs, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS}, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within V_{SS}, the standby current will be greater.

RESET# may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

Refer to the *AC Characteristics* tables for RESET# parameters and to Figure 19.5 on page 68 for the timing diagram.

8.28.1 V_{CC} Power-up and Power-down Sequencing

The device imposes no restrictions on V_{CC} power-up or power-down sequencing. Asserting RESET# to V_{IL} is required during the entire V_{CC} power sequence until the respective supplies reach their operating voltages. Once V_{CC} attains its operating voltage, de-assertion of RESET# to V_{IH} is permitted.

8.29 Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The outputs are placed in the high impedance state.

8.30 Secured Silicon Sector SectorFlash Memory Region

The Secured Silicon Sector feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The Secured Silicon Sector is 256 words in length. All reads outside of the 256 word address range will return non-valid data. The Factory Indicator Bit (DQ7) is used to indicate whether or not the Factory Secured Silicon Sector is locked when shipped from the factory. The Customer Indicator Bit (DQ6) is used to indicate whether or not the Customer Secured Silicon Sector is locked when shipped from the factory. The Factory Secured Silicon bits are permanently set at the factory and cannot be changed, which prevents cloning of a factory locked part. This ensures the security of the ESN and customer code once the product is shipped to the field.

Spansion offers the device with a Factory Secured Silicon Sector that is locked and a Customer Secured Silicon Sector that is either locked or is lockable. The Factory Secured Silicon Sector is always protected when shipped from the factory, and has the Factory Indicator Bit (DQ7) permanently set to a "1". The Customer Secured Silicon Sector is shipped unprotected, allowing customers to utilize that sector in any manner they choose. Once the Customer Secured Silicon Sector area is protected, the Customer Indicator Bit will be permanently set to "1."

The system accesses the Secured Silicon Sector through a command sequence (see *Enter/Exit Secured Silicon Sector Command Sequence* *on page 40*). After the system has written the Enter Secured Silicon Sector command sequence, it may read the Secured Silicon Sector by using the addresses normally occupied by sector SA0 of the memory array. This mode of operation continues until the system issues the Exit Secured Silicon Sector command sequence, or until power is removed from the device. While Secured Silicon Sector access is enabled, Memory Array read access, program operations, and erase operations to all sectors other than SA0 are also available. On power-up, or following a hardware reset, the device reverts to sending commands to the normal address space.

8.30.1 Factory Locked: Factor Secured Silicon Sector Programmed and Protected At the Factory

In a factory sector locked device, the Factory Secured Silicon Sector is protected when the device is shipped from the factory. The Factory Secured Silicon Sector cannot be modified in any way. The device is pre programmed with both a random number and a secure ESN. The Factory Secured Silicon Sector is located at addresses 000000h–00007Fh.

The device is available pre programmed with one of the following:

- A random, secure ESN only within the Factor Secured Silicon Sector
- Customer code within the Customer Secured Silicon Sector through the Spansion™ programming services
- Both a random, secure ESN and customer code through the Spansion™ programming services.

Table 8.12 Secured Silicon SectorSecure Sector Addresses

Sector	Sector Size	Address Range
Customer	128 words	000080h-0000FFh
Factory	128 words	000000h-00007Fh

Customers may opt to have their code programmed by Spansion through the Spansion™ programming services. Spansion programs the customer's code, with or without the random ESN. The devices are then shipped from Spansion's factory with the Factory Secured Silicon Sector and Customer Secured Silicon Sector permanently locked. Contact an Spansion representative for details on using Spansion's Spansion™ programming services.

8.30.2 Customer Secured Silicon Sector

If the security feature is not required, the Customer Secured Silicon SectorSecure Sector can be treated as an additional Flash memory space. The Customer Secured Silicon Sector can be read any number of times, but can be programmed and locked only once. Note that the accelerated programming (ACC) and unlock bypass functions are not available when programming the Customer Secured Silicon Sector, but reading the first Bank through the last bank is available. The Customer Secured Silicon Sector is located at addresses 000080h–0000FFh.

The Customer Secured Silicon Sector area can be protected by writing the Secured Silicon Sector Protection Bit Lock command sequence.

Once the Customer Secured Silicon Sector is locked and verified, the system must write the Exit Secured Silicon Sector Region command sequence to return to reading and writing SA0 in the memory array.

The Customer Secured Silicon Sector lock must be used with caution since, once locked, there is no procedure available for unlocking the Customer Secured Silicon Sector area and none of the bits in the Customer Secured Silicon Sector memory space can be modified in any way.

9. Common Flash Memory Interface (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 9.1–9.5. To terminate reading CFI data, the system must write the reset command.

For further information, please refer to the CFI Specification and CFI Publication 100, available via the World Wide Web at http://www.amd.com/flash/cfi. Alternatively, contact the local sales representative for copies of these documents.

Table 9.1 CFI Query Identification String

Addresses	Data			Description
	S29NS256N	S29NS128N	S29NS064N	
10h 11h 12h	0051h 0052h 0059h			Query Unique ASCII string “QRY”
13h 14h	0002h 0000h			Primary OEM Command Set
15h 16h	0040h 0000h			Address for Primary Extended Table
17h 18h	0000h 0000h			Alternate OEM Command Set (00h = none exists)
19h 1Ah	0000h 0000h			Address for Alternate OEM Extended Table (00h = none exists)

Table 9.2 System Interface String

Addresses	Data			Description
	S29NS256N	S29NS128N	S29NS064N	
1Bh	0017h			V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	0019h			V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	0000h			ACC Min. voltage (00h = no ACC pin present) Refer to 4Dh
1Eh	0000h			ACC Max. voltage (00h = no ACC pin present) Refer to 4Eh
1Fh	0006h			Typical timeout per single byte/word write 2^N µs
20h	0009h			Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	000Ah			Typical timeout per individual block erase 2^N ms
22h	0000h			Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	0003h			Max. timeout for byte/word write 2^N times typical
24h	0001h			Max. timeout for buffer write 2^N times typical
25h	0002h			Max. timeout per individual block erase 2^N times typical
26h	0000h			Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 9.3 Device Geometry Definition

Addresses	Data			Description
	S29NS256N	S29NS128N	S29NS064N	
27h	0019h	0018h	0017h	Device Size = 2N byte
28h	0001h			Flash Device Interface description (refer to CFI publication 100)
29h	0000h			
2Ah	0006h			Max. number of bytes in multi-byte write = 2N (00h = not supported)
2Bh	0000h			
2Ch	0002h			Number of Erase Block Regions within device
2Dh	00FEh	007Eh	007Eh	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
2Eh	0000h	0000h	0000h	
2Fh	0000h	0000h	0000h	
30h	0002h	0002h	0001h	
31h	0003h		0007h	Erase Block Region 2 Information
32h	0000h		0000h	
33h	0080h		0020h	
34h	0000h		0000h	
35h	0000h			Erase Block Region 3 Information
36h	0000h			
37h	0000h			
38h	0000h			
39h	0000h			Erase Block Region 4 Information
3Ah	0000h			
3Bh	0000h			
3Ch	0000h			

Table 9.4 Primary Vendor-Specific Extended Query

Addresses	Data			Description
	S29NS256N	S29NS128N	S29NS064N	
40h	0050h			Query-unique ASCII string “PRI”
41h	0052h			
42h	0049h			
43h	0031h			Major version number, ASCII
44h	0034h			Minor version number, ASCII
45h	0010h			Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Silicon Revision Number (Bits 7-2)
46h	0002h			Erase Suspend 0 = Not Supported, 1 = To Read Only, 2= To Read & Write
47h	0001h			Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	0000h			Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	0008h			Sector Protect/Unprotect scheme 08 = Advanced Sector Protection
4Ah	00F0h	0078h	0070h	Simultaneous Operation Number of Sectors in all banks except boot bank
4Bh	0001h			Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	0000h			Page Mode 00 = Not Supported, 01 = Supported
4Dh	0085h			ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mv
4Eh	0095h			ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mv
4Fh	0003h			Top/Bottom Boot Sector Flag 0001h = Top/Middle Boot Device, 0002h = Bottom Boot Device, 03h = Top Boot Device
50h	0001h			Program Suspend. 00h = not supported
51h	0001h			Unlock Bypass 00 = Not Supported, 01 = Supported
52h	0008h			Secured Silicon Sector (Customer OTP Area) Size 2N bytes
53h	0008h			Hardware Reset Low Time-out during an embedded algorithm to read more mode Maximum 2N ns
54h	0008h			Hardware Reset Low Time-out during an embedded algorithm to read more mode Maximum 2N ns
55h	0005h			Erase Suspend Time-out Maximum 2N ns
56h	0005h			Program Suspend Time-out Maximum 2N ns
57h	0010h	0010h	0008h	Bank Organization: X = Number of banks
58h	0010h	0008h	0010h	Bank 0 Region Information. X = Number of sectors in banks
59h	0010h	0008h	0010h	Bank 1 Region Information. X = Number of sectors in banks
5Ah	0010h	0008h	0010h	Bank 2 Region Information. X = Number of sectors in banks
5Bh	0010h	0008h	0010h	Bank 3 Region Information. X = Number of sectors in banks
5Ch	0010h	0008h	0010h	Bank 4 Region Information. X = Number of sectors in banks
5Dh	0010h	0008h	0010h	Bank 5 Region Information. X = Number of sectors in banks
5Eh	0010h	0008h	0010h	Bank 6 Region Information. X = Number of sectors in banks
5Fh	0010h	0008h	0013h	Bank 7 Region Information. X = Number of sectors in banks
60h	0010h	0008h	0000h	Bank 8 Region Information. X = Number of sectors in banks
61h	0010h	0008h	0000h	Bank 9 Region Information. X = Number of sectors in banks
62h	0010h	0008h	0000h	Bank 10 Region Information. X = Number of sectors in banks
63h	0010h	0008h	0000h	Bank 11 Region Information. X = Number of sectors in banks
64h	0010h	0008h	0000h	Bank 12 Region Information. X = Number of sectors in banks
65h	0010h	0008h	0000h	Bank 13 Region Information. X = Number of sectors in banks
66h	0010h	0008h	0000h	Bank 14 Region Information. X = Number of sectors in banks
67h	0013h	000Bh	0000h	Bank 15 Region Information. X = Number of sectors in banks
68h	0002h			Process Technology. 00h = 230nm, 01h = 170nm, 02h = 130nm/110nm

Table 9.5 Sector Address Table, S29NS256N (Sheet 1 of 3)

Bank	Sector	Sector Size	Address Range
Bank 0	SA0	64 Kwords	000000h–00FFFFh
	SA1	64 Kwords	010000h–01FFFFh
	SA2	64 Kwords	020000h–02FFFFh
	SA3	64 Kwords	030000h–03FFFFh
	SA4	64 Kwords	040000h–04FFFFh
	SA5	64 Kwords	050000h–05FFFFh
	SA6	64 Kwords	060000h–06FFFFh
	SA7	64 Kwords	070000h–07FFFFh
	SA8	64 Kwords	080000h–08FFFFh
	SA9	64 Kwords	090000h–09FFFFh
	SA10	64 Kwords	0A0000h–0AFFFFh
	SA11	64 Kwords	0B0000h–0BFFFFh
	SA12	64 Kwords	0C0000h–0CFFFFh
	SA13	64 Kwords	0D0000h–0DFFFFh
	SA14	64 Kwords	0E0000h–0EFFFFh
	SA15	64 Kwords	0F0000h–0FFFFFh
Bank 1	SA16	64 Kwords	100000h–10FFFFh
	SA17	64 Kwords	110000h–11FFFFh
	SA18	64 Kwords	120000h–12FFFFh
	SA19	64 Kwords	130000h–13FFFFh
	SA20	64 Kwords	140000h–14FFFFh
	SA21	64 Kwords	150000h–15FFFFh
	SA22	64 Kwords	160000h–16FFFFh
	SA23	64 Kwords	170000h–17FFFFh
	SA24	64 Kwords	180000h–18FFFFh
	SA25	64 Kwords	190000h–19FFFFh
	SA26	64 Kwords	1A0000h–1AFFFFh
	SA27	64 Kwords	1B0000h–1BFFFFh
	SA28	64 Kwords	1C0000h–1CFFFFh
	SA29	64 Kwords	1D0000h–1DFFFFh
	SA30	64 Kwords	1E0000h–1EFFFFh
	SA31	64 Kwords	1F0000h–1FFFFFh
Bank 4	SA64	64 Kwords	400000h–40FFFFh
	SA65	64 Kwords	410000h–41FFFFh
	SA66	64 Kwords	420000h–42FFFFh
	SA67	64 Kwords	430000h–43FFFFh
	SA68	64 Kwords	440000h–44FFFFh
	SA69	64 Kwords	450000h–45FFFFh
	SA70	64 Kwords	460000h–46FFFFh
	SA71	64 Kwords	470000h–47FFFFh
	SA72	64 Kwords	480000h–48FFFFh
	SA73	64 Kwords	490000h–49FFFFh
	SA74	64 Kwords	4A0000h–4AFFFFh
	SA75	64 Kwords	4B0000h–4BFFFFh
	SA76	64 Kwords	4C0000h–4CFFFFh
	SA77	64 Kwords	4D0000h–4DFFFFh
	SA78	64 Kwords	4E0000h–4EFFFFh
	SA79	64 Kwords	4F0000h–4FFFFFh

Bank	Sector	Sector Size	Address Range
Bank 2	SA32	64 Kwords	200000h–20FFFFh
	SA33	64 Kwords	210000h–21FFFFh
	SA34	64 Kwords	220000h–22FFFFh
	SA35	64 Kwords	230000h–23FFFFh
	SA36	64 Kwords	240000h–24FFFFh
	SA37	64 Kwords	250000h–25FFFFh
	SA38	64 Kwords	260000h–26FFFFh
	SA39	64 Kwords	270000h–27FFFFh
	SA40	64 Kwords	280000h–28FFFFh
	SA41	64 Kwords	290000h–29FFFFh
	SA42	64 Kwords	2A0000h–2AFFFFh
	SA43	64 Kwords	2B0000h–2BFFFFh
	SA44	64 Kwords	2C0000h–2CFFFFh
	SA45	64 Kwords	2D0000h–2DFFFFh
	SA46	64 Kwords	2E0000h–2EFFFFh
	SA47	64 Kwords	2F0000h–2FFFFFh
Bank 3	SA48	64 Kwords	300000h–30FFFFh
	SA49	64 Kwords	310000h–31FFFFh
	SA50	64 Kwords	320000h–32FFFFh
	SA51	64 Kwords	330000h–33FFFFh
	SA52	64 Kwords	340000h–34FFFFh
	SA53	64 Kwords	350000h–35FFFFh
	SA54	64 Kwords	360000h–36FFFFh
	SA55	64 Kwords	370000h–37FFFFh
	SA56	64 Kwords	380000h–38FFFFh
	SA57	64 Kwords	390000h–39FFFFh
	SA58	64 Kwords	3A0000h–3AFFFFh
	SA59	64 Kwords	3B0000h–3BFFFFh
	SA60	64 Kwords	3C0000h–3CFFFFh
	SA61	64 Kwords	3D0000h–3DFFFFh
	SA62	64 Kwords	3E0000h–3EFFFFh
	SA63	64 Kwords	3F0000h–3FFFFFh
Bank 6	SA96	64 K words	600000h–60FFFFh
	SA97	64 K words	610000h–61FFFFh
	SA98	64 K words	620000h–62FFFFh
	SA99	64 K words	630000h–63FFFFh
	SA100	64 K words	640000h–64FFFFh
	SA101	64 K words	650000h–65FFFFh
	SA102	64 K words	660000h–66FFFFh
	SA103	64 K words	670000h–67FFFFh
	SA104	64 K words	680000h–68FFFFh
	SA105	64 K words	690000h–69FFFFh
	SA106	64 K words	6A0000h–6AFFFFh
	SA107	64 K words	6B0000h–6BFFFFh
	SA108	64 K words	6C0000h–6CFFFFh
	SA109	64 K words	6D0000h–6DFFFFh
	SA110	64 K words	6E0000h–6EFFFFh
	SA111	64 K words	6F0000h–6FFFFFh

Table 9.5 Sector Address Table, S29NS256N (Sheet 2 of 3)

Bank	Sector	Sector Size	Address Range
Bank 5	SA80	64 Kwords	500000h–50FFFFh
	SA81	64 Kwords	510000h–51FFFFh
	SA82	64 Kwords	520000h–52FFFFh
	SA83	64 Kwords	530000h–53FFFFh
	SA84	64 Kwords	540000h–54FFFFh
	SA85	64 Kwords	550000h–55FFFFh
	SA86	64 Kwords	560000h–56FFFFh
	SA87	64 Kwords	570000h–57FFFFh
	SA88	64 Kwords	580000h–58FFFFh
	SA89	64 Kwords	590000h–59FFFFh
	SA90	64 Kwords	5A0000h–5AFFFFh
	SA91	64 Kwords	5B0000h–5BFFFFh
	SA92	64 Kwords	5C0000h–5CFFFFh
	SA93	64 Kwords	5D0000h–5DFFFFh
	SA94	64 Kwords	5E0000h–5EFFFFh
	SA95	64 Kwords	5F0000h–5FFFFFh
Bank 8	SA128	64 Kwords	800000h–80FFFFh
	SA129	64 Kwords	810000h–81FFFFh
	SA130	64 Kwords	820000h–82FFFFh
	SA131	64 Kwords	830000h–83FFFFh
	SA132	64 Kwords	840000h–84FFFFh
	SA133	64 Kwords	850000h–85FFFFh
	SA134	64 Kwords	860000h–86FFFFh
	SA135	64 Kwords	870000h–87FFFFh
	SA136	64 Kwords	880000h–88FFFFh
	SA137	64 Kwords	890000h–89FFFFh
	SA138	64 Kwords	8A0000h–8AFFFFh
	SA139	64 Kwords	8B0000h–8BFFFFh
	SA140	64 Kwords	8C0000h–8CFFFFh
	SA141	64 Kwords	8D0000h–8DFFFFh
	SA142	64 Kwords	8E0000h–8EFFFFh
	SA143	64 Kwords	8F0000h–8FFFFFh
Bank 9	SA144	64 Kwords	900000h–90FFFFh
	SA145	64 Kwords	910000h–91FFFFh
	SA146	64 Kwords	920000h–92FFFFh
	SA147	64 Kwords	930000h–93FFFFh
	SA148	64 Kwords	940000h–94FFFFh
	SA149	64 Kwords	950000h–95FFFFh
	SA150	64 Kwords	960000h–96FFFFh
	SA151	64 Kwords	970000h–97FFFFh
	SA152	64 Kwords	980000h–98FFFFh
	SA153	64 Kwords	990000h–99FFFFh
	SA154	64 Kwords	9A0000h–9AFFFFh
	SA155	64 Kwords	9B0000h–9BFFFFh
	SA156	64 Kwords	9C0000h–9CFFFFh
	SA157	64 Kwords	9D0000h–9DFFFFh
	SA158	64 Kwords	9E0000h–9EFFFFh
	SA159	64 Kwords	9F0000h–9FFFFFh

Bank	Sector	Sector Size	Address Range
Bank 7	SA112	64 K words	700000h–70FFFFh
	SA113	64 K words	710000h–71FFFFh
	SA114	64 K words	720000h–72FFFFh
	SA115	64 K words	730000h–73FFFFh
	SA116	64 K words	740000h–74FFFFh
	SA117	64 K words	750000h–75FFFFh
	SA118	64 K words	760000h–76FFFFh
	SA119	64 K words	770000h–77FFFFh
	SA120	64 K words	780000h–78FFFFh
	SA121	64 K words	790000h–79FFFFh
	SA122	64 K words	7A0000h–7AFFFFh
	SA123	64 K words	7B0000h–7BFFFFh
	SA124	64 K words	7C0000h–7CFFFFh
	SA125	64 K words	7D0000h–7DFFFFh
	SA126	64 K words	7E0000h–7EFFFFh
	SA127	64 K words	7F0000h–7FFFFFh
Bank 10	SA160	64 Kwords	A00000h–A0FFFFh
	SA161	64 Kwords	A10000h–A1FFFFh
	SA162	64 Kwords	A20000h–A2FFFFh
	SA163	64 Kwords	A30000h–A3FFFFh
	SA164	64 Kwords	A40000h–A4FFFFh
	SA165	64 Kwords	A50000h–A5FFFFh
	SA166	64 Kwords	A60000h–A6FFFFh
	SA167	64 Kwords	A70000h–A7FFFFh
	SA168	64 Kwords	A80000h–A8FFFFh
	SA169	64 Kwords	A90000h–A9FFFFh
	SA170	64 Kwords	AA0000h–AAFFFFh
	SA171	64 Kwords	AB0000h–ABFFFFh
	SA172	64 Kwords	AC0000h–ACFFFFh
	SA173	64 Kwords	AD0000h–ADFFFFh
	SA174	64 Kwords	AE0000h–AEFFFFh
	SA175	64 Kwords	AF0000h–AFFFFFh
Bank 11	SA176	64 Kwords	B00000h–B0FFFFh
	SA177	64 Kwords	B10000h–B1FFFFh
	SA178	64 Kwords	B20000h–B2FFFFh
	SA179	64 Kwords	B30000h–B3FFFFh
	SA180	64 Kwords	B40000h–B4FFFFh
	SA181	64 Kwords	B50000h–B5FFFFh
	SA182	64 Kwords	B60000h–B6FFFFh
	SA183	64 Kwords	B70000h–B7FFFFh
	SA184	64 Kwords	B80000h–B8FFFFh
	SA185	64 Kwords	B90000h–B9FFFFh
	SA186	64 Kwords	BA0000h–BAFFFFh
	SA187	64 Kwords	BB0000h–BBFFFFh
	SA188	64 Kwords	BC0000h–BCFFFFh
	SA189	64 Kwords	BD0000h–BDFFFFh
	SA190	64 Kwords	BE0000h–BEFFFFh
	SA191	64 Kwords	BF0000h–BFFFFFh

Table 9.5 Sector Address Table, S29NS256N (Sheet 3 of 3)

Bank	Sector	Sector Size	Address Range
Bank 12	SA192	64 Kwords	C00000h–C0FFFFh
	SA193	64 Kwords	C10000h–C1FFFFh
	SA194	64 Kwords	C20000h–C2FFFFh
	SA195	64 Kwords	C30000h–C3FFFFh
	SA196	64 Kwords	C40000h–C4FFFFh
	SA197	64 Kwords	C50000h–C5FFFFh
	SA198	64 Kwords	C60000h–C6FFFFh
	SA199	64 Kwords	C70000h–C7FFFFh
	SA200	64 Kwords	C80000h–C8FFFFh
	SA201	64 Kwords	C90000h–C9FFFFh
	SA202	64 Kwords	CA0000h–CAFFFFh
	SA203	64 Kwords	CB0000h–CBFFFFh
	SA204	64 Kwords	CC0000h–CCFFFFh
	SA205	64 Kwords	CD0000h–CDFFFFh
	SA206	64 Kwords	CE0000h–CEFFFFh
	SA207	64 Kwords	CF0000h–CFFFFFh
Bank 13	SA208	64 Kwords	D00000h–D0FFFFh
	SA209	64 Kwords	D10000h–D1FFFFh
	SA210	64 Kwords	D20000h–D2FFFFh
	SA211	64 Kwords	D30000h–D3FFFFh
	SA212	64 Kwords	D40000h–D4FFFFh
	SA213	64 Kwords	D50000h–D5FFFFh
	SA214	64 Kwords	D60000h–D6FFFFh
	SA215	64 Kwords	D70000h–D7FFFFh
	SA216	64 Kwords	D80000h–D8FFFFh
	SA217	64 Kwords	D90000h–D9FFFFh
	SA218	64 Kwords	DA0000h–DAFFFFh
	SA219	64 Kwords	DB0000h–DBFFFFh
	SA220	64 Kwords	DC0000h–DCFFFFh
	SA221	64 Kwords	DD0000h–DDFFFFh
	SA222	64 Kwords	DE0000h–DEFFFFh
	SA223	64 Kwords	DF0000h–DFFFFFh

Bank	Sector	Sector Size	Address Range
Bank 14	SA224	64 K words	E00000h–E0FFFFh
	SA225	64 K words	E10000h–E1FFFFh
	SA226	64 K words	E20000h–E2FFFFh
	SA227	64 K words	E30000h–E3FFFFh
	SA228	64 K words	E40000h–E4FFFFh
	SA229	64 K words	E50000h–E5FFFFh
	SA230	64 K words	E60000h–E6FFFFh
	SA231	64 K words	E70000h–E7FFFFh
	SA232	64 K words	E80000h–E8FFFFh
	SA233	64 K words	E90000h–E9FFFFh
	SA234	64 K words	EA0000h–EAFFFFh
	SA235	64 K words	EB0000h–EBFFFFh
	SA236	64 K words	EC0000h–ECFFFFh
	SA237	64 K words	ED0000h–EDFFFFh
	SA238	64 K words	EE0000h–EEFFFFh
	SA239	64 K words	EF0000h–EFFFFFh
Bank 15	SA240	64 K words	F00000h–F0FFFFh
	SA241	64 K words	F10000h–F1FFFFh
	SA242	64 K words	F20000h–F2FFFFh
	SA243	64 K words	F30000h–F3FFFFh
	SA244	64 K words	F40000h–F4FFFFh
	SA245	64 K words	F50000h–F5FFFFh
	SA246	64 K words	F60000h–F6FFFFh
	SA247	64 K words	F70000h–F7FFFFh
	SA248	64 K words	F80000h–F8FFFFh
	SA249	64 K words	F90000h–F9FFFFh
	SA250	64 K words	FA0000h–FAFFFFh
	SA251	64 K words	FB0000h–FBFFFFh
	SA252	64 K words	FC0000h–FCFFFFh
	SA253	64 K words	FD0000h–FDFFFFh
	SA254	64 K words	FE0000h–FEFFFFh
	SA255	16 K words	FF0000h–FF3FFFh
	SA256	16 K words	FF4000h–FF7FFFh
	SA257	16 K words	FF8000h–FFBFFFh
	SA258	16 K words	FFC000h–FFFFFFh

Table 9.6 Sector Address Table, S29NS128N (Sheet 1 of 2)

Bank	Sector	Sector Size	Address Range
Bank 0	SA0	64 Kwords	000000h–00FFFFh
	SA1	64 Kwords	010000h–01FFFFh
	SA2	64 Kwords	020000h–02FFFFh
	SA3	64 Kwords	030000h–03FFFFh
	SA4	64 Kwords	040000h–04FFFFh
	SA5	64 Kwords	050000h–05FFFFh
	SA6	64 Kwords	060000h–06FFFFh
	SA7	64 Kwords	070000h–07FFFFh
Bank 1	SA8	64 Kwords	080000h–08FFFFh
	SA9	64 Kwords	090000h–09FFFFh
	SA10	64 Kwords	0A0000h–0AFFFFh
	SA11	64 Kwords	0B0000h–0BFFFFh
	SA12	64 Kwords	0C0000h–0CFFFFh
	SA13	64 Kwords	0D0000h–0DFFFFh
	SA14	64 Kwords	0E0000h–0EFFFFh
	SA15	64 Kwords	0F0000h–0FFFFFh
Bank 2	SA16	64 Kwords	100000h–10FFFFh
	SA17	64 Kwords	110000h–11FFFFh
	SA18	64 Kwords	120000h–12FFFFh
	SA19	64 Kwords	130000h–13FFFFh
	SA20	64 Kwords	140000h–14FFFFh
	SA21	64 Kwords	150000h–15FFFFh
	SA22	64 Kwords	160000h–16FFFFh
	SA23	64 Kwords	170000h–17FFFFh
Bank 3	SA24	64 Kwords	180000h–18FFFFh
	SA25	64 Kwords	190000h–19FFFFh
	SA26	64 Kwords	1A0000h–1AFFFFh
	SA27	64 Kwords	1B0000h–1BFFFFh
	SA28	64 Kwords	1C0000h–1CFFFFh
	SA29	64 Kwords	1D0000h–1DFFFFh
	SA30	64 Kwords	1E0000h–1EFFFFh
	SA31	64 Kwords	1F0000h–1FFFFFh
Bank 8	SA64	64 Kwords	400000h–40FFFFh
	SA65	64 Kwords	410000h–41FFFFh
	SA66	64 Kwords	420000h–42FFFFh
	SA67	64 Kwords	430000h–43FFFFh
	SA68	64 Kwords	440000h–44FFFFh
	SA69	64 Kwords	450000h–45FFFFh
	SA70	64 Kwords	460000h–46FFFFh
	SA71	64 Kwords	470000h–47FFFFh
Bank 9	SA72	64 Kwords	480000h–48FFFFh
	SA73	64 Kwords	490000h–49FFFFh
	SA74	64 Kwords	4A0000h–4AFFFFh
	SA75	64 Kwords	4B0000h–4BFFFFh
	SA76	64 Kwords	4C0000h–4CFFFFh
	SA77	64 Kwords	4D0000h–4DFFFFh
	SA78	64 Kwords	4E0000h–4EFFFFh
	SA79	64 Kwords	4F0000h–4FFFFFh

Bank	Sector	Sector Size	Address Range
Bank 4	SA32	64 Kwords	200000h–20FFFFh
	SA33	64 Kwords	210000h–21FFFFh
	SA34	64 Kwords	220000h–22FFFFh
	SA35	64 Kwords	230000h–23FFFFh
	SA36	64 Kwords	240000h–24FFFFh
	SA37	64 Kwords	250000h–25FFFFh
	SA38	64 Kwords	260000h–26FFFFh
	SA39	64 Kwords	270000h–27FFFFh
Bank 5	SA40	64 Kwords	280000h–28FFFFh
	SA41	64 Kwords	290000h–29FFFFh
	SA42	64 Kwords	2A0000h–2AFFFFh
	SA43	64 Kwords	2B0000h–2BFFFFh
	SA44	64 Kwords	2C0000h–2CFFFFh
	SA45	64 Kwords	2D0000h–2DFFFFh
	SA46	64 Kwords	2E0000h–2EFFFFh
	SA47	64 Kwords	2F0000h–2FFFFFh
Bank 6	SA48	64 Kwords	300000h–30FFFFh
	SA49	64 Kwords	310000h–31FFFFh
	SA50	64 Kwords	320000h–32FFFFh
	SA51	64 Kwords	330000h–33FFFFh
	SA52	64 Kwords	340000h–34FFFFh
	SA53	64 Kwords	350000h–35FFFFh
	SA54	64 Kwords	360000h–36FFFFh
	SA55	64 Kwords	370000h–37FFFFh
Bank 7	SA56	64 Kwords	380000h–38FFFFh
	SA57	64 Kwords	390000h–39FFFFh
	SA58	64 Kwords	3A0000h–3AFFFFh
	SA59	64 Kwords	3B0000h–3BFFFFh
	SA60	64 Kwords	3C0000h–3CFFFFh
	SA61	64 Kwords	3D0000h–3DFFFFh
	SA62	64 Kwords	3E0000h–3EFFFFh
	SA63	64 Kwords	3F0000h–3FFFFFh
Bank 12	SA96	64 K words	600000h–60FFFFh
	SA97	64 K words	610000h–61FFFFh
	SA98	64 K words	620000h–62FFFFh
	SA99	64 K words	630000h–63FFFFh
	SA100	64 K words	640000h–64FFFFh
	SA101	64 K words	650000h–65FFFFh
	SA102	64 K words	660000h–66FFFFh
	SA103	64 K words	670000h–67FFFFh
Bank 13	SA104	64 K words	680000h–68FFFFh
	SA105	64 K words	690000h–69FFFFh
	SA106	64 K words	6A0000h–6AFFFFh
	SA107	64 K words	6B0000h–6BFFFFh
	SA108	64 K words	6C0000h–6CFFFFh
	SA109	64 K words	6D0000h–6DFFFFh
	SA110	64 K words	6E0000h–6EFFFFh
	SA111	64 K words	6F0000h–6FFFFFh

Table 9.6 Sector Address Table, S29NS128N (Sheet 2 of 2)

Bank	Sector	Sector Size	Address Range
Bank 10	SA80	64 Kwords	500000h–50FFFFh
	SA81	64 Kwords	510000h–51FFFFh
	SA82	64 Kwords	520000h–52FFFFh
	SA83	64 Kwords	530000h–53FFFFh
	SA84	64 Kwords	540000h–54FFFFh
	SA85	64 Kwords	550000h–55FFFFh
	SA86	64 Kwords	560000h–56FFFFh
	SA87	64 Kwords	570000h–57FFFFh
Bank 11	SA88	64 Kwords	580000h–58FFFFh
	SA89	64 Kwords	590000h–59FFFFh
	SA90	64 Kwords	5A0000h–5AFFFFh
	SA91	64 Kwords	5B0000h–5BFFFFh
	SA92	64 Kwords	5C0000h–5CFFFFh
	SA93	64 Kwords	5D0000h–5DFFFFh
	SA94	64 Kwords	5E0000h–5EFFFFh
	SA95	64 Kwords	5F0000h–5FFFFFh

Bank	Sector	Sector Size	Address Range
Bank 14	SA112	64 K words	700000h–70FFFFh
	SA113	64 K words	710000h–71FFFFh
	SA114	64 K words	720000h–72FFFFh
	SA115	64 K words	730000h–73FFFFh
	SA116	64 K words	740000h–74FFFFh
	SA117	64 K words	750000h–75FFFFh
	SA118	64 K words	760000h–76FFFFh
	SA119	64 K words	770000h–77FFFFh
Bank 15	SA120	64 K words	780000h–78FFFFh
	SA121	64 K words	790000h–79FFFFh
	SA122	64 K words	7A0000h–7AFFFFh
	SA123	64 K words	7B0000h–7BFFFFh
	SA124	64 K words	7C0000h–7CFFFFh
	SA125	64 K words	7D0000h–7DFFFFh
	SA126	64 K words	7E0000h–7EFFFFh
	SA127	16 K words	7F0000h–7F3FFFh
	SA128	16 K words	7F4000h–7F7FFFh
	SA129	16 K words	7F8000h–7FBFFFh
	SA130	16 K words	7FC000h–7FFFFFh

Table 9.7 Sector Address Table, S29NS064N (Sheet 1 of 3)

Bank	Sector	Sector Size	Address Range
Bank 0	SA0	32 Kwords	000000h-007FFFh
	SA1	32 Kwords	008000h-00FFFFh
	SA2	32 Kwords	010000h-017FFFh
	SA3	32 Kwords	018000h-01FFFFh
	SA4	32 Kwords	020000h-027FFFh
	SA5	32 Kwords	028000h-02FFFFh
	SA6	32 Kwords	030000h-037FFFh
	SA7	32 Kwords	038000h-03FFFFh
	SA8	32 Kwords	040000h-047FFFh
	SA9	32 Kwords	048000h-04FFFFh
	SA10	32 Kwords	050000h-057FFFh
	SA11	32 Kwords	058000h-05FFFFh
	SA12	32 Kwords	060000h-067FFFh
	SA13	32 Kwords	068000h-06FFFFh
	SA14	32 Kwords	070000h-077FFFh
	SA15	32 Kwords	078000h-0F7FFFh

Bank	Sector	Sector Size	Address Range
Bank 2	SA32	32 Kwords	100000h-107FFFh
	SA33	32 Kwords	108000h-10FFFFh
	SA34	32 Kwords	110000h-117FFFh
	SA35	32 Kwords	118000h-11FFFFh
	SA36	32 Kwords	120000h-127FFFh
	SA37	32 Kwords	128000h-12FFFFh
	SA38	32 Kwords	130000h-137FFFh
	SA39	32 Kwords	138000h-13FFFFh
	SA40	32 Kwords	140000h-147FFFh
	SA41	32 Kwords	148000h-14FFFFh
	SA42	32 Kwords	150000h-157FFFh
	SA43	32 Kwords	158000h-15FFFFh
	SA44	32 Kwords	160000h-167FFFh
	SA45	32 Kwords	168000h-16FFFFh
	SA46	32 Kwords	170000h-177FFFh
	SA47	32 Kwords	178000h-17FFFFh

Table 9.7 Sector Address Table, S29NS064N (Sheet 2 of 3)

Bank	Sector	Sector Size	Address Range
Bank 1	SA16	32 Kwords	080000h-087FFFh
	SA17	32 Kwords	088000h-08FFFFh
	SA18	32 Kwords	090000h-097FFFh
	SA19	32 Kwords	098000h-09FFFFh
	SA20	32 Kwords	0A0000h-0A7FFFh
	SA21	32 Kwords	0A8000h-0AFFFFh
	SA22	32 Kwords	0B0000h-0B7FFFh
	SA23	32 Kwords	0B8000h-0BFFFFh
	SA24	32 Kwords	0C0000h-0C7FFFh
	SA25	32 Kwords	0C8000h-0CFFFFh
	SA26	32 Kwords	0D0000h-0D7FFFh
	SA27	32 Kwords	0D8000h-0DFFFFh
	SA28	32 Kwords	0E0000h-0E7FFFh
	SA29	32 Kwords	0E8000h-0EFFFFh
	SA30	32 Kwords	0F0000h-0F7FFFh
	SA31	32 Kwords	0F8000h-0FFFFFh
Bank 4	SA64	32 Kwords	200000h-207FFFh
	SA65	32 Kwords	208000h-20FFFFh
	SA66	32 Kwords	210000h-217FFFh
	SA67	32 Kwords	218000h-21FFFFh
	SA68	32 Kwords	220000h-227FFFh
	SA69	32 Kwords	228000h-22FFFFh
	SA70	32 Kwords	230000h-237FFFh
	SA71	32 Kwords	238000h-23FFFFh
	SA72	32 Kwords	240000h-247FFFh
	SA73	32 Kwords	248000h-24FFFFh
	SA74	32 Kwords	250000h-257FFFh
	SA75	32 Kwords	258000h-25FFFFh
	SA76	32 Kwords	260000h-267FFFh
	SA77	32 Kwords	268000h-26FFFFh
	SA78	32 Kwords	270000h-277FFFh
	SA79	32 Kwords	278000h-2F7FFFh

Bank	Sector	Sector Size	Address Range
Bank 3	SA48	32 Kwords	180000h-187FFFh
	SA49	32 Kwords	188000h-18FFFFh
	SA50	32 Kwords	190000h-197FFFh
	SA51	32 Kwords	198000h-19FFFFh
	SA52	32 Kwords	1A0000h-1A7FFFh
	SA53	32 Kwords	1A8000h-1AFFFFh
	SA54	32 Kwords	1B0000h-1B7FFFh
	SA55	32 Kwords	1B8000h-1BFFFFh
	SA56	32 Kwords	1C0000h-1C7FFFh
	SA57	32 Kwords	1C8000h-1CFFFFh
	SA58	32 Kwords	1D0000h-1D7FFFh
	SA59	32 Kwords	1D8000h-1DFFFFh
	SA60	32 Kwords	1E0000h-1E7FFFh
	SA61	32 Kwords	1E8000h-1EFFFFh
	SA62	32 Kwords	1F0000h-1F7FFFh
	SA63	32 Kwords	1F8000h-1FFFFFh
Bank 6	SA96	32 Kwords	300000h-307FFFh
	SA97	32 Kwords	308000h-30FFFFh
	SA98	32 Kwords	310000h-317FFFh
	SA99	32 Kwords	318000h-31FFFFh
	SA100	32 Kwords	320000h-327FFFh
	SA101	32 Kwords	328000h-32FFFFh
	SA102	32 Kwords	330000h-337FFFh
	SA103	32 Kwords	338000h-33FFFFh
	SA104	32 Kwords	340000h-347FFFh
	SA105	32 Kwords	348000h-34FFFFh
	SA106	32 Kwords	350000h-357FFFh
	SA107	32 Kwords	358000h-35FFFFh
	SA108	32 Kwords	360000h-367FFFh
	SA109	32 Kwords	368000h-36FFFFh
	SA110	32 Kwords	370000h-377FFFh
	SA111	32 Kwords	378000h-37FFFFh

Table 9.7 Sector Address Table, S29NS064N (Sheet 3 of 3)

Bank	Sector	Sector Size	Address Range
Bank 5	SA80	32 Kwords	280000h-287FFFh
	SA81	32 Kwords	288000h-28FFFFh
	SA82	32 Kwords	290000h-297FFFh
	SA83	32 Kwords	298000h-29FFFFh
	SA84	32 Kwords	2A0000h-2A7FFFh
	SA85	32 Kwords	2A8000h-2AFFFFh
	SA86	32 Kwords	2B0000h-2B7FFFh
	SA87	32 Kwords	2B8000h-2BFFFFh
	SA88	32 Kwords	2C0000h-2C7FFFh
	SA89	32 Kwords	2C8000h-2CFFFFh
	SA90	32 Kwords	2D0000h-2D7FFFh
	SA91	32 Kwords	2D8000h-2DFFFFh
	SA92	32 Kwords	2E0000h-2E7FFFh
	SA93	32 Kwords	2E8000h-2EFFFFh
	SA94	32 Kwords	2F0000h-2F7FFFh
	SA95	32 Kwords	2F8000h-2FFFFFh

Bank	Sector	Sector Size	Address Range
Bank 7	SA112	32 Kwords	380000h-387FFFh
	SA113	32 Kwords	388000h-38FFFFh
	SA114	32 Kwords	390000h-397FFFh
	SA115	32 Kwords	398000h-39FFFFh
	SA116	32 Kwords	3A0000h-3A7FFFh
	SA117	32 Kwords	3A8000h-3AFFFFh
	SA118	32 Kwords	3B0000h-3B7FFFh
	SA119	32 Kwords	3B8000h-3BFFFFh
	SA120	32 Kwords	3C0000h-3C7FFFh
	SA121	32 Kwords	3C8000h-3CFFFFh
	SA122	32 Kwords	3D0000h-3D7FFFh
	SA123	32 Kwords	3D8000h-3DFFFFh
	SA124	32 Kwords	3E0000h-3E7FFFh
	SA125	32 Kwords	3E8000h-3EFFFFh
	SA126	32 Kwords	3F0000h-3F7FFFh
	SA127	8 Kwords	3F8000h-3F9FFFh
	SA128	8 Kwords	3FA000h-3FBFFFh
	SA129	8 Kwords	3FC000h-3FDFFFh
	SA130	8 Kwords	3FE000h-3FFFFFh

10. Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. Table 11.4 on page 52 defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** resets the device to reading array data.

All addresses are latched on the rising edge of AVD#. All data is latched on the rising edge of WE#. Refer to the *AC Characteristics* section for timing diagrams.

10.1 Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data in asynchronous mode. Each bank is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the corresponding bank enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See *Erase Suspend/Erase Resume Commands on page 46* for more information.

After the device accepts a Program Suspend command, the corresponding bank enters the program-suspend-read mode, after which the system can read data from any non-program-suspended sector within the same bank.

The system *must* issue the reset command to return a bank to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the bank is in the autoselect mode.

See also *VersatileIO™ (VIO) Control on page 14* and *Requirements for Synchronous (Burst) Read Operation on page 15* in the *Device Bus Operations* section for more information. The *Asynchronous*

Read and *Synchronous/Burst Read* tables provide the read parameters, and Figure 19.3 on page 66 and Figure 19.4 on page 67 show the timings.

10.2 Set Configuration Register Command Sequence

The device uses a configuration register to set the various burst parameters: number of wait states, burst read mode, RDY configuration, and synchronous mode active. The configuration register must be set before the device will enter burst mode.

The configuration register is loaded with a four-cycle command sequence. The first two cycles are standard unlock sequences. On the third cycle, the data should be D0h and address bits should be 555h. During the fourth cycle, the configuration code should be entered onto the data bus with the address bus set to address 000h. Once the data has been programmed into the configuration register, a software reset command is required to set the device into the correct state. The device will power up or after a hardware reset with the default setting, which is in asynchronous mode. The register must be set before the device can enter synchronous mode. The configuration register can not be changed during device operations (program, erase, or sector lock).

10.3 Read Configuration Register Command Sequence

The configuration register can be read with a four-cycle command sequence. The first two cycles are standard unlock sequences. On the third cycle, the data should be C6h and address bits should be 555h. During the fourth cycle, the configuration code should be read out of the data bus with the address bus set to address 000h. Once the data has been read from the configuration register, a software reset command is required to set the device into the correct set mode.

10.3.1 Read Mode Setting

On power-up or hardware reset, the device is set to be in asynchronous read mode. This setting allows the system to enable or disable burst mode during system operations.

10.3.2 Programmable Wait State Configuration

The programmable wait state feature informs the device of the number of clock cycles that must elapse after AVD# is driven active before data will be available. This value is determined by the input frequency of the device. **Configuration Bit CR13–CR11** determine the setting (see Table 10.1).

The wait state command sequence instructs the device to set a particular number of clock cycles for the initial access in burst mode. The number of wait states that should be programmed into the device is directly related to the clock frequency.

Table 10.1 Programmable Wait State Settings

CR13	CR12	CR11	Total Initial Access Cycles
0	0	0	2
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	7 (default)
1	1	0	Reserved
1	1	1	Reserved

Notes

1. *Upon power-up or hardware reset, the default setting is seven wait states.*
2. *RDY will default to being active with data when the Wait State Setting is set to a total initial access cycle of 2.*

It is recommended that the wait state command sequence be written, even if the default wait state value is desired, to ensure the device is set as expected. A hardware reset will set the wait state to the default setting.

10.3.3 Programmable Wait State

The host system should set **CR13-CR11** to 101/100/011 for a clock frequency of 80/66 MHz for the system/device to execute at maximum speed.

Table 10.2 describes the typical number of clock cycles (wait states) for various conditions.

Table 10.2 Wait States for Handshaking

Conditions at Address	Typical No. of Clock Cycles after AVD# Low	
	80 MHz	66 MHz
Initial address (V_{CCQ} = 1.8 V)	7	6

10.3.4 Handshaking

For optimal burst mode performance, the host system must set the appropriate number of wait states in the flash device depending on the clock frequency.

The autoselect function allows the host system to determine whether the flash device is enabled for handshaking.

10.3.5 Burst Length Configuration

The device supports four different read modes: continuous mode, and 8, 16, and 32 word linear with or without wrap around modes. A continuous sequence (default) begins at the starting address and advances the address pointer until the burst operation is complete. If the highest address in the device is reached during the continuous burst read mode, the address pointer wraps around to the lowest address.

For example, an eight-word linear read with wrap around begins on the starting address written to the device and then advances to the next 8 word boundary. The address pointer then returns to the 1st word after the previous eight word boundary, wrapping through the starting location. The sixteen- and thirty-two linear wrap around modes operate in a fashion similar to the eight-word mode.

Table 10.3 shows the **CR2-CR0** and settings for the four read modes.

Table 10.3 Burst Length Configuration

Burst Modes	Address Bits		
	CR2	CR1	CR0
Continuous	0	0	0
8-word linear	0	1	0
16-word linear	0	1	1
32-word linear	1	0	0

Notes

1. *Upon power-up or hardware reset the default setting is continuous.*
2. *All other conditions are reserved.*

10.3.6 Burst Wrap Around

By default, the device will perform burst wrap around with **CR3** set to a ‘1’. Changing the **CR3** to a ‘0’ disables burst wrap around.

10.3.7 RDY Configuration

By default, the device is set so that the RDY pin will output V_{OH} whenever there is valid data on the outputs. The device can be set so that RDY goes active one data cycle before active data. **CR8** determines this setting; “1” for RDY active (default) with data, “0” for RDY active one clock cycle before valid data.

10.3.8 RDY Polarity

By default, the RDY pin will always indicate that the device is ready to handle a new transaction with **CR10** set to a '1'. In this case, the RDY pin is active high. Changing the **CR10** to a '0' sets the RDY pin to be active low. In this case, the RDY pin will always indicate that the device is ready to handle a new transaction when low.

11. Configuration Register

Table 11.1 shows the address bits that determine the configuration register settings for various device functions.

Table 11.1 Configuration Register

CR Bit	Function	Settings (Binary)
CR15	Reserved	0 = Default
CR14	Reserved	0 = Default
CR13 CR12 CR11	Programmable Wait State	000 = Data is valid on the 2nd active CLK edge after AVD# transition to V_{IH} 001 = Data is valid on the 3rd active CLK edge after AVD# transition to V_{IH} 010 = Data is valid on the 4th active CLK edge after AVD# transition to V_{IH} 011 = Data is valid on the 5th active CLK edge after AVD# transition to V_{IH} 100 = Data is valid on the 6th active CLK edge after AVD# transition to V_{IH} 101 = Data is valid on the 7th active CLK edge after AVD# transition to V_{IH} (default) 110 = Reserved 111 = Reserved
CR10	RDY Polarity	0 = RDY signal is active low 1 = RDY signal is active high (default)
CR9	Reserved	1 = Default
CR8	RDY	0 = RDY active one clock cycle before data 1 = RDY active with data (default)
CR7	Reserved	1 = default
CR6	Reserved	1 = default
CR5	Reserved	0 = default
CR4	Reserved	0 = default
CR3	Burst Wrap Around	0 = No Wrap Around Burst 1 = Wrap Around Burst (default)
CR2 CR1 CR0	Burst Length	000 = Continuous (default) 010 = 8-Word Linear Burst 011 = 16-Word Linear Burst 100 = 32-Word Linear Burst (All other bit settings are reserved)

Notes

1. *Device will be in the default state upon power-up or hardware reset.*
2. *CR3 will always equal to 1 (Wrap around mode) when CR0,CR1,CR2 = 000 (continuous Burst mode).*
3. *A software reset command is required after a read or write command.*

11.1 Reset Command

Writing the reset command resets the banks to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the bank to which the system was writing to the read mode. **Once erasure begins, however, the device ignores reset commands until the operation is complete**.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the bank to which the system was writing to the read mode. If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. **Once programming begins, however, the device ignores reset commands until the operation is complete**.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If a bank entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the banks to the read mode (or erase-suspend-read mode if that bank was in Erase Suspend).

Note: If DQ1 goes high during a Write Buffer Programming operation, the system must write the “Write to Buffer Abort Reset” command sequence to RESET the device to reading array data. The standard RESET command will not work. See Table 11.4 on page 52 for details on this command sequence.

11.2 Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. Table 11.4 on page 52 shows the address and data requirements. The autoselect command sequence may be written to an address within a bank that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing in the other bank. Autoselect does not support simultaneous operations or burst mode.

Table 11.2 Device ID

Description	Address	Read Data		
		256N	128N	064N
Manufacturer ID	(BA) + 00h	0001h	0001h	0001h
Device ID, Word 1	(BA) + 01h	2D7E	2C7Eh	2B7Eh
Device ID, Word 2	(BA) + 0Eh	2D2F	2C35h	2B33h
Device ID, Word 3	(BA) + 0Fh	2D00	2C00h	2B00h
Revision ID	(BA) + 03h	TBD		
Sector Block Lock/Unlock	(SA) = 02h	0001 - Locked 0000 - Unlocked		
Indicator Bits	(BA) + 07h	DQ15 - DQ8 = Reserved DQ7 - Factory Lock Bit 1 = Locked, 0 = Not Locked DQ6 - Customer Lock Bit 1 = Locked, 0 = Not Locked DQ5 Handshake Bit 1 = Reserved 0 = Standard Handshake DQ4 & DQ3 - WP# Protections Boot Code 01 = WP# Protects only the Top Boot Sectors DQ2-DQ0 = Reserved		

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the bank address and the autoselect command. The bank then enters the autoselect mode. The system may read at any address within the same bank any number of times without initiating another autoselect command sequence. The following table describes the address requirements for the various autoselect functions, and the resulting data. BA represents the bank address. The device ID is read in three cycles. During this time, other banks are still available to read the data from the memory.

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the bank was previously in Erase Suspend).

11.3 Enter/Exit Secured Silicon Sector Command Sequence

The Secured Silicon Sector region provides a secured data area containing a random, eight word electronic serial number (ESN). The system can access the Secured Silicon Sector region by issuing the three-cycle Enter Secured Silicon Sector command sequence. The device continues to access the Secured Silicon Sector region until the system issues the four-cycle Exit Secured Silicon Sector command sequence. The Exit Secured Silicon Sector command sequence returns the device to normal operation. The Secured Silicon Sector is not accessible when the device is executing an Embedded Program or embedded Erase algorithm. Table 11.4 on page 52 shows the address and data requirements for both command sequences.

11.3.1 Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program faster than the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. That bank then enters the unlock bypass mode.

During the unlock bypass mode only the command is valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the bank address and the data 90h. The second cycle need only contain the data 00h. The bank then returns to the read mode.

11.4 Program Command Sequence

11.4.1 Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 11.4 on page 52 shows the address and data requirements for the program command sequence.

When the Embedded Program algorithm is complete, that bank then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by monitoring DQ7 or DQ6/DQ2. Refer to the *Write Operation Status on page 55* for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the program operation. The program command sequence should be reinitiated once that bank has returned to the read mode, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from "0" back to a "1."** Attempting to do so may causes that bank to set DQ5 = 1 (change-up condition). However, a succeeding read will show that the data is still "0." Only erase operations can convert a "0" to a "1."

11.4.2 Program Command Sequence (Unlock Bypass Mode)

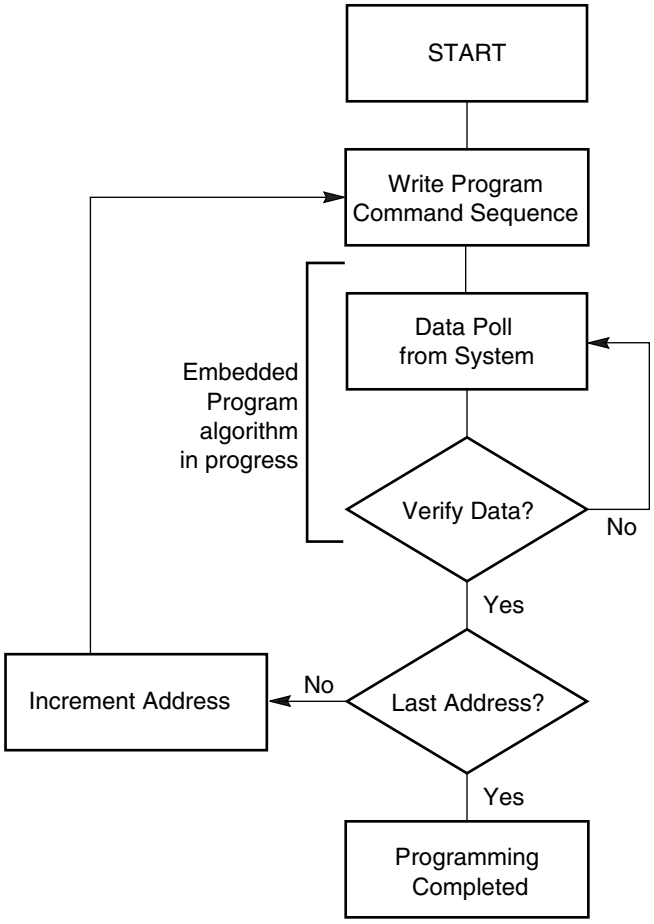
Once the device enters the unlock bypass mode, then a two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 11.4 on page 52 shows the requirements for the unlock bypass command sequences.

11.5 Accelerated Program

The device offers accelerated program operations through the ACC input. When the system asserts ACC on this input, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the ACC input to accelerate the operation.

Figure 11.1 illustrates the algorithm for the program operation. Refer to Table 19.5, *Erase/Program Operations on page 69* and Figure 19.6 on page 70 for timing diagrams.

Figure 11.1 Program Operation



Note
See Table 11.4 on page 52 for program.

11.6 Write Buffer Programming Command Sequence

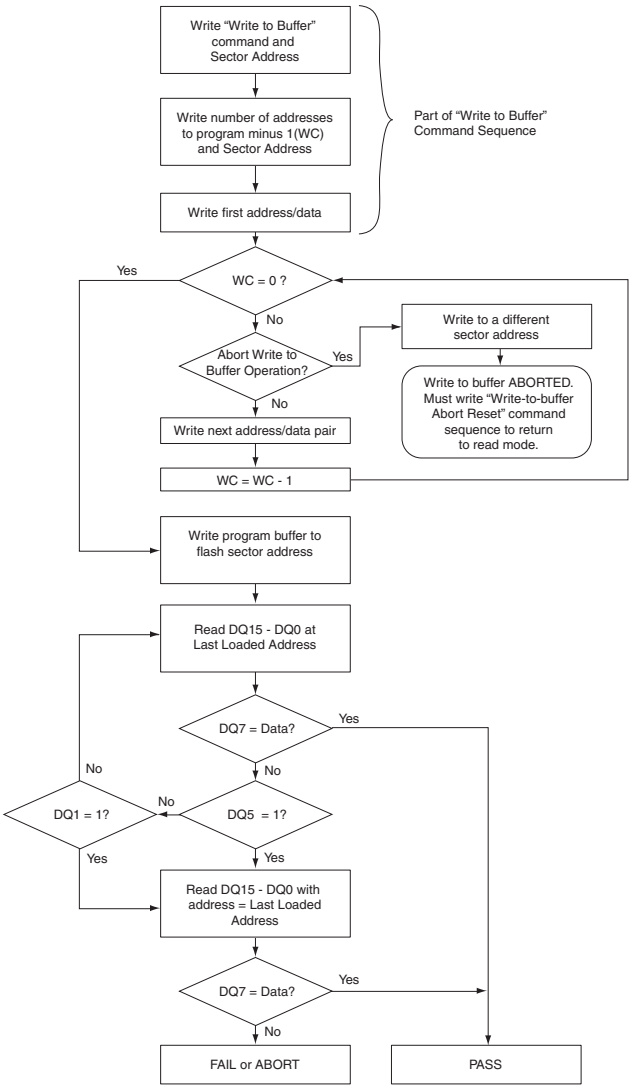
Write Buffer Programming Sequence allows for faster programming as compared to the standard Program Command Sequence. See Table 11.3 on page 43 for the program command sequence.

Table 11.3 Write Buffer Command Sequence

Sequence	Address	Data	Comment
Unlock Command 1	555	00AA	Not required in the Unlock Bypass mode
Unlock Command 2	2AA	0055	Same as above
Write Buffer Load	Starting Address	0025h	
Specify the Number of Program Locations	Starting Address	Word Count	Number of locations to program minus 1
Load 1st data word	Starting Address	Program Data	All addresses must be within write-buffer-page boundaries, but do not have to be loaded in any order
Load next data word	Write Buffer Location	Program Data	Same as above
...	...	...	Same as above
Load last data word	Write Buffer Location	Program Data	Same as above
Write Buffer Program Confirm	Sector Address	0029h	This command must follow the last write buffer location loaded, or the operation will ABORT
Device goes busy			
Status monitoring through DQ pins (Perform Data Bar Polling on the **Last Loaded Address**)			

Note
Write buffer addresses must be loaded in sequential order.

Figure 11.2 Write Buffer Programming Operation



11.7 Chip Erase Command Sequence

11.7.1 Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 11.4 on page 52 shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, that bank returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7 or DQ6/DQ2. Refer to *Write Operation Status* *on page 55* for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

11.8 Sector Erase Command Sequence

11.8.1 Sector Erase Command Sequence

Sector erase in normal mode is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 11.4 on page 52 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of no less than t_{SEA}, sector erase accept, occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than t_{SEA}. Any sector erase address and command following the exceeded time-out may or may not be accepted. **Any command other than Sector Erase or Erase Suspend during the time-out period resets that bank to the read mode.**

The system can monitor DQ3 to determine if the sector erase timer has timed out (See the section on DQ3: Sector Erase start timeout state indicator.). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the bank returns to reading array data and addresses are no longer latched. Note that while the Embedded Erase operation is in progress, the system can read data from the non-erasing banks. The system can determine the status of the erase operation by reading DQ7 or DQ6/ DQ2 in the erasing bank. Refer to *Write Operation Status* *on page 55* for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

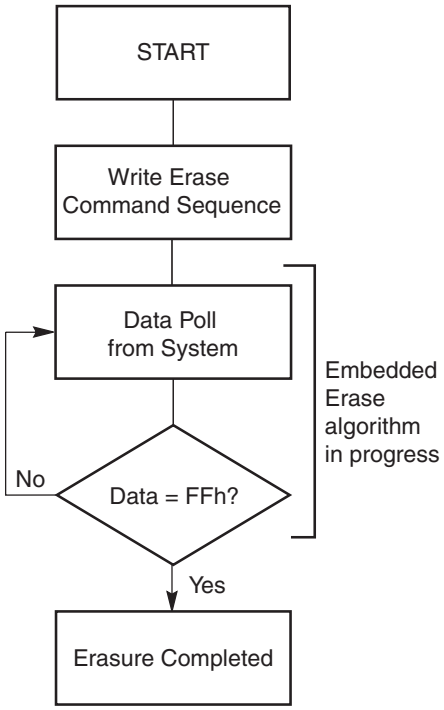
11.8.2 Accelerated Sector Erase

The device offers accelerated sector erase operation through the ACC function. This method of erasing sectors is faster than the standard sector erase command sequence. **The accelerated sector erase function must not be used more than 100 times per sector.** In addition, accelerated sector erase should be performed at room temperature (30°C +-10°C).

The following procedure is used to perform accelerated sector erase:

1. Sectors to be erased must be PPB and DYB cleared. All sectors that remain locked will not be erased.
2. Apply 9V to the ACC input. This voltage must be applied at least 1 µs before executing step 3
3. Issue the standard chip erase command.
4. Monitor status bits DQ2/DQ6 or DQ7 to determine when erasure is complete, just as in the standard erase operation. See *Write Operation Status* *on page 55* for further details.
5. Lower ACC from 9V to V_{CC}.

Figure 11.3 Erase Operation



Note
See the section on DQ3 for information on the sector erase start timeout state indicator.

11.9 Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, program data to, any sector not selected for erasure. The system may also lock or unlock any sector while the erase operation is suspended. **The system must not write the sector lock/unlock command to sectors selected for erasure.** The bank address is required when writing this command. This command is valid only during the sector erase operation, including the minimum t_{SEA} time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of t_{ESL}, erase suspend latency, to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the bank enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) The system may also lock or unlock any sector while in the erase-suspend-read mode. Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to *Write Operation Status* *on page 55* for information on these status bits.

After an erase-suspended program operation is complete, the bank returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. Refer to *Write Operation Status* *on page 55* for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. Refer to the Autoselect Functions and Autoselect Command Sequence sections for details.

To resume the sector erase operation, the system must write the Erase Resume command. The bank address of the erase-suspended bank is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Note: While an erase operation can be suspended and resumed multiple times, a minimum delay of t_{ERS} (Erase Resume to Erase Suspend) is required from resume to the next suspend.

11.10 Program Suspend/Program Resume Commands

The Program Suspend command allows the system to interrupt a embedded programming operation or a "Write to Buffer" programming operation so that data can read from any non-suspended sector. When the Program Suspend command is written during a programming process, the device halts the programming operation within t_{PSL}, program suspend latency, and updates the status bits. Addresses are defined when writing the Program Suspend command.

After the programming operation has been suspended, the system can read array data from any non-suspended sector. The Program Suspend command may also be issued during a programming operation while an erase is suspended. In this case, data may be read from any addresses not in Erase Suspend or Program Suspend. If a read is needed from the Secured Silicon Sector area (One Time Program area), then user must use the proper command sequences to enter and exit this region.

The system may also write the autoselect command sequence when the device is in Program Suspend mode. The device allows reading autoselect codes in the suspended sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to Program Suspend mode, and is ready for another valid operation. See "Autoselect Command Sequence" for more information.

After the Program Resume command is written, the device reverts to programming. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See "Write Operation Status" for more information.

The system must write the Program Resume command (address bits are "don't care") to exit the Program Suspend mode and continue the programming operation. Further writes of the Program Resume command are ignored. Another Program Suspend command can be written after the device has resume programming.

Note: While a program operation can be suspended and resumed multiple times, a minimum delay of t_{PRS} (Program Resume to Program Suspend) is required from resume to the next suspend.

11.11 Lock Register Command Set Definitions

The Lock Register Command Set permits the user to one-time program the Persistent Protection Mode Lock Bit or Password Protection Mode Lock Bit. The Lock Command Set also allows for the reading of the Persistent Protection Mode Lock Bit or Password Protection Mode Lock Bit.

The Lock Register Command Set Entry command sequence must be issued prior to any of the commands listed following to enable proper command execution.

Note that issuing the **Lock Register Command Set Entry** command disables reads and writes for Bank 0. Reads from other banks excluding Bank 0 are allowed.

- Lock Register Program Command
- Lock Register Read Command
- Lock Register Exit Command

The **Lock Register Command Set Exit** command **must** be issued after the execution of the commands to reset the device to read mode, and re-enables reads and writes for Bank 0.

For the device to be permanently set to the Persistent Protection Mode or the Password Protection Mode, the sequence of a Lock Register Command Set Exit command, must be initiated after issuing the **Persistent Protection Mode Lock Bit Program** and the **Password Protection Mode Lock Bit Program** commands. Note that if the **Persistent Protection Mode Lock Bit** and the **Password Protection Mode Lock Bit** are programmed at the same time, neither will be programmed.

11.12 Password Protection Command Set Definitions

The Password Protection Command Set permits the user to program the 64-bit password, verify the programming of the 64-bit password, and then later unlock the device by issuing the valid 64-bit password.

The **Password Protection Command Set Entry** command sequence must be issued prior to any of the commands listed following to enable proper command execution.

Note that issuing the Password Protection Command Set Entry command disables reads and writes for Bank 0. Reads for other banks excluding Bank 0 are allowed. *However Writes to any bank are not allowed.*

- Password Program Command
- Password Read Command
- Password Unlock Command

The Password Program Command permits programming the password that is used as part of the hardware protection scheme. The actual password is 64-bits long. There is no special addressing order required for programming the password.

Once the Password is written and verified, the Password Mode Locking Bit must be set in order to prevent verification. The Password Program Command is only capable of programming “0”s. Programming a “1” after a cell is programmed as a “0” results in a time-out by the Embedded Program Algorithm with the cell remaining as a “0”. The password is all 1’s when shipped from the factory. All 64-bit password combinations are valid as a password.

The Password Verify Command is used to verify the Password. The Password is verifiable only when the Password Mode Lock Bit is not programmed. If the Password Mode Lock Bit is programmed and the user attempts to verify the Password, the device will always drive all 1’s onto the DQ data bus.

The lower two address bits (A1–A0) are valid during the Password Read, Password Program, and Password Unlock.

The Password Unlock command is used to clear the PPB Lock Bit so that the PPBs can be unlocked for modification, thereby allowing the PPBs to become accessible for modification. The exact password must be entered in order for the unlocking function to occur. This command cannot be issued any faster than 1 µs at a time to prevent a hacker from running through the all 64-bit combinations in an attempt to correctly match a password. If the command is issued before the 1 µs execution window for each portion of the unlock, the command will be ignored.

The Password Unlock function is accomplished by writing Password Unlock command and data to the device to perform the clearing of the PPB Lock Bit. The password is 64 bits long. A1 and A0 are used for matching. Writing the Password Unlock command does not need to be address order specific. An example sequence is starting with the lower address A1–A0= 00, followed by A1–A0= 01, A1–A0= 10, and A1–A0= 11.

Approximately 1 µs is required for unlocking the device after the valid 64-bit password is given to the device. It is the responsibility of the microprocessor to keep track of the entering the portions of the 64-bit password with the Password Unlock command, the order, and when to read the PPB Lock bit to confirm successful password unlock. In order to re-lock the device into the Password Mode, the PPB Lock Bit Set command can be re-issued.

The **Password Protection Command Set Exit** command must be issued after the execution of the commands listed previously to reset the device to read mode, otherwise the device will hang. Note that issuing the **Password Protection Command Set Exit** command re-enables reads and writes for Bank 0.

11.13 Non-Volatile Sector Protection Command Set Definitions

The Non-Volatile Sector Protection Command Set permits the user to program the Persistent Protection Bits (PPBs), erase all of the Persistent Protection Bits (PPBs), and read the logic state of the Persistent Protection Bits (PPBs).

The **Non-Volatile Sector Protection Command Set Entry** command sequence must be issued prior to any of the commands listed following to enable proper command execution.

Note that issuing the **Non-Volatile Sector Protection Command Set Entry** command disables reads and writes for *Active Bank*. Reads from other banks excluding *Active Bank* are allowed.

- PPB Program Command
- All PPB Erase Command
- PPB Status Read Command

The PPB Program command is used to program, or set, a given PPB. Each PPB is individually programmed (but is bulk erased with the other PPBs). The specific sector addresses (A_{MAX}–A14) are written at the same time as the program command. If the PPB Lock Bit is set, the PPB Program command will not execute and the command will time-out without programming the PPB.

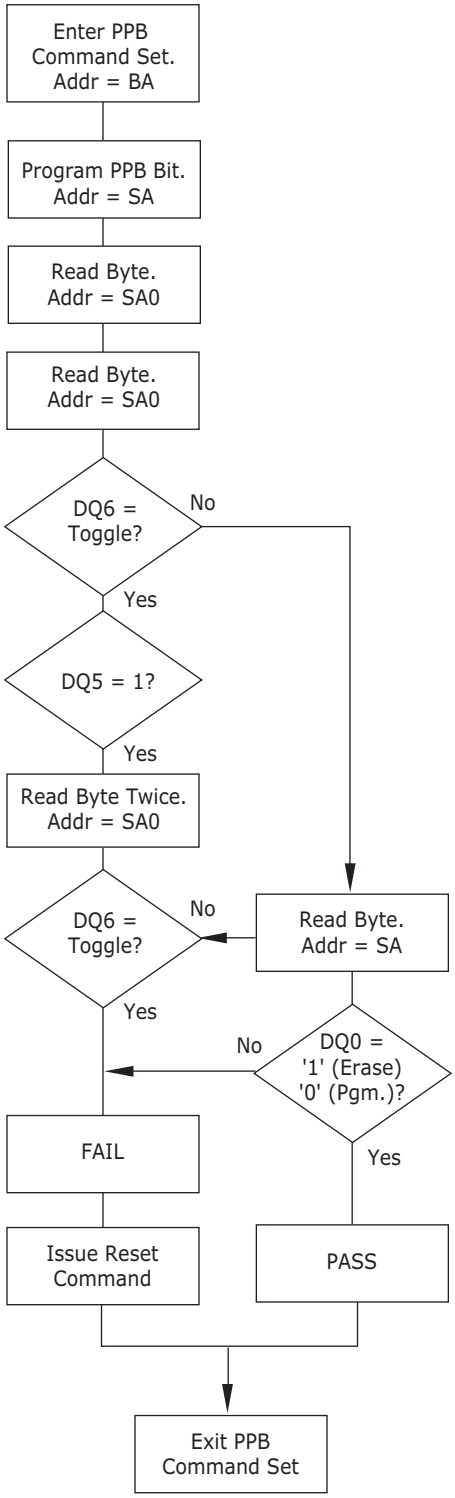
The All PPB Erase command is used to erase all PPBs in bulk. There is no means for individually erasing a specific PPB. Unlike the PPB program, no specific sector address is required. However, when the PPB erase command is written, all Sector PPBs are erased in parallel. If the PPB Lock Bit is set the ALL PPB Erase command will not execute and the command will time-out without erasing the PPBs.

The device will preprogram all PPBs prior to erasing when issuing the All PPB Erase command. Also note that the total number of PPB program/erase cycles has the same endurance as the flash memory array.

The programming state of the PPB for a given sector can be verified by writing a PPB Status Read Command to the device. See Table 11.4 on page 50 for the PPB program/erase algorithm.

Note: PPB reads data only asynchronously.

Figure 11.4 PPB Program/Erase Algorithm



Note

The bank entered during entry is the active bank. Take for example the active bank is BA0. Any reads in BA0 will result in status reads of the PPB bit. If the user wants to set (programmed to "0") in a different bank other than the active bank, say for example BA5, then the active bank switches from BA0 to BA5. Reading in BA5 will result in status read of the bit whereas reading in BA0 will result in true data.

The **Non-Volatile Sector Protection Command Set Exit** command **must** be issued after the execution of the commands listed previously to reset the device to read mode. Note that issuing the **Non-Volatile Sector Protection Command Set Exit** command re-enables *reads and writes for Active Bank.*

After entering the PPB Mode

- The PPB Status Read (BA) is the Mode entry (BA)
- If PPB Program command is given, the new PPB Status Read (BA) will be the same (BA) as given in the PPB Program.
- If PPB Erase command is given, the new PPB Status Read (BA) is the same (BA) as given in the PPB Program or PPB Set Entry, whichever was last.
- During PPB Program or Erase Operation, PPB status read is not available. Only polling data is available in Bank0 and no other bank. Reading from all other banks will give core data.

11.14 Global Volatile Sector Protection Freeze Command Set

The Global Volatile Sector Protection Freeze Command Set permits the user to set the PPB Lock Bit and reading the logic state of the PPB Lock Bit.

The **Volatile Sector Protection Freeze Command Set Entry** command sequence must be issued prior to any of the commands listed following to enable proper command execution.

Reads from all banks excluding mode entry bank are allowed.

- PPB Lock Bit Set Command
- PPB Lock Bit Status Read Command

The PPB Lock Bit Set command is used to set the PPB Lock bit if it is cleared either at reset or if the Password Unlock command was successfully executed. There is no PPB Lock Bit Clear command. Once the PPB Lock Bit is set, it cannot be cleared unless the device is taken through a power-on clear (for Persistent Sector Protection Mode) or the Password Unlock command is executed (for Password Sector Protection Mode). If the Password Mode Locking Bit is set, the PPB Lock Bit status is reflected as set, even after a power-on reset cycle.

The programming state of the PPB Lock Bit can be verified by executing a PPB Lock Bit Status Read Command to the device.

The **Global Volatile Sector Protection Freeze Command Set Exit** command must be issued after the execution of the commands listed previously to reset the device to read mode.

11.15 Volatile Sector Protection Command Set

The Volatile Sector Protection Command Set permits the user to set the Dynamic Protection Bit (DYB), clear the Dynamic Protection Bit (DYB), and read the logic state of the Dynamic Protection Bit (DYB).

The **Volatile Sector Protection Command Set Entry** command sequence must be issued prior to any of the commands listed following to enable proper command execution.

Note that issuing the **Volatile Sector Protection Command Set Entry** command disables reads and writes for the bank selected with the command. Reads for other banks excluding the selected bank are allowed.

- DYB Set Command
- DYB Clear Command
- DYB Status Read Command

The DYB Set/Clear command is used to set or clear a DYB for a given sector. The high order address bits (A23–A14 for the NS256N, A22–A14 for the NS128N and A21-A14 for the NS064N) are issued at the same time as the code 00h or 01h on DQ7-DQ0. All other DQ data bus pins are ignored during the data write cycle. The DYBs are modifiable at any time, regardless of the state of the PPB or PPB Lock Bit. The DYBs are set at power-up or hardware reset.

The programming state of the DYB for a given sector can be verified by writing a DYB Status Read Command to the device.

Note that DYB reads data only asynchronously.

Note: The bank entered during entry is the active bank. Take for example the active bank is BA0. Any reads in BA0 will result in status reads of the DYB bit. If the user wants to set (programmed to “0”) in a different bank other than the active bank, say for example BA5, then the active bank switches from BA0 to BA5. Reading in BA5 will result in status read of the bit whereas reading in BA0 will result in true data.

The **Volatile Sector Protection Command Set Exit** command must be issued after the execution of the commands listed previously to reset the device to read mode.

Note that issuing the **Volatile Sector Protection Command Set Exit** command re-enables reads and writes for the bank selected.

Table 11.4 Command Definitions (Sheet 1 of 3)

Command Sequence (Notes)		Cycles	Bus Cycles (Notes 1–6)													
			First		Second		Third		Fourth		Fifth		Sixth		Seventh	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Asynchronous Read (7)		1	RA	RD												
Reset (8)		1	XXX	F0												
Autoselect (9)	Manufacturer ID	4	555	AA	2AA	55	(BA) 555	90	(BA) X00	0001						
	Device ID	6	555	AA	2AA	55	(BA) 555	90	(BA) X01	(Note 10)	(BA) X0E	(Note 10)	(BA) X0F	(Note 10)		
	Indicator Bits (11)	4	555	AA	2AA	55	(BA) 555	90	(BA) X0D	(Note 11)						
	Revision ID	4	555	AA	2AA	55	(BA) 555	90	(BA) X03							
Unlock Bypass	Mode Entry	3	555	AA	2AA	55	555	20								
	Program (12)	2	XXX	A0	PA	PD										
	Reset (13)	2	BA	90	XXX	00										
CFI		1	55	98												
Program		4	555	AA	2AA	55	555	A0	PA	PD						
Write to Buffer (17)		6	555	AA	2AA	55	SA	25	SA	WC	PA	PD	WBL	PD		
Program Buffer to Flash		1	SA	29												
Write to Buffer Abort Reset (20)		3	555	AA	2AA	55	555	F0								
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10		
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30		
Erase Suspend / Program Suspend (14)		1	BA	B0												
Erase Resume / Program Resume (15)		1	BA	30												
Set Config. Register (28)		4	555	AA	2AA	55	555	D0	X00	CR						
Read Configuration Register		4	555	AA	2AA	55	555	C6	X00	CR						

Table 11.4 Command Definitions (Sheet 2 of 3)

Command Sequence (Notes)		Cycles	Bus Cycles (Notes 1–6)													
			First		Second		Third		Fourth		Fifth		Sixth		Seventh	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Lock Register Command Set Definitions																
Lock	Lock Register Command Set Entry	3	555	AA	2AA	55	555	40								
	Lock Register Bits Program (23)	2	XX	A0	00	data										
	Lock Register Bits Read	1	(BA0) 00	data												
	Lock Register Command Set Exit (24)	2	XX	90	XX	00										
Password Protection Command Set Definitions																
Pass-word	Password Protection Command Set Entry	3	555	AA	2AA	55	555	60								
	Password Program (24, 26)	2	XX	A0	00/ 01/ 02/ 03	PWD0 / PWD1 / PWD2 / PWD3										
	Password Read (27)	4	00	PWD 0	01	PWD1	02	PWD2	03	PWD3						
	Password Unlock (26)	7	00	25	00	03	00	PWD0	01	PWD1	02	PWD2	03	PWD3	00	29
	Password Protection Command Set Exit	2	XX	90	XX	00										
Non-Volatile Sector Protection Command Set Definitions																
PPB	Non-Volatile Sector Protection Command Set Entry	3	555	AA	2AA	55	(BA) 555	C0								
	PPB Program (29)	2	XX	A0	(BA) SA	00										
	All PPB Erase (19, 29)	2	XX	80	SA0	30										
	PPB Status Read	1	(BA) SA	RD (0)												
	Non-Volatile Sector Protection Command Set Exit	2	XX	90	XX	00										
Global Volatile Sector Protection Command Set Definitions																
PPB Lock Bit	Global Volatile Sector Protection Freeze Command Set Entry	3	555	AA	2AA	55	(BA) 555	50								
	PPB Lock Bit Set	2	XX	A0	XX	00										
	PPB Lock Bit Status Read	1	(BA)XX	RD (0)												
	Global Volatile Sector Protection Freeze Command Set Exit	2	XX	90	XX	00										

Table 11.4 Command Definitions (Sheet 3 of 3)

Command Sequence (Notes)		Cycles	Bus Cycles (Notes 1–6)													
			First		Second		Third		Fourth		Fifth		Sixth		Seventh	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Secured Silicon Sector Command Definitions																
Secured Silicon Sector	Secured Silicon Sector Entry (21)	3	555	AA	2AA	55	555	88								
	Secured Silicon Sector Program	2	XX	A0	00	data										
	Secured Silicon Sector Read	1	00	data												
	Secured Silicon Sector Exit (24)	4	555	AA	2AA	55	555	90	XX	00						
Volatile Sector Protection Command Set Definitions																
DYB	Volatile Sector Protection Command Set Entry (21)	3	555	AA	2AA	55	(BA) 555	E0								
	DYB Set	2	XX	A0	(BA) SA	00										
	DYB Clear	2	XX	A0	(BA) SA	01										
	DYB Status Read	1	(BA) SA	RD(0)												
	Volatile Sector Protection Command Set Exit (24)	2	XX	90	XX	00										

Legend

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

PD(0) = Secured Silicon Sector Lock Bit. PD(0), or bit[0].

PD(1) = Persistent Protection Mode Lock Bit. PD(1), or bit[1], must be set to '0' for protection while PD(2), bit[2] must be left as '1'.

PD(2) = Password Protection Mode Lock Bit. PD(2), or bit[2], must be set to '0' for protection while PD(1), bit[1] must be left as '1'.

PD(3) = Protection Mode OTP Bit. PD(3) or bit[3].

SA = Address of the sector to be verified (in autoselect mode) or erased. SA includes BA. Address bits A_{max}–A14 uniquely select any sector (NS256N and NS128N), and address bits A_{max} - A13 uniquely select any sector (NS064N).

BA = Address of the bank (A23–A20 for S29NS256N, A22–A19 for S29NS128N), and A21-A19 for S29NS064N, that is being switched to autoselect mode, is in bypass mode, or is being erased.

CR = Configuration Register set by data bits D15-D0.

PWD3–PWD0 = Password Data. PD3–PD0 present four 16 bit combinations that represent the 64-bit Password

PWA = Password Address. Address bits A1 and A0 are used to select each 16-bit portion of the 64-bit entity.

PWD = Password Data.

RD(0) = DQ0 protection indicator bit. If protected, DQ0 = 0, if unprotected, DQ0 = 1.

RD(1) = DQ1 protection indicator bit. If protected, DQ1 = 0, if unprotected, DQ1 = 1.

RD(2) = DQ2 protection indicator bit. If protected, DQ2 = 0, if unprotected, DQ2 = 1.

RD(4) = DQ4 protection indicator bit. If protected, DQ4 = 0, if unprotected, DQ4 = 1.

WBL = Write Buffer Location. Address must be within the same write buffer page as PA.

WC = Word Count. Number of write buffer locations to load minus 1.

Notes

1. *See Table 8.1 on page 14 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.*
4. *Data bits DQ15–DQ8 are don't care in command sequences, except for RD and PD.*
5. *Unless otherwise noted, address bits A_{max}–A12 are don't cares.*
6. *Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. The system must write the reset command to return the device to reading array data.*
7. *No unlock or command cycles required when bank is reading array data.*

8. *The Reset command is required to return to reading array data (or to the erase-suspend-read mode if previously in Erase Suspend) when a bank is in the autoselect mode, or if DQ5 goes high (while the bank is providing status information).*
9. *The fourth cycle of the autoselect command sequence is a read cycle. The system must read device IDs across the 4th, 5th, and 6th cycles, The system must provide the bank address. See the Autoselect Command Sequence section for more information.*
10. *See Table 11.2 on page 40 for description of bus operations.*
11. *See the Autoselect Command Sequence on page 40.*
12. *The Unlock Bypass command sequence is required prior to this command sequence.*
13. *The Unlock Bypass Reset command is required to return to reading array data when the bank is in the unlock bypass mode.*
14. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation, and requires the bank address.*
15. *The Erase Resume command is valid only during the Erase Suspend mode, and requires the bank address.*
16. *Command is valid when device is ready to read array data or when device is in autoselect mode.*
17. *The total number of cycles in the command sequence is determined by the number of words written to the write buffer. The maximum number of cycles in the command sequence is 37.*
18. *The entire four bus-cycle sequence must be entered for which portion of the password.*
19. *The ALL PPB ERASE command will pre-program all PPBs before erasure to prevent over-erasure of PPBs.*
20. *Command sequence resets device for next command after write-to-buffer operation.*
21. *Entry commands are needed to enter a specific mode to enable instructions only available within that mode.*
22. *Write Buffer Programming can be initiated after Unlock Bypass Entry.*
23. *If both the Persistent Protection Mode Locking Bit and the password Protection Mode Locking Bit are set a the same time, the command operation will abort and return the device to the default Persistent Sector Protection Mode.*
24. *The Exit command must be issued to reset the device into read mode. Otherwise the device will hang.*
25. *Note: Autoselect, CFI, OTP, Unlock Bypass Mode and all ASP modes cannot be nested with each other.*
26. *Only A7 - A0 (lower address bits) are used*
27. *A_{max}–A0 (all address bits) are used.*
28. *Requires the RESET# command to configure the configuration register.*
29. *See Figure 11.4 on page 50 for details.*

12. Write Operation Status

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 12.2 on page 60 and the following subsections describe the function of these bits. DQ7 and DQ6 each offers a method for determining whether a program or erase operation is complete or in progress.

12.1 DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether a bank is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence. **Note that the Data# Polling is valid only for the last word being programmed in the write-buffer-page during Write Buffer Programming. Reading Data# Polling status on any word other than the last word to be programmed in the write-buffer-page will return false status information.**

During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately t_{PSP}, then that bank returns to the read mode.

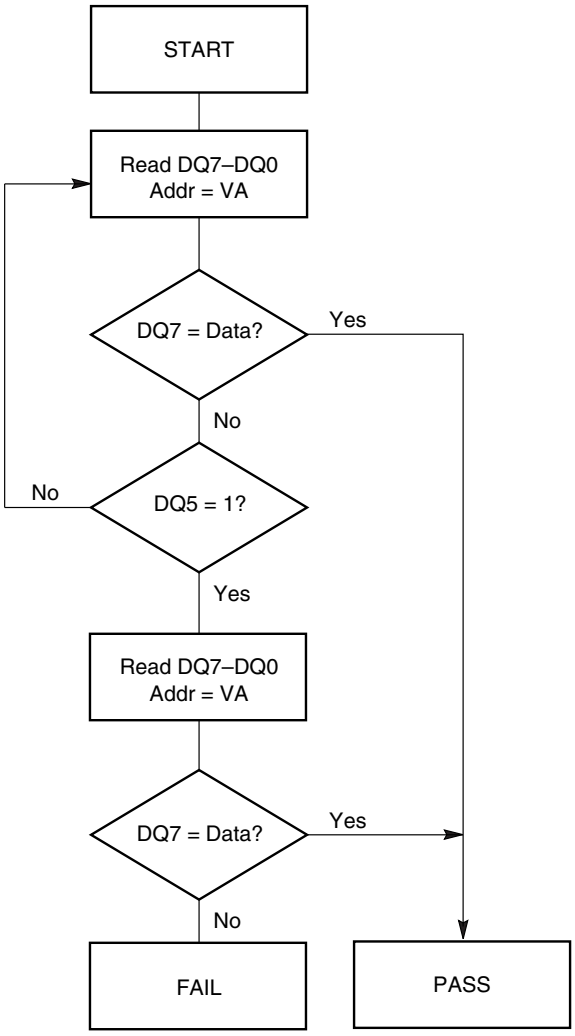
During the Embedded Erase algorithm, Data# Polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, or if the bank enters the Erase Suspend mode, Data# Polling produces a “1” on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately t_{ASP}, then the bank returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ6–DQ0 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ6–DQ0 may be still invalid. Valid data on DQ7–DQ0 will appear on successive read cycles.

Table 12.2 on page 60 shows the outputs for Data# Polling on DQ7. Figure 12.1 on page 56 shows the Data# Polling algorithm. Figure 19.9 on page 72 in the *AC Characteristics* section shows the Data# Polling timing diagram.

Figure 12.1 Data# Polling Algorithm



Notes

1. *VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.*

12.2 RDY: Ready

The RDY pin is a dedicated status output that indicates valid output data on A/DQ15–A/DQ0 during burst (synchronous) reads. When RDY is asserted (RDY = V_{OH}), the output data is valid and can be read. When RDY is de-asserted (RDY = V_{OL}), the system should wait until RDY is re-asserted before expecting the next word of data.

In synchronous (burst) mode with CE# = OE# = V_{IL}, RDY is de-asserted under the following conditions: during the initial access; after crossing the internal boundary between addresses 7Eh and 7Fh (and addresses offset from these by a multiple of 64). The RDY pin will also switch during status reads when a clock signal drives the CLK input. In addition, RDY = V_{OH} when CE# = V_{IL} and OE# = V_{IH}, and RDY is Hi-Z when CE# = V_{IH}.

In asynchronous (non-burst) mode, the RDY pin does not indicate valid or invalid output data. Instead, RDY = V_{OH} when CE# = V_{IL}, and RDY is Hi-Z when CE# = V_{IH}.

12.3 DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address in the same bank, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. Note that OE# must be low during toggle bit status reads. When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately t_{ASP}, all sectors protected toggle time, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on *DQ7: Data# Polling on page 55*).

If a program address falls within a protected sector, DQ6 toggles for approximately t_{PSP} after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

See the following for additional information: (toggle bit flowchart), *DQ6: Toggle Bit I on page 57* (description), Figure 19.10 on page 73 (toggle bit timing diagram), and Table 12.1 on page 59 (compares DQ2 and DQ6).

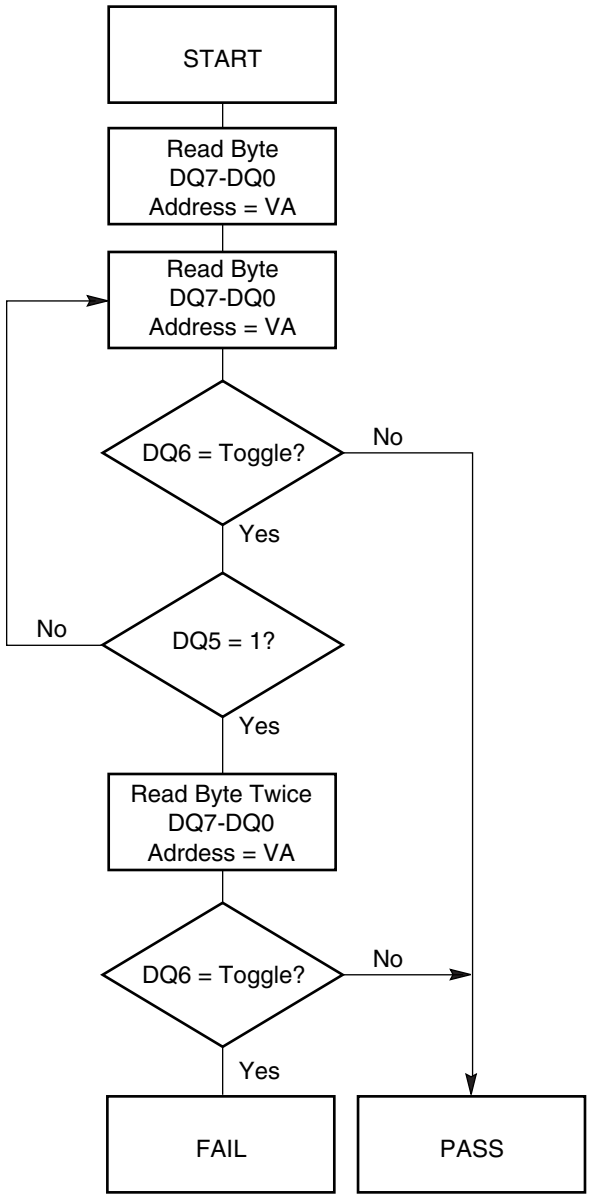
12.4 DQ2: Toggle Bit II

The “Toggle Bit II” on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. Note that OE# must be low during toggle bit status reads. But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 12.2 on page 60 to compare outputs for DQ2 and DQ6.

See the following for additional information: (toggle bit flowchart), *DQ6: Toggle Bit I on page 57* (description), Figure 19.10 on page 73 (toggle bit timing diagram), and Table 12.1 on page 59 (compares DQ2 and DQ6).

Figure 12.2 Toggle Bit Algorithm



Note
The system should recheck the toggle bit even if DQ5 = "1" because the toggle bit may stop toggling as DQ5 changes to "1." See the subsections on DQ6 and DQ2 for more information.

Table 12.1 DQ6 and DQ2 Indications

If device is	and the system reads	then DQ6	and DQ2
programming,	at any address,	toggles,	does not toggle.
actively erasing,	at an address within a sector selected for erasure,	toggles,	also toggles.
	at an address within sectors *not* selected for erasure,	toggles,	does not toggle.
erase suspended,	at an address within a sector selected for erasure,	does not toggle,	toggles.
	at an address within sectors *not* selected for erasure,	returns array data,	returns array data. The system can read from any sector not selected for erasure.
programming in erase suspend	at any address,	toggles,	is not applicable.

12.5 Reading Toggle Bits DQ6/DQ2

Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation.

12.6 DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a “1,” indicating that the program or erase cycle was not successfully completed.

The device may output a “1” on DQ5 if the system tries to program a “1” to a location that was previously programmed to “0.” **Only an erase operation can change a “0” back to a “1.”** Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a “1.”

Under both these conditions, the system must write the reset command to return to the read mode (or to the erase-suspend-read mode if a bank was previously in the erase-suspend-program mode).

12.7 DQ3: Sector Erase Start Timeout State Indicator

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a “0” to a “1.” If the time between additional sector erase commands from the system can be assumed to be less than t_{SEA}, the system need not monitor DQ3. See also the *Sector Erase Command Sequence* section.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is “1,” the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is “0,” the device will accept additional sector erase commands.

To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 12.2 on page 60 shows the status of DQ3 relative to the other status bits.

12.8 DQ1: Write to Buffer Abort

DQ1 indicates whether a Write to Buffer operation was aborted. Under these conditions DQ1 produces a '1'. The system must issue the Write to Buffer Abort Reset command sequence to return the device to reading array data. See *Write Buffer Programming Operation on page 18* for more details.

Table 12.2 Write Operation Status

Status			DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	DQ1 (Note 4)
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	N/A
Program Suspend Mode (Note 3)	Reading within Program Suspended Sector		Valid data for all address except the address being programed, which will return invalid data					
	Reading within Non-Program Suspended Sector		Data					
Erase Suspend Mode	Erase-Suspend-Read	Erase Suspended Sector	1	No toggle	0	N/A	Toggle	N/A
		Non-Erase Suspended Sector	Data	Data	Data	Data	Data	Data
	Erase-Suspend-Program		DQ7#	Toggle	0	N/A	N/A	N/A
Write to Buffer (Note 5)	BUSY State		DQ7#	Toggle	0	N/A	N/A	0
	Exceeded Timing Limits		DQ7#	Toggle	1	N/A	N/A	0
	ABORT State		DQ7#	Toggle	0	N/A	N/A	1

Notes

1. *DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*
3. *Data are invalid for addresses in a Program Suspended sector.*
4. *DQ1 indicates the Write to Buffer ABORT status during Write Buffer Programming operations.*
5. *The data-bar polling algorithm should be used for Write Buffer Programming operations. Note that DQ7# during Write Buffer Programming indicates the data-bar for DQ7 data* ***for the LAST LOADED WRITE-BUFFER ADDRESS location****.*

13. Absolute Maximum Ratings

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –65°C to +125°C

Voltage with Respect to Ground, All Inputs and I/Os except ACC (Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V

V_{CC} (Note 1) . . . . . –0.5 V to +2.5 V

ACC (Note 2) . . . . . –0.5 V to + 9.5 V

Output Short Circuit Current (Note 3) . . . . . 100 mA

Notes

1. *Minimum DC voltage on input or I/Os is –0.5 V. During voltage transitions, input at I/Os may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 13.1 on page 61. Maximum DC voltage on input and I/Os is V_{CC} + 0.5 V. During voltage transitions outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See Figure 13.2 on page 61.*
2. *Minimum DC input voltage on ACC is –0.5 V. During voltage transitions, ACC may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 13.1 on page 61. Maximum DC input voltage on ACC is +9.5 V which may overshoot to +10.5 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
4. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

Figure 13.1 Maximum Negative Overshoot Waveform

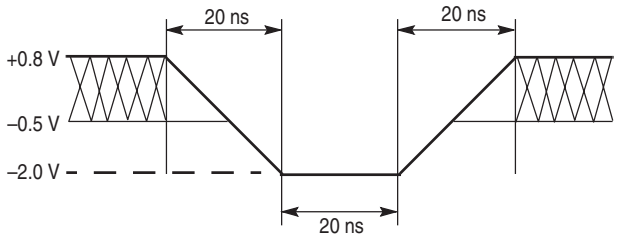
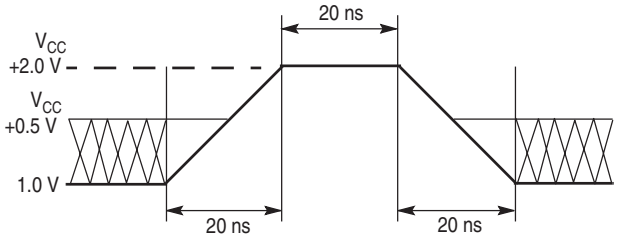


Figure 13.2 Maximum Positive Overshoot Waveform



14. Operating Ranges

Ambient Temperature (T_A) . . . . . –25°C to +85°C

Ambient Temperature (T_A) during Accelerated Sector Erase . . . . . +20°C to +40°C

V_{CC} Supply Voltages

V_{CC} min . . . . . +1.70 V

V_{CC} max . . . . . +1.95 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

15. DC Characteristics

15.1 CMOS Compatible

Parameter	Description	Test Conditions (Note 1)		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1	µA
I_{CCB}	V_{CC} Active Burst Read Current (Note 5)	CE# = V_{IL}, OE# = V_{IL}, burst length = 8	80 MHz		26	36	mA
			66 MHz		24	33	
		CE# = V_{IL}, OE# = V_{IL}, burst length = 16	80 MHZ		26	38	mA
			66 MHz		24	35	
		CE# = V_{IL}, OE# = V_{IL}, burst length = 32	80 MHZ		28	40	mA
			66 MHz		26	37	
		CE# = V_{IL}, OE# = V_{IL}, burst length = continuous	80 MHZ		30	42	mA
			66 MHz		28	39	
I_{CC1}	V_{CC} Active Asynchronous Read Current (Note 2)	CE# = V_{IL}, OE# = V_{IH}	5 MHz		15	18	mA
			1 MHz		3	4	mA
I_{CC2}	V_{CC} Active Write Current (Note 3)	CE# = V_{IL}, OE# = V_{IH}, ACC = V_{IH}			19	52.5	mA
I_{CC3}	V_{CC} Standby Current (Note 4)	CE# = V_{IH}, RESET# = V_{IH} (Note 8)			20	70	µA
I_{CC4}	V_{CC} Reset Current	RESET# = V_{IL}, CLK = V_{IL} (Note 8)			80	150	µA
I_{CC5}	V_{CC} Active Current (Read While Write)	CE# = V_{IL}, OE# = V_{IL} (Note 8) (Note 9)			50	60	mA
I_{CC6}	V_{CC} Sleep Current	CE# = V_{IL}, OE# = V_{IH}			20	70	µA
I_{PPW}	Accelerated Program Current (Note 6)	ACC = 9 V			20	30	mA
I_{PPE}	Accelerated Erase Current (Note 6)	ACC = 9 V			20	30	mA
V_{IL}	Input Low Voltage			–0.5		0.4	V
V_{IH}	Input High Voltage			V_{CCQ} – 0.4		V_{CCQ} + 0.2	V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA, $V_{CC} = V_{CC\ min}$				0.1	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA, $V_{CC} = V_{CC\ min}$		V_{CCQ} – 0.1			V
V_{ID}	Voltage for Accelerated Program			8.5		9.5	V
V_{LKO}	Low V_{CC} Lock-out Voltage			1.0		1.4	V

Notes

1. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}$max.*
2. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.*
3. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
4. *Device enters automatic sleep mode when addresses are stable for t_{ACC} + 20 ns. Typical sleep mode current is equal to I_{CC3}.*
5. *Specifications assume 8 I/Os switching.*
6. *Not 100% tested. ACC is not a power supply pin.*
7. *While measuring Output Leakage Current, CE# should be at V_{IH}.*
8. *$V_{IH} = V_{CC}$ ± -0.2 V and V_{IL} > -0.1V.*
9. *Clock Frequency 66 MHz and in Continuous Mode.*

16. Test Conditions

Figure 16.1 Test Setup

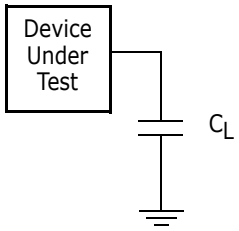


Table 16.1 Test Specifications

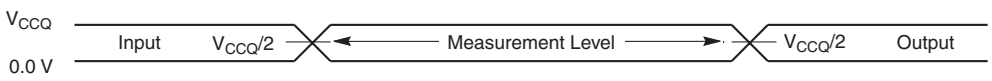
Test Condition	All Speeds	Unit
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	2.5 @ 80 MHz, 3 @ 66 MHz	ns
Input Pulse Levels	0.0–V_{CC}	V
Input timing measurement reference levels	$V_{CCQ}/2$	V
Output timing measurement reference levels	$V_{CCQ}/2$	V

17. Key to Switching Waveforms

Waveform	Inputs	Outputs
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

18. Switching Waveforms

Figure 18.1 Input Waveforms and Measurement Levels



19. AC Characteristics

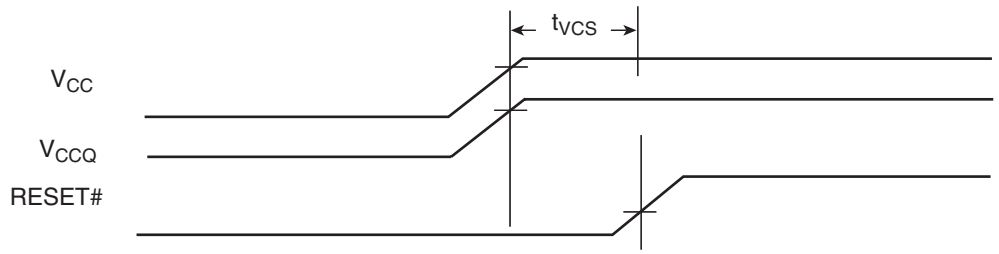
19.1 V_{CC} Power-up

Parameter	Description	Test Setup	Speed	Unit
t_{VCS}	V_{CC} Setup Time	Min	1	ms

Notes

1. *V_{CC} >+ V_{CCQ} - 100 mV*
2. *V_{CC} ramp rate is >1 V/100 µs*

Figure 19.1 V_{CC} Power-up Diagram CLK Characterization

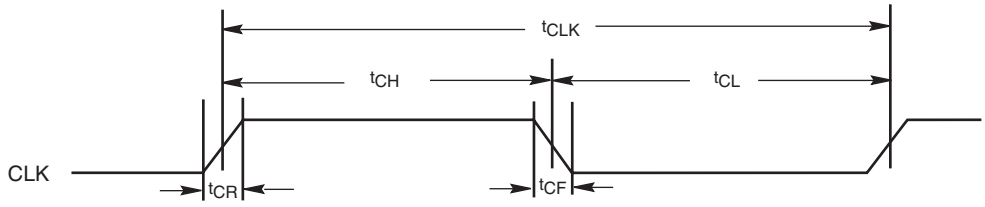


Parameter	Description		(80 MHz)	(66 MHz)	Unit
f_{CLK}	CLK Frequency	Max	80	66	MHz
t_{CLK}	CLK Period	Min	12.5	15.0	ns
t_{CH}	CLK High Time	Min	5	6.1	ns
t_{CL}	CLK Low Time				
t_{CR} (Note)	CLK Rise Time	Max	2.5	3	ns
t_{CF} (Note)	CLK Fall Time				

Notes

1. *Clock jitter of +/- 5% permitted.*
2. *Not 100% tested.*

Figure 19.2 CLK Characterization

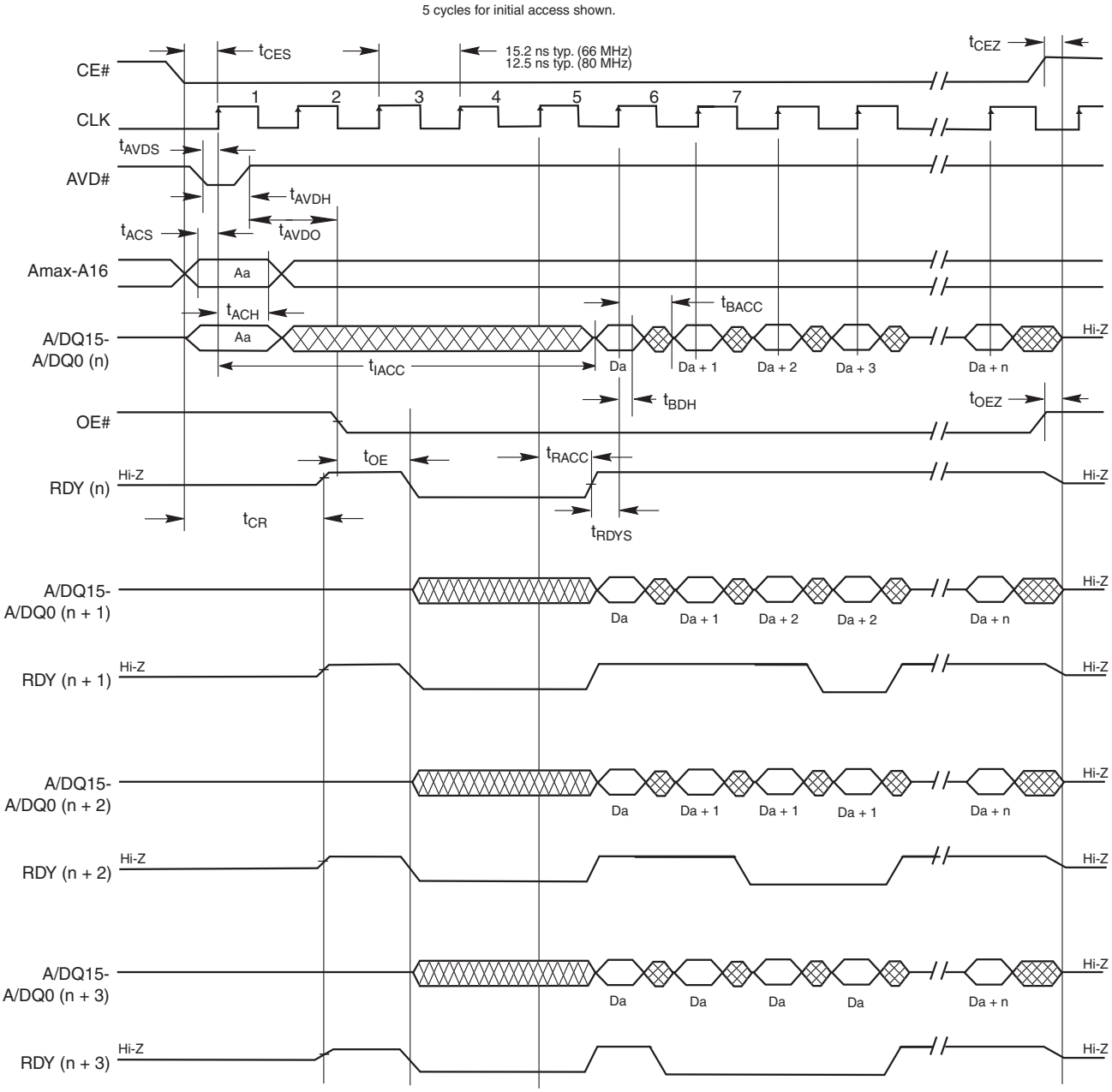


19.2 Synchronous/Burst Read

Parameter		Description		(80 MHz)	(66 MHz)	Unit
JEDEC	Standard					
	t_{IACC}	Initial Access Time	Max	80		ns
	t_{BACC}	Burst Access Time Valid Clock to Output Delay	Max	9	11.0	ns
	t_{AVDS}	AVD# Setup Time to CLK	Min	4	4	ns
	t_{AVDH}	AVD# Hold Time from CLK	Min	6	6	ns
	t_{AVDO}	AVD# High to OE# Low	Min	0		ns
	t_{ACS}	Address Setup Time to CLK	Min	4	4	ns
	t_{ACH}	Address Hold Time from CLK	Min	6	6	ns
	t_{BDH}	Data Hold Time from Next Clock Cycle	Min	3	3	ns
	t_{OE}	Output Enable to Data, or RDY Valid	Max	9	11.0	ns
	t_{CEZ}	Chip Enable to High Z (Note)	Max	8	10	ns
	t_{OEZ}	Output Enable to High Z (Note)	Max	8	10	ns
	t_{CES}	CE# Setup Time to CLK	Min	4		ns
	t_{RDYS}	RDY Setup Time to CLK	Min	3.5	4	ns
	t_{RACC}	Ready access time from CLK	Max	9	11.0	ns

Note
Not 100% tested.

Figure 19.3 Burst Mode Read



Notes

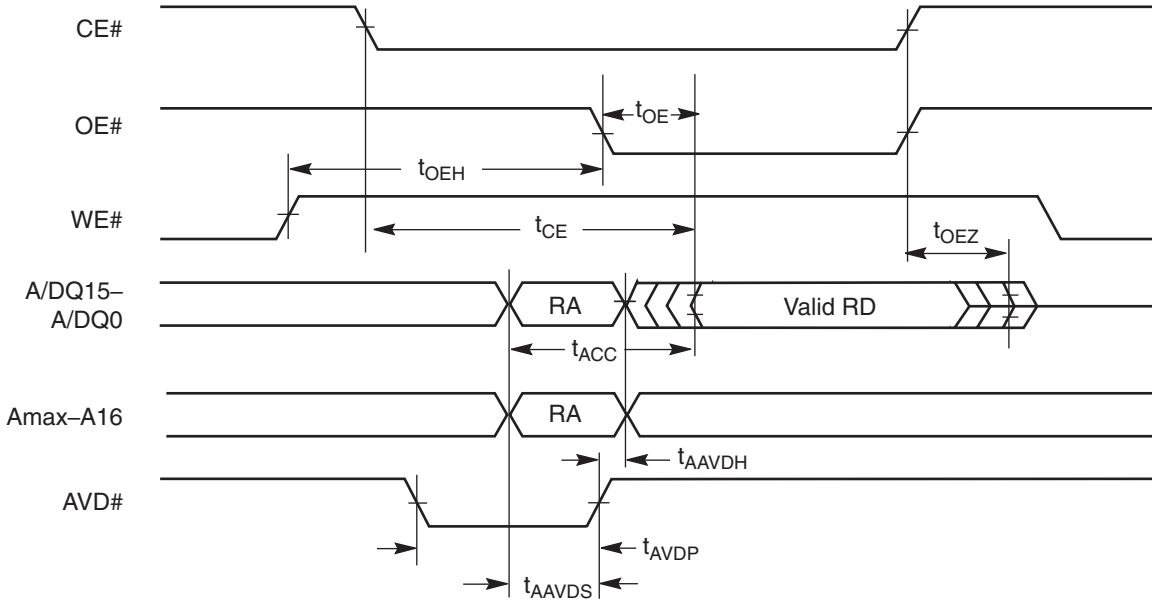
1. *Figure shows total number of clock set to five.*
2. *If any burst address occurs at “address + 1”, “address + 2”, or “address +3”, additional clock delays are inserted, and are indicated by RDY.*

19.3 Asynchronous Read

Parameter		Description			(80 MHz)	(66 MHz)	Unit
JEDEC	Standard						
	t_{CE}	Access Time from CE# Low		Max	80		ns
	t_{ACC}	Asynchronous Access Time		Max	80		ns
	t_{AVDP}	AVD# Low Time		Min	8		ns
	t_{AAVDS}	Address Setup Time to Rising Edge of AVD		Min	4	4	ns
	t_{AAVDH}	Address Hold Time from Rising Edge of AVD		Min	3.7	3.7	ns
	t_{OE}	Output Enable to Output Valid		Max	9	11.0	ns
	t_{OEH}	Output Enable Hold Time	Read	Min	0		ns
			Toggle and Data# Polling	Min	10		ns
	t_{OEZ}	Output Enable to High Z (See Note)		Max	10		ns

Note
Not 100% tested.

Figure 19.4 Asynchronous Mode Read



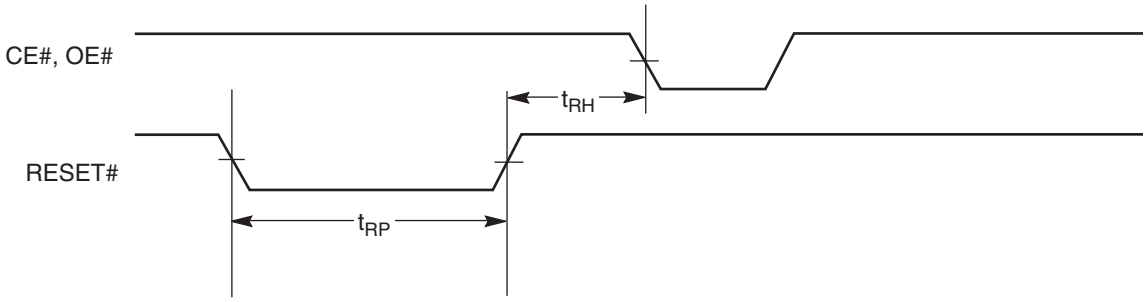
Note
RA = Read Address, RD = Read Data.

19.4 Hardware Reset (RESET#)

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{RP}	RESET# Pulse Width	Min	200	ns
	t_{RH}	Reset High Time Before Read	Min	10	µs

Note
Not 100% tested

Figure 19.5 Reset Timings



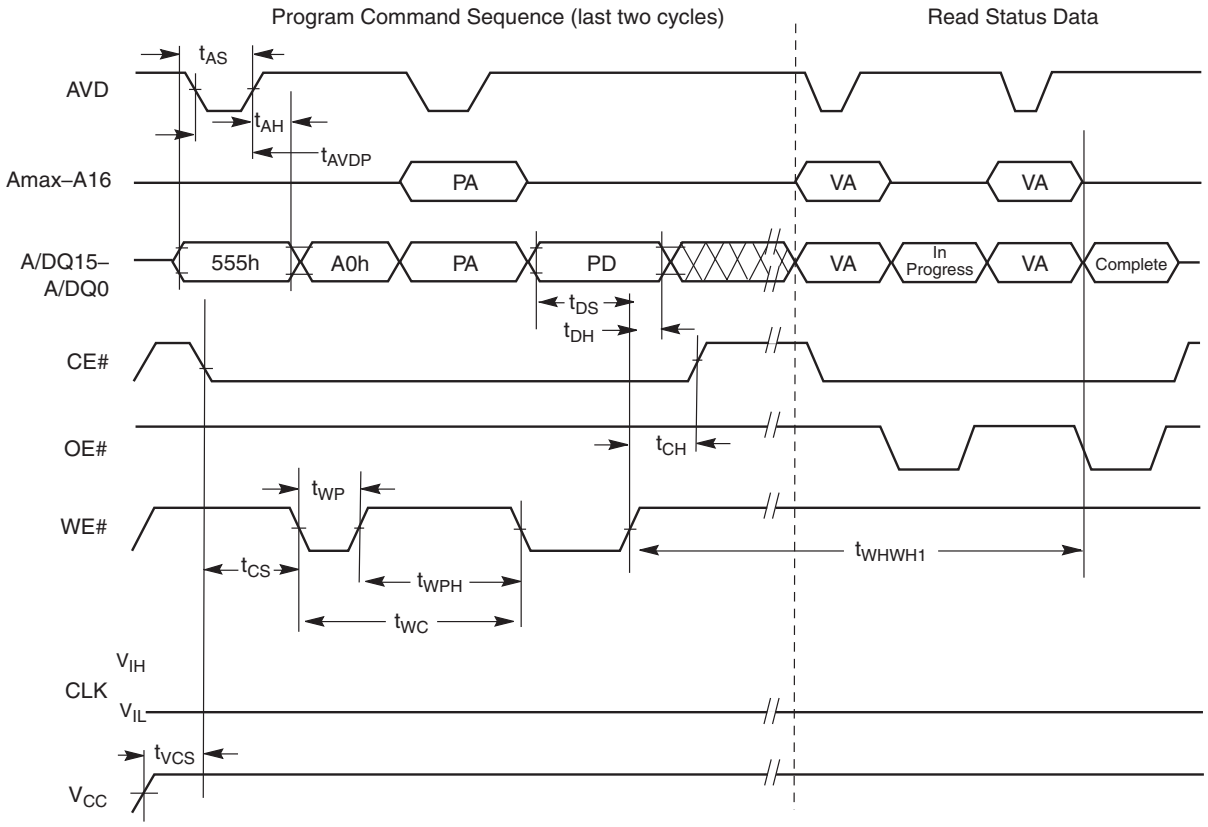
19.5 Erase/Program Operations

Parameter		Description		(80 MHz)	(66 MHz)	Unit
JEDEC	Standard					
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	45	45	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	4	4	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	6	6	ns
	t_{AVDP}	AVD# Low Time	Min	8		ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	20	25	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0		ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write	Typ	0		ns
t_{ELWL}	t_{CS}	CE# Setup Time to WE#	Typ	8	8	ns
t_{WHEH}	t_{CH}	CE# Hold Time	Typ	0		ns
t_{WLWH}	t_{WP}/t_{WRL}	Write Pulse Width	Typ	30		ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Typ	20		ns
	$t_{SR/W}$	Latency Between Read and Write Operations	Min	0		ns
	t_{ACC}	ACC Rise and Fall Time	Min	500		ns
	t_{VPS}	ACC Setup Time (During Accelerated Programming)	Min	1		µs
	t_{VCS}	V_{CC} Setup Time	Min	50		µs
	t_{SEA}	Sector Erase Accept Time-out	Max	50		µs
	t_{ESL}	Erase Suspend Latency	Max	35		µs
	t_{PSL}	Program Suspend Latency	Max	35		µs
	t_{ERS}	Erase Resume to Erase Suspend	Min	30		µs
	t_{PRS}	Program Resume to Program Suspend	Min	30		µs
	t_{PSP}	Toggle Time During Programming Within a Protected Sector	Typ	1		µs
	t_{ASP}	Toggle Time During Sector Protection	Typ	100		µs
	t_{WEP}	Noise Pulse Margin on WE#	Max	3		ns

Notes

1. *Not 100% tested.*
2. *See the Erase and Programming Performance section for more information.*
3. *Does not include the preprogramming time.*

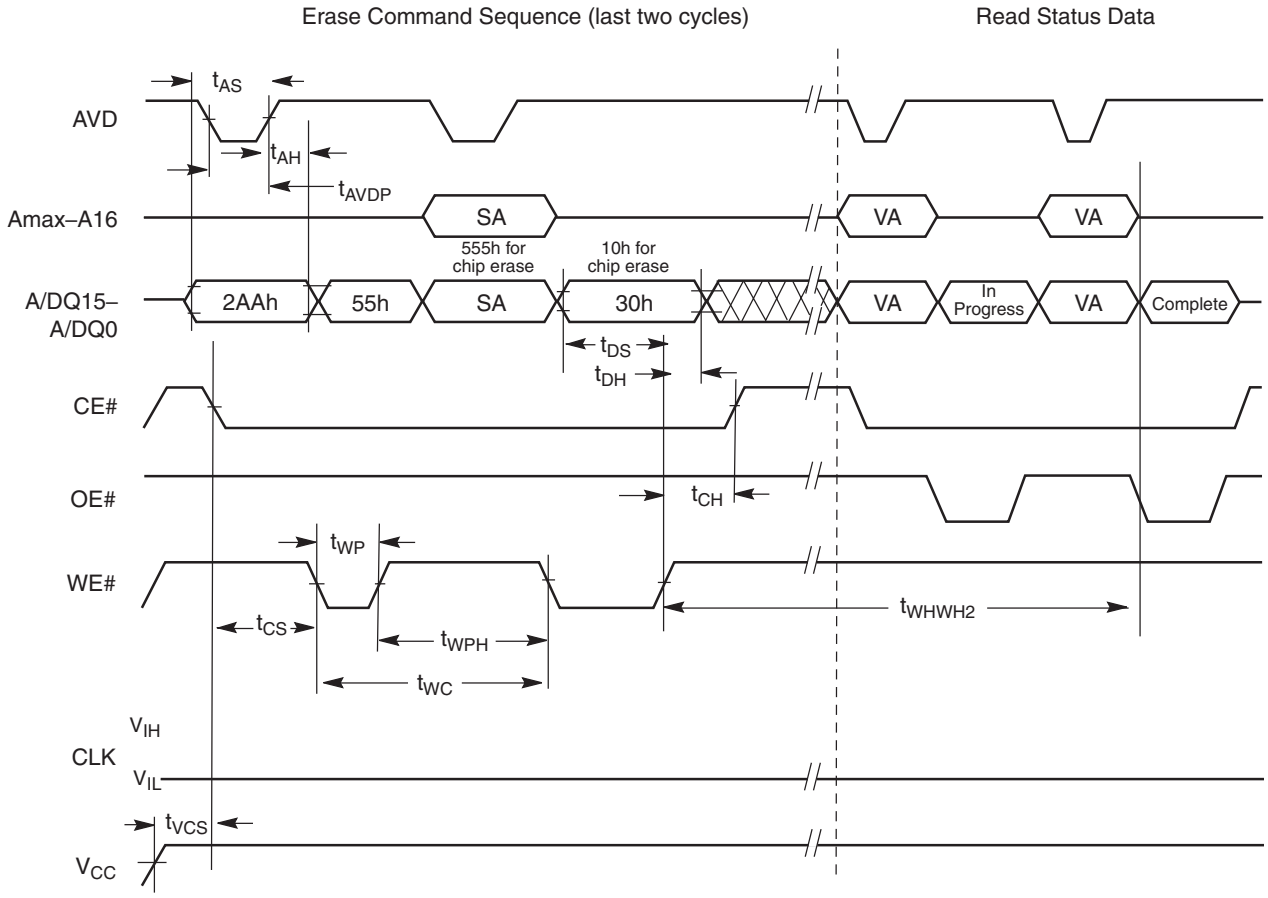
Figure 19.6 Program Operation Timings



Notes

1. *PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.*
2. *"In progress" and "complete" refer to status of program operation.*
3. *A_{max}–A16 are don't care during command sequence unlock cycles.*

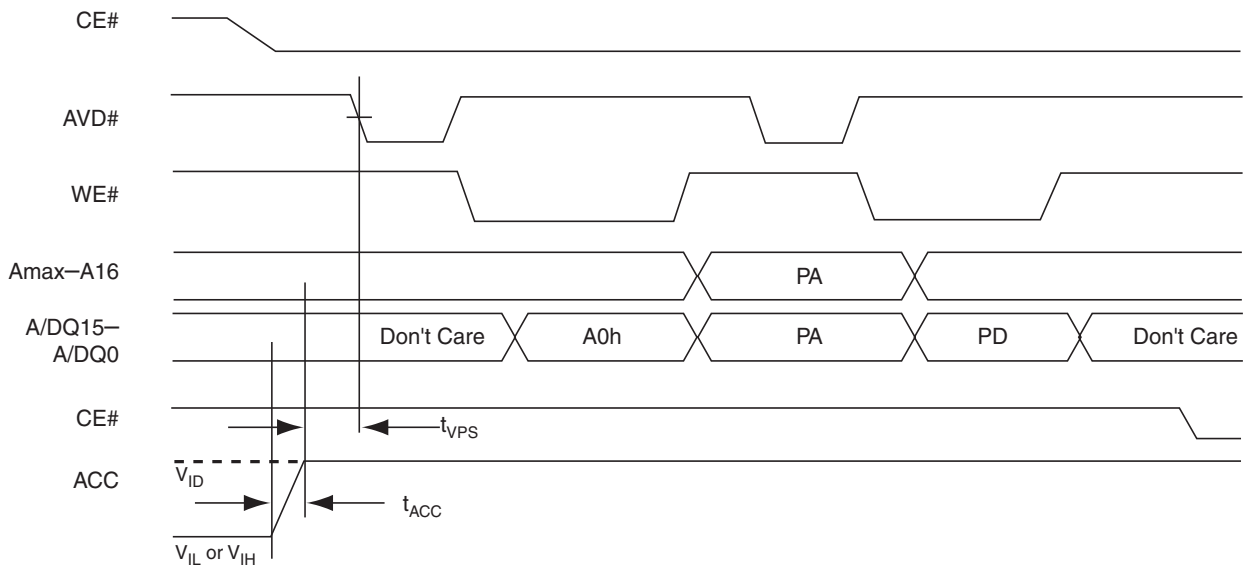
Figure 19.7 Chip/Sector Erase Operations



Notes

1. *SA is the sector address for Sector Erase.*
2. *Address bits A_{max}–A16 are don't cares during unlock cycles in the command sequence.*

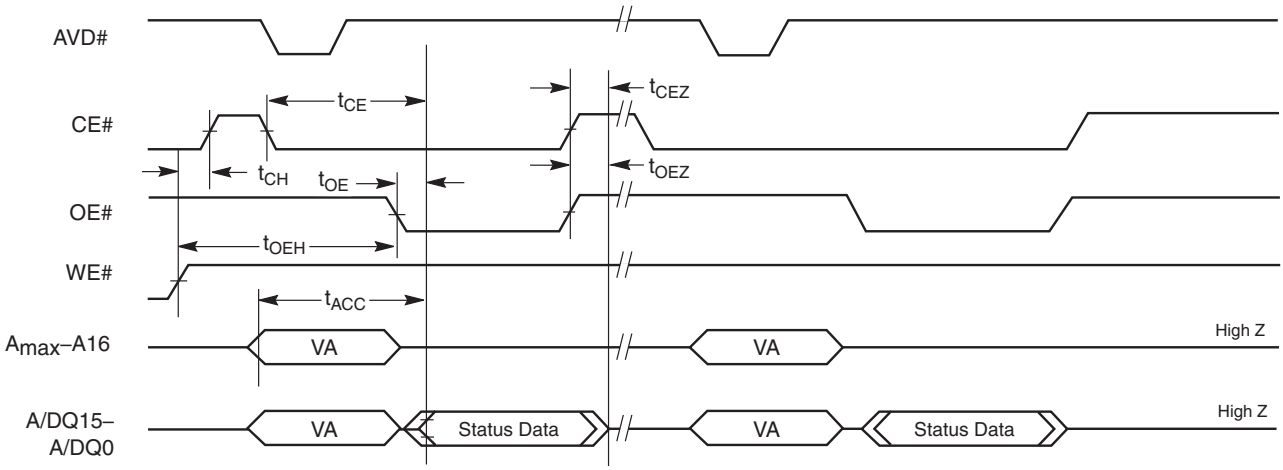
Figure 19.8 Accelerated Unlock Bypass Programming Timing



Notes

1. *ACC can be left high for subsequent programming pulses.*
2. *Use setup and hold times from conventional program operation.*

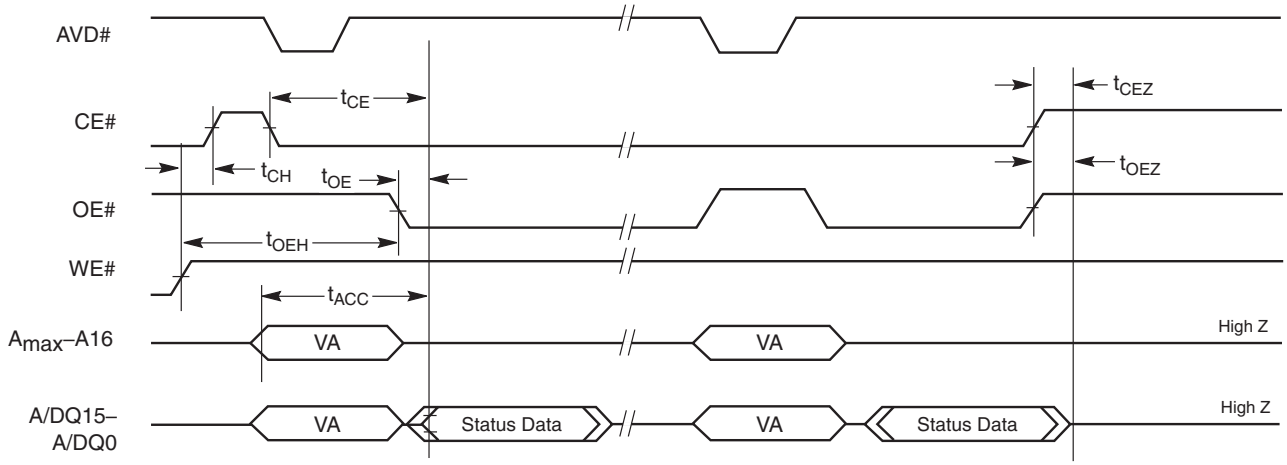
Figure 19.9 Data# Polling Timings (During Embedded Algorithm)



Notes

1. *All status reads are asynchronous.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, and Data# Polling will output true data.*

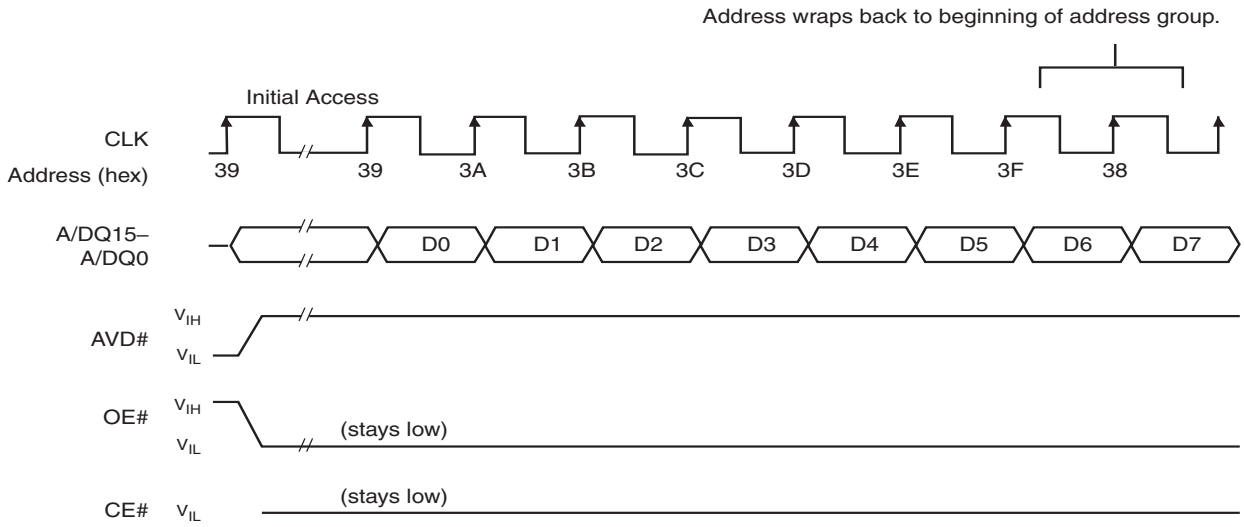
Figure 19.10 Toggle Bit Timings (During Embedded Algorithm)



Notes

1. *All status reads are asynchronous.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, the toggle bits will stop toggling.*

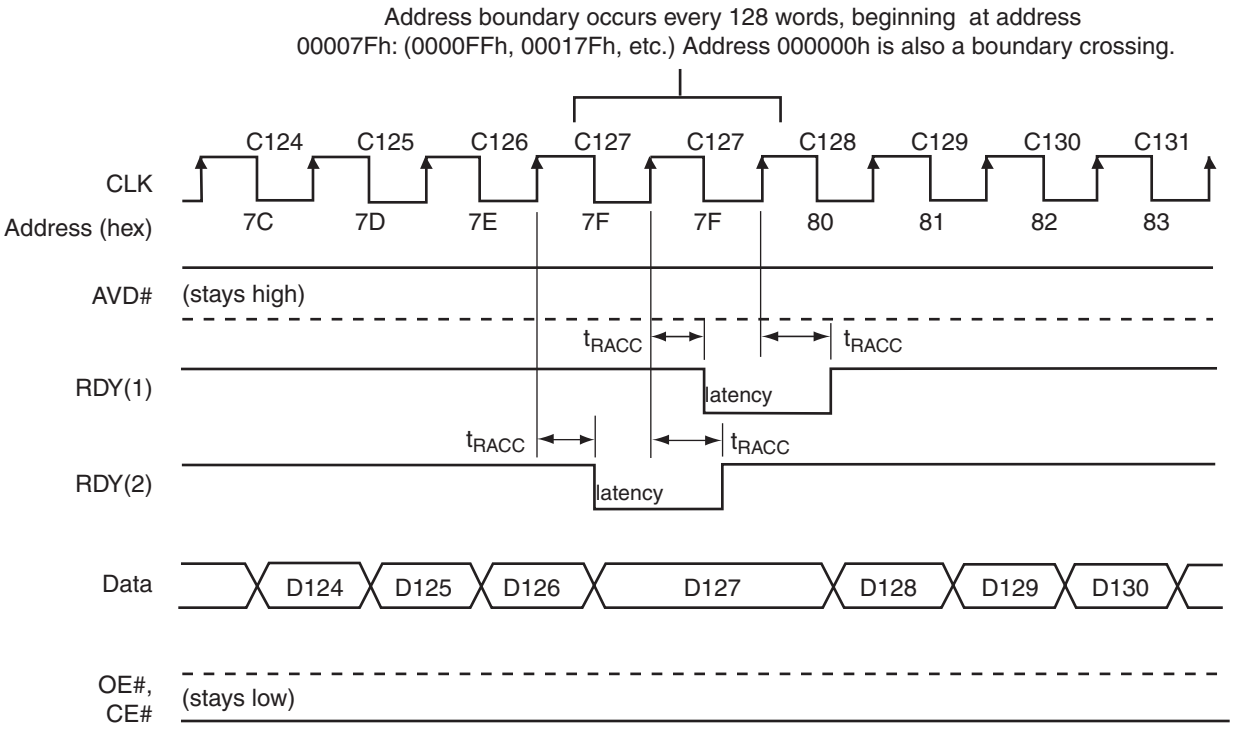
Figure 19.11 8-, 16-, and 32-Word Linear Burst Address Wrap Around



Note

8-word linear burst mode shown. 16- and 32-word linear burst read modes behave similarly. D0 represents the first word of the linear burst.

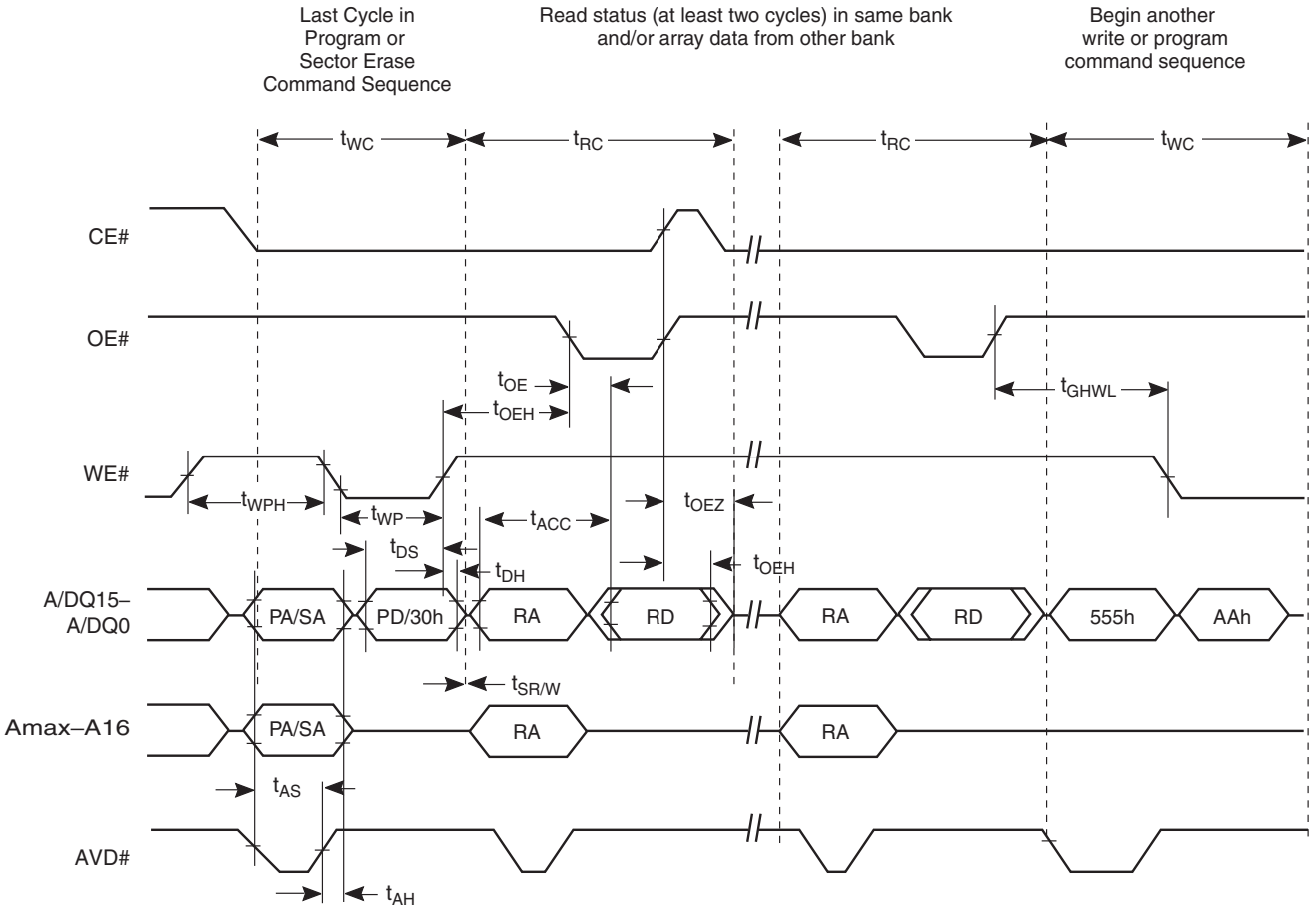
Figure 19.12 Latency with Boundary Crossing



Notes

1. *Cxx indicates the clock that triggers data Dxx on the outputs; for example, C60 triggers D60.*
2. *At frequencies less than or equal to 66 Mhz, there is no latency.*

Figure 19.13 Back-to-Back Read/Write Cycle Timings



Note

Breakpoints in waveforms indicate that system may alternately read array data from the "non-busy bank" while checking the status of the program or erase operation in the "busy" bank. The system should read status twice to ensure valid information.

20. Erase and Programming Performance

Parameter			Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time	64 Kword	V_{CC}	0.8	3.5	s	Excludes 00h programming prior to erasure (Note 5)
	32 Kword	V_{CC}	0.6	3		
	16 Kword	V_{CC}	0.15	2		
	8 Kword	V_{CC}	0.12	2		
Chip Erase Time		V_{CC}	154 (NS256N)	308 (NS256N)		
			77 (NS128N)	154 (NS128N)		
			58 (NS064N)	116 (NS064N)		
		ACC	131 (NS256N)	262 (NS256N)		
			66 (NS128N)	132 (NS128N)		
			50 (NS064N)	100 (NS064N)		
Single Word Programming Time		V_{CC}	40	400	us	
		ACC	24	240		
Effective Word Programming Time utilizing Program Write Buffer		V_{CC}	9.4	94		
		ACC	6	60		
Total 32-Word Buffer Programming Time		V_{CC}	300	3000		
		ACC	192	1920		
Chip Programming Time (Note 4)		V_{CC}	157.3 (NS256N)	314.6 (NS256N)	s	Excludes system level overhead (Note 6)
			78.6 (NS128N)	157.3 (NS128N)		
			39.3 (NS064N)	78.6 (NS064N)		
		ACC	101 (NS256N)	202 (NS256N)		
			51 (NS128N)	102 (NS128N)		
			26 (NS064N)	52 (NS064N)		

Notes

1. *Typical program and erase times assume the following conditions: 25°C, 1.8 V V_{CC}, 10,000 cycles typical. Additionally, programming typicals assume checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 1.70 V, 100,000 cycles.*
3. *Effective write buffer specification is based upon a 32-word write buffer operation.*
4. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most words program faster than the maximum program times listed.*
5. *In the pre-programming step of the Embedded Erase algorithm, all words are programmed to 00h before erasure.*
6. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 11.4 on page 52 for further information on command definitions.*

21. BGA Ball Capacitance

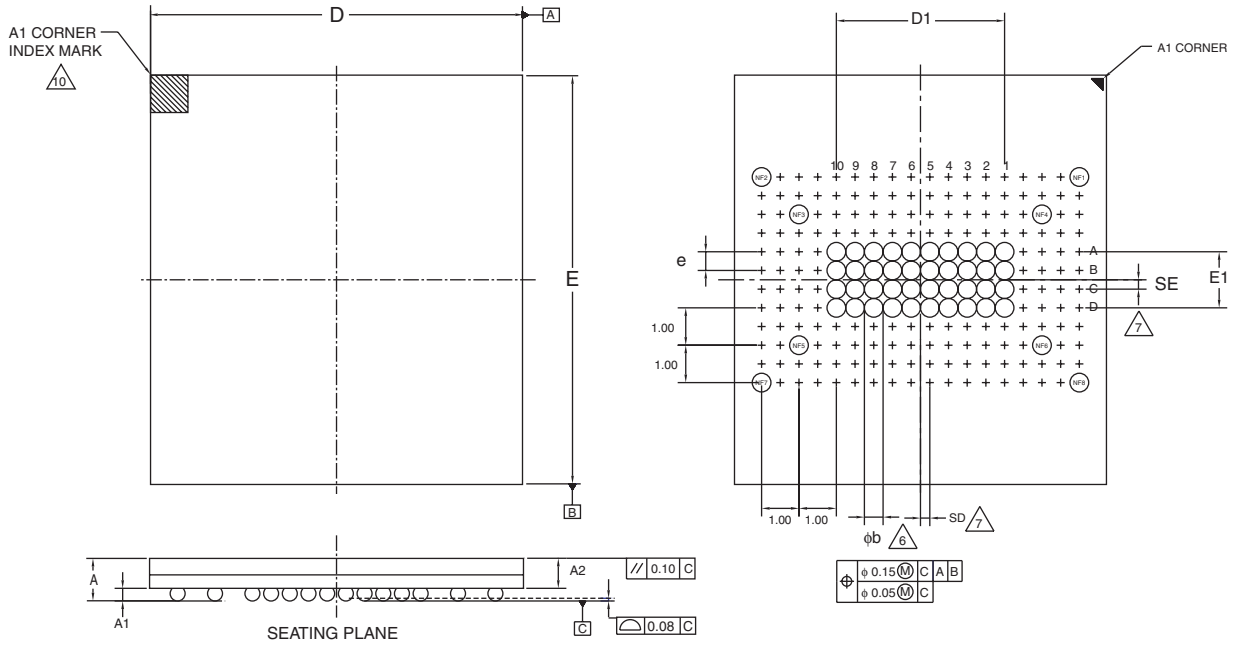
Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	4.2	5.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	5.4	6.5	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	3.9	4.7	pF

Notes

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

22. Physical Dimensions (S29NS256N)

22.1 VDC048—48-Ball Very Thin Fine-Pitch Ball Grid Array (FBGA) 11 x 10 mm Package



PACKAGE	VDC 048			
JEDEC	N/A			
	9.95 mm x 10.95 mm NOM PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	0.86	---	1.00	OVERALL THICKNESS
A1	0.20	---	---	BALL HEIGHT
A2	0.66	0.71	0.76	BODY THICKNESS
D	9.85	9.95	10.05	BODY SIZE
E	10.85	10.95	11.05	BODY SIZE
D1		4.50		BALL FOOTPRINT
E1		1.50		BALL FOOTPRINT
MD		10		ROW MATRIX SIZE D DIRECTION
ME		4		ROW MATRIX SIZE E DIRECTION
N		48		TOTAL BALL COUNT
φb	0.25	0.30	0.35	BALL DIAMETER
e		0.50		BALL PITCH
SD / SE		0.25		SOLDER BALL PLACEMENT

?

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010 (EXCEPT AS NOTED).
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.

   N IS THE TOTAL NUMBER OF SOLDER BALLS.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN ? THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. NOT USED.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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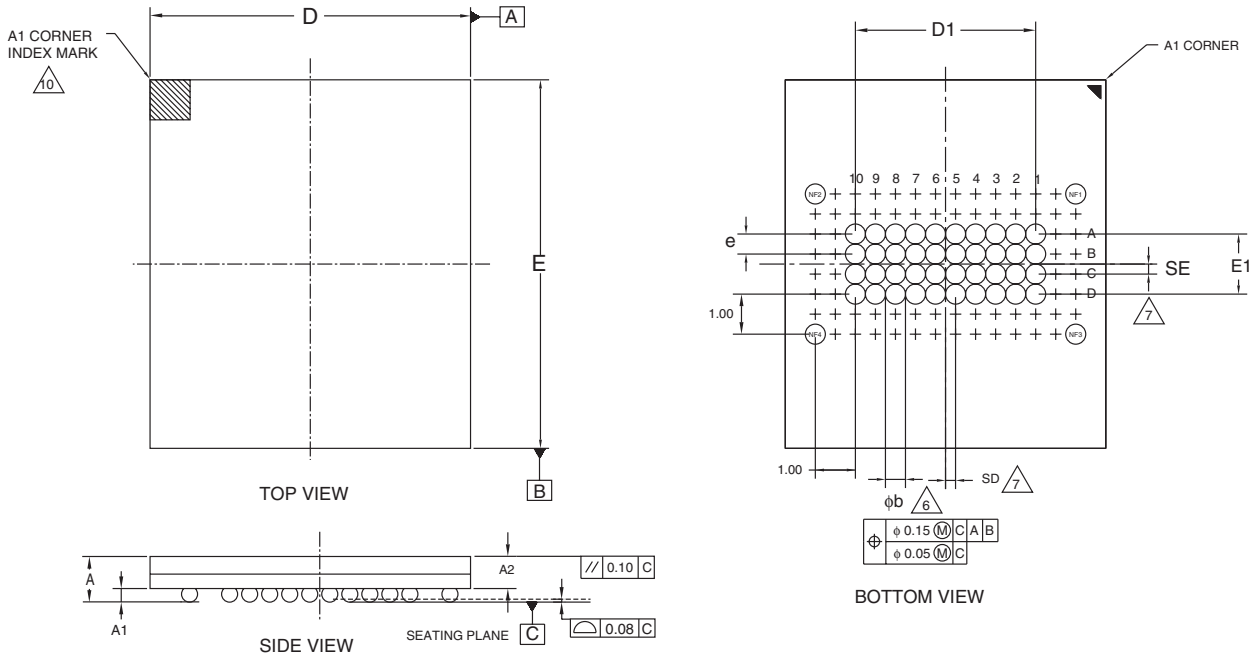
*For reference only. BSC is an ANSI standard for Basic Space Centering

23. Physical Dimensions (S29NS128N)

23.1 VDD044—44-Ball Very Thin Fine-Pitch Ball Grid Array (FBGA) 9.2 x 8 mm Package



PACKAGE	VDD 044			
JEDEC	N/A			
	8.00 mm x 9.20 mm NOM PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	0.86	---	1.00	OVERALL THICKNESS
A1	0.20	---	---	BALL HEIGHT
A2	0.66	0.71	0.76	BODY THICKNESS
D	7.90	8.00	8.10	BODY SIZE
E	9.10	9.20	9.30	BODY SIZE
D1		4.50		BALL FOOTPRINT
E1		1.50		BALL FOOTPRINT
MD		10		ROW MATRIX SIZE D DIRECTION
ME		4		ROW MATRIX SIZE E DIRECTION
N		44		TOTAL BALL COUNT
ϕb	0.25	0.30	0.35	BALL DIAMETER
e		0.50		BALL PITCH
SD / SE		0.25		SOLDER BALL PLACEMENT

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010 (EXCEPT AS NOTED).
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.

   N IS THE TOTAL NUMBER OF SOLDER BALLS.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. NOT USED.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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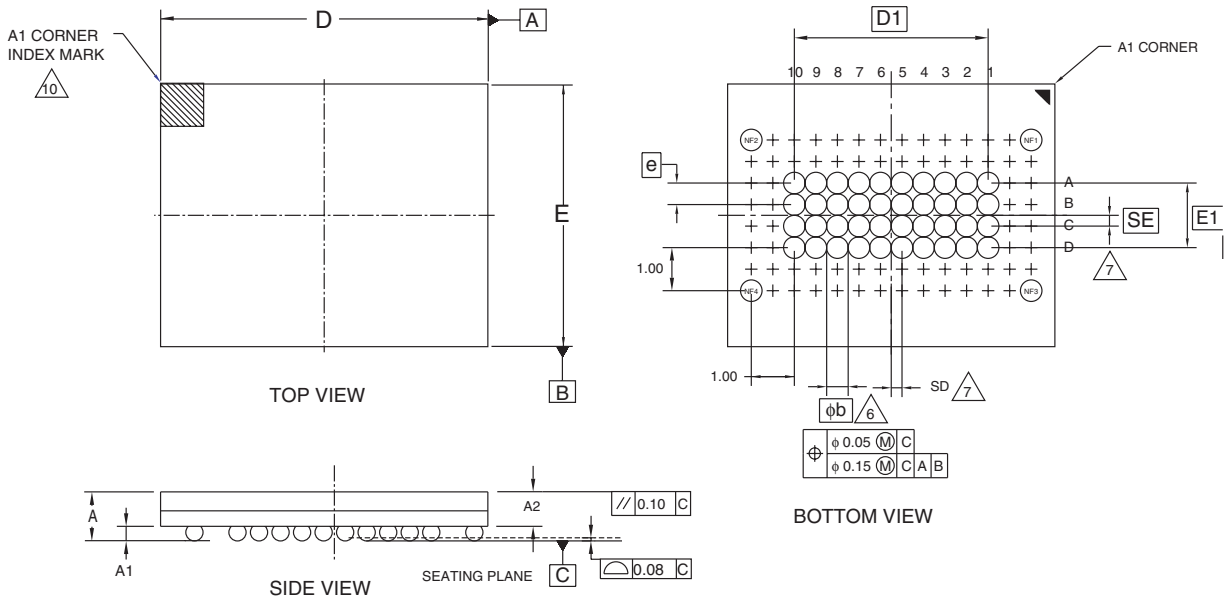
23.2 VDE044—44-Ball Very Thin Fine-Pitch Ball Grid Array (FBGA) 7.7 x 6.2mm Package



PACKAGE	VDE 044			
JEDEC	N/A			
	7.60 mm x 6.10 mm NOM PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	0.86	---	1.00	OVERALL THICKNESS
A1	0.20	---	---	BALL HEIGHT
A2	0.66	0.71	0.76	BODY THICKNESS
D	7.50	7.60	7.70	BODY SIZE
E	6.00	6.10	6.20	BODY SIZE
D1	4.50			BALL FOOTPRINT
E1	1.50			BALL FOOTPRINT
MD	10			ROW MATRIX SIZE D DIRECTION
ME	4			ROW MATRIX SIZE E DIRECTION
N	44			TOTAL BALL COUNT
ϕb	0.25	0.30	0.35	BALL DIAMETER
e	0.50 BSC.			BALL PITCH
SD / SE	0.25 BSC.			SOLDER BALL PLACEMENT
				DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010 (EXCEPT AS NOTED).
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.

   N IS THE TOTAL NUMBER OF SOLDER BALLS.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. NOT USED.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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24. Revision Summary

24.1 Revision A (April 16, 2004)

Initial Release.

24.2 Revision A1 (June 28, 2004)

General Description
Corrected the effective temperature range to -25°C to +85°C.

Connection Diagram
Corrected pin B5 on the S29NS256N to A23.

Corrected pin B1 on the S29NS256N to V_{CC}.

Corrected pin B1 on the S29NS128N to V_{CC}.

Corrected pin B1 on the S29NS064N to V_{CC}.

Created separate illustrations for S29NS128N and S29NS064N.

Ordering Information
Corrected the Package Type offerings.

Valid Combinations table
Included package type description for S29NS064N device.
Completely revised format and layout.

8-, 16-, and 32-Word Linear Burst without Wrap Around
Corrected information in this section.

Lock Register
Section and table were substantially revised.

Programmable Wait State
Corrected information in this section.

Handshaking Feature
Corrected information in this section.

Autoselect Command Sequence
Corrected information in this section.

Physical Dimensions
Corrected the drawing for the S29NS064N device.

Write Buffer Command Sequence
Corrected the address for the Write Buffer Load sequence.

24.3 Revision A2 (September 9, 2004)

Connection Diagrams
Updated pin labels.

Ordering Information
Completely updated the OPN table.

Valid Combinations table
Updated this table.

Continuous Burst
Added information to this section.

Lock Register
Updated the lock register table.

Configuration Register
Updated the settings for CR15.

Device ID table
Updated the indicator bits information.

Figure 7
Updated the waveform.

Figure 21
Updated the waveform.

24.4 Revision A3 (November 16, 2004)

Table "Primary Vendor-Specific Extended Query"
Updated the data values for addresses 45h, 53h, and 54h.

Global
Updated the synchronous and asynchronous access times.

Programmable Wait State
Updated this section.

Write Buffer Programming Command Sequence
Added a note to the table.

24.5 Revision A3a (April 5, 2005)

Global
Updated reference links.

Distinctive Characteristics
Added note to ACC is represented as V_{PP} in older documentation.

General Description
Added note regarding ACC and V_{PP}.

Block Diagram
Added same note regarding ACC and V_{PP}.

Added WP# term and arrow to State Control and Command Register block.

Block Diagram of Simultaneous Operation Circuit
Changed V_{PP} to V_{ssq}.

Added WP# term and arrow to State Control and Command Register block.

Added ACC term and arrow to State Control and Command Register block.

Added note to ACC is represented as V_{PP} in older documentation.

Input/Output Description
Added V_{PP} term adjacent to ACC term.

Tables 2, 3, 4, 5, 6, 7, 8, and 9
Change Wait State titles and columns in these tables.

Table 24
Changed Function column and Settings to represent Reserved CR Bits.

Table 27
Removed several bold lines between columns.

DC Characteristics
Reduced Typ and Max values for I_{CCB}.

Added note for clock frequency in continuous mode.

Erase & Programming Performance Table
Corrected Sector Erase Time Typ. Value for 64 Kword from 0.6 to 0.8 in Erase and Programming Performance table

Physical Dimensions (S29NS046N)
Replaced VDE044 with new package drawing.

Device History
Updated Device History table

24.6 Revision A4 (April 12, 2005)

Global Changes
Removed 64Mb density.

Removed 54MHz speed option.

Changed ACC to V_{PP}.

Read Access Times
Removed burst access for 54MHz.

Defined asynchronous random access and synchronous random access to 80 ns for all speed options.

DC Characteristics
CMOS Compatible Table.

Updated I_{CC3} and I_{CC6} values from 40µA to 70µA.

24.7 Revision A5 (August 15, 2005)

Added S29NS064N with new sector and bank architecture.

Added VDE044 package type for S29NS064N

Erase/Program Operations table
Updated description and values for t_{CS}.

Device History
Updated table with latest revision information.

24.8 Revision A6 (August 24, 2005)

AC Characteristics
Updated the notes for the V_{CC} Power-up table

Erase and Programming Performance Operations

Updated max value for 8 Kword Sector Erase Time

Updated typical and max values for Chip Programming Time

24.9 Revision A7 (September 16, 2005)

Ordering Information
Updated the Package Type options

Valid Combinations table
Updated entire table to show new options

24.10 Revision A8 (September 23, 2005)

Dynamic Protection Bit (DYB)
Added note: Dynamic protection bits revert back to their default values after programming the device “Lock Register.”

Lock Register Table
Added Note: When the device lock register is programmed (PPB mode lock bit is programmed, password mode lock bit programmed, or the Secured Silicon lock bit is programmed) all DYBs revert to the power-on default state.

24.11 Revision A9 (November 15, 2005)

Write Buffer Programming Operation
Updated the flowchart

24.12 Revision A10 (March 23, 2006)

Asynchronous Read AC Characteristics table
Updated the minimum specifications of t_{AAVDH} for both speed bins.

Global Change
Changed V_{PP} to ACC

24.13 Revision A11 (April 20, 2006)

Global Change
Changed layout and font

Absolute Maximum Ratings
Updated Figure 13.1 and 13.2

24.14 Revision A12 (June 13, 2006)

Global Change
Publication Identification number was incorrectly set to S29NS-N_01 for revision 11 instead of S29NS-N_00. It is corrected in this revision. The document file name was not affected by this error.

Added a note to Table 8.1 Device Bus Operations

Added a note to Table 11.1 Configuration Register

Added a note to section 11.9 Erase Suspend/Erase Resume Commands

Added a note to section 11.10 Program Suspend/Program Resume Commands

Added a note to section 11.13 Non-Volatile Sector Protection Command Set Definitions

Added a note to section 11.15 Volatile Sector Protection Command Set

Modified the “All PPB Erase” row of Table 11.4 Command Definitions (Sheet 2 of 3)

Changed $V_{I/O}$ to V_{CCQ} in section 15.1 CMOS Compatible

Changed $V_{I/O}$ to V_{CCQ} in Table 16.1 Test Specifications

Changed $V_{I/O}$ to V_{CCQ} in Figure 18.1 Input Waveforms and Measurement Levels

Added parameters t_{ERS} and t_{PRS} in section 19.5 Erase/Program Operations

Colophon

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