



STS5DNF20V

N-channel 20V - 0.030Ω - 5A SO-8
2.7V - drive STripFET™ II Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STS5DNF20V	20V	<0.040Ω (@ 4.5) <0.045Ω (@ 2.7)	5A

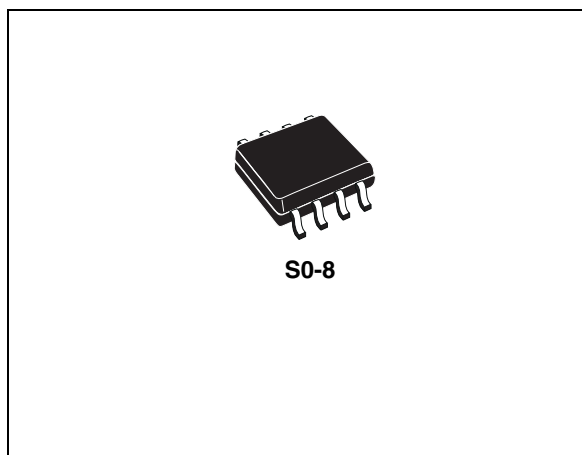
- Ultra low threshold gate drive (2.7 V)
- Standard outline for easy automated surface mount assembly

Description

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

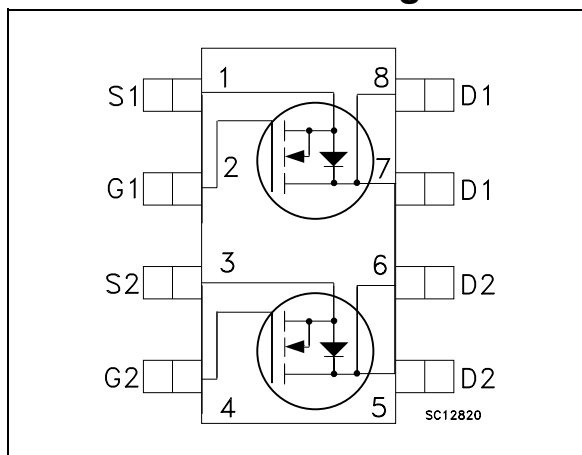
Applications

- Switching application



SO-8

Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STS5DNF20V	S5DNF20V	SO-8	Tape & reel

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($v_{GS} = 0$)	20	V
V_{GS}	Gate- source voltage	± 12	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	5	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	3	A
$I_{DM}^{(1)}$	Drain current (pulsed)	20	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$ dual operation	1.6	W
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$ single operation	2	W

1. Pulse width limited by safe operating area

Table 2. Thermal data

R_{thj-a}	Thermal resistance junction-ambient single operation	62.5	$^\circ\text{C/W}$
	Thermal resistance junction-ambient dual operation	78	$^\circ\text{C/W}$
T_J	Max. operating junction temperature	-55 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature	-55 to 150	$^\circ\text{C}$

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown voltage	I _D = 250 μA, V _{GS} = 0	20			V
I _{DSS}	Zero gate voltage Drain current (V _{GS} = 0)	V _{DS} = Max rating V _{DS} =Max rating, T _C =125°C			1 10	μA μA
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 12V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250μA	0.6			V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 4.5V, I _D = 2.5A V _{GS} = 2.7V, I _D = 2.5A		0.030 0.037	0.040 0.045	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g _{fs} ⁽¹⁾	Forward transconductance	V _{DS} = 15V, I _D =2.5 A		10		S
C _{iss}	Input capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		460		pF
C _{oss}	Output capacitance			200		pF
C _{rss}	Reverse transfer capacitance			50		pF
Q _g	Total gate charge	V _{DD} = 16V, I _D = 5A, V _{GS} = 4.5V (see Figure 13)		8.5	11.5	nC
Q _{gs}	Gate-source charge			1.8		nC
Q _{gd}	Gate-drain charge			2.4		nC

1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 .

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)} t _r	Turn-on delay time Rise time	V _{DD} =10 V, I _D =2.5A, R _G =4.7Ω, V _{GS} = 4.5V (see Figure 12)		7 33		ns ns
t _{d(off)} t _f	Turn-off Delay Time Fall Time	V _{DD} = 10 V, I _D = 2.5A R _G =4.7Ω, V _{GS} = 4.5V (see Figure 12)		27 10		ns ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				20	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 5A, V_{GS} = 0$			1.2	V
t_{rr}	Reverse recovery time	$I_{SD} = 5A, V_{DD} = 10V$ $di/dt = 100A/\mu s,$ $T_j = 150^\circ C$ (see Figure 14)		26		ns
Q_{rr}	Reverse recovery charge			13		nC
I_{RRM}	Reverse recovery current			1		A

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

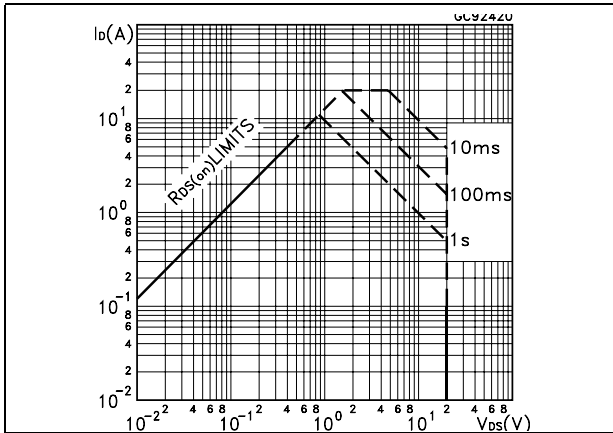


Figure 2. Thermal impedance

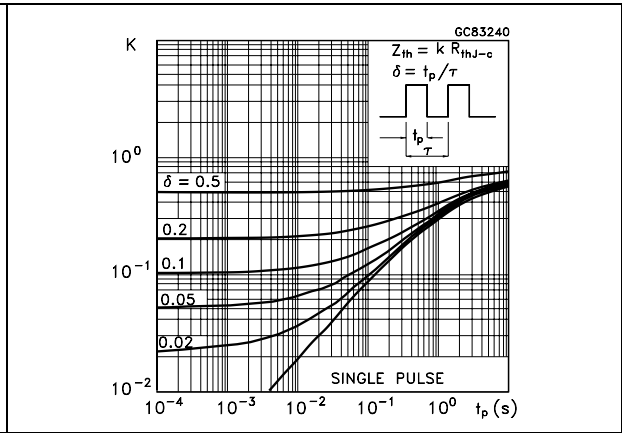


Figure 3. Output characteristics

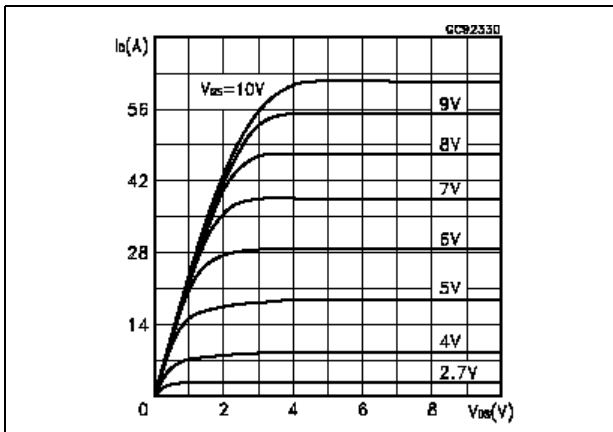


Figure 4. Transfer characteristics

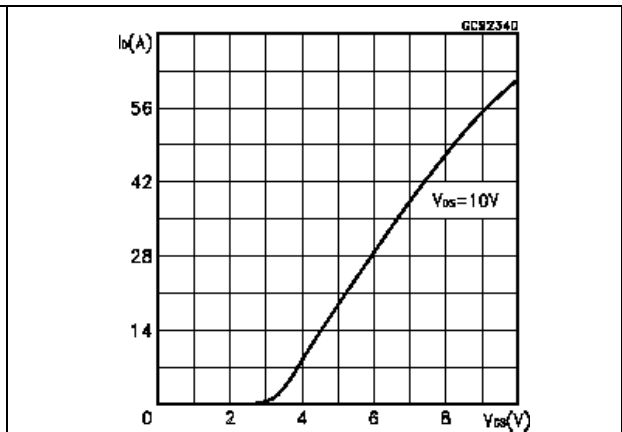


Figure 5. Transconductance

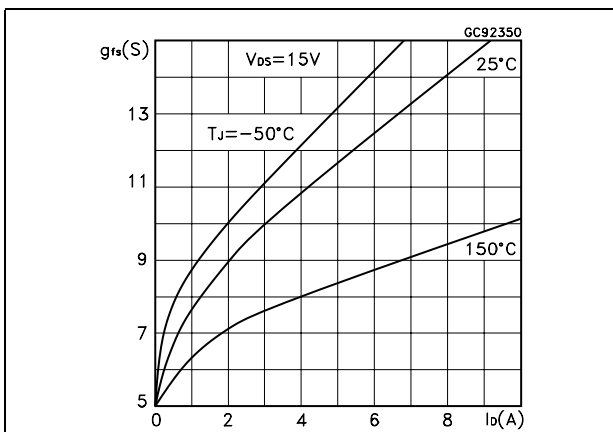


Figure 6. Static drain-source on resistance

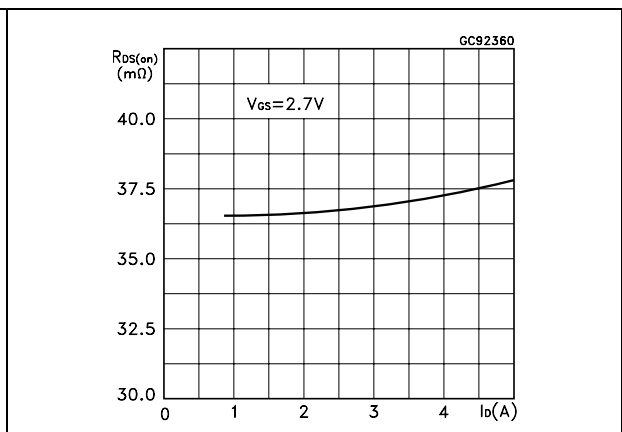


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

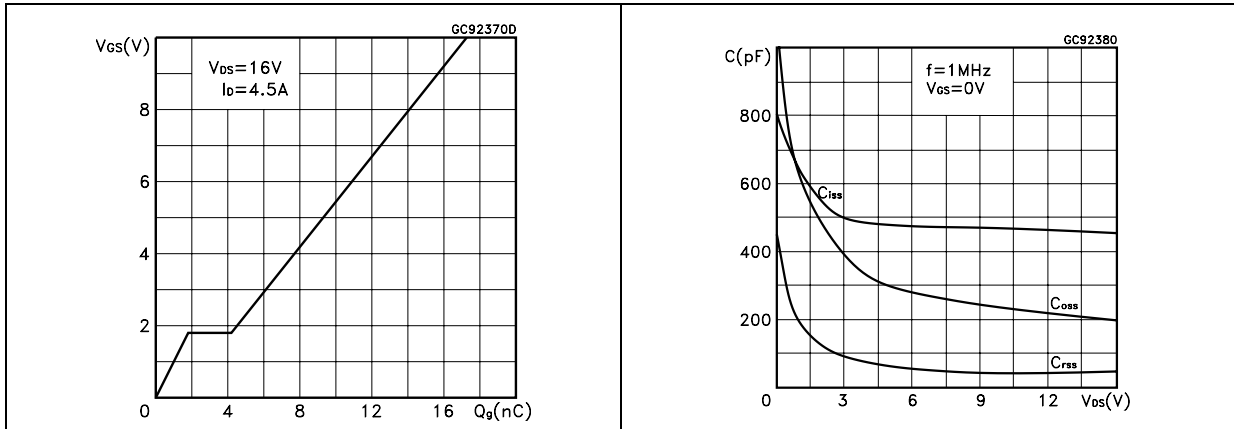


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

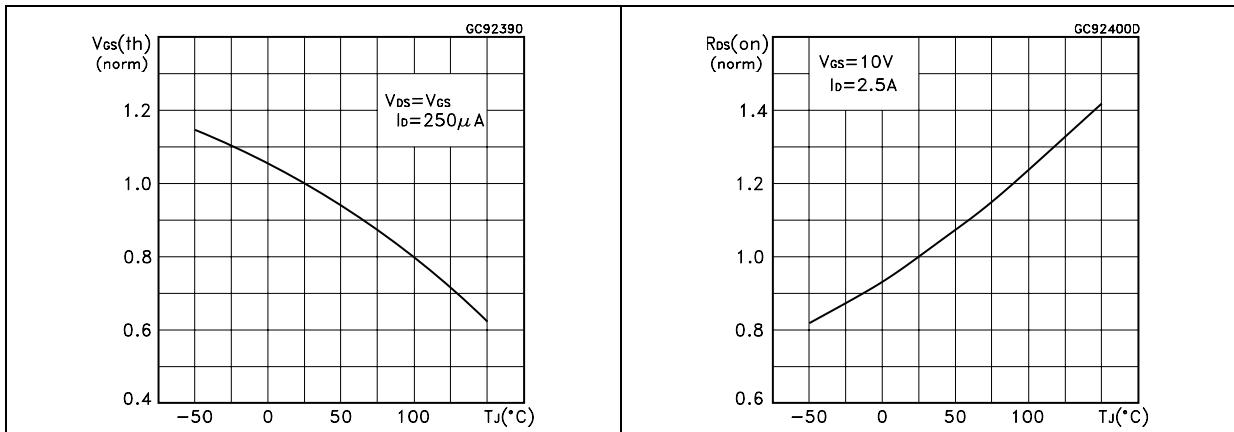
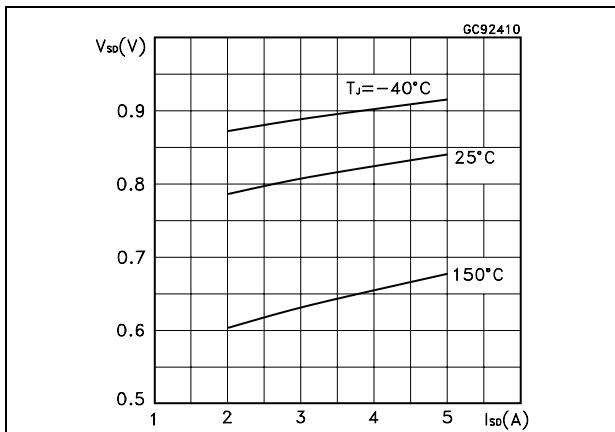


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load



Figure 13. Gate charge test circuit



Figure 14. Test circuit for inductive load switching and diode recovery times

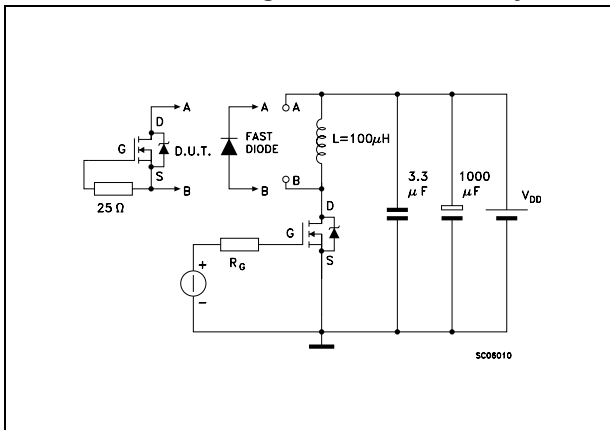


Figure 15. Unclamped Inductive load test circuit

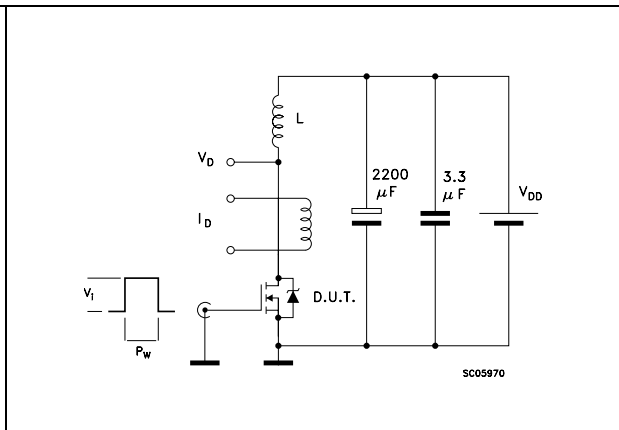


Figure 16. Unclamped inductive waveform

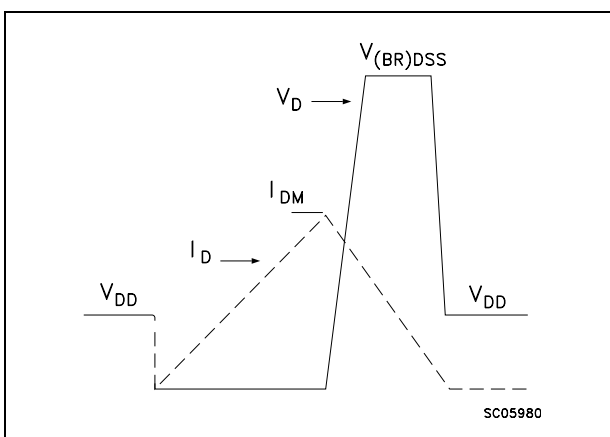
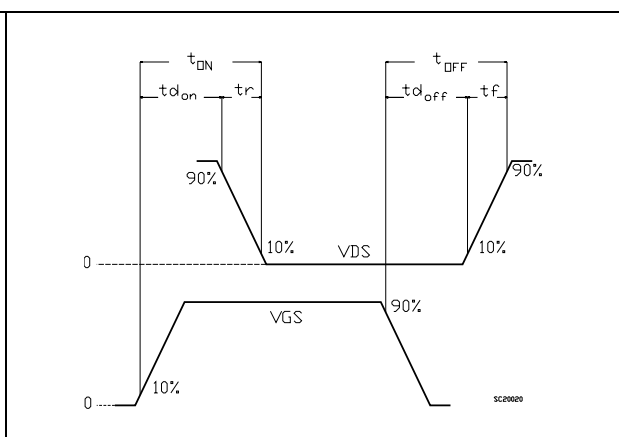


Figure 17. Switching time waveform

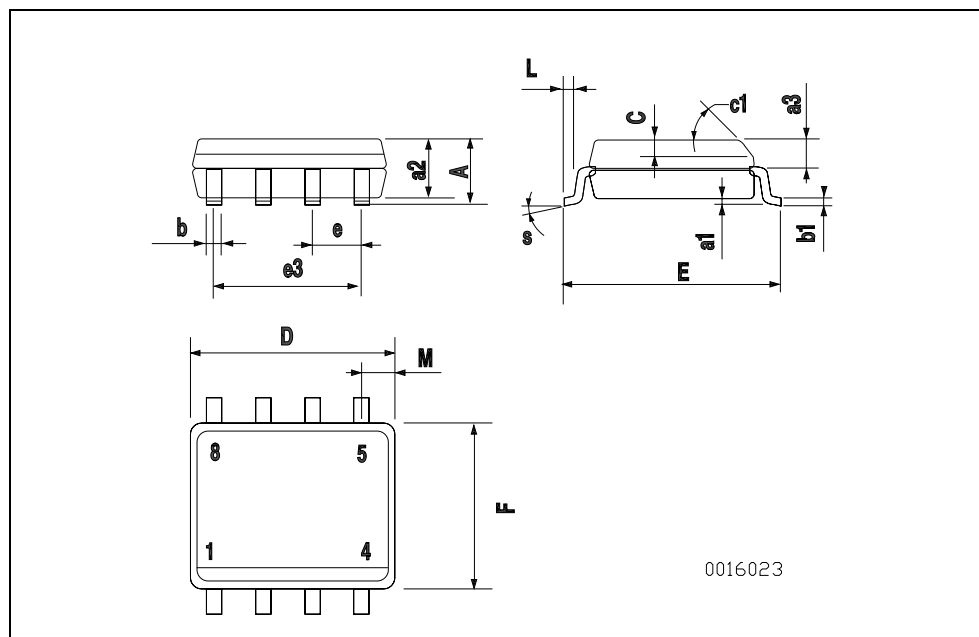


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at : www.st.com

SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



5 Revision history

Table 7. Revision history

Date	Revision	Changes
21-Jun-2004	4	Complete document
13-Nov-2006	5	The document has been reformatted

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