S6B0721

132 SEG / 65 COM DRIVER & CONTROLLER FOR STN LCD

June.2000.

Ver. 0.1

Prepared by: Ko Jae Su Jae-Su, Ko

Ko1942@samsung.co.kr

S6B0721 Specification Revision History		
Version	**Content**	**Date**
0.0	Initial version	Nov.1999
0.1	Read timing is changed (Figure 5)	Jun.2000

CONTENTS

INTRODUCTION

The S6B0721 is a driver & controller LSI for graphic dot-matrix liquid crystal display systems. It contains 65 commons and 132 segments driver circuits. This chip is connected directly to a microprocessor, accepts serial or 8-bit parallel display data and stores in an on-chip Display Data RAM of 65 x 132 bits. It provides a high-flexible display section due to 1-to-1 correspondence between on-chip display data RAM bits and LCD panel pixels. And it performs display data RAM read/write operation with no externally operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

FEATURES

Driver Output Circuits

– 65 common outputs / 132 segment outputs

On-chip Display Data RAM

– Capacity: 65 x 132 = 8,580 bits

Applicable Duty Ratios

Duty ratio	Applicable LCD bias	Maximum display area
1/65	1/7 or 1/9	65 × 132
1/49	1/6 or 1/8	49 × 132
1/33	1/5 or 1/6	33 × 132

Microprocessor Interface

– 8-bit parallel bi-directional interface with 6800-series or 8080-series
– Serial interface (only write operation) available

Function Set

– Various instructions sets
– H/W, S/W reset capable

Built-in Analog Circuit

– On-chip oscillator circuit
– Voltage converter (x2, x3, x4, x5)
– Voltage regulator (temperature coefficient: -0.05%/°C, -0.2%/°C)
– Voltage follower
– Electronic contrast control function (64 steps)

Operating Voltage Range

– Supply voltage (V_{DD}): 2.4 to 3.6 V
– LCD driving voltage (V_{LCD} = V0 - V_{SS}): 4.0 to 15.0 V

Low Power Consumption

– 70 μA Typ. (V_{DD} = 3V, x4 boosting, V0 = 11V, internal power supply ON)
– 10 μA Max. (during power save [standby] mode)

Package Type

– Gold bump chip or TCP

Series Specifications

Product code	Internal TEMPS	Temp. coefficient	Package	Chip thickness
S6B0721X01-B0CZ	0 (VSS connected)	-0.05%/°C	COG	670 μm
S6B0721X01-B0CY				470 μm
S6B0721X11-B0CZ	1 (VDD connected)	-0.2%/°C		670 μm
S6B0721X11-B0CY				470 μm
S6B0721X01-xxX0	0 (VSS connected)	-0.05%/°C	TCP	670 μm
S6B0721X01-xxXN				470 μm
S6B0721X11-xxX0	1 (VDD connected)	-0.2%/°C		670 μm
S6B0721X11-xxXN				470 μm

* XX: TCP ordering number

BLOCK DIAGRAM

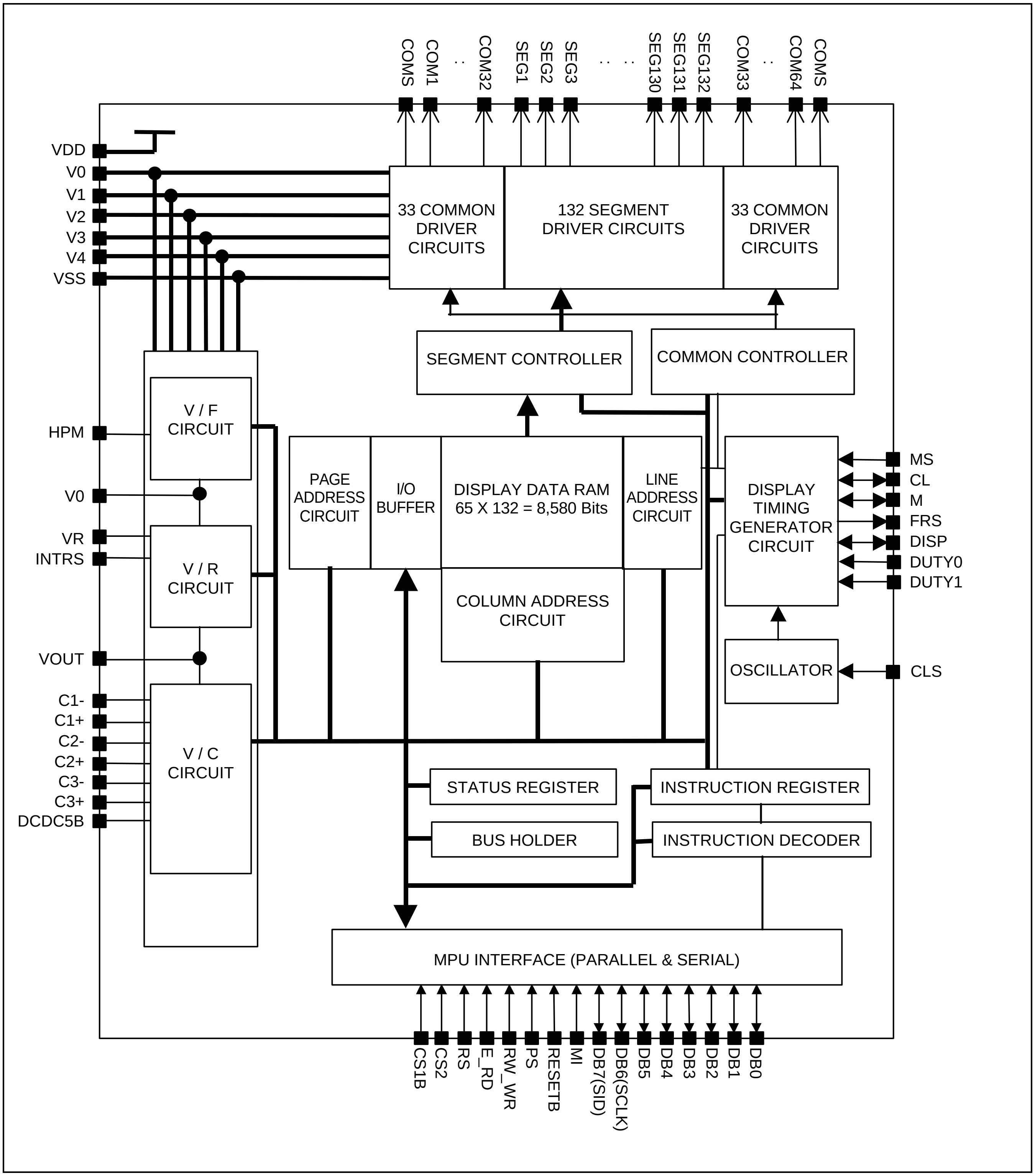


Figure 1. Block Diagram

PAD CONFIGURATION

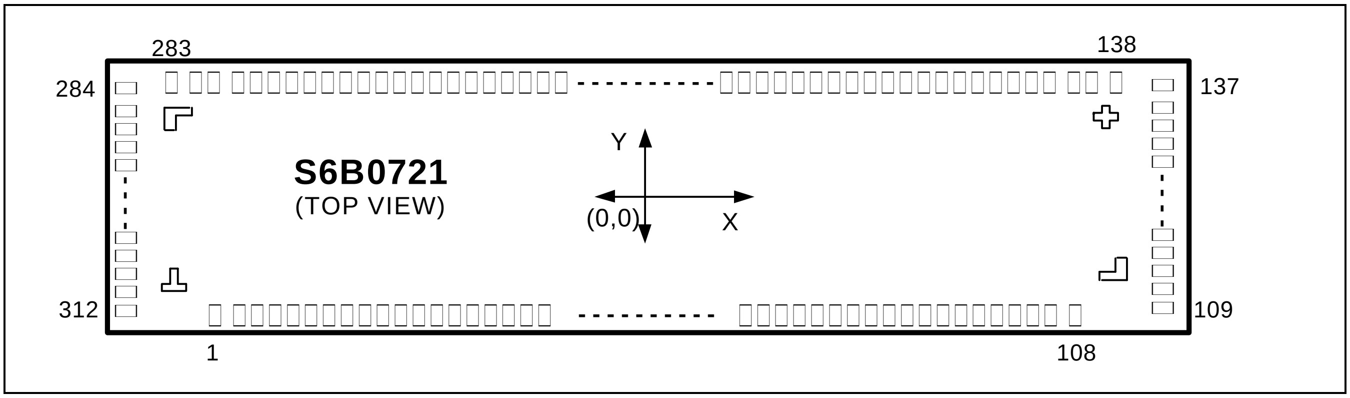
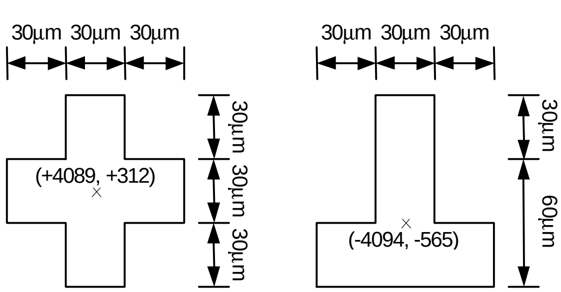


Figure 2. S6B0721 Chip Configuration

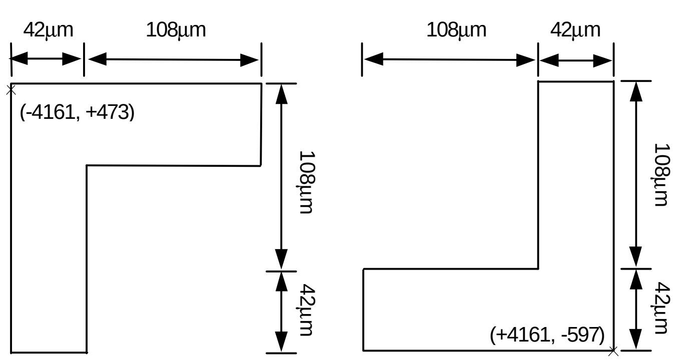
Table 1. S6B0721 Pad Dimensions

Items	Pad No.	Size		Unit
		X	Y	
Chip size	-	9640	2020	µm
Pad pitch	1,108,109,137,138,283, 284,312	90		
	2 to 107	70		
	110 to 136, 139 to 282 285 to 311	60		
Bumped pad size (Top size)	1,108	70	100	
	2 to 107	50	100	
	109,137,284,312	110	60	
	110 to 136,285 to 311	110	45	
	139 to 282	45	110	
	138,283	60	110	
Bumped pad height	1 to 312	14(Typ.)		

COG Align Key Coordinate



ILB Align Key Coordinate



SAMSUNG ELECTRONICS

PAD CENTER COORDINATES

Table 2. Pad Center Coordinates

[Unit: µm]

Pad No	Pad Name	X	Y	Pad No	Pad Name	X	Y	Pad No	Pad Name	X	Y
1	DUMMY	-3765	-895	55	VDD	35	-895	109	DUMMY	4673	-850
2	FRS	-3675	-895	56	VOUT	105	-895	110	COMS	4673	-780
3	M	-3605	-895	57	VOUT	175	-895	111	COM1	4673	-720
4	CL	-3535	-895	58	VOUT	245	-895	112	COM2	4673	-660
5	DISP	-3465	-895	59	VOUT	315	-895	113	COM3	4673	-600
6	VSS	-3395	-895	60	C3+	385	-895	114	COM4	4673	-540
7	CS1B	-3325	-895	61	C3+	455	-895	115	COM5	4673	-480
8	CS2	-3255	-895	62	C3+	525	-895	116	COM6	4673	-420
9	VDD	-3185	-895	63	C3+	595	-895	117	COM7	4673	-360
10	RESETB	-3115	-895	64	C3-	665	-895	118	COM8	4673	-300
11	RS	-3045	-895	65	C3-	735	-895	119	COM9	4673	-240
12	VSS	-2975	-895	66	C3-	805	-895	120	COM10	4673	-180
13	RW_WR	-2905	-895	67	C3-	875	-895	121	COM11	4673	-120
14	E_RD	-2835	-895	68	C1+	945	-895	122	COM12	4673	-60
15	VDD	-2765	-895	69	C1+	1015	-895	123	COM13	4673	0
16	DB0	-2695	-895	70	C1+	1085	-895	124	COM14	4673	60
17	DB1	-2625	-895	71	C1+	1155	-895	125	COM15	4673	120
18	DB2	-2555	-895	72	C1-	1225	-895	126	COM16	4673	180
19	DB3	-2485	-895	73	C1-	1295	-895	127	COM17	4673	240
20	DB4	-2415	-895	74	C1-	1365	-895	128	COM18	4673	300
21	DB5	-2345	-895	75	C1-	1435	-895	129	COM19	4673	360
22	DB6	-2275	-895	76	C2+	1505	-895	130	COM20	4673	420
23	DB7	-2205	-895	77	C2+	1575	-895	131	COM21	4673	480
24	VSS	-2135	-895	78	C2+	1645	-895	132	COM22	4673	540
25	DUMMY	-2065	-895	79	C2+	1715	-895	133	COM23	4673	600
26	DUMMY	-1995	-895	80	C2-	1785	-895	134	COM24	4673	660
27	VDD	-1925	-895	81	C2-	1855	-895	135	COM25	4673	720
28	DUTY0	-1855	-895	82	C2-	1925	-895	136	COM26	4673	780
29	DUTY1	-1785	-895	83	C2-	1995	-895	137	DUMMY	4673	850
30	VSS	-1715	-895	84	VSS	2065	-895	138	DUMMY	4380	863
31	MS	-1645	-895	85	VSS	2135	-895	139	COM27	4290	863
32	CLS	-1575	-895	86	VR	2205	-895	140	COM28	4230	863
33	VDD	-1505	-895	87	VR	2275	-895	141	COM29	4170	863
34	MI	-1435	-895	88	V0	2345	-895	142	COM30	4110	863
35	PS	-1365	-895	89	V0	2415	-895	143	COM31	4050	863
36	VSS	-1295	-895	90	V1	2485	-895	144	COM32	3990	863
37	VSS	-1225	-895	91	V1	2555	-895	145	SEG1	3930	863
38	VSS	-1155	-895	92	V2	2625	-895	146	SEG2	3870	863
39	VSS	-1085	-895	93	V2	2695	-895	147	SEG3	3810	863
40	VSS	-1015	-895	94	V3	2765	-895	148	SEG4	3750	863
41	VSS	-945	-895	95	V3	2835	-895	149	SEG5	3690	863
42	VSS	-875	-895	96	V4	2905	-895	150	SEG6	3630	863
43	VSS	-805	-895	97	V4	2975	-895	151	SEG7	3570	863
44	VSS	-735	-895	98	VSS	3045	-895	152	SEG8	3510	863
45	VSS	-665	-895	99	VSS	3115	-895	153	SEG9	3450	863
46	VDD	-595	-895	100	DUMMY	3185	-895	154	SEG10	3390	863
47	VDD	-525	-895	101	DCDC5B	3255	-895	155	SEG11	3330	863
48	VDD	-455	-895	102	VDD	3325	-895	156	SEG12	3270	863
49	VDD	-385	-895	103	HPM	3395	-895	157	SEG13	3210	863
50	VDD	-315	-895	104	INTRS	3465	-895	158	SEG14	3150	863
51	VDD	-245	-895	105	VSS	3535	-895	159	SEG15	3090	863
52	VDD	-175	-895	106	DUMMY	3605	-895	160	SEG16	3030	863
53	VDD	-105	-895	107	VDD	3675	-895	161	SEG17	2970	863
54	VDD	-35	-895	108	TESTCK	3765	-895	162	SEG18	2910	863

Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

Pad No	Pad Name	X	Y	Pad No	Pad Name	X	Y	Pad No	Pad Name	X	Y
163	SEG19	2850	863	217	SEG73	-390	863	271	SEG127	-3630	863
164	SEG20	2790	863	218	SEG74	-450	863	272	SEG128	-3690	863
165	SEG21	2730	863	219	SEG75	-510	863	273	SEG129	-3750	863
166	SEG22	2670	863	220	SEG76	-570	863	274	SEG130	-3810	863
167	SEG23	2610	863	221	SEG77	-630	863	275	SEG131	-3870	863
168	SEG24	2550	863	222	SEG78	-690	863	276	SEG132	-3930	863
169	SEG25	2490	863	223	SEG79	-750	863	277	COMS	-3990	863
170	SEG26	2430	863	224	SEG80	-810	863	278	COM64	-4050	863
171	SEG27	2370	863	225	SEG81	-870	863	279	COM63	-4110	863
172	SEG28	2310	863	226	SEG82	-930	863	280	COM62	-4170	863
173	SEG29	2250	863	227	SEG83	-990	863	281	COM61	-4230	863
174	SEG30	2190	863	228	SEG84	-1050	863	282	COM60	-4290	863
175	SEG31	2130	863	229	SEG85	-1110	863	283	DUMMY	-4380	863
176	SEG32	2070	863	230	SEG86	-1170	863	284	DUMMY	-4673	850
177	SEG33	2010	863	231	SEG87	-1230	863	285	COM59	-4673	780
178	SEG34	1950	863	232	SEG88	-1290	863	286	COM58	-4673	720
179	SEG35	1890	863	233	SEG89	-1350	863	287	COM57	-4673	660
180	SEG36	1830	863	234	SEG90	-1410	863	288	COM56	-4673	600
181	SEG37	1770	863	235	SEG91	-1470	863	289	COM55	-4673	540
182	SEG38	1710	863	236	SEG92	-1530	863	290	COM54	-4673	480
183	SEG39	1650	863	237	SEG93	-1590	863	291	COM53	-4673	420
184	SEG40	1590	863	238	SEG94	-1650	863	292	COM52	-4673	360
185	SEG41	1530	863	239	SEG95	-1710	863	293	COM51	-4673	300
186	SEG42	1470	863	240	SEG96	-1770	863	294	COM50	-4673	240
187	SEG43	1410	863	241	SEG97	-1830	863	295	COM49	-4673	180
188	SEG44	1350	863	242	SEG98	-1890	863	296	COM48	-4673	120
189	SEG45	1290	863	243	SEG99	-1950	863	297	COM47	-4673	60
190	SEG46	1230	863	244	SEG100	-2010	863	298	COM46	-4673	0
191	SEG47	1170	863	245	SEG101	-2070	863	299	COM45	-4673	-60
192	SEG48	1110	863	246	SEG102	-2130	863	300	COM44	-4673	-120
193	SEG49	1050	863	247	SEG103	-2190	863	301	COM43	-4673	-180
194	SEG50	990	863	248	SEG104	-2250	863	302	COM42	-4673	-240
195	SEG51	930	863	249	SEG105	-2310	863	303	COM41	-4673	-300
196	SEG52	870	863	250	SEG106	-2370	863	304	COM40	-4673	-360
197	SEG53	810	863	251	SEG107	-2430	863	305	COM39	-4673	-420
198	SEG54	750	863	252	SEG108	-2490	863	306	COM38	-4673	-480
199	SEG55	690	863	253	SEG109	-2550	863	307	COM37	-4673	-540
200	SEG56	630	863	254	SEG110	-2610	863	308	COM36	-4673	-600
201	SEG57	570	863	255	SEG111	-2670	863	309	COM35	-4673	-660
202	SEG58	510	863	256	SEG112	-2730	863	310	COM34	-4673	-720
203	SEG59	450	863	257	SEG113	-2790	863	311	COM33	-4673	-780
204	SEG60	390	863	258	SEG114	-2850	863	312	DUMMY	-4673	-850
205	SEG61	330	863	259	SEG115	-2910	863				
206	SEG62	270	863	260	SEG116	-2970	863				
207	SEG63	210	863	261	SEG117	-3030	863				
208	SEG64	150	863	262	SEG118	-3090	863				
209	SEG65	90	863	263	SEG119	-3150	863				
210	SEG66	30	863	264	SEG120	-3210	863				
211	SEG67	-30	863	265	SEG121	-3270	863				
212	SEG68	-90	863	266	SEG122	-3330	863				
213	SEG69	-150	863	267	SEG123	-3390	863				
214	SEG70	-210	863	268	SEG124	-3450	863				
215	SEG71	-270	863	269	SEG125	-3510	863				
216	SEG72	-330	863	270	SEG126	-3570	863				

PIN DESCRIPTION

POWER SUPPLY

Table 3. Power Supply Pin Description

Name	I/O	Description
VDD	Supply	Power supply
VSS	Supply	Ground
V0 V1 V2 V3 V4	I/O	LCD driver supply voltages The voltage determined by LCD pixel is impedance-converted by an operational amplifier for application. Voltages should have the following relationship; V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS When the internal power circuit is active, these voltages are generated as following table according to the state of LCD Bias.

LCD bias	V1	V2	V3	V4
1/9 bias	(8/9) x V0	(7/9) x V0	(2/9) x V0	(1/9) x V0
1/8 bias	(7/8) x V0	(6/8) x V0	(2/8) x V0	(1/8) x V0
1/7 bias	(6/7) x V0	(5/7) x V0	(2/7) x V0	(1/7) x V0
1/6 bias	(5/6) x V0	(4/6) x V0	(2/6) x V0	(1/6) x V0
1/5 bias	(4/5) x V0	(3/5) x V0	(2/5) x V0	(1/5) x V0

LCD DRIVER SUPPLY

Table 4. LCD Driver Supply Pin Description

Name	I/O	Description
C1-	O	Capacitor 1 negative connection pin for voltage converter
C1+	O	Capacitor 1 positive connection pin for voltage converter
C2-	O	Capacitor 2 negative connection pin for voltage converter
C2+	O	Capacitor 2 positive connection pin for voltage converter
C3-	O	Capacitor 3 negative connection pin for voltage converter
C3+	O	Capacitor 3 positive connection pin for voltage converter
VOUT	I/O	Voltage converter input / output pin
DCDC5B	I	5 times boosting circuit enable input pin When this pin is low in 4 times boosting circuit, the 5-times boosting voltage appears at VOUT.
VR	I	V0 voltage adjustment pin It is valid only when on-chip resistors are not used (INTRS = “L”).

SYSTEM CONTROL

Table 5. System Control Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>MS</td><td>I</td><td>Master / Slave operation select pin
– MS = "H": master operation
– MS = "L": slave operation
The following table depends on the MS status.
<table>
<tr><th>MS</th><th>CLS</th><th>OSC circuit</th><th>Power supply circuit</th><th>CL</th><th>M</th><th>FRS</th><th>DISP</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>Enabled</td><td>Enabled</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>Disabled</td><td>Enabled</td><td>Input</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>-</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td><td>Output</td><td>Input</td></tr>
</table>
</td></tr>
<tr><td>CLS</td><td>I</td><td>Built-in oscillator circuit enable / disable select pin
– CLS = “H”: enable
– CLS = “L”: disable (external display clock input to CL pin)</td></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock input / output pin
When the S6B0721 is used in master/slave mode (multi-chip), the CL pins must be connected each other.</td></tr>
<tr><td>M</td><td>I/O</td><td>LCD AC signal input / output pin
When the S6B0721 is used in master/slave mode (multi-chip), the M pins must be connected each other.
– MS = “H”: output
– MS = “L”: input</td></tr>
<tr><td>FRS</td><td>O</td><td>Static driver segment output pin
This pin is used together with the M pin.</td></tr>
<tr><td>DISP</td><td>I/O</td><td>LCD display blanking control input / output
When S6B0721 is used in master/slave mode (multi-chip), the DISP pins must be connected each other.
– MS = “H”: output
– MS = “L”: input</td></tr>
<tr><td>INTRS</td><td>I</td><td>Internal resistors select pin
This pin selects the resistors for adjusting V0 voltage level.
– INTRS = "H": use the internal resistors.
– INTRS = "L": use the external resistors.
V0 voltage is controlled with VR pin and external resistive divider.</td></tr>
<tr><td>HPM</td><td>I</td><td>Power control pin of the power supply circuit for LCD driver
– HPM = "H": high power mode
– HPM = "L": normal mode
This pin is valid in master operation.</td></tr>
</table>

Table 5. System Control Pin Description (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th colspan="3">Description</th></tr>
<tr><td rowspan="6">DUTY0
DUTY1</td><td rowspan="6">I</td><td colspan="3">The LCD driver duty ratio depends on the following table</td></tr>
<tr><td>DUTY1</td><td>DUTY0</td><td>Duty ratio</td></tr>
<tr><td>L</td><td>L</td><td>1/33</td></tr>
<tr><td>L</td><td>H</td><td>1/49</td></tr>
<tr><td>H</td><td>L/H</td><td>1/65</td></tr>
<tr><td colspan="3"></td></tr>
</table>

MICROPROCESSOR INTERFACE

Table 6. Microprocessor Interface Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>RESETB</td><td>I</td><td>Reset input pin
When RESETB is “L”, initialization is executed.</td></tr>
<tr><td>PS</td><td>I</td><td>Parallel / Serial data input select input
<table>
<tr><td>PS</td><td>Interface mode</td><td>Chip select</td><td>Data / instruction</td><td>Data</td><td>Read / Write</td><td>Serial clock</td></tr>
<tr><td>H</td><td>Parallel</td><td>CS1B, CS2</td><td>RS</td><td>DB0 to DB7</td><td>E_RD
RW_WR</td><td>-</td></tr>
<tr><td>L</td><td>Serial</td><td>CS1B, CS2</td><td>RS</td><td>SID(DB7)</td><td>Write only</td><td>SCLK(DB6)</td></tr>
</table>
*NOTE: In serial mode, it is impossible to read data from the on-chip RAM. And DB0 to DB5 are high impedance and E_RD and RW_WR must be fixed to either “H” or “L”.</td></tr>
<tr><td>MI</td><td>I</td><td>Microprocessor interface selects input pin
– MI = "H": 6800-series MPU interface
– MI = "L": 8080-series MPU interface</td></tr>
<tr><td>CS1B
CS2</td><td>I</td><td>Chip select input pins
Data / instruction I/O is enabled only when CS1B is “L” and CS2 is “H”.
When chip select is non-active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td>RS</td><td>I</td><td>Register select input pin
– RS = "H": DB0 to DB7 are display data
– RS = "L": DB0 to DB7 are control data</td></tr>
<tr><td>RW_WR</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><td>MI</td><td>MPU type</td><td>RW_WR</td><td>Description</td></tr>
<tr><td>H</td><td>6800-series</td><td>RW</td><td>Read / Write control input pin
– RW = “H”: read
– RW = “L”: write</td></tr>
<tr><td>L</td><td>8080-series</td><td>/WR</td><td>Write enable clock input pin
The data ON DB0 to DB7 are latched at the rising edge of the /WR signal.</td></tr>
</table></td></tr>
</table>

Table 6. Microprocessor Interface Pin Description (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th colspan="4">Description</th></tr>
<tr><td rowspan="5">E_RD</td><td rowspan="5">I</td><td colspan="4">Read / Write execution control pin</td></tr>
<tr><td>MI</td><td>MPU type</td><td>E_RD</td><td>Description</td></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read / Write control input pin
– RW = “H”: When E is “H”, DB0 to DB7 are in an output status.
– RW = “L”: The data on DB0 to DB7 are latched at the falling edge of the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>/RD</td><td>Read enable clock input pin
When /RD is “L”, DB0 to DB7 are in an output status.</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td>DB0
to
DB7</td><td>I/O</td><td colspan="4">8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus. When the serial interface selected (PS = "L");
– DB0 to DB5: high impedance
– DB6: serial input clock (SCLK)
– DB7: serial input data (SID)
When chip select is not active, DB0 to DB7 may be high impedance.</td></tr>
</table>

LCD DRIVER OUTPUTS

Table 7. LCD Driver Outputs Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>SEG1
to
SEG132</td><td>O</td><td>LCD segment driver outputs
The display data and the M signal control the output voltage of segment driver.
<table>
<tr><td rowspan="2">Display data</td><td rowspan="2">M</td><td colspan="2">Segment driver output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>Vss</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>Vss</td></tr>
<tr><td colspan="2">Power save mode</td><td>Vss</td><td>Vss</td></tr>
</table></td></tr>
<tr><td>COM1
to
COM64</td><td>O</td><td>LCD common driver outputs
The internal scanning data and M signal control the output voltage of common driver.
<table>
<tr><td>Scan data</td><td>M</td><td>Common driver output voltage</td></tr>
<tr><td>H</td><td>H</td><td>Vss</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>L</td><td>V4</td></tr>
<tr><td colspan="2">Power save mode</td><td>Vss</td></tr>
</table></td></tr>
<tr><td>COMS</td><td>O</td><td>Common output for the icons
The output signals of two pins are same. When not used, these pins should be left open. In multi-chip (master / slave) mode, all COMS pins on both master and slave units are the same signal.</td></tr>
</table>

NOTE: **DUMMY - These pins should be opened (floated).**

FUNCTIONAL DESCRIPTION

MICROPROCESSOR INTERFACE

Chip Select Input

There are CS1B and CS2 pins for Chip Selection. The S6B0721 can interface with an MPU only when CS1B is “L” and CS2 is “H”. When these pins are set to any other combination, RS, E_RD, and RW_WR inputs are disabled and DB0 to DB7 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

Parallel / Serial Interface

S6B0721 has three types of interface with an MPU, which are one serial and two parallel interfaces. This parallel or serial interface is determined by PS pin as shown in table 8.

Table 8. Parallel / Serial Interface Mode

PS	Type	CS1B	CS2	MI	Interface mode
H	Parallel	CS1B	CS2	H	6800-series MPU mode
				L	8080-series MPU mode
L	Serial	CS1B	CS2	*×	Serial-mode

*× : Don't care

Parallel Interface (PS = "H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by MI as shown in table 9. The type of data transfer is determined by signals at RS, E_RD and RW_WR as shown in table10.

Table 9. Microprocessor Selection for Parallel Interface

MI	CS1B	CS2	RS	E_RD	RW_WR	DB0 to DB7	MPU bus
H	CS1B	CS2	RS	E	RW	DB0 to DB7	6800-series
L	CS1B	CS2	RS	/RD	/WR	DB0 to DB7	8080-series

Table 10. Parallel Data Transfer

Common	6800-series		8080-series		Description
RS	E_RD (E)	RW_WR (RW)	E_RD (/RD)	RW_WR (/WR)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

Serial Interface (PS = "L")

When the S6B0721 is active, serial data (DB7) and serial clock (DB6) inputs are enabled. And not active, the internal 8-bit shift register and the 3-bit counter are reset. Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock. Serial data input is display data when RS is high and control data when RS is low. Since the clock signal (DB6) is easy to be affected by the external noise caused by the line length, the operation check on the actual machine is recommended.

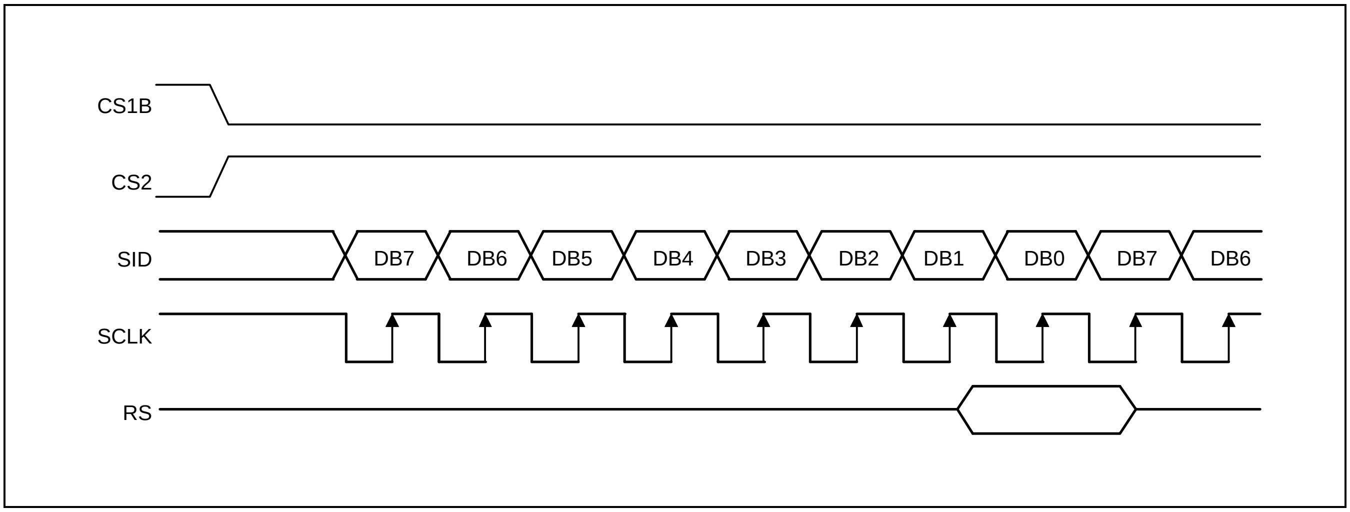


Figure 3. Serial Interface Timing

Busy Flag

The Busy Flag indicates whether the S6B0721 is operating or not. When DB7 is “H” in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each instruction, which improves the MPU performance.

Data Transfer

The S6B0721 uses bus holder and internal data bus for Data Transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in figure 4. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in figure 5. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

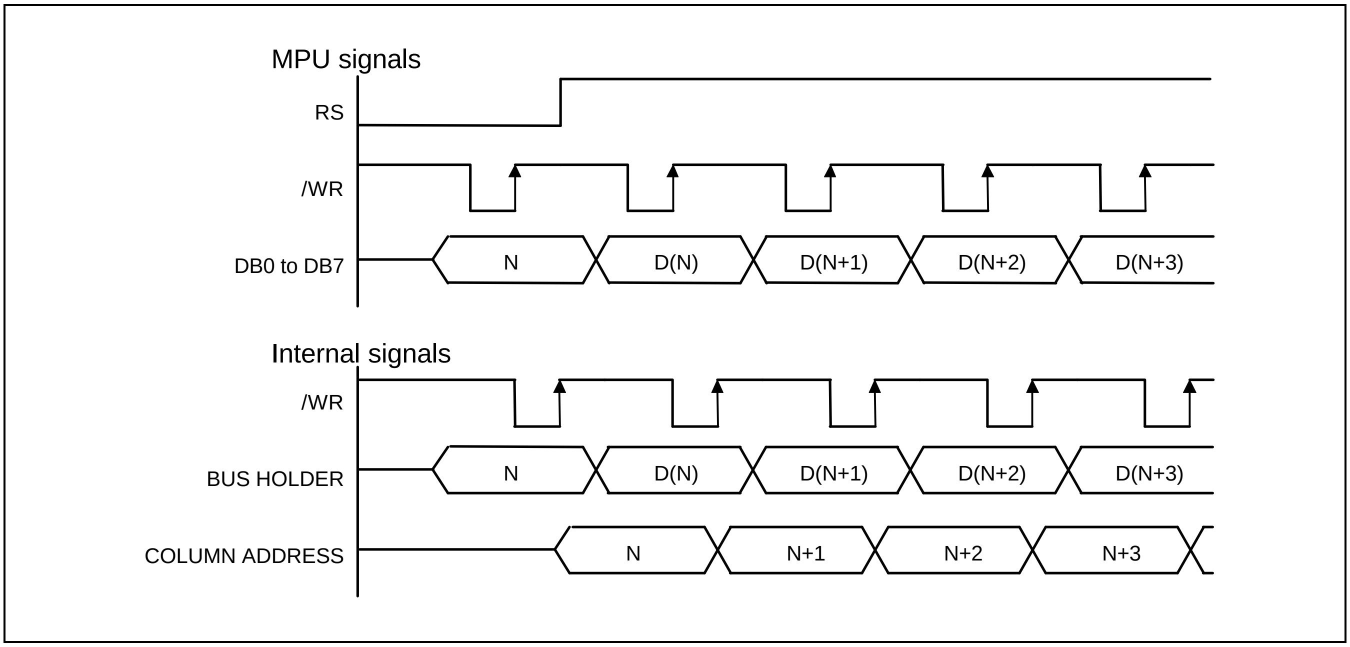


Figure 4. Write Timing

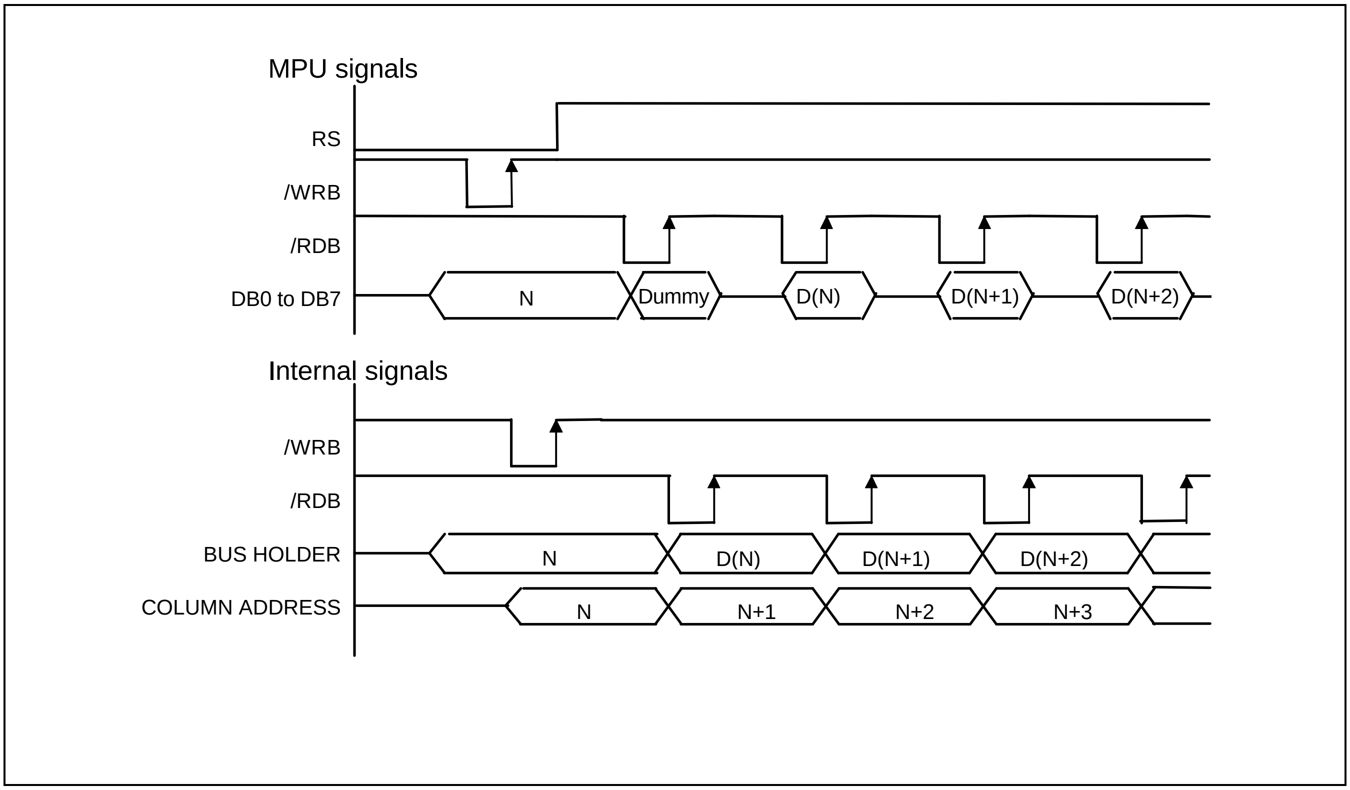


Figure 5. Read Timing

DISPLAY DATA RAM (DDRAM)

The Display Data RAM stores pixel data for the LCD. It is 65-row by 132-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 65 rows are divided into 8 pages of 8 lines and the 9th page with a single line (DB0 only). Data is read from or written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines as shown in Figure 6. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

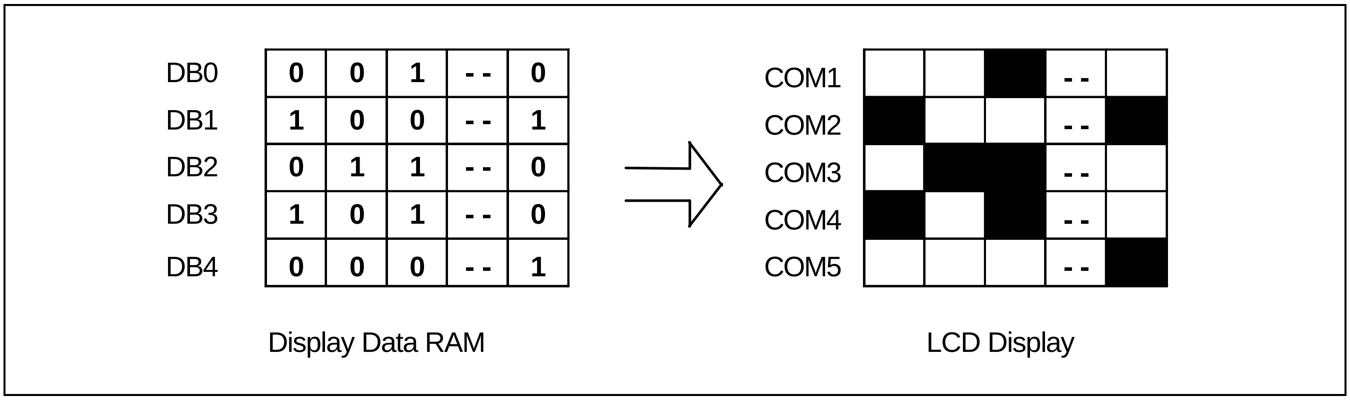


Figure 6. RAM-to-LCD Data Transfer

Page Address Circuit

This circuit is for providing a Page Address to Display Data RAM shown in figure 8. It incorporates 4-bit Page Address register changed by only the “Set Page” instruction. Page Address 8 (DB3 is “H”, but DB2, DB1 and DB0 are “L”) is a special RAM area for the icons and display data DB0 is only valid. When Page Address is above 8, it is impossible to access to on-chip RAM.

Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM1) of the display. Therefore, by setting line address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM as shown in figure 8. It incorporates 6-bit line address register changed by only the initial display line instruction and 6-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the Line Address for transferring the 132-bit RAM data to the display data latch circuit. However, display data of icons are not scrolled because the MPU can not access Line Address of icons.

Column Address Circuit

Column address circuit has a 8-bit preset counter that provides column address to the Display Data RAM as shown in figure 8. When set Column Address MSB / LSB instruction is issued, 8-bit [Y7:Y0] is updated. And, since this address is increased by 1 each a Read or Write Data instruction, microprocessor can access the display data continuously. However, the counter is not increased and locked if a non-existing address above 84H. It is unlocked if a column address is set again by set Column Address MSB / LSB instruction. And the Column Address counter is independent of page address register.

ADC select instruction makes it possible to invert the relationship between the Column Address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing ADC select instruction. Refer to the following figure 7.

SEG output	SEG 1	SEG 2	SEG 3	SEG 4	... ...	SEG 129	SEG 130	SEG 131	SEG 132
Column address [Y7:Y0]	00H	01H	02H	03H	... ...	80H	81H	82H	83H
Display data	1	0	1	0		1	1	0	0

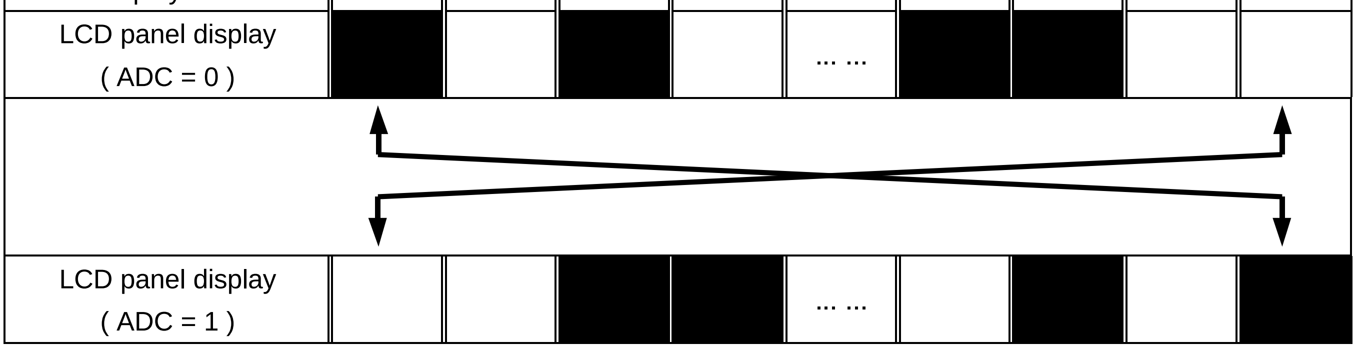
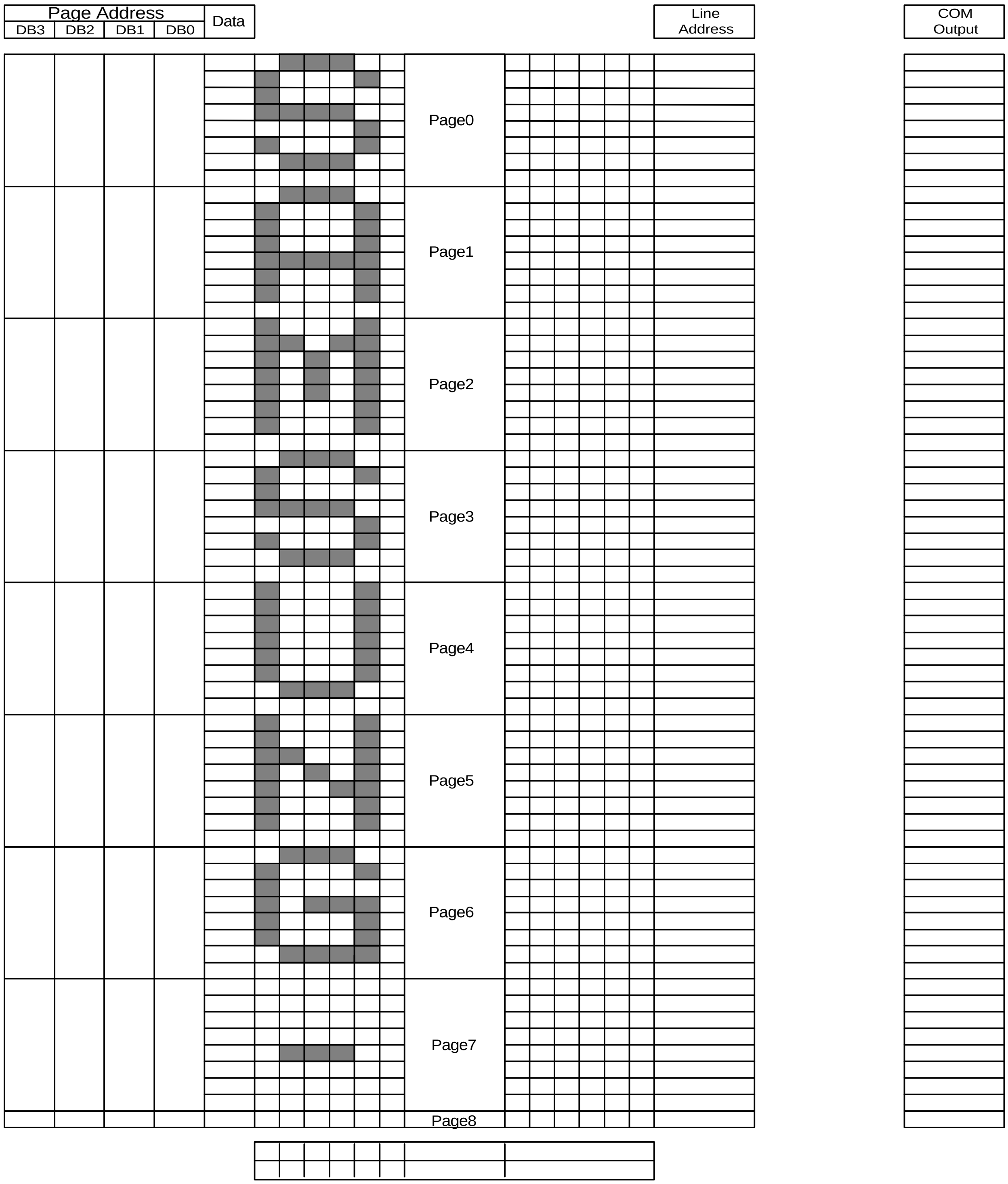


Figure 7. The Relationship between the Column Address and the Segment Outputs

Segment Control Circuit

This circuit controls the display data by the Display ON / OFF, Reverse display ON / OFF and entire display ON / OFF instructions without changing the data in the display data RAM.


Page Address
DB3
DB2
DB1
DB0
Data
Line Address
COM Output
Page0
Page1
Page2
Page3
Page4
Page5
Page6
Page7
Page8

LCD DISPLAY CIRCUITS

Oscillator

This is completely on-chip oscillator and its frequency is nearly independent of V_{DD}. This oscillator signal is used in the voltage converter and display timing generation circuit.

* Test condition: Temperature: 25°C & 85°C, TEMPS="L", No load

Figure 9. V_{DD} vs. f_{OSC}

Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL, generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock (CL) and the 132-bit display data is latched by the display data latch circuit in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M) which enables the LCD driver to make a AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. Driving 2-frame AC driver waveform and internal timing signal are shown in figure 9.

In a multiple-chip configuration, the slave chip requires the M, CL and DISP signals from the master. Table 11 shows the M, CL, and DISP status.

Table 11. Master and Slave Timing Signal Status

Operation mode	Oscillator	M	CL	DISP
Master	ON (internal clock used)	Output	Output	Output
	OFF (external clock used)	Output	Input	Output
Slave	-	Input	Input	Input

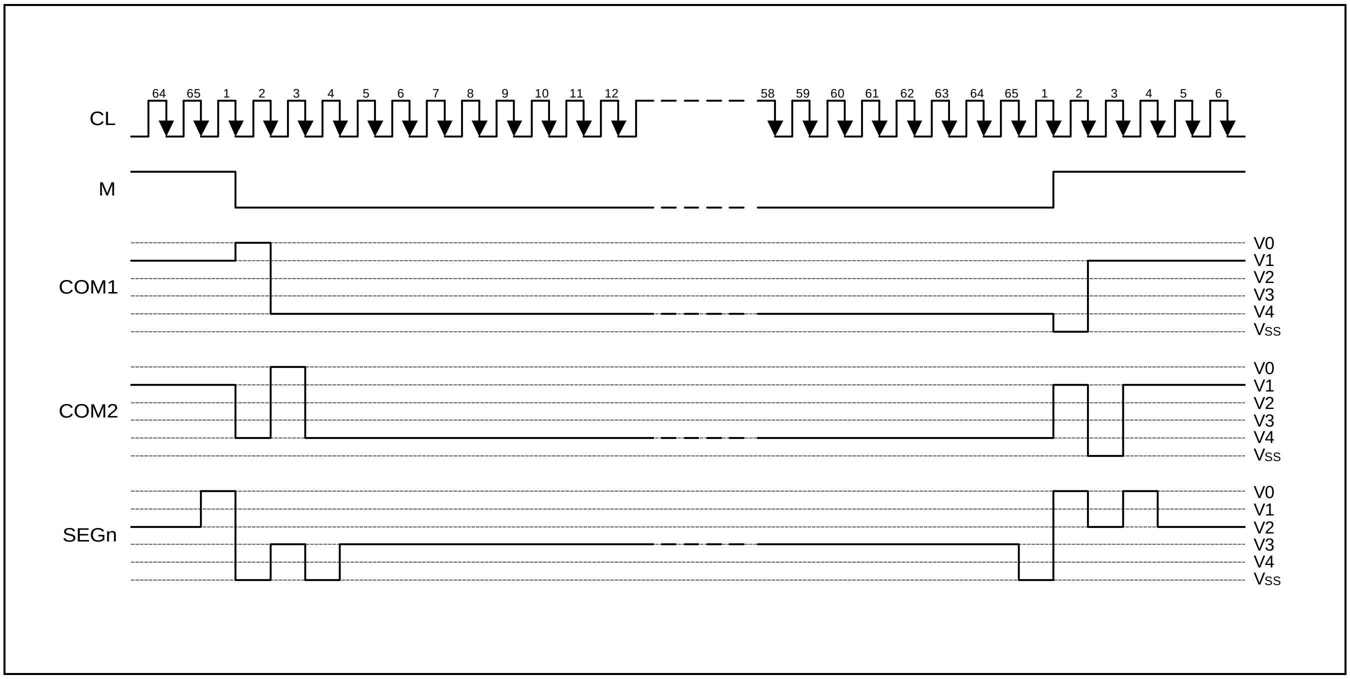


Figure 10. 2-frame AC Driving Waveform (Duty ratio = 1/65)

Common Output Control Circuit

This circuit controls the relationship between the number of common output and specified duty ratio. SHL Select Instruction specifies the scanning direction of the common output pins.

Table 12. The Relationship between Duty Ratio and Common Output

Duty	SHL	Common output pins					
		COM[1:16]	COM[17:24]	COM[25:40]	COM[41:48]	COM[49:64]	COMS
1/33	0	COM[1:16]	*NC			COM[17:32]	COMS
	1	COM[32:17]	*NC			COM[16:1]	
1/49	0	COM[1:24]		*NC	COM[25:48]		COMS
	1	COM[48:25]		*NC	COM[24:1]		
1/65	0	COM[1:64]					COMS
	1	COM[64:1]					

*NC: No Connection

LCD DRIVER CIRCUIT

This driver circuit is configured by 66-channel common drivers (including 2 COMS channels) and 132-channel segment drivers. This LCD panel driver voltage depends on the combination of display data and M signal.

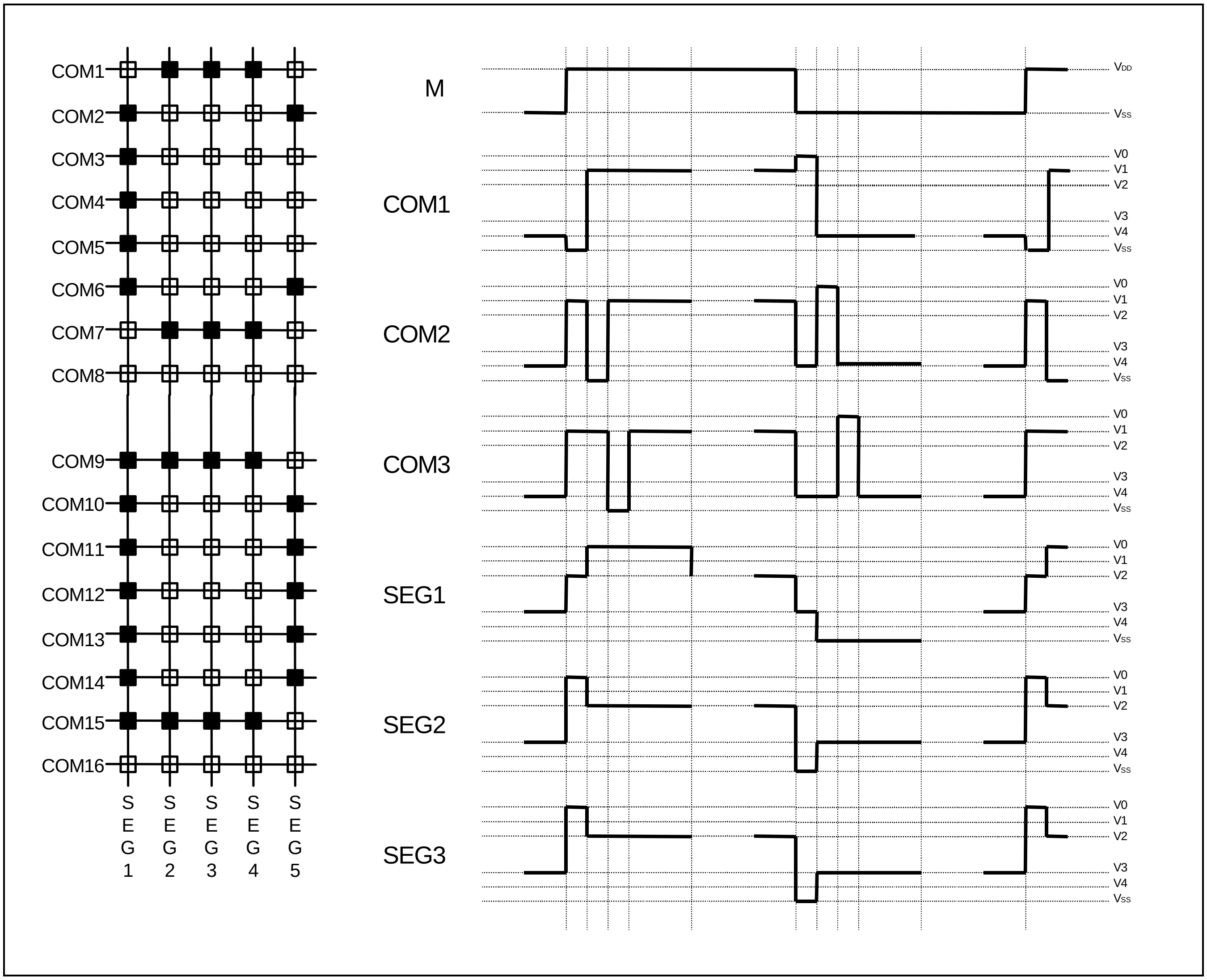


Figure 11. Segment and Common Timing

SAMSUNG ELECTRONICS

POWER SUPPLY CIRCUITS

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are valid only in master operation and controlled by power control instruction. For details, refers to "Instruction Description". Table 13 shows the referenced combinations in using power supply circuits.

Table 13. Recommended Power Supply Combinations

User setup	Power control (VC VR VF)	V/C circuits	V/R circuits	V/F circuits	VOUT	V0	V1 to V4
Only the internal power supply circuits are used	1 1 1	ON	ON	ON	Open	Open	Open
Only the voltage regulator circuits and voltage follower circuits are used	0 1 1	OFF	ON	ON	External input	Open	Open
Only the voltage follower circuits are used	0 0 1	OFF	OFF	ON	Open	External input	Open
Only the external power supply circuits are used	0 0 0	OFF	OFF	OFF	Open	External input	External input

Voltage Converter Circuits

These circuits boost up the electric potential between VDD and VSS to 2,3,4 or 5 times toward positive side and boosted voltage is outputted from VOUT pin.

[C1 = 1.0 to 4.7 mF]

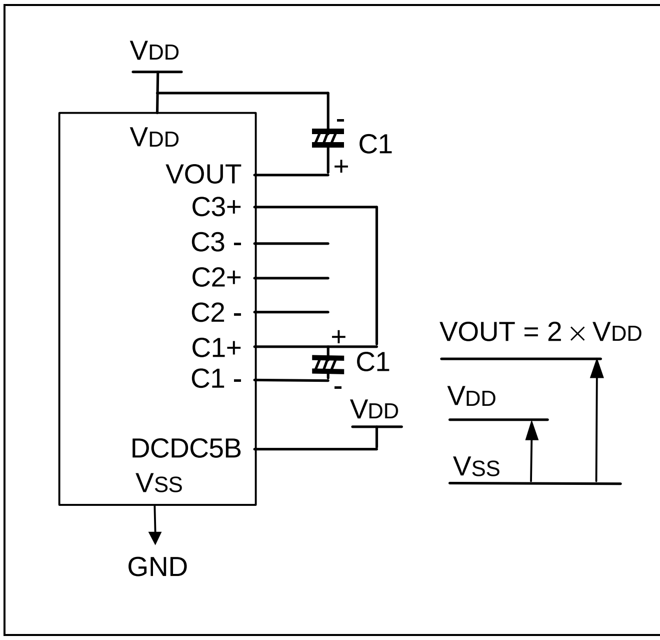


Figure 12. Two Times Boosting Circuit

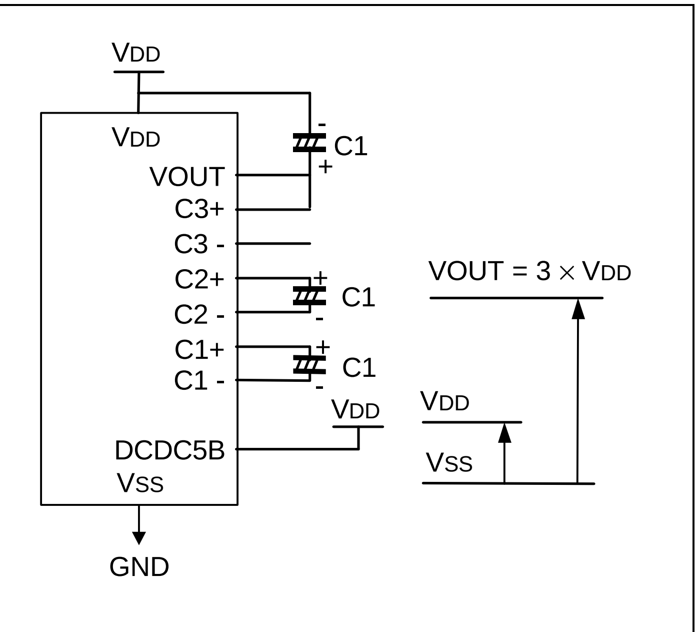


Figure 13. Three Times Boosting Circuit

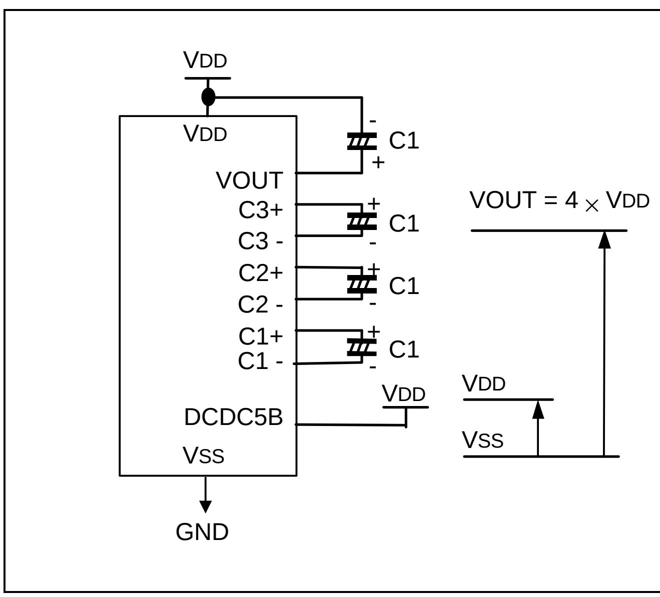


Figure 14. Four Times Boosting Circuit

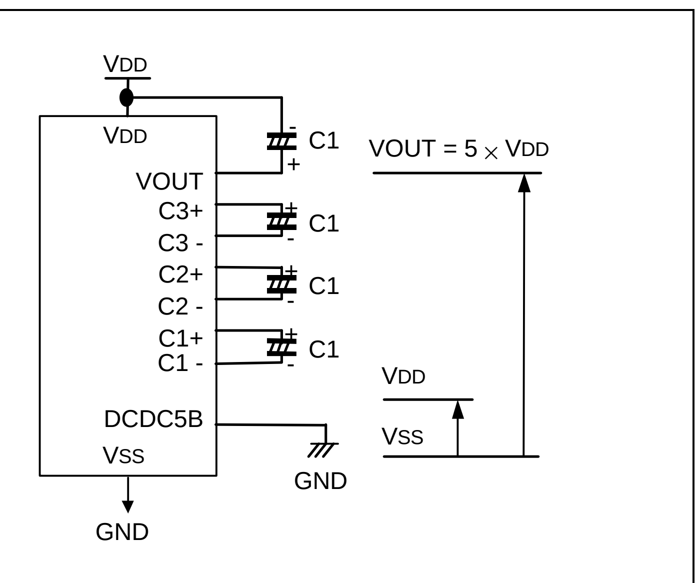


Figure 15. Five Times Boosting Circuit

SAMSUNG ELECTRONICS

Voltage Regulator Circuits

The function of the internal Voltage Regulator circuits is to determine liquid crystal operating voltage, V0, by adjusting resistors, Ra and Rb, within the range of |V0| < |VOUT|. Because VOUT is the operating voltage of operational-amplifier circuits shown in figure 16, it is necessary to be applied internally or externally.

For the Eq. 1, we determine V0 by Ra, Rb and V_{EV}. The Ra and Rb are connected internally or externally by INTRS pin. And V_{EV} called the voltage of electronic volume is determined by Eq. 2, where the parameter α is the value selected by instruction, "Set Reference Voltage Register", within the range 0 to 63. V_{REF} voltage at Ta = 25°C is shown in table 14-1.

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad [V] \text{ ------ (Eq. 1)}$$

$$V_{EV} = \left(1 - \frac{(63 - \alpha)}{300}\right) \times V_{REF} \quad [V] \text{ ------ (Eq. 2)}$$

Table 14-1. V_{REF} Voltage at Ta = 25 °C

TEMPS	Temp. coefficient	V_{REF} [V]
L	-0.05% / °C	2.0
H	-0.2% / °C	2.0

Table 14-2. Reference Voltage Parameters (α)

SV5	SV4	SV3	SV2	SV1	SV0	Reference voltage parameter (α)
0	0	0	0	0	0	0
0	0	0	0	0	1	1
: :	: :	: :	: :	: :	: :	: :
1	1	1	1	1	0	62
1	1	1	1	1	1	63

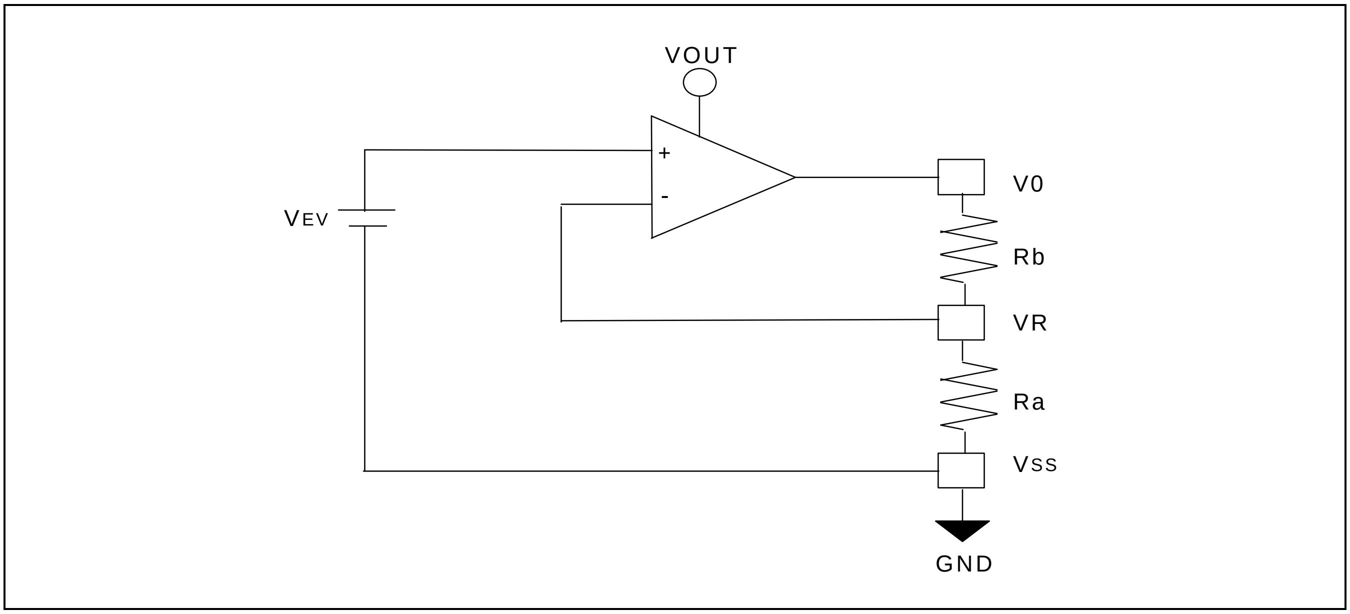


Figure 16. Internal Voltage Regulator Circuit

In Case of Using Internal Resistors, Ra and Rb (INTRS = "H")

When INTRS pin is “H”, resistor Ra is connected internally between VR pin and Vss, and Rb is connected between V0 and VR. We determine V0 by two instructions, "Regulator Resistor Select" and "Set Reference Voltage".

Table 15. Internal Rb / Ra Ratio depending on 3-bit Data (R2 R1 R0)

	3-bit data settings (R2 R1 R0)							
	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
1+(Rb / Ra)	1.90	2.19	2.55	3.02	3.61	4.35	5.29	6.48

The following figure shows V0 voltage measured by adjusting internal regulator resistor ratio (Rb / Ra) and 6-bit electronic volume registers for each temperature coefficient at Ta = 25 °C.

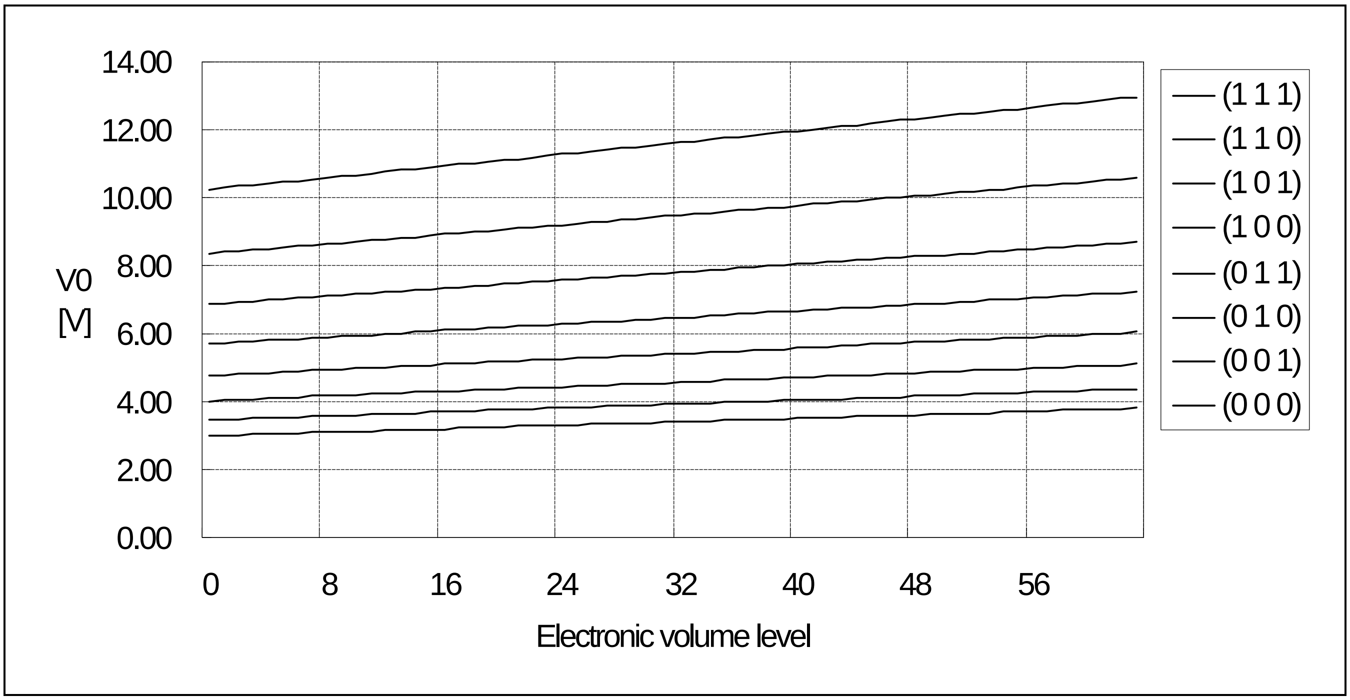


Figure 17. Electronic Volume Level

In Case of Using External Resistors, Ra and Rb. (INTRS = "L")

When INTRS pin is “L”, it is necessary to connect external regulator resistor Ra between VR and V_{SS}, and Rb between V0 and VR.

Example: For the following requirements

1. LCD driver voltage, V0 = 10V
2. 6-bit reference voltage register = (1, 0, 0, 0, 0, 0)
3. Maximum current flowing Ra, Rb = 1 uA

From Eq. 1

$$10 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad [V] \text{ ------ (Eq. 3)}$$

From Eq. 2

$$V_{EV} = \left(1 - \frac{(63 - 32)}{300}\right) \times 2.0 = 1.79 \quad [V] \text{ ------ (Eq. 4)}$$

From requirement 3.

$$\frac{10}{Ra + Rb} = 1\ [uA] \text{ ------ (Eq. 5)}$$

From equations Eq. 3, 4 and 5
Ra = 1.79 [MΩ]
Rb = 8.21 [MΩ]

The following table shows the range of V0 depending on the above requirements.

Table 16. V0 Depending on Electronic Volume Level

	Electronic volume level				
	0	**.......**	**32**	**.......**	**63**
V0	8.83	....	10.00	....	11.17

Voltage Follower Circuits

VLCD voltage (V0) is resistively divided into four voltage levels (V1, V2, V3 and V4) and those output impedance are converted by the Voltage Follower for increasing drive capability. The following table shows the relationship between V1 to V4 level and each duty ratio.

Table 17. The Relationship between V1 to V4 level and Duty Ratio

Duty Ratio	DUTY1	DUTY0	LCD Bias	V1	V2	V3	V4
1/33	L	L	1/5	(4/5) x V0	(3/5) x V0	(2/5) x V0	(1/5) x V0
			1/6	(5/6) x V0	(4/6) x V0	(2/6) x V0	(1/6) x V0
1/49	L	H	1/6	(5/6) x V0	(4/6) x V0	(2/6) x V0	(1/6) x V0
			1/8	(7/8) x V0	(6/8) x V0	(2/8) x V0	(1/8) x V0
1/65	H	L/H	1/7	(6/7) x V0	(5/7) x V0	(2/7) x V0	(1/7) x V0
			1/9	(8/9) x V0	(7/9) x V0	(2/9) x V0	(1/9) x V0

REFERECE CIRCUIT EXAMPLES

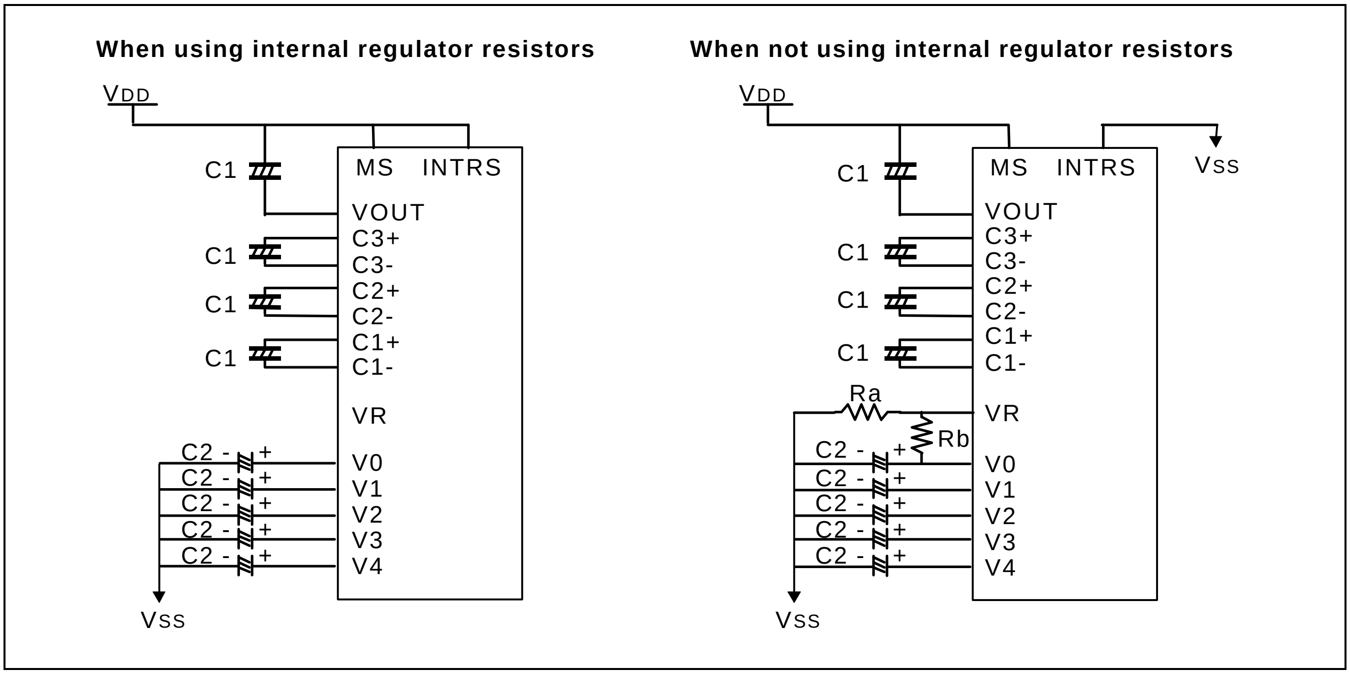


Figure 18. When Using all LCD Power Circuits (4-Time V/C: ON, V/R: ON, V/F: ON)

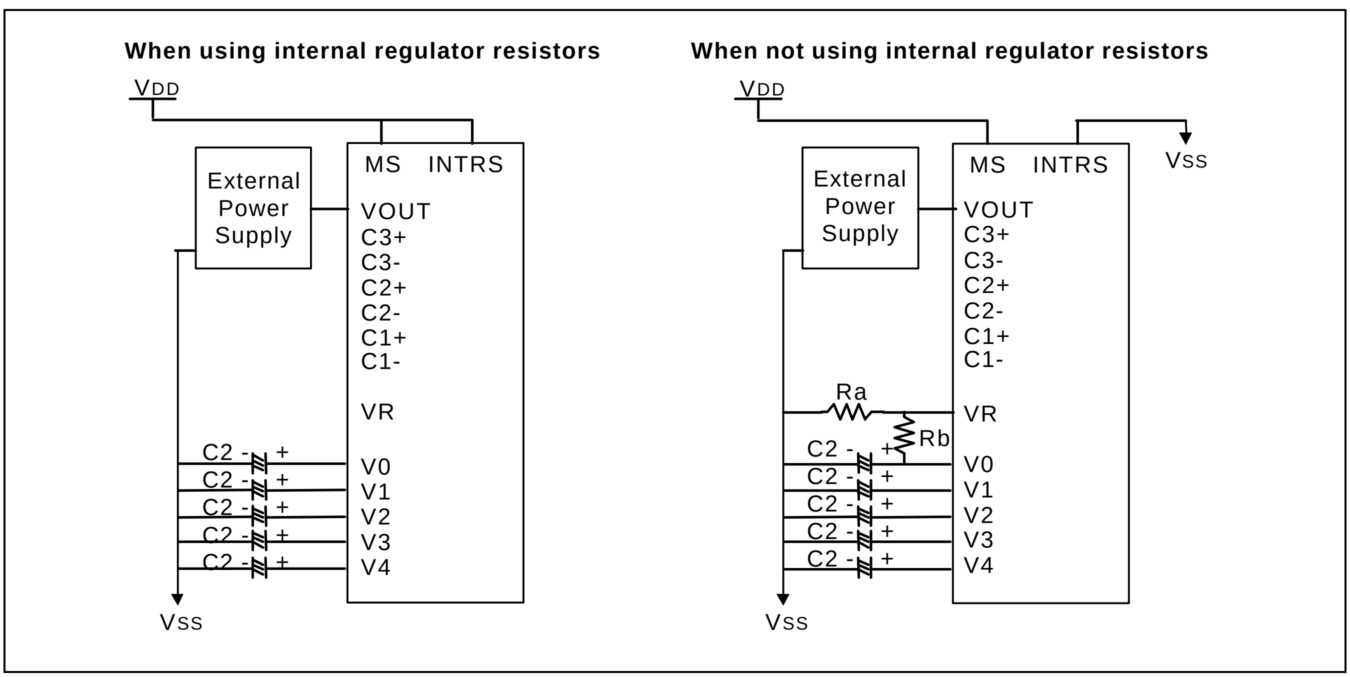


Figure 19. When Using some LCD Power Circuits (V/C: OFF, V/R: ON, V/F: ON)

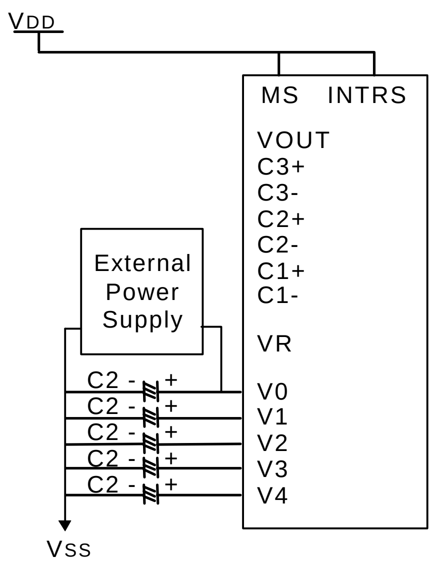
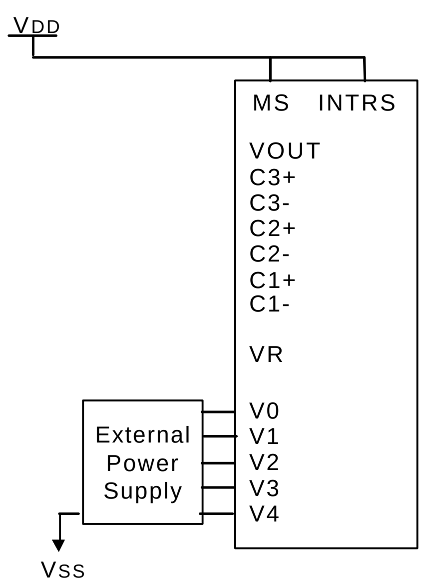


Figure 20. When Using some LCD Power Circuits (V/C: OFF, V/R: OFF, V/F: ON)



Value of external Capacitance

Item	Value	Unit
C1	1.0 to 4.7	µF
C2	0.47 to 1.0	

Figure 21. When Not Using any Internal LCD Power Supply Circuits (V/C: OFF, V/R: OFF, V/F: OFF)

RESET CIRCUIT

Setting RESETB to “L” or Reset instruction can initialize internal function.
When RESETB becomes “L”, following procedure is occurred.

Display ON / OFF: OFF
Entire display ON / OFF: OFF (normal)
ADC select: OFF (normal)
Reverse display ON / OFF: OFF (normal)
Power control register (VC, VR, VF) = (0, 0, 0)
LCD bias ratio: 1/7 (1/65 duty), 1/6 (1/49 duty), 1/5 (1/33 duty)
Read-modify-write: OFF
SHL select: OFF (normal)
Static indicator mode: OFF
Static indicator register: (S1, S0) = (0, 0)
Display start line: 0 (first)
Column address: 0
Page address: 0
Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)
Reference voltage set: OFF
Reference voltage control register: (SV5, SV4, SV3, SV2, SV1, SV0) = (1, 0, 0, 0, 0, 0)

When RESET instruction is issued, following procedure is occurred.

Read-modify-write: OFF
Static indicator mode: OFF
Static indicator register: (S1, S0) = (0, 0)
SHL select: 0
Display start line: 0 (first)
Column address: 0
Page address: 0
Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)
Reference voltage set: OFF
Reference voltage control register: (SV5, SV4, SV3, SV2, SV1, SV0) = (1, 0, 0, 0, 0, 0)

While RESETB is “L” or Reset instruction is executed, no instruction except read status can be accepted. Reset status appears at DB4. After DB4 becomes ”L”, any instruction can be accepted. RESETB must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RESETB is essential before used.

INSTRUCTION DESCRIPTION

Table 18. Instruction Table

× : Don't care

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Read display data	1	1	Read data								Read data from DDRAM
Write display data	1	0	Write data								Write data into DDRAM
Read status	0	1	BUSY	ADC	ON/OFF	RESETB	0	0	0	0	Read the internal status
Display ON / OFF	0	0	1	0	1	0	1	1	1	DON	Turn on/off LCD panel When DON = 0: display OFF When DON = 1: display ON
Initial display line	0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0	Specify DDRAM line for COM1
Set reference voltage mode	0	0	1	0	0	0	0	0	0	1	Set reference voltage Mode
Set reference voltage register	0	0	×	×	SV5	SV4	SV3	SV2	SV1	SV0	Set reference voltage register
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	Y7	Y6	Y5	Y4	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y3	Y2	Y1	Y0	Set column address LSB
ADC select	0	0	1	0	1	0	0	0	0	ADC	Select SEG output direction When ADC = 0: normal direction (SEG1→SEG132) When ADC = 1: reverse direction (SEG132→SEG1)
Reverse display ON / OFF	0	0	1	0	1	0	0	1	1	REV	Select normal / reverse display When REV = 0: normal display When REV = 1: reverse display
Entire display ON / OFF	0	0	1	0	1	0	0	1	0	EON	Select normal / entire display ON When EON = 0: normal display. When EON = 1: entire display ON
LCD bias select	0	0	1	0	1	0	0	0	1	BIAS	Select LCD bias
Set modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset modify-read	0	0	1	1	1	0	1	1	1	0	Release modify-read mode
Reset	0	0	1	1	1	0	0	0	1	0	Initialize the internal functions
SHL select	0	0	1	1	0	0	SHL	×	×	×	Select COM output direction When SHL = 0: normal direction (COM1→COM64) When SHL = 1: reverse direction (COM64→COM1)
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Regulator resistor select	0	0	0	0	1	0	0	R2	R1	R0	Select internal resistance ratio of the regulator resistor
Set static indicator mode	0	0	1	0	1	0	1	1	0	SM	Set static indicator mode
Set static indicator register	0	0	×	×	×	×	×	×	S1	S0	Set static indicator register
Power save	-	-	-	-	-	-	-	-	-	-	Compound instruction of display OFF and entire display ON
Test instruction	0	0	1	1	1	1	×	×	×	×	***Don't use this instruction.***

Read Display Data

8-bit data from Display Data RAM specified by the column address and page address can be read by this instruction. As the column address is increased by 1 automatically after each this instruction, the microprocessor can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register. Display Data cannot be read through the serial interface.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read data							

Write Display Data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	Write data							

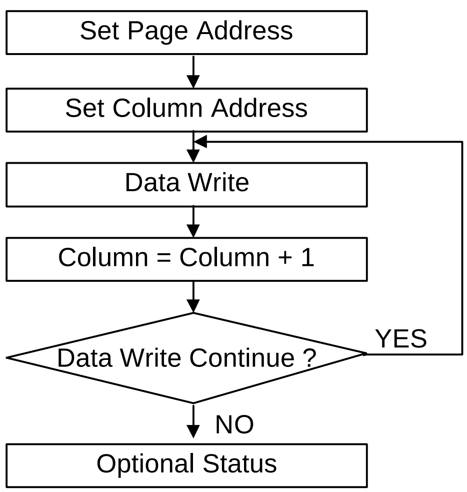


Figure 22. Sequence for Writing Display Data

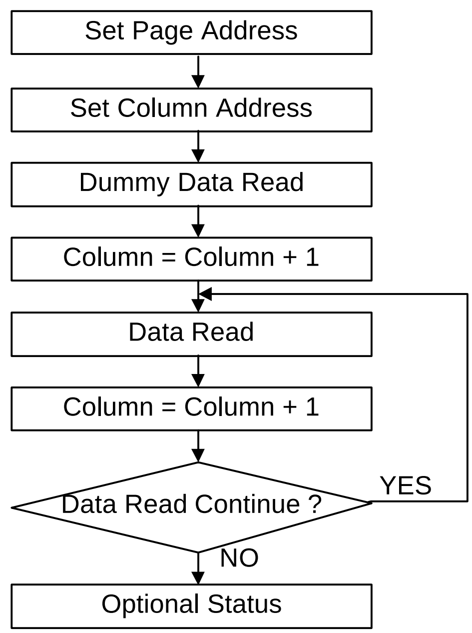


Figure 23. Sequence for Reading Display Data

Read Status

Indicates the internal status of the S6B0721.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	ADC	ON/OFF	RESETB	0	0	0	**0**

Flag	Description
BUSY	The device is busy when internal operation or reset. Any instruction is rejected until BUSY goes Low. 0: chip is active, 1: chip is being busy.
ADC	Indicates the relationship between RAM column address and segment driver. 0: reverse direction (SEG132 $\rightarrow$ SEG1), 1: normal direction (SEG1 $\rightarrow$ SEG132)
ON / OFF	Indicates display ON / OFF status 0: display ON, 1: display OFF
RESETB	Indicates the initialization is in progress by RESETB signal. 0: chip is active, 1: chip is being reset.

Display ON / OFF

Turns the display ON or OFF

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	DON

DON = 1: display ON
DON = 0: display OFF

Initial Display Line

Sets the line address of display RAM to determine the Initial Display Line. The RAM display data is displayed at the top row (COM1 when SHL = L, COM64 when SHL = H) of LCD panel.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0

ST5	ST4	ST3	ST2	ST1	ST0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

Reference Voltage Select

Consists of 2-byte instruction
The 1st instruction sets reference voltage mode, the 2nd one updates the contents of reference voltage register. After second instruction, reference voltage mode is released.

The 1st Instruction: Set Reference Voltage Select Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1

The 2nd Instruction: Set Reference Voltage Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	SV5	SV4	SV3	SV2	SV1	SV0

SV5	SV4	SV3	SV2	SV1	SV0	Reference voltage parameter (α)
0	0	0	0	0	0	0
0	0	0	0	0	1	1
: :	: :	: :	: :	: :	: :	: :
1	1	1	1	1	0	62
1	1	1	1	1	1	63

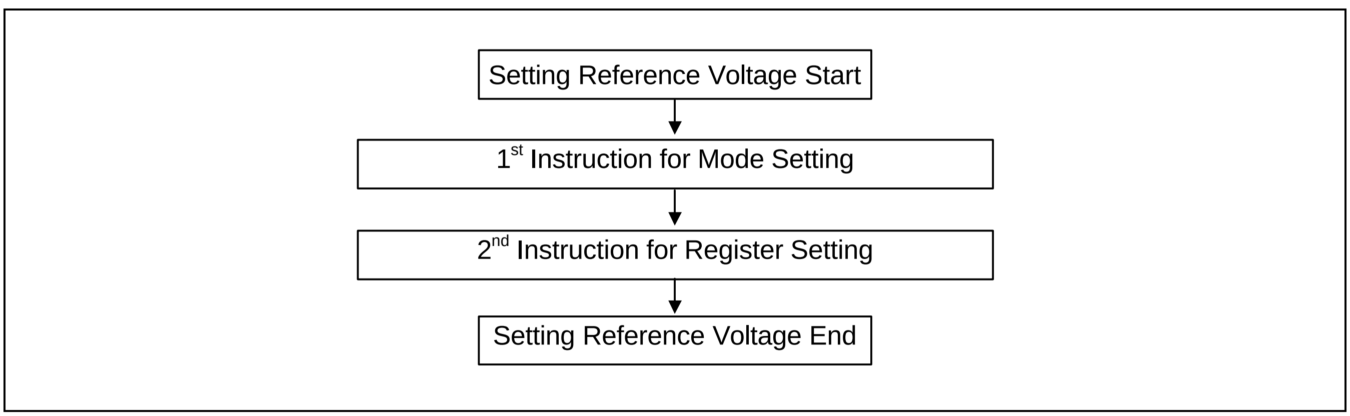


Figure 24. Sequence for Setting the Reference Voltage

Set Page Address

Sets the Page Address of display data RAM from the microprocessor into the Page Address register. Any RAM data bit can be accessed when its Page Address and column address are specified. Along with the column address, the Page Address defines the address of the display RAM to write or read display data. Changing the Page Address doesn't effect to the display status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	P3	P2	P1	P0

P3	P2	P1	P0	Page
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
0	1	1	1	7
1	0	0	0	8

Set Column Address

Sets the Column Address of display RAM from the microprocessor into the Column Address register. Along with the Column Address, the Column Address defines the address of the display RAM to write or read display data. When the microprocessor reads or writes display data to or from display RAM, column addresses are automatically increased.

Set Column Address MSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	Y7	Y6	Y5	Y4

Set Column Address LSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	Y3	Y2	Y1	Y0

Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131

ADC Select

Changes the relationship between RAM column address and segment driver. The direction of segment driver output pins can be reversed by software. This makes IC layout flexible in LCD module assembly.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	ADC

ADC = 0: normal direction (SEG1 → SEG132)
ADC = 1: reverse direction (SEG132 → SEG1)

Reverse Display ON / OFF

Reverses the display status on LCD panel without rewriting the contents of the display data RAM.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	1	REV

REV	RAM bit data = “1”	RAM bit data = “0”
0 (normal)	LCD pixel is illuminated	LCD pixel is not illuminated
1 (reverse)	LCD pixel is not illuminated	LCD pixel is illuminated

Entire Display ON / OFF

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This instruction has priority over the reverse display ON / OFF instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	0	EON

EON = 0: normal display
EON = 1: entire display ON

Select LCD Bias

Selects LCD bias ratio of the voltage required for driving the LCD.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	1	Bias

Duty ratio	DUTY1	DUTY0	LCD bias	
			Bias = 0	Bias = 1
1/33	0	0	1/5	1/6
1/49	0	1	1/6	1/8
1/65	1	0/1	1/7	1/9

Set Modify-Read

This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the write display data instruction. And it reduces the load of microprocessor when the data of a specific area is repeatedly changed during cursor blinking or others. This mode is canceled by the reset Modify-read instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0

Reset Modify-Read

This instruction cancels the Modify-read mode, and makes the column address return to its initial value just before the set Modify-read instruction is started.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	1	0

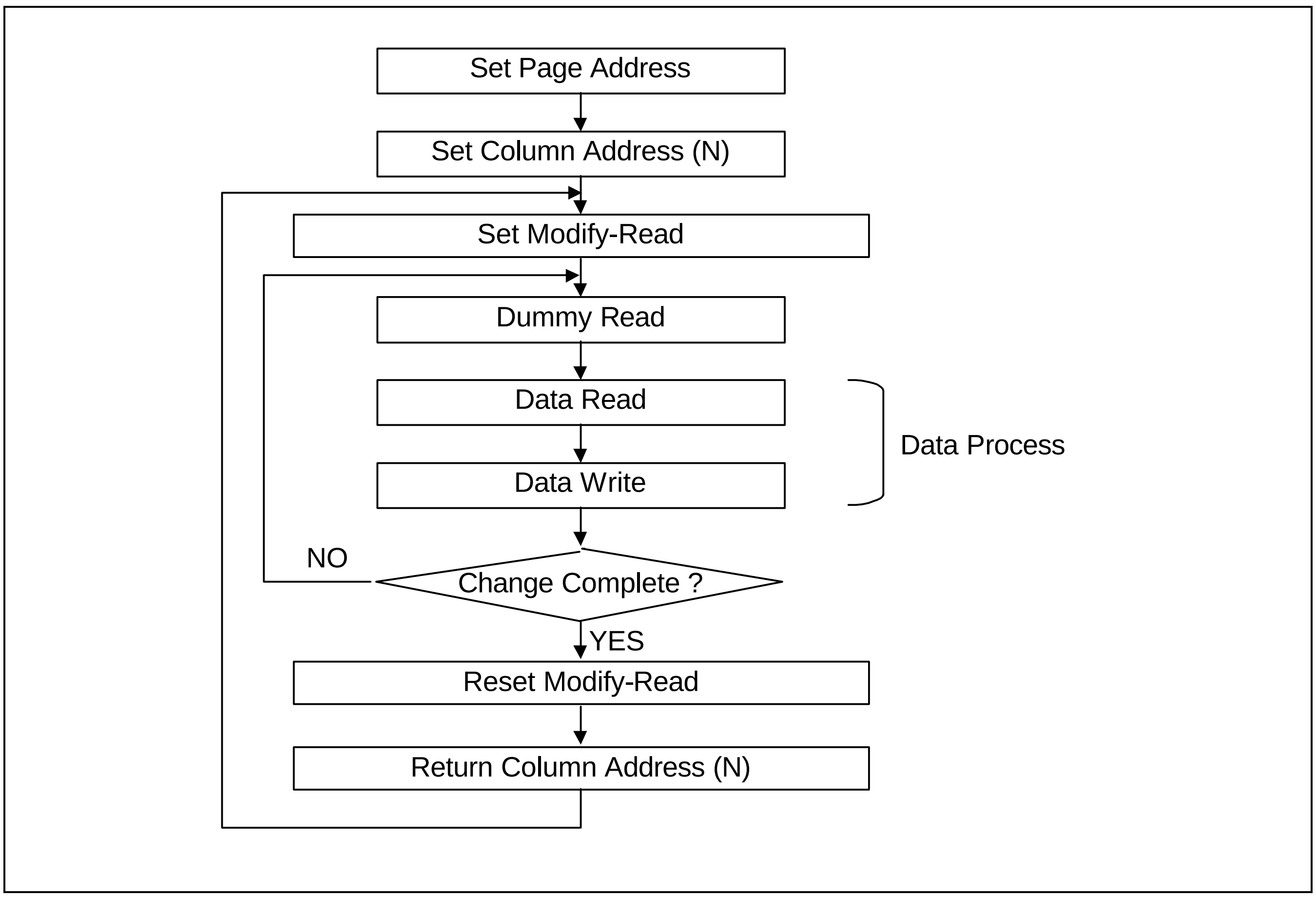


Figure 25. Sequence for Cursor Display

Reset

This instruction resets initial display line, column address, page address, and common output status select to their initial status, but dose not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply which is initialized by the RESETB pin.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

SHL Select

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	SHL	×	×	×

× : Don't care

SHL = 0: normal direction (COM1 → COM64)
SHL = 1: reverse direction (COM64 → COM1)

Power control

Selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	VC	VR	VF

VC	VR	VF	Status of internal power supply circuits
0 1			Internal voltage converter circuit is OFF Internal voltage converter circuit is ON
	0 1		Internal voltage regulator circuit is OFF Internal voltage regulator circuit is ON
		0 1	Internal voltage follower circuit is OFF Internal voltage follower circuit is ON

Regulator Resistor Select

Selects resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit. Refer to the table 15.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	1 + (Rb / Ra)
0	0	0	1.90
0	0	1	2.19
0	1	0	2.55
0	1	1	3.02
1	0	0	3.61
1	0	1	4.35
1	1	0	5.29
1	1	1	6.48

Set Static Indicator State

Consists of two bytes instruction. The first byte instruction (set Static Indicator mode) enables the second byte instruction (set Static Indicator register) to be valid. The first byte sets the static indicator ON / OFF. When it is on, the second byte updates the contents of static indicator register without issuing any other instruction and this static indicator state is released after setting the data of indicator register.

The 1st Instruction: Set Static Indicator Mode (ON / OFF)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	0	SM

SM = 0: static indicator OFF
SM = 1: static indicator ON

The 2nd Instruction: Set Static Indicator Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	×	×	×	×	S1	S0

S1	S0	Status of static indicator output
0	0	OFF
0	1	ON (about 1 second blinking)
1	0	ON (about 0.5 second blinking)
1	1	ON (always ON)

Power Save (Compound Instruction)

If the entire display ON / OFF instruction is issued during the display OFF state, S6B0721 enters the Power Save status to reduce the power consumption to the static power consumption value. According to the status of static indicator mode, power save is entered to one of two modes (sleep and standby mode). When static indicator mode is ON, standby mode is issued, when OFF, sleep mode is issued. Power Save mode is released by the display ON and entire display OFF instruction.

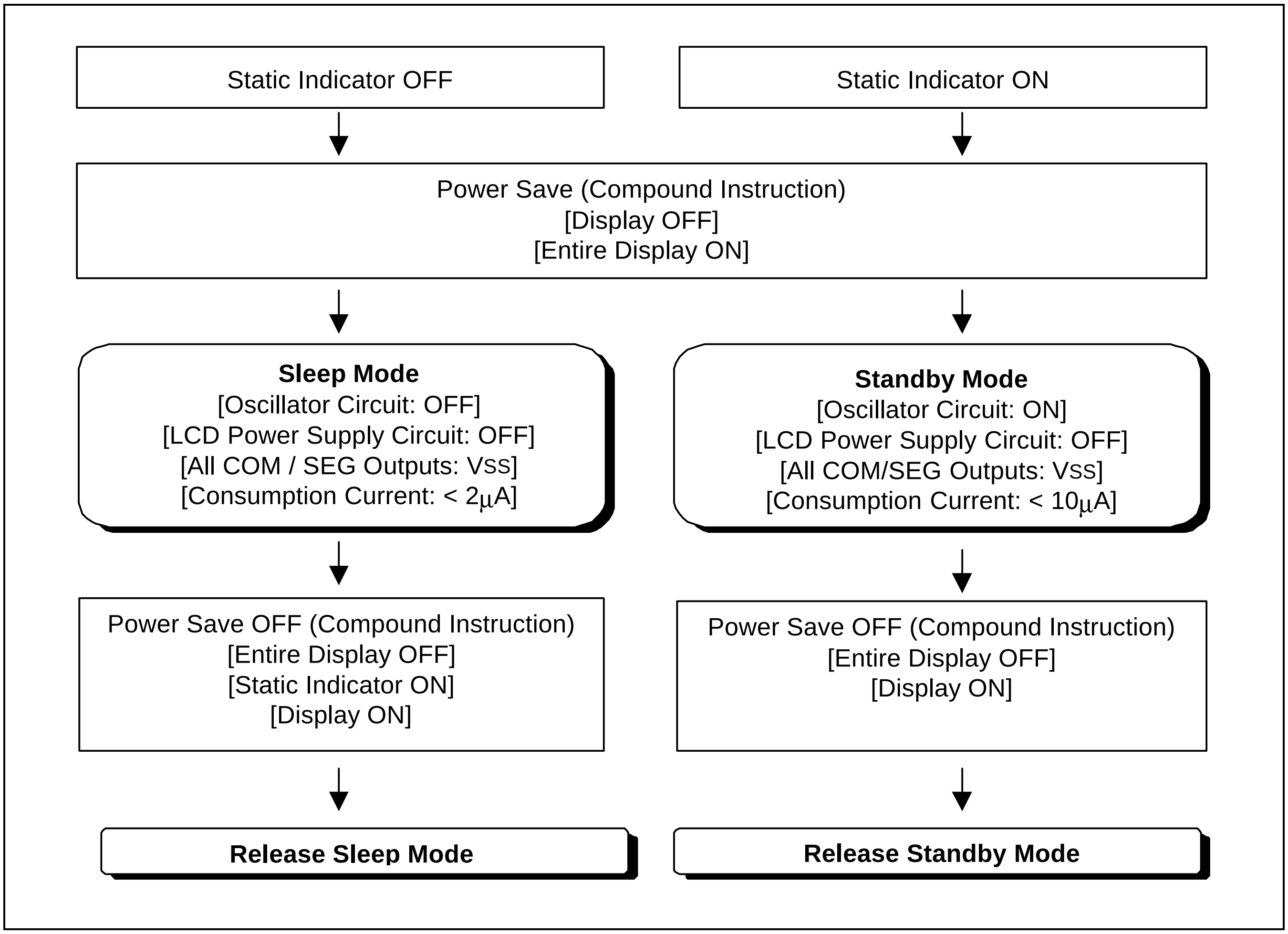


Figure 26. Power Save Routine

Referential Instruction Setup Flow (1)

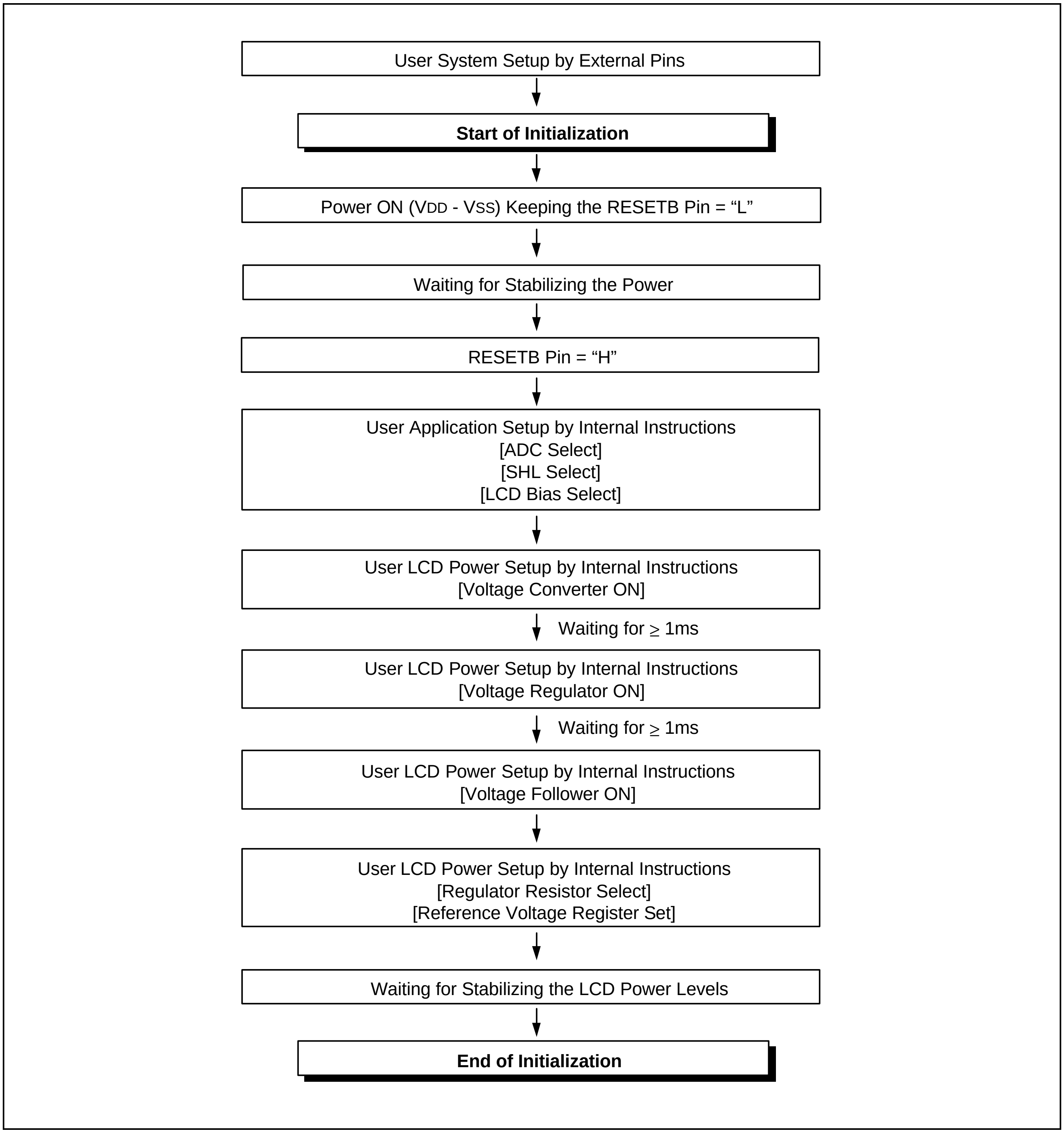


Figure 27. Initializing with the Built-in Power Supply Circuits

Referential Instruction Setup Flow (2)

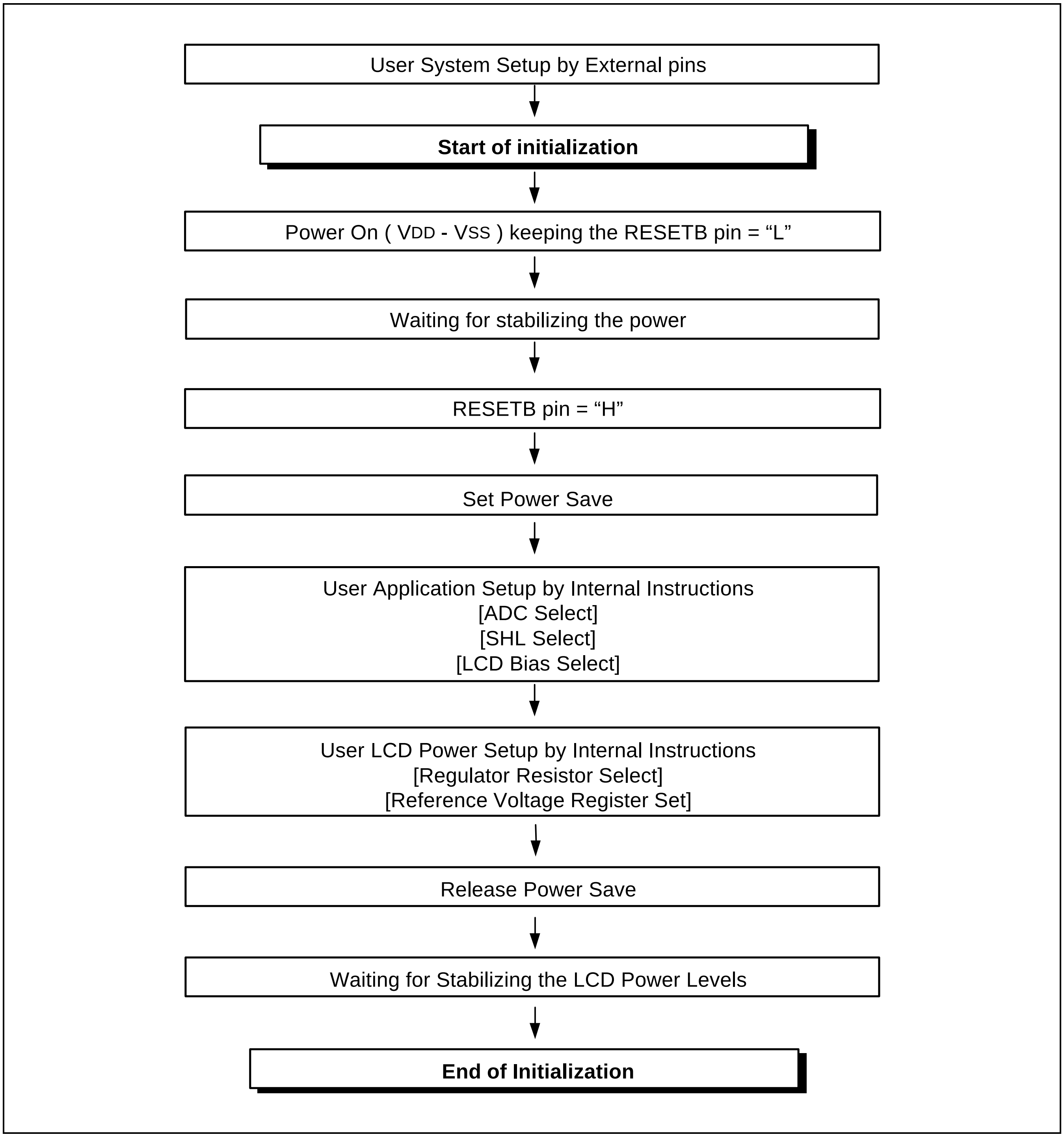


Figure 28. Initializing without the Built-in Power Supply Circuits

Referential Instruction Setup Flow (3)

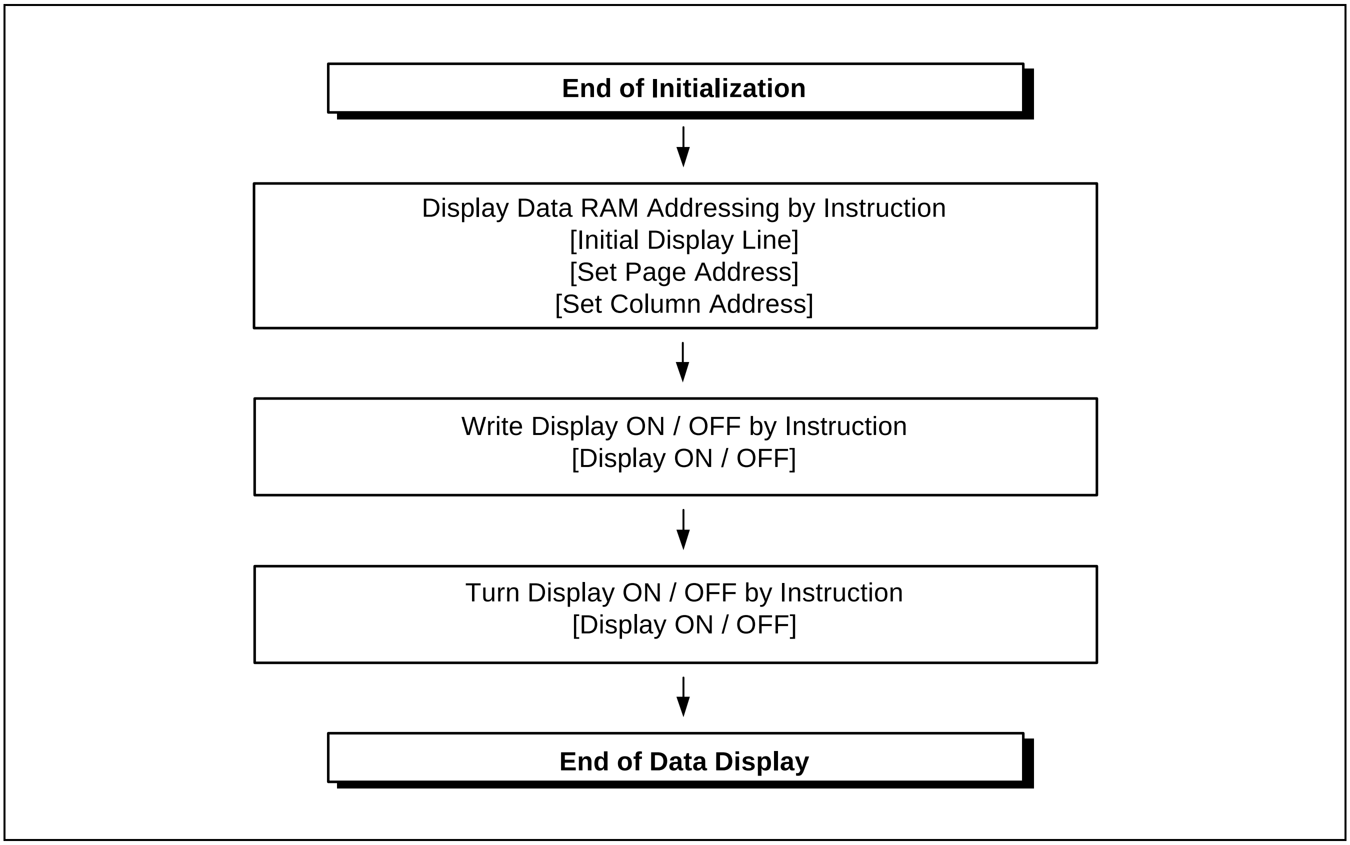


Figure 29. Data Displaying

Referential Instruction Setup Flow (4)

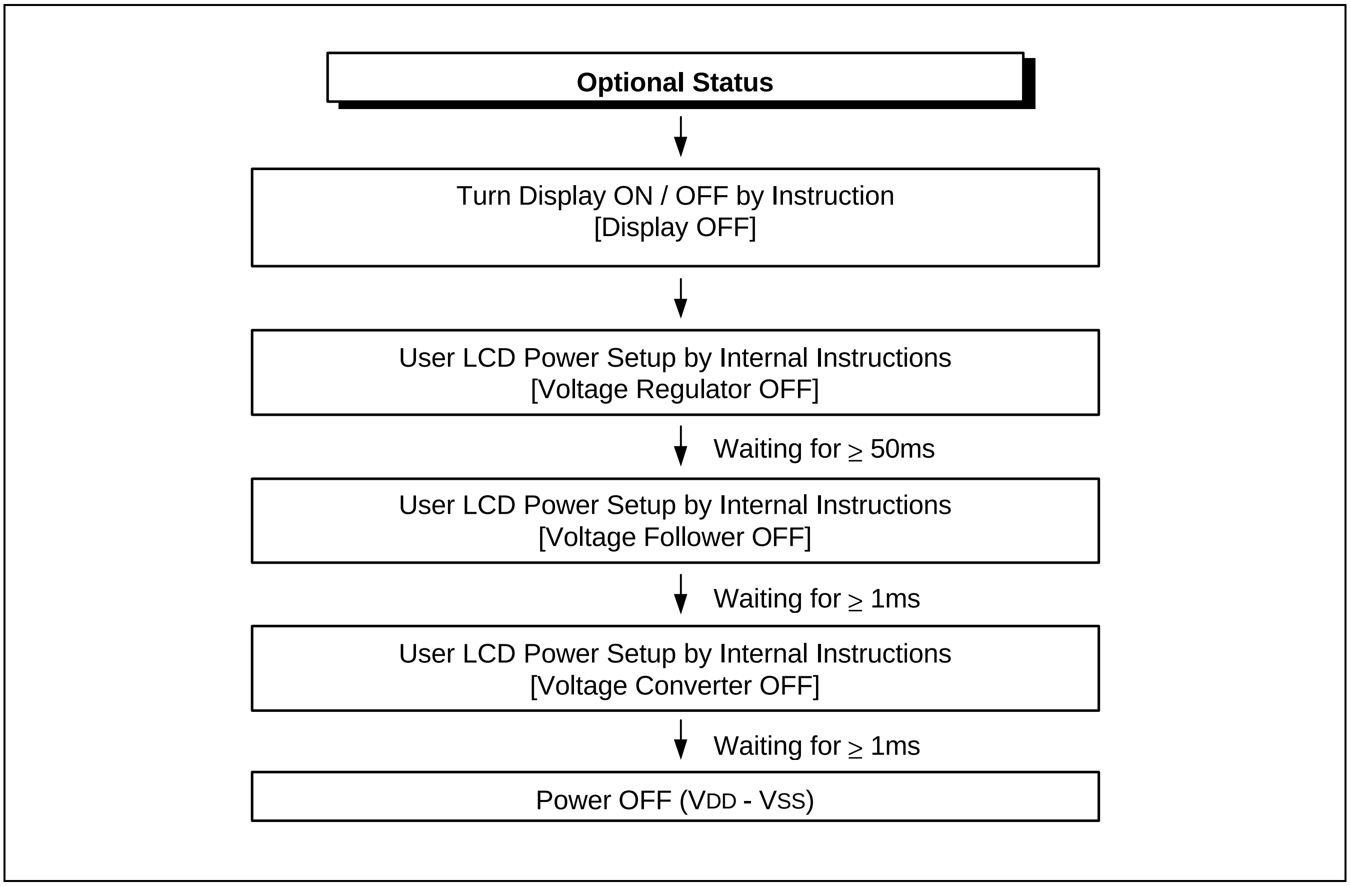


Figure 30. Power OFF

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 19. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	-0.3 to +7.0	V
	V_{LCD}	-0.3 to +17.0	V
Input voltage range	V_{IN}	-0.3 to V_{DD} +0.3	V
Operating temperature range	T_{OPR}	-40 to +85	°C
Storage temperature range	T_{STR}	-55 to +125	°C

NOTES:

1. VDD and VLCD are based on VSS = 0V.
2. Voltages V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS must always be satisfied. (VLCD = V0 – VSS)
3. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently.
   It is desirable to use this LSI under electrical characteristic conditions during general operation.
   Otherwise, this LSI may malfunction or reduced LSI reliability may result.

DC CHARACTERISTICS

Table 20. DC Characteristics

(V_{SS} = 0V, V_{DD} = 2.4 to 3.6V, Ta = -40 to 85°C)

Item		Symbol	Condition		Min.	Typ.	Max	Unit	Pin used
Operating voltage (1)		V_{DD}			2.4	-	3.6	V	V_{DD} *1
Operating voltage (2)		V0			4.0	-	15.0	V	V0 *2
Input voltage	High	V_{IH}			0.8V_{DD}	-	V_{DD}	V	*3
	Low	V_{IL}			V_{SS}	-	0.2V_{DD}		
Output voltage	High	V_{OH}	I_{OH} = -0.5mA		0.8V_{DD}	-	V_{DD}	V	*4
	Low	V_{OL}	I_{OL} = 0.5mA		V_{SS}	-	0.2V_{DD}		
Input leakage current		I_{IL}	V_{IN} = V_{DD} or V_{SS}		- 1.0	-	+ 1.0	µA	*5
Output leakage current		I_{OZ}	V_{IN} = V_{DD} or V_{SS}		- 3.0	-	+ 3.0	µA	*6
LCD driver ON resistance		R_{ON}	Ta = 25°C, V0 = 8V		-	2.0	3.0	kΩ	SEGn COMn *7
Oscillator frequency	Internal	f_{OSC}	Ta = 25°C Duty ratio = 1/65		32.7	43.6	54.5	kHz	CL *8
	External	f_{CL}			4.09	5.45	6.81		
Voltage converter input voltage		V_{DD}	× 2		2.4	-	3.6	V	V_{DD}
			× 3		2.4	-	3.6		
			× 4		2.4	-	3.6		
			× 5		2.4	-	3.0		
Voltage converter output voltage		VOUT	×2 / ×3 / ×4 / ×5 voltage conversion (no-load)		95	99	-	%	VOUT
Voltage regulator operating voltage		VOUT			4.0	-	15.0	V	VOUT
Voltage follower operating voltage		V0			4.0	-	15.0	V	V0 *9
Reference voltage		V_{REF0}	Ta = 25°C	-0.05%/°C	1.94	2.00	2.06	V	*10
		V_{REF1}		-0.2%/°C	1.94	2.00	2.06	V	*10

SAMSUNG ELECTRONICS

Dynamic Current Consumption (1) when the Built-in Power Circuit is OFF (At Operate Mode)

(Ta = 25 °C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption (1)	I_{DD1}	V_{DD} = 3.0V V0 – V_{SS} = 11.0V 1/65 duty ratio Display pattern OFF	-	-	20	µA	*11

Dynamic Current Consumption (2) when the built-in power circuit is ON (At operate mode)

(Ta = 25 °C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption (2)	I_{DD2}	V_{DD} = 3.0V, quad boosting, V0 – V_{SS} = 11.0V, 1/65 duty ratio, Display pattern OFF, Normal power mode	-	70	100	µA	*12
		V_{DD} = 3.0V, quad boosting, V0 – V_{SS} = 11.0V, 1/65 duty ratio, Display pattern checker, Normal power mode	-	95	160	µA	*12

Current Consumption During Power Save Mode

(Ta = 25 °C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Sleep mode current	I_{DDS1}	During sleep	-	-	2.0	µA	
Standby mode current	I_{DDS2}	During standby	-	-	10.0	µA	

Table 21. The Relationship between Oscillation Frequency and Frame Frequency

Duty Ratio	Item	FCL	FM
1/65	On-chip oscillator circuit is used	$\frac{Fosc}{8}$	$\frac{Fosc}{2 \times 8 \times 65}$
	On-chip oscillator circuit is not used	External input (fCL)	$\frac{Fosc}{2 \times 65}$
1/49	On-chip oscillator circuit is used	$\frac{Fosc}{10}$	$\frac{Fosc}{2 \times 10 \times 49}$
	On-chip oscillator circuit is not used	External input (fCL)	$\frac{Fosc}{2 \times 49}$
1/33	On-chip oscillator circuit is used	$\frac{Fosc}{15}$	$\frac{Fosc}{2 \times 15 \times 33}$
	On-chip oscillator circuit is not used	External input (fCL)	$\frac{Fosc}{2 \times 33}$

(fOSC: oscillation frequency, fCL: display clock frequency, fM: LCD AC signal frequency)

[* Remark Solves]
*1. Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the MPU.
*2. In case of external power supply is applied.
*3. CS1B, CS2, RS, DB0 to DB7, E_RD, RW_WR, RESETB, MS, MI, PS, INTRS, HPM, DCDC5B, CLS, CL, M, DISP pins.
*4. DB0 to DB7, M, FRS, DISP, CL pins.
*5. CS1B, CS2, RS, DB [7:0], E_RD, RW_WR, RESETB, MS, MI, PS, INTRS, HPM, DCDC5B, CLS, CL, M, DISP pins.
*6. Applies when the DB [7:0], M, DISP, and CL pins are in high impedance.
*7. Resistance value when ± 0.1[mA] is applied during the ON status of the output pin SEGn or COMn.
RON= ΔV / 0.1 [kΩ] (ΔV: voltage change when ± 0.1[mA] is applied in the ON status.)
*8. See table 21 for the relationship between oscillation frequency and frame frequency.
*9. The voltage regulator circuit adjusts V0 within the voltage follower operating voltage range
*10. On-chip reference voltage source of the voltage regulator circuit to adjust V0.
*11,12. Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU.
The current consumption, when the built-in power supply circuit is ON or OFF.
The current flowing through voltage regulation resistors (Ra and Rb) is not included.
It does not include the current of the LCD panel capacity, wiring capacity, etc.

REFERENCE DATA

I_{DD1} vs. V_{DD}

* Test Condition: Temperature: 25°C & 85°C, V0 = 11V (External), TEMPS = 'L', 1/65 duty, Normal Power Mode

TBD

Figure 31. Display Pattern is OFF

I_{DD2} VS. V_{DD}

* Test Condition: Temperature: 25°C & 85°C, 1/65 duty, Quad Boosting, RR = 6, EV = 32

TBD

Figure 32. Display Pattern is OFF

TBD

Figure 33. Display Pattern is Checker

AC CHARACTERISTICS

Read / Write Characteristics (8080-series MPU)

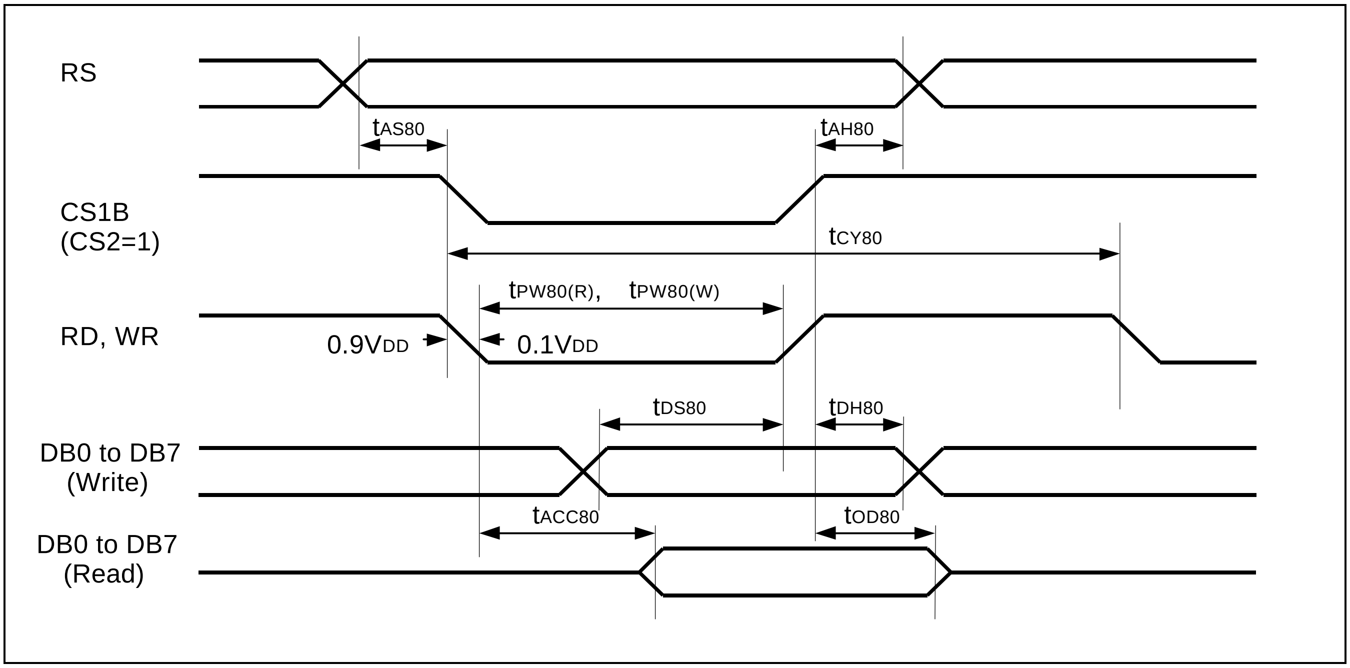


Figure 34. Read / Write Characteristics (8080-series MPU)

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS	t_{AS80} t_{AH80}	13 17	-	-	ns	
System cycle time	RS	t_{CY80}	400	-	-	ns	
Pulse width (WR)	RW_WR	$t_{PW80\ (W)}$	55	-	-	ns	
Pulse width (RD)	E_RD	$t_{PW80\ (R)}$	125	-	-	ns	
Data setup time Data hold time	DB7 to DB0	t_{DS80} t_{DH80}	35 13	-	-	ns	
Read access time Output disable time		t_{ACC80} t_{OD80}	- 10	-	125 90	ns	C_L = 100 pF

Read / Write Characteristics (6800-series Microprocessor)

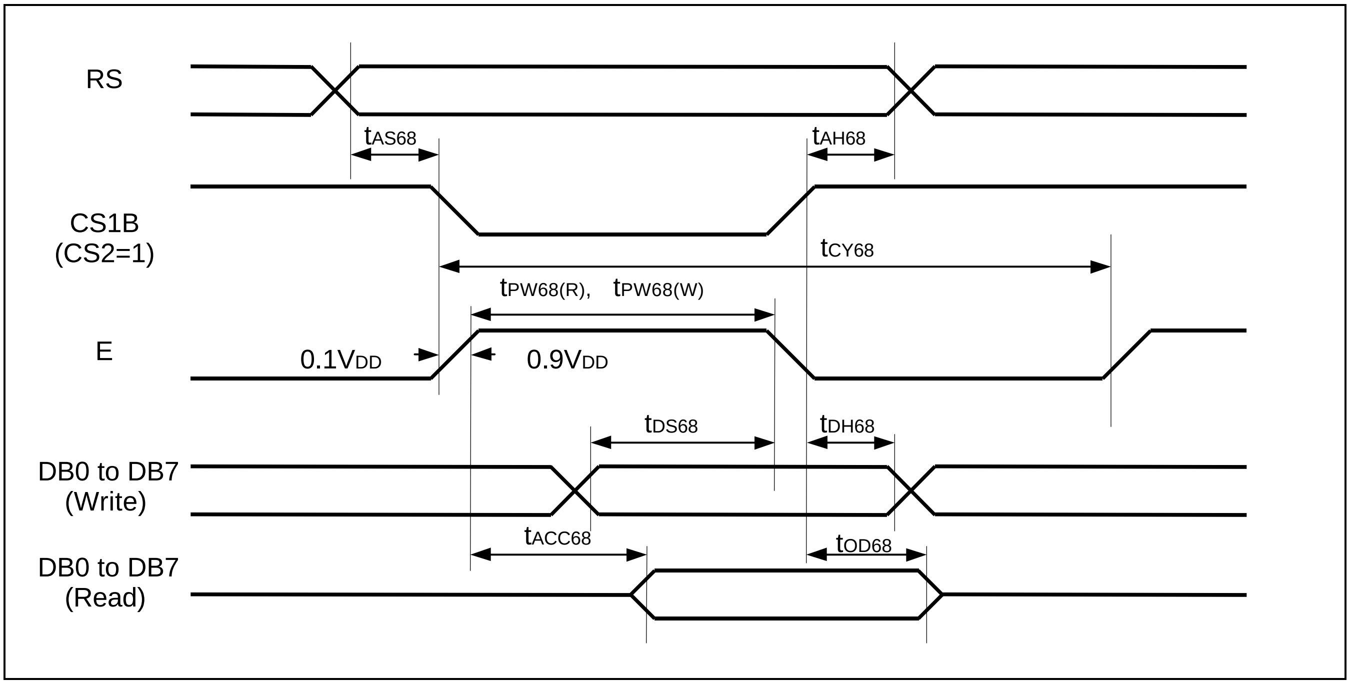


Figure 35. Read/Write Characteristics (6800-series Microprocessor)

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS	T_{AS68} T_{AH68}	13 17	-	-	ns	
System cycle time	RS	T_{CY68}	400	-	-	ns	
Data setup time Data hold time	DB7 to DB0	T_{DS68} T_{DH68}	35 13	-	-	ns	
Access time Output disable time	DB7 to DB0	T_{ACC68} T_{OD68}	- 10	-	125 90	ns	C_L = 100 pF
Enable pulse width: Read Enable pulse width: write	E_RD	T_{PW68} (R) T_{PW68} (W)	125 55	-	-	-	

Serial Interface Characteristics

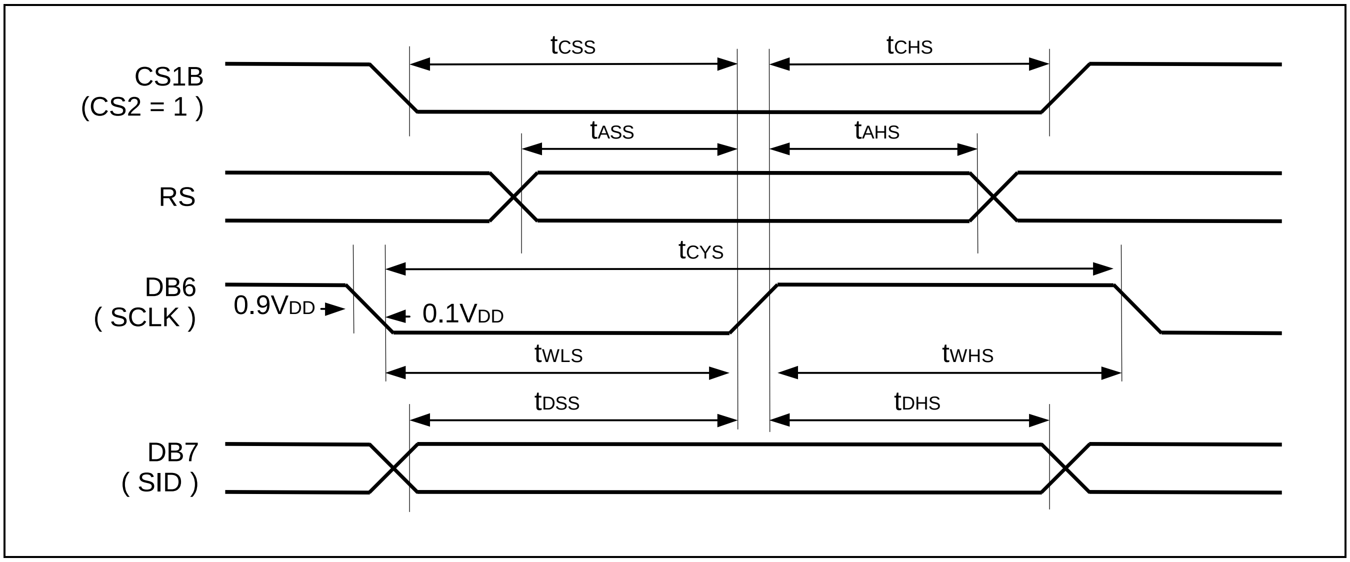


Figure 36. Serial Interface Characteristics

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	t_{CYS} t_{WHS} t_{WLS}	450 180 135	- - -	- - -	ns	
Address setup time Address hold time	RS	t_{ASS} t_{AHS}	90 360	- -	- -	ns	
Data setup time Data hold time	DB7 (SID)	t_{DSS} t_{DHS}	90 90	- -	- -	ns	
CS1B setup time CS1B hold time	CS1B	t_{CSS} t_{CHS}	55 180	- -	- -	ns	

Reset Input Timing

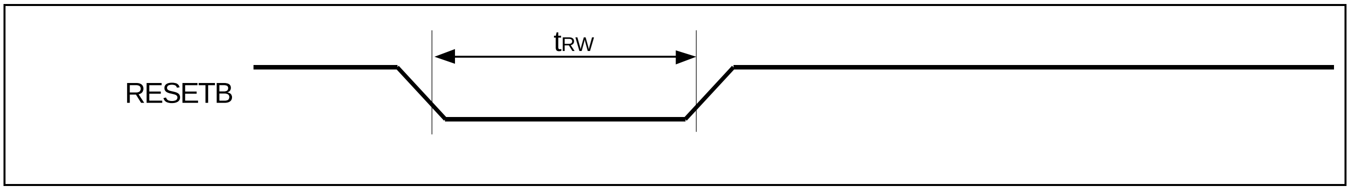


Figure 37. Reset Input Timing

(VDD = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Reset low pulse width	RESETB	tRW	900	-	-	ns	

Display Control Output Timing

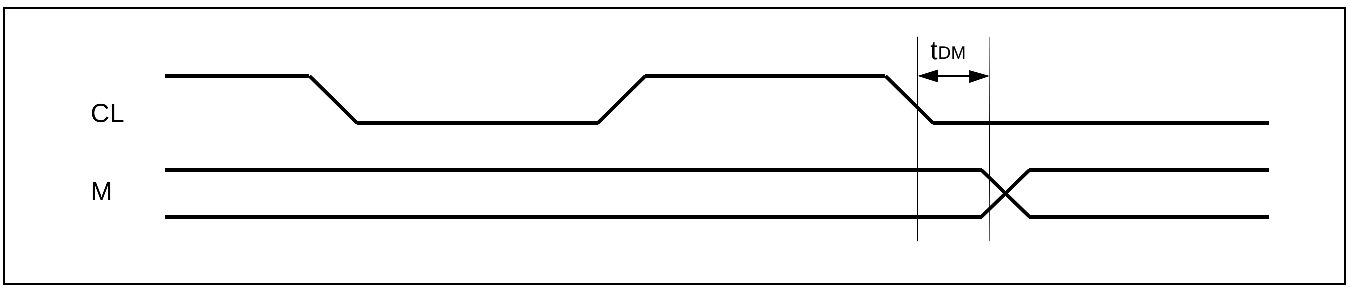


Figure 38. Display Control Output Timing

(VDD = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
M delay time	M	tDM	-	13	70	ns	

REFERENCE APPLICATIONS

MICROPROCESSOR INTERFACE

In Case of Interfacing with 6800-series (PS = “H”, MI = “H”)

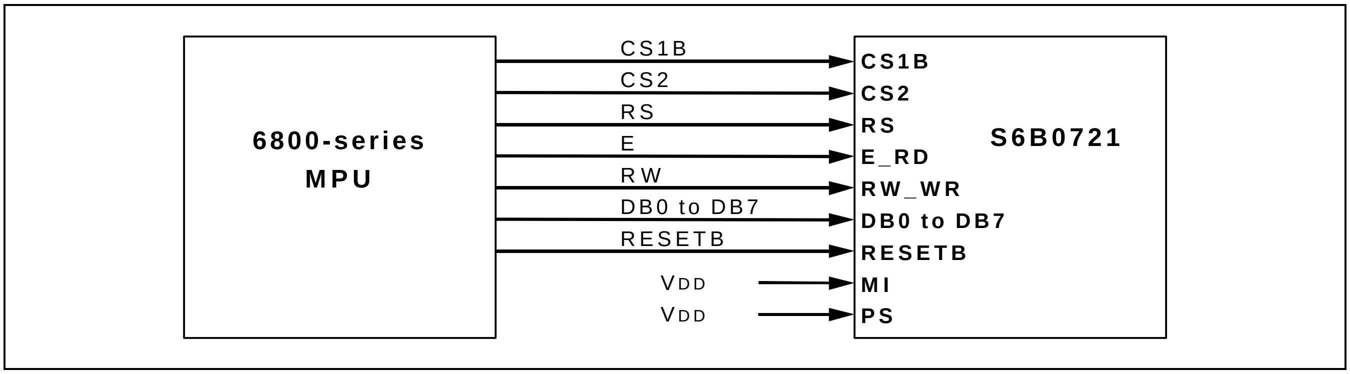


Figure 39. Interfacing with 6800-series (PS = “H”, MI = “H”)

In Case of Interfacing with 8080-series (PS = “H”, MI = “L”)

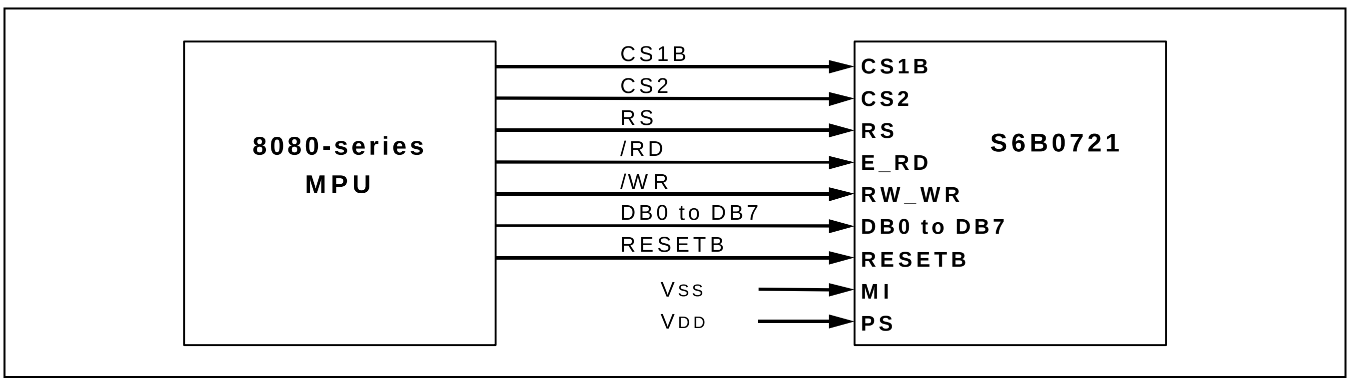


Figure 40. Interfacing with 8080-series (PS = “H”, MI = “L”)

In Case of Serial Interface (PS = “L”, MI = “H/L”)

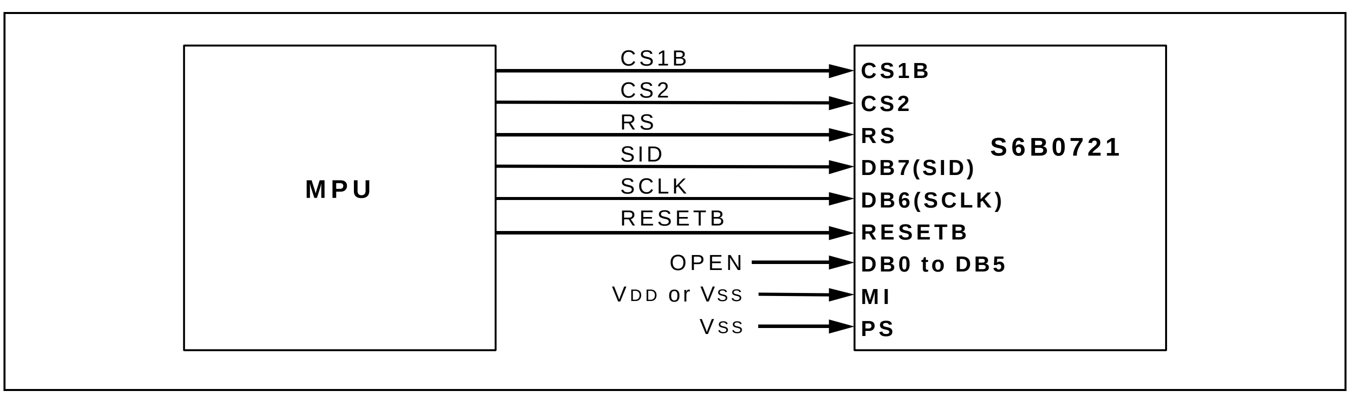


Figure 41. Serial Interface (PS = “L”, MI = “H/L”)

CONNECTIONS BETWEEN S6B0721 AND LCD PANEL

Single Chip Configuration (1/65 Duty Configurations)

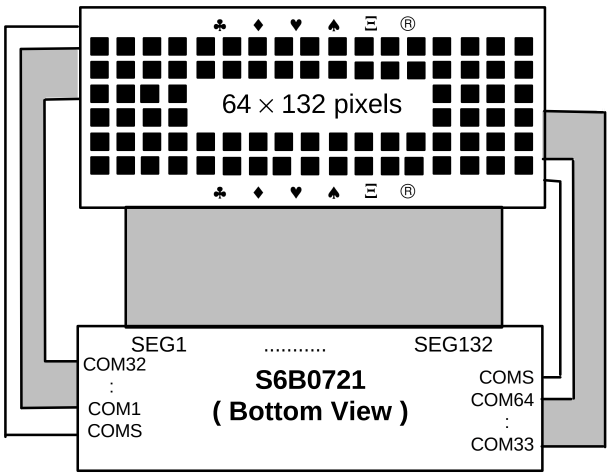


Figure 42. SHL = 0, ADC = 0

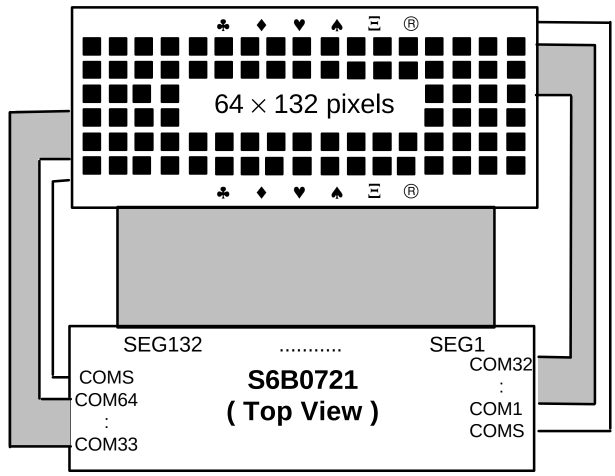


Figure 43. SHL = 0, ADC = 1

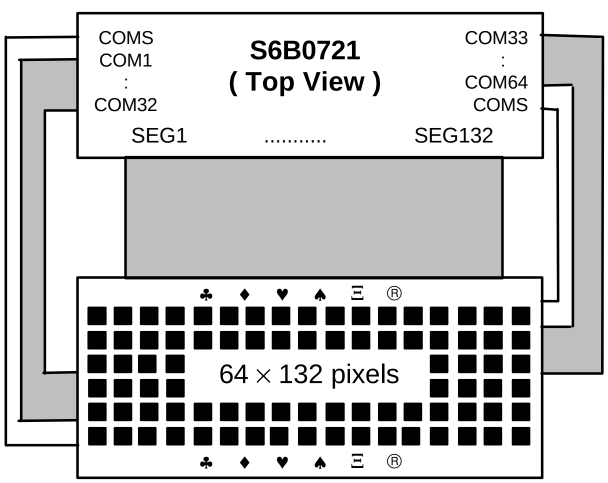


Figure 44. SHL = 1, ADC = 0

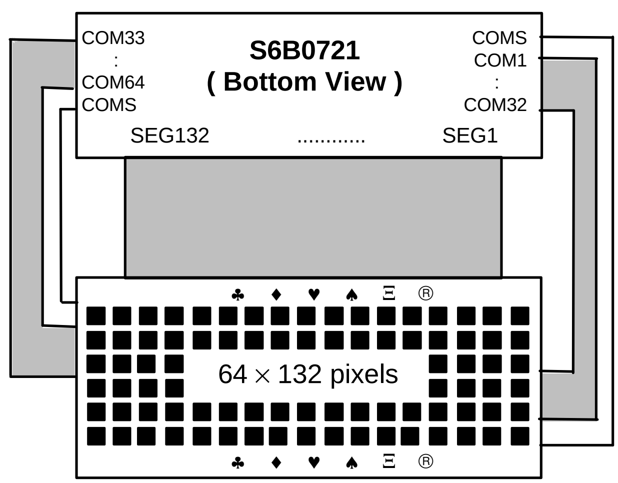


Figure 45. SHL = 1, ADC = 1

Single Chip Configuration (1/49 Duty Configurations)

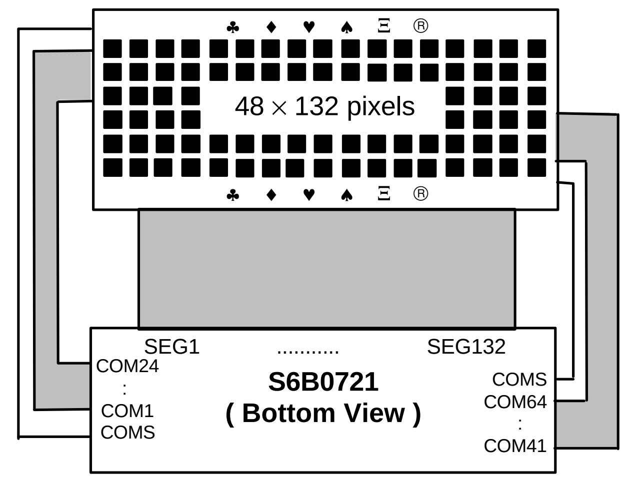


Figure 46. SHL = 0, ADC = 0

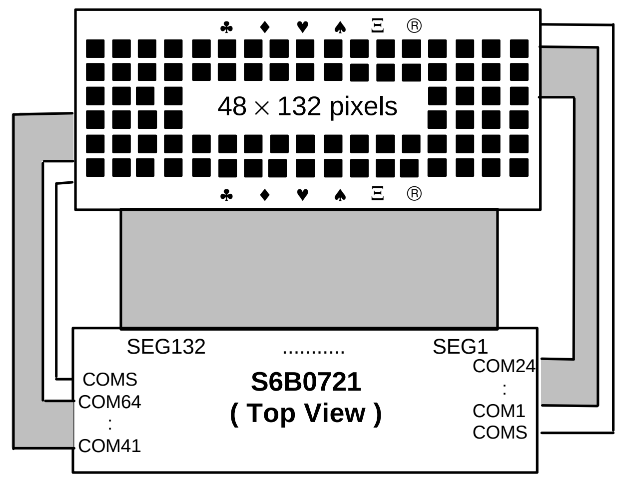


Figure 47. SHL = 0, ADC = 1

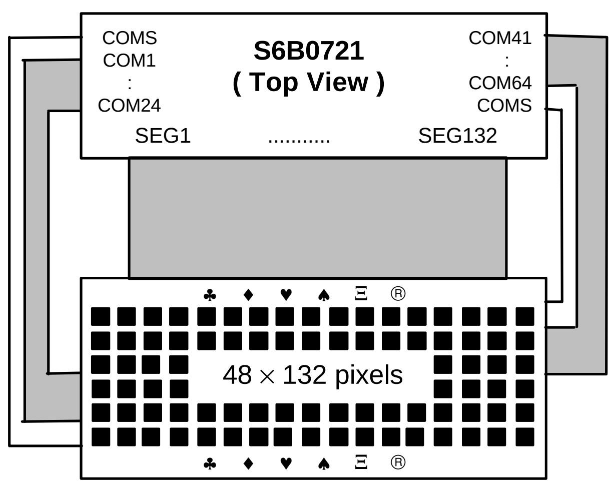


Figure 48. SHL = 1, ADC = 0

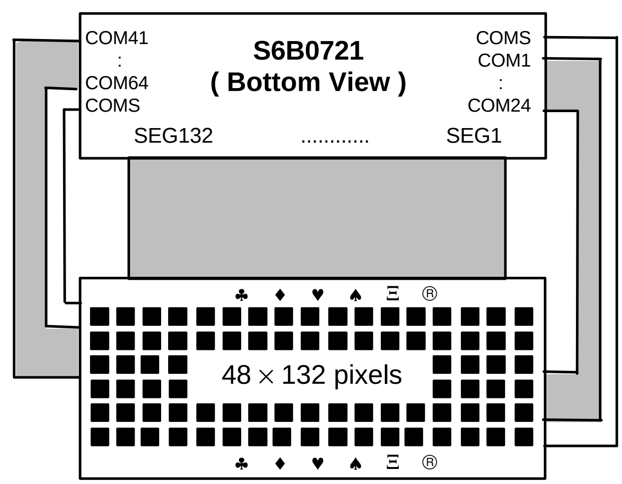


Figure 49. SHL = 1, ADC = 1

Single Chip Configuration (1/33 Duty Configurations)

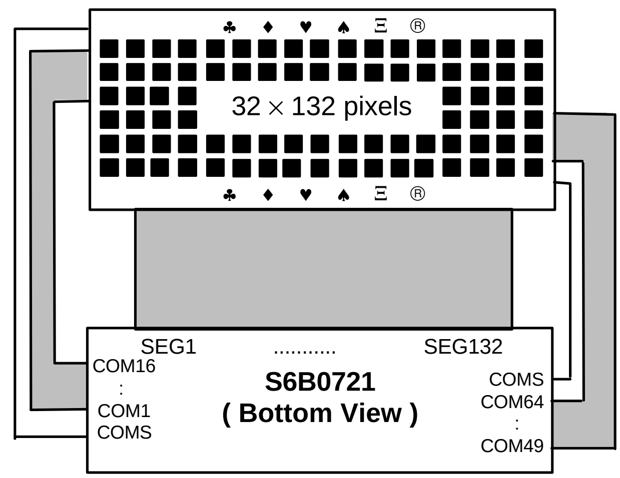


Figure 50. SHL = 0, ADC = 0

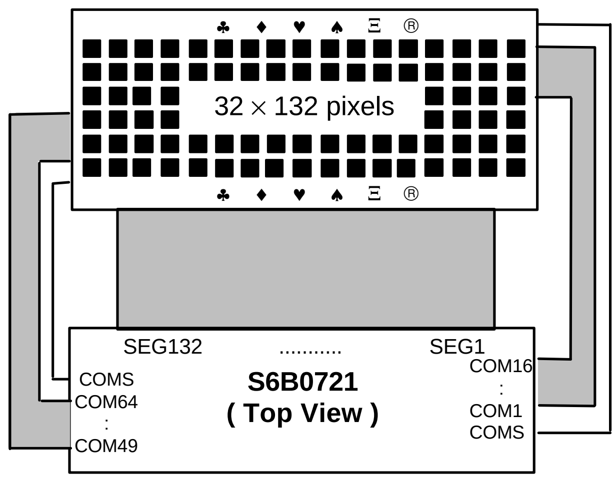


Figure 51. SHL = 0, ADC = 1

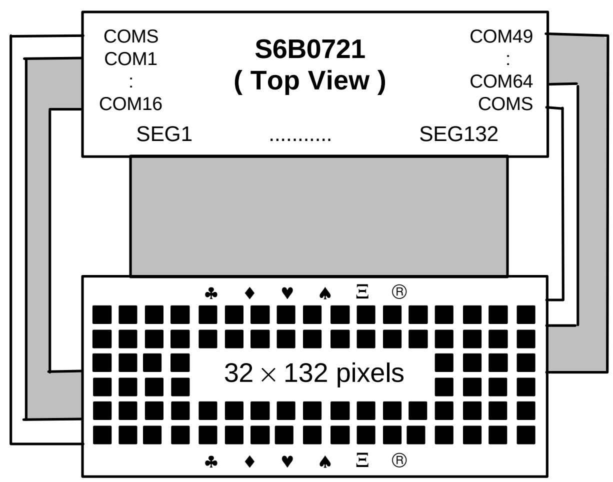


Figure 52. SHL = 1, ADC = 0

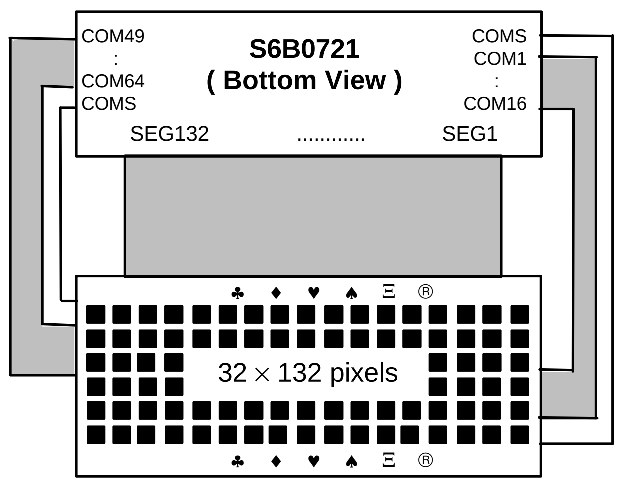


Figure 53. SHL = 1, ADC = 1

Multiple Chip Configuration

- 65COM (64COM + 1COMS) × 264SEG (132SEG × 2)

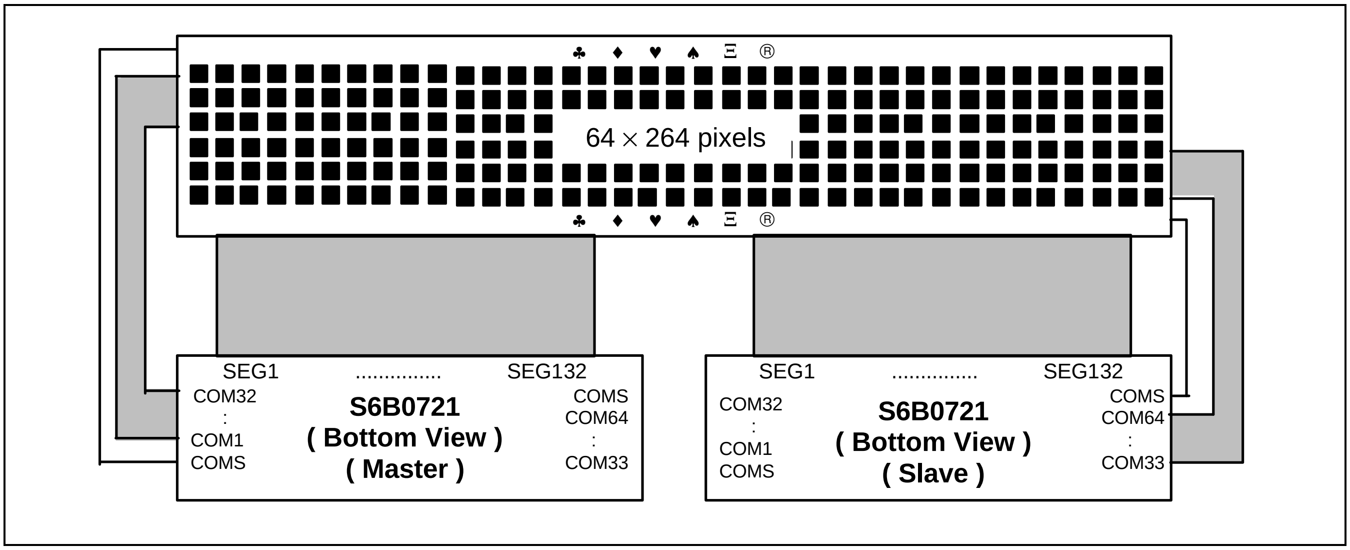


Figure 54. SHL = 0, ADC = 0

♦ Connect the following pins of two chips each other
- Display clock pins: CL, M
- Display control pin: DISP
- LCD power pins: V0, V1, V2, V3, V4

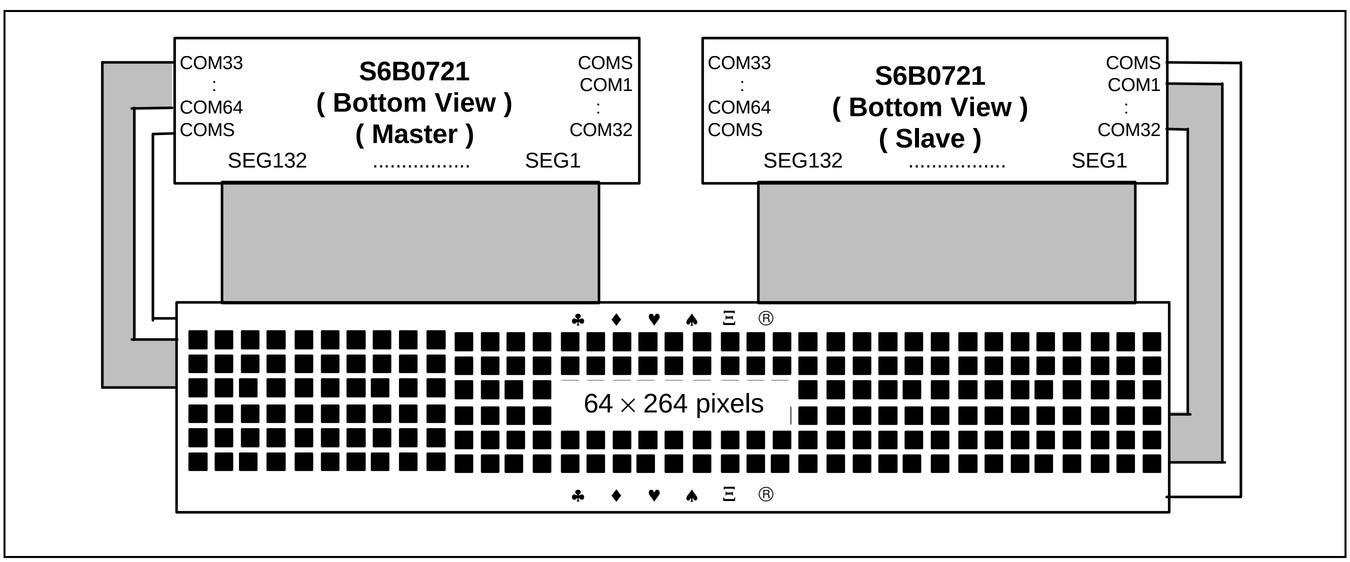


Figure 55. SHL = 1, ADC = 1

♦ Connect the following pins of two chips each other
- Display clock pins: CL, M
- Display control pin: DISP
- LCD power pins: V0, V1, V2, V3, V4

- **130COM (128COM + 2COMS) × 132SEG**

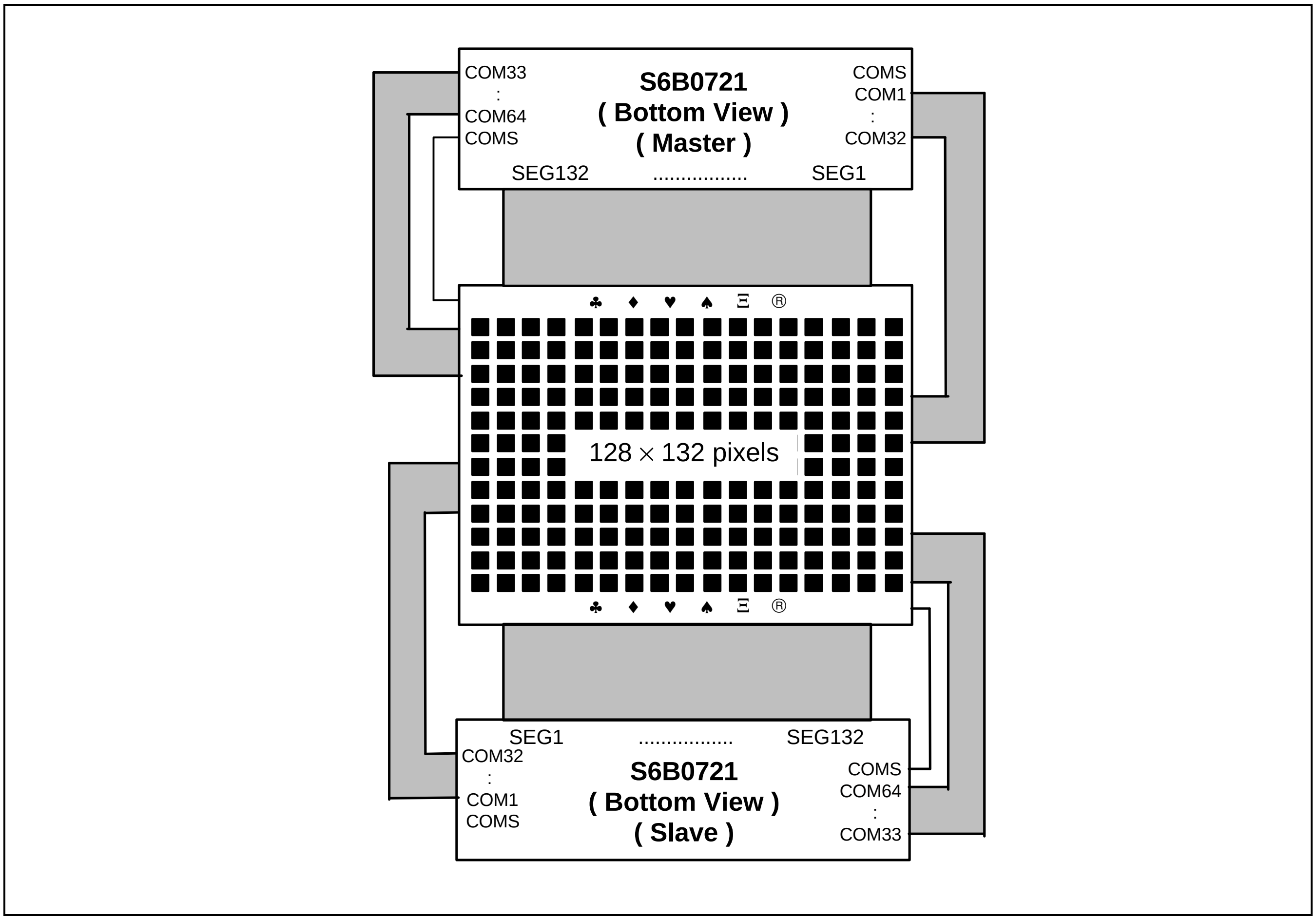


Figure 56. 130COM (128COM + 2COMS) × 132SEG

- Connect the following pins of two chips each other
  - Display clock pins: CL, M
  - Display control pin: DISP
  - LCD power pins: V0, V1, V2, V3, V4

- Common / Segment output direction select
  - Master chip: SHL = 1, ADC = 1
  - Slave chip: SHL = 0, ADC = 0

TCP PIN LAYOUT (SAMPLE)

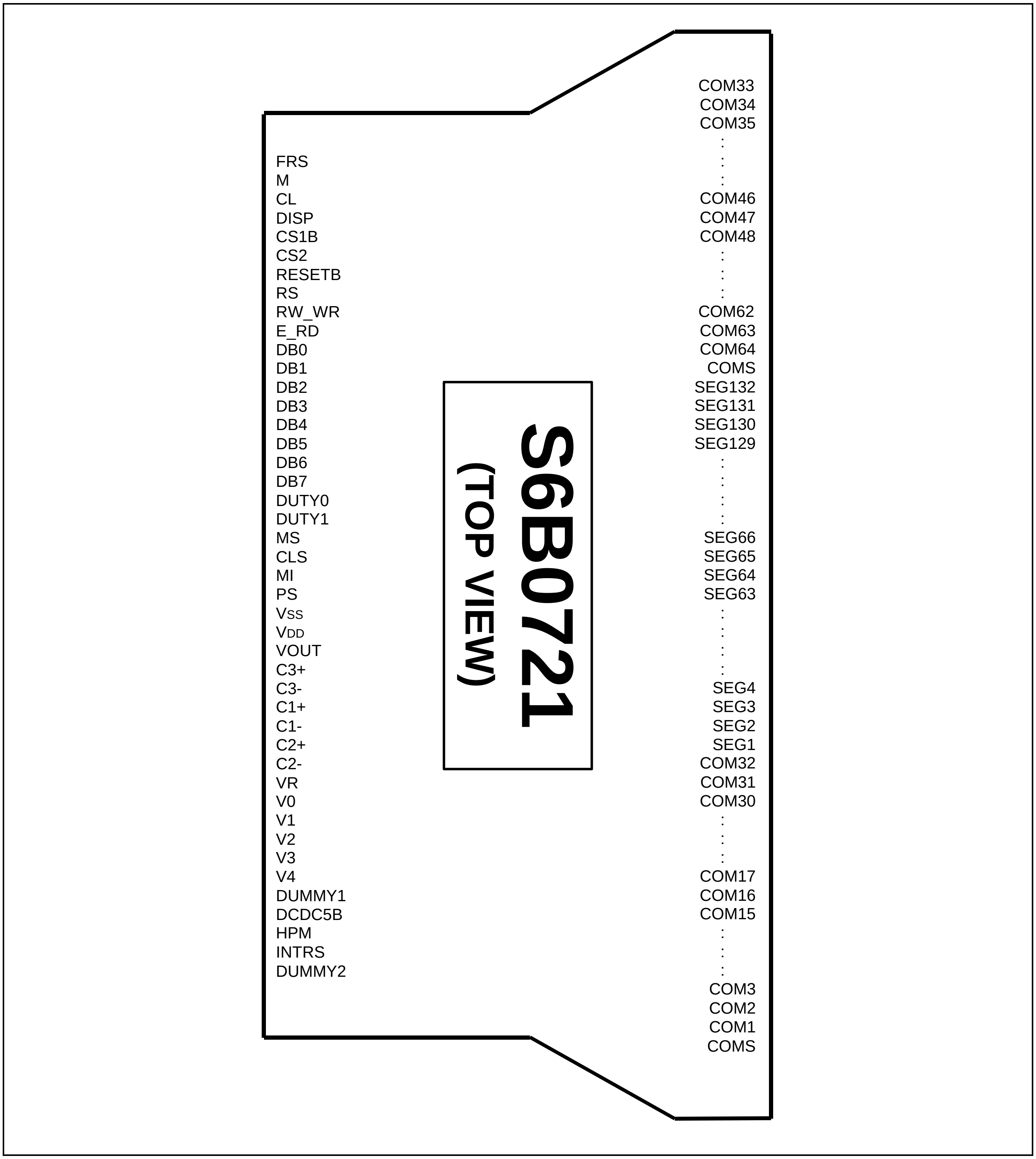


Figure 57. TCP Pin Layout