# S7INS-N MCP Products

## MirrorBit™ 1.8 Volt-only Simultaneous Read/Write, Burst-mode Multiplexed Flash Memory: 256 Mb (16 Mb x 16-bit), 128 Mb (8 Mb x 16-bit) and 64 Mb (4 Mb x 16-bit) with Burst-mode Multiplexed pSRAM: 64 Mb (4 Mb x 16-bit), 32 Mb (2 Mb x 16-bit) and 16 Mb (1 Mb x 16-bit)

*Data Sheet*

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**Publication Number** S7INS-N_00 **Revision** A **Amendment** 3 **Issue Date** October 10, 2006

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# S71NS-N MCP Products

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**ADVANCE INFORMATION**

# General Description

The S71NS-N Series is a product line of stacked Multi-Chip Product (MCP) packages and consists of the following items:

- One or more S29NS-N flash memory die
- Mux burst-mode pSRAM

The products covered by this document are listed in the table below. For details about their specifications, please refer to their individual datasheet for further details.

| | pSRAM | | | |
|---|---|---|---|---|
| | **Density** | **16 Mb** | **32 Mb** | **64 Mb** |
| **Flash** | 64 Mb | S71NS064NA0 | | |
| | 128 Mb | S71NS128NA0 | S71NS128NB0 | S71NS128NC0 |
| | 256 Mb | | S71NS256NB0 | S71NS256NC0 |

# Distinctive Characteristics

### MCP Features

- **Power supply voltage of 1.7 V to 1.95 V**
- **Burst Speed: 66 MHz**
- **Package - MCP BGA: 0.5 mm ball pitch**
  - — 8.0 x 9.2 mm, 56 ball for NS064N and NS128N based MCPs
  - — 10.0 x 11.0 mm, 60 ball for NS256N based MCPs
- **Operating Temperature**
  - — Wireless, –25°C to +85°C

For detailed specifications, please refer to the individual data sheets:

| Document | Publication Identification Number |
|---|---|
| S29NS-N | S29NS-N_00 |
| 16 M Multiplexed pSRAM Type 2 | muxpsram_05 |
| 16 M Multiplexed pSRAM Type 3 | muxpsram_03 |
| 32 M Multiplexed pSRAM Type 3 | muxpsram_04 |
| 64 M Multiplexed pSRAM Type 3 | muxpsram_01 |

# 1 Ordering Information

The ordering part number is formed by a valid combination of the following:

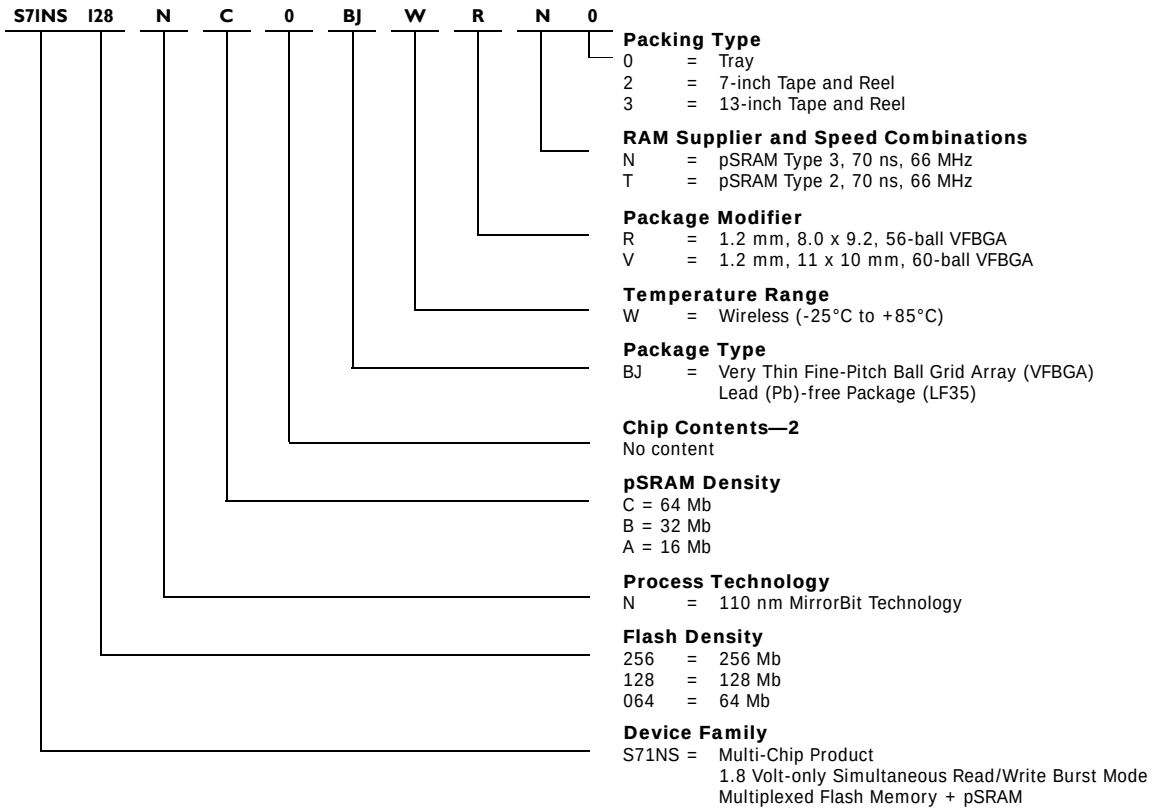



**Table 1.1 MCP Configurations and Valid Combinations**

| Base Ordering Part Number (Note 2) | Package & Temperature | Model Number | Packing Type | pSRAM Type | Flash Speed Options | pSRAM Speed Options |
|---|---|---|---|---|---|---|
| S71NS064NA0 | BJW | RT | 0, 1, 2 | pSRAM Type 2 | 66 MHz | 66 MHz |
| | | RN | | pSRAM Type 3 | 66 MHz | 66 MHz |
| S71NS128NA0 | | RN | | pSRAM Type 3 | 66 MHz | 66 MHz |
| S71NS128NB0 | | RN | | pSRAM Type 3 | 66 MHz | 66 MHz |
| S71NS128NC0 | | RN | | pSRAM Type 3 | 66 MHz | 66 MHz |
| S71NS256NB0 | | VN | | pSRAM Type 3 | 66 MHz | 66 MHz |
| S71NS256NC0 | | VN | | pSRAM Type 3 | 66 MHz | 66 MHz |

***Package Marking Note:***

*The package marking omits the leading* S *from the ordering part number.*

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

# 2 Input/Output Descriptions

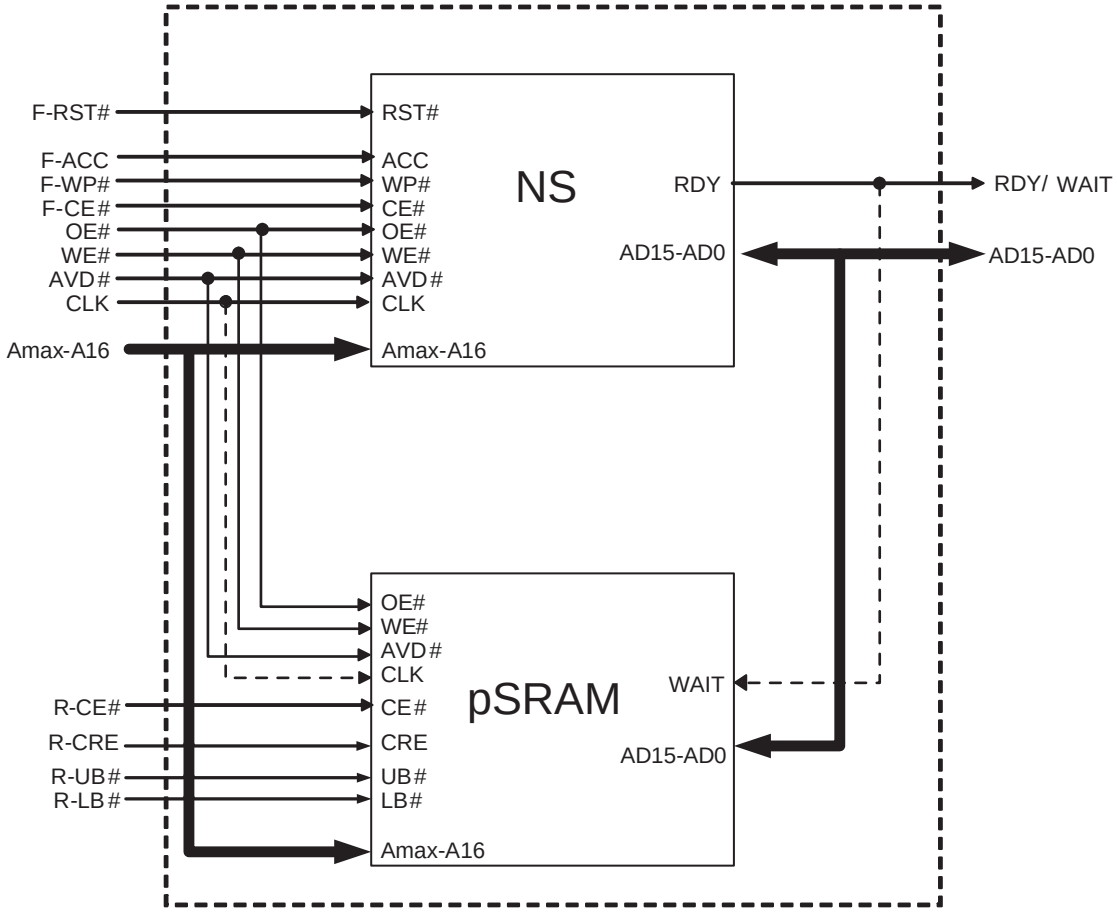
Table 2.1 identifies the input and output package connections provided on the device.

**Table 2.1 Input/Output Descriptions**

| Symbol | Description | Flash | RAM |
|---|---|---|---|
| AMAX – A16 | Address inputs | X | X |
| ADQ15 – ADQ0 | Multiplexed Address/Data | X | X |
| OE# | Output Enable input. Asynchronous relative to CLK for the Burst mode. | X | X |
| WE# | Write Enable input. | X | X |
| $V_{SS}$ | Ground | X | X |
| NC | No Connect; not connected internally | X | X |
| RDY | Ready output. Indicates the status of the Burst read. The WAIT# pin of the pSRAM is tied to RDY. | X | X |
| CLK | Clock input. In burst mode, after the initial word is output, subsequent active edges of CLK increment the internal address counter. Should be at $V_{IL}$ or $V_{IH}$ while in asynchronous mode | X | X |
| AVD# | Address Valid input. Indicates to device that the valid address is present on the address inputs.<br>Low = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched.<br>High = device ignores address inputs | X | X |
| F-RST# | Hardware reset input. Low = device resets and returns to reading array data | X | |
| F-WP# | Hardware write protect input. At $V_{IL}$, disables program and erase functions in the four outermost sectors. Should be at $V_{IH}$ for all other conditions. | X | |
| F-ACC | Accelerated input. At $V_{HH}$, accelerates programming; automatically places device in unlock bypass mode. At $V_{IL}$, disables all program and erase functions. Should be at $V_{IH}$ for all other conditions. | X | |
| R-CE1# | Chip-enable input for pSRAM. | | X |
| F-CE# | Chip-enable input for Flash. Asynchronous relative to CLK for Burst Mode. | X | |
| R-CRE | Control Register Enable (pSRAM). | | X |
| F-VCC | Flash 1.8 Volt-only single power supply. | X | |
| R-VCC | pSRAM Power Supply. | | X |
| R-UB# | Upper Byte Control (pSRAM). | | X |
| R-LB# | Lower Byte Control (pSRAM) | | X |
| DNU | Do Not Use | | |

# 3 MCP Block Diagram

**Figure 3.1 MCP Block Diagram**




***Note:*** *The CLK and WAIT signals on the pSRAM are not present on the pSRAM Type 2; therefore, for those MCP's, those signals will only be connected to the NS flash, but not to the pSRAM. Also, on this pSRAM, the CRE signal will not be present at all.*

# 4 Connection Diagrams/Physical Dimensions

This section contains the I/O designations and package specifications for the S71NS-N.

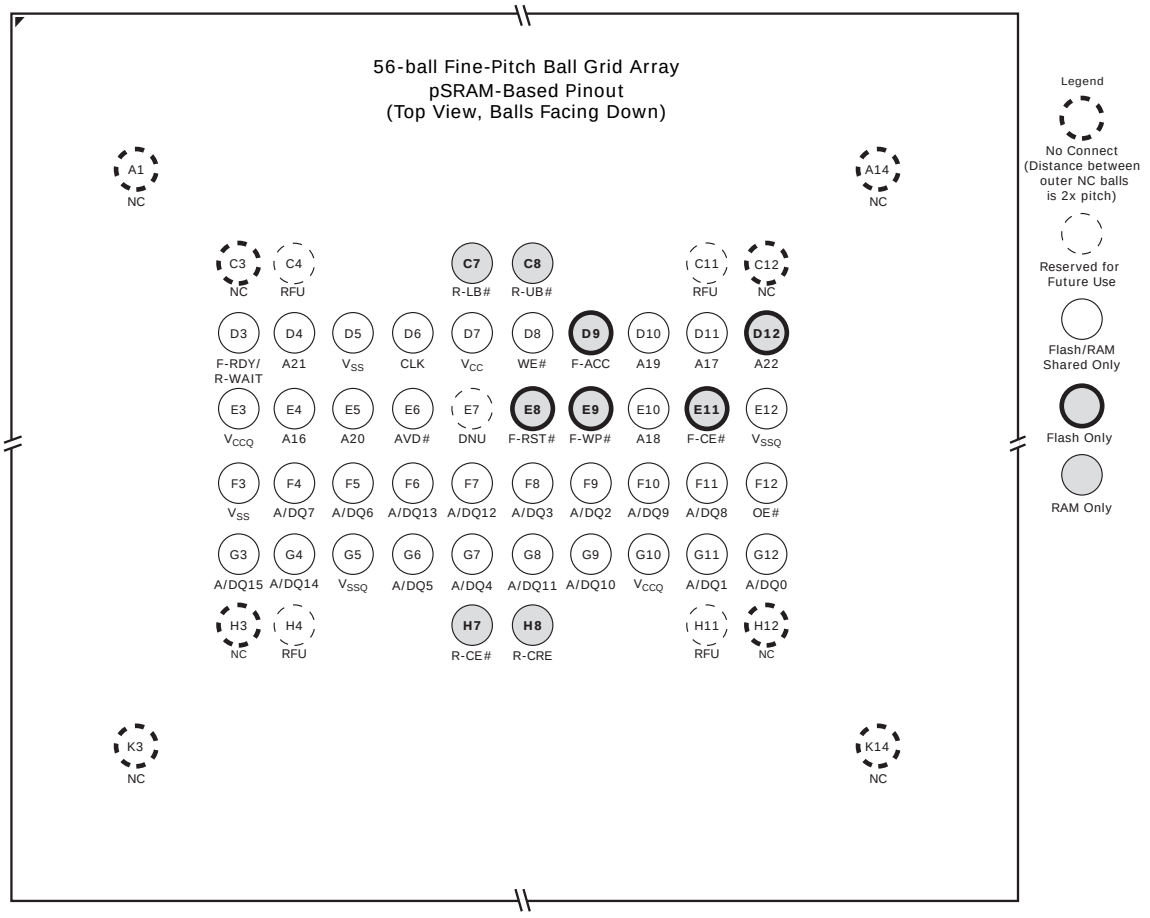
## 4.1 Special Handling Instructions for FBGA Packages

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

## 4.2 Connection Diagrams

### 4.2.1 pSRAM Based Pinout, 56-Ball, VFBGA



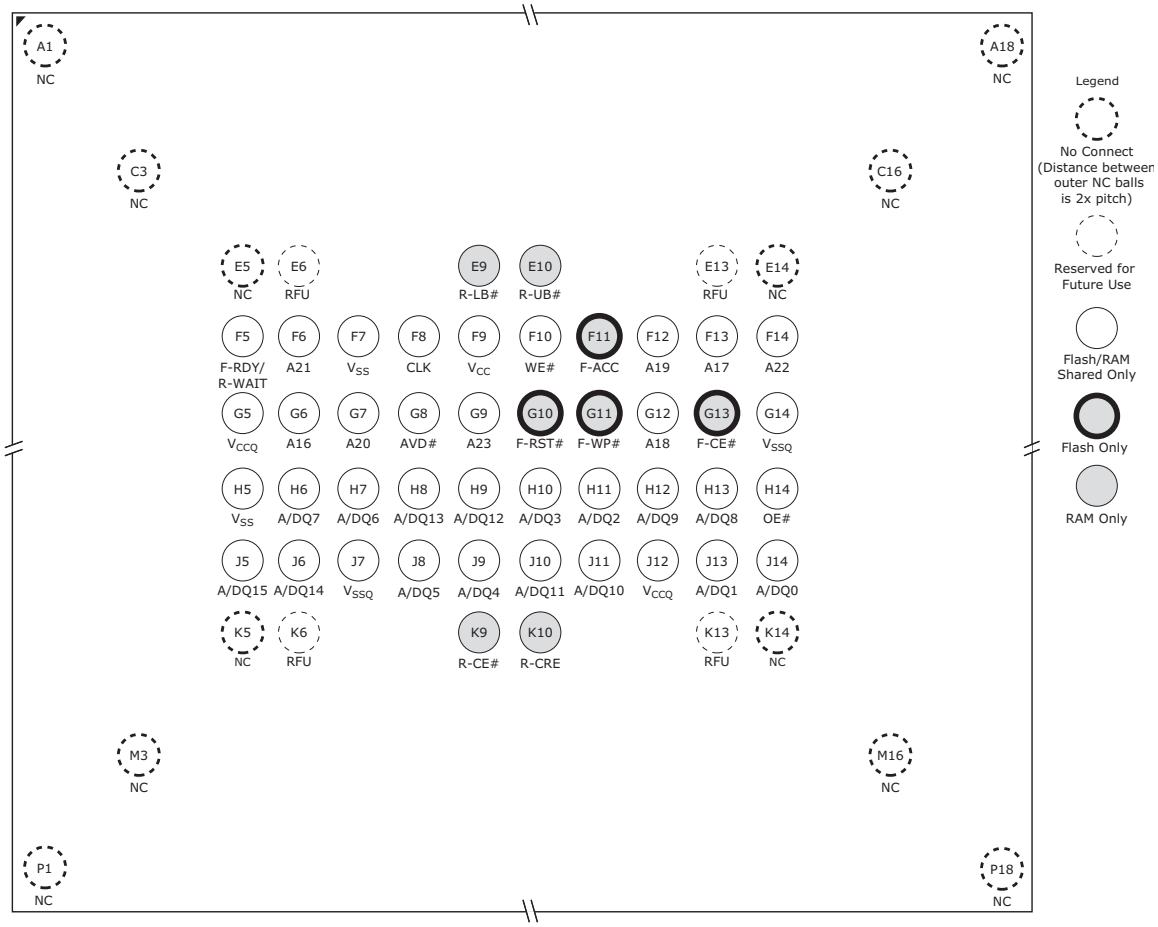

***Notes:***

1. *Addresses are shared between Flash and RAM depending on the density of the pSRAM.*
2. *CLK and WAIT signals are Flash only for the S71NS064NA0-RT, while on that MCP, the CRE signal won't exist.*

| MCP | Flash-Only Addresses | Shared Addresses | Shared ADQ Pins |
|---|---|---|---|
| S71NS128NC0 | A22 | A21-A16 | ADQ15 – ADQ0 |
| S71NS128NB0 | A22-A21 | A20-A16 | ADQ15 – ADQ0 |
| S71NS128NA0 | A22-A20 | A19-A16 | ADQ15 – ADQ0 |
| S71NS064NA0 | A21-A20 | A19-A16 | ADQ15 – ADQ0 |

**Figure 4.1 pSRAM Based Pinout, 56-Ball, VFBGA**

### 4.2.2 pSRAM Based Pinout, 60-Ball, VFBGA




***Note:*** *Addresses are shared between Flash and RAM depending on the density of the pSRAM.*

| MCP | Flash-Only Addresses | Shared Addresses | Shared ADQ Pins |
|---|---|---|---|
| S71NS256NC0 | A23-A22 | A21–A16 | ADQ15 – ADQ0 |
| S71NS256NB0 | A23-A21 | A20-A16 | ADQ15 – ADQ0 |

**Figure 4.2 pSRAM Based Pinout, 60-Ball, VFBGA**

### 4.2.3 Look Ahead Connection Diagram
### 112-ball x16 MUX NOR Flash + x16 MUX pSRAM on Shared Bus and x16 NAND Interface ORNAND on Bus 2

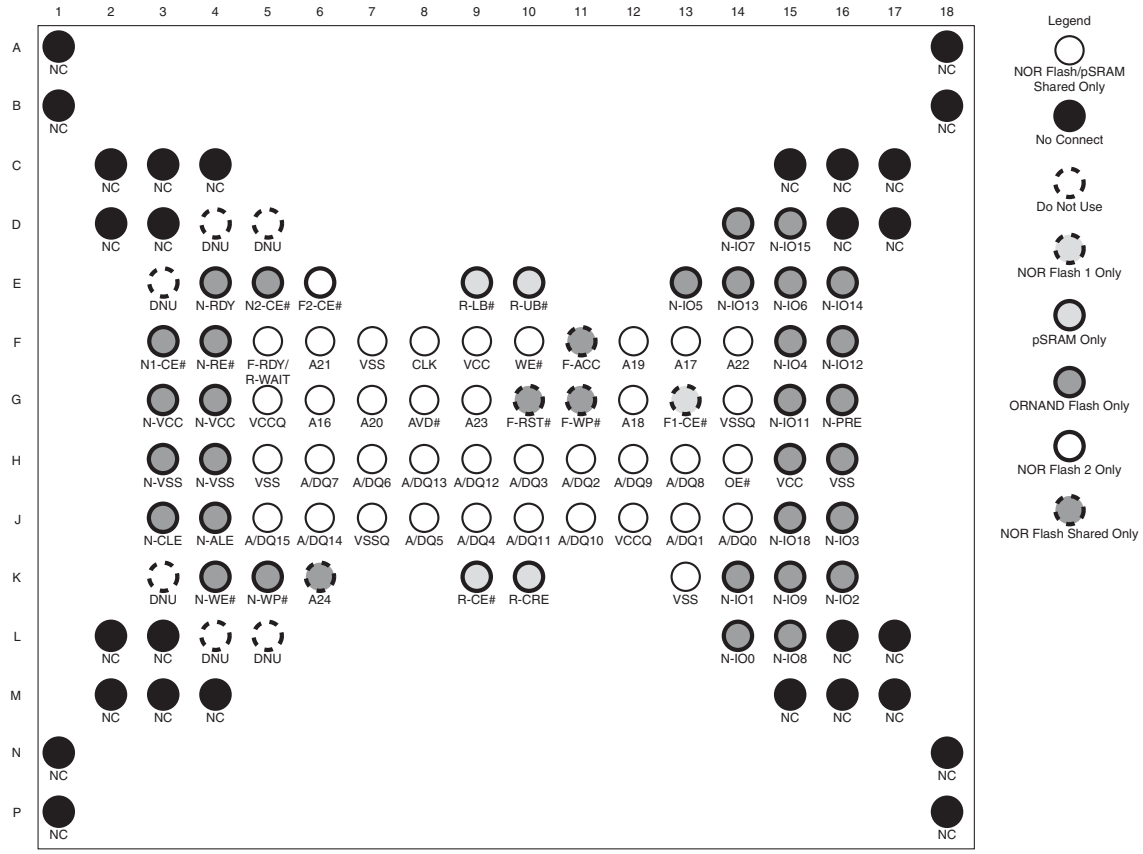
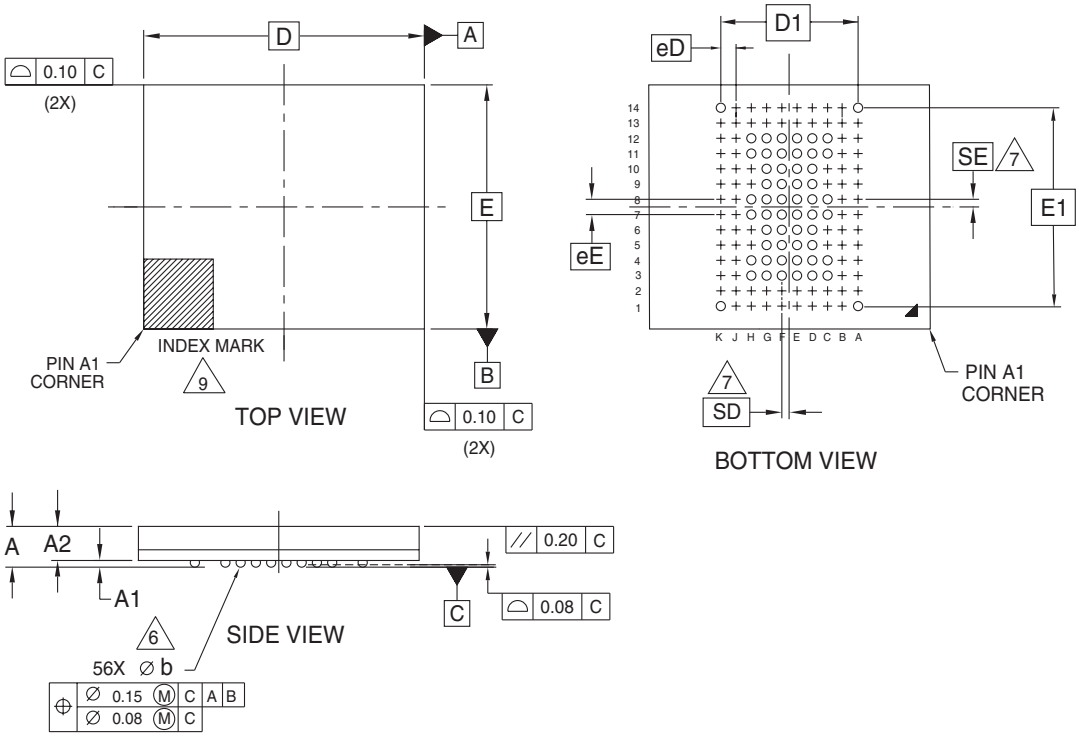



**Figure 4.3 Look Ahead Connection Diagram**
**112-ball x16 MUX NOR Flash + x16 MUX pSRAM on Shared Bus and x16 NAND Interface ORNAND on Bus 2**

## 4.3 Physical Dimensions

### 4.3.1 NLB056—9.2 x 8.0 mm, 56-ball VFBGA




| PACKAGE | NLB 056 | | | |
|---|---|---|---|---|
| JEDEC | N/A | | | |
| D x E | 9.20 mm x 8.00 mm PACKAGE | | | |
| SYMBOL | MIN | NOM | MAX | NOTE |
| A | --- | --- | 1.20 | PROFILE |
| A1 | 0.20 | --- | --- | BALL HEIGHT |
| A2 | 0.85 | --- | 0.97 | BODY THICKNESS |
| D | | 9.20 BSC. | | BODY SIZE |
| E | | 8.00 BSC. | | BODY SIZE |
| D1 | | 4.50 BSC. | | MATRIX FOOTPRINT |
| E1 | | 6.50 BSC. | | MATRIX FOOTPRINT |
| MD | | 10 | | MATRIX SIZE D DIRECTION |
| ME | | 14 | | MATRIX SIZE E DIRECTION |
| n | | 56 | | BALL COUNT |
| Øb | 0.25 | 0.30 | 0.35 | BALL DIAMETER |
| eE | | 0.50 BSC. | | BALL PITCH |
| eD | | 0.50 BSC | | BALL PITCH |
| SD / SE | | 0.25 BSC. | | SOLDER BALL PLACEMENT |
| | A2 – A13,B1 – B14 C1,C2,C5,C6,C9,C10,C13,C14 D1,D2,D13,D14,E1,E2,E13,E14,F1,F2,F13,F14 G1,G2,G13,G14,H1,H2,H5,H6,H9,H10,H13,H14 J1 – J14, K2 – K13 | | | DEPOPULATED SOLDER BALLS |

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. OUTLINE AND DIMENSIONS PER CUSTOMER REQUIREMENT.

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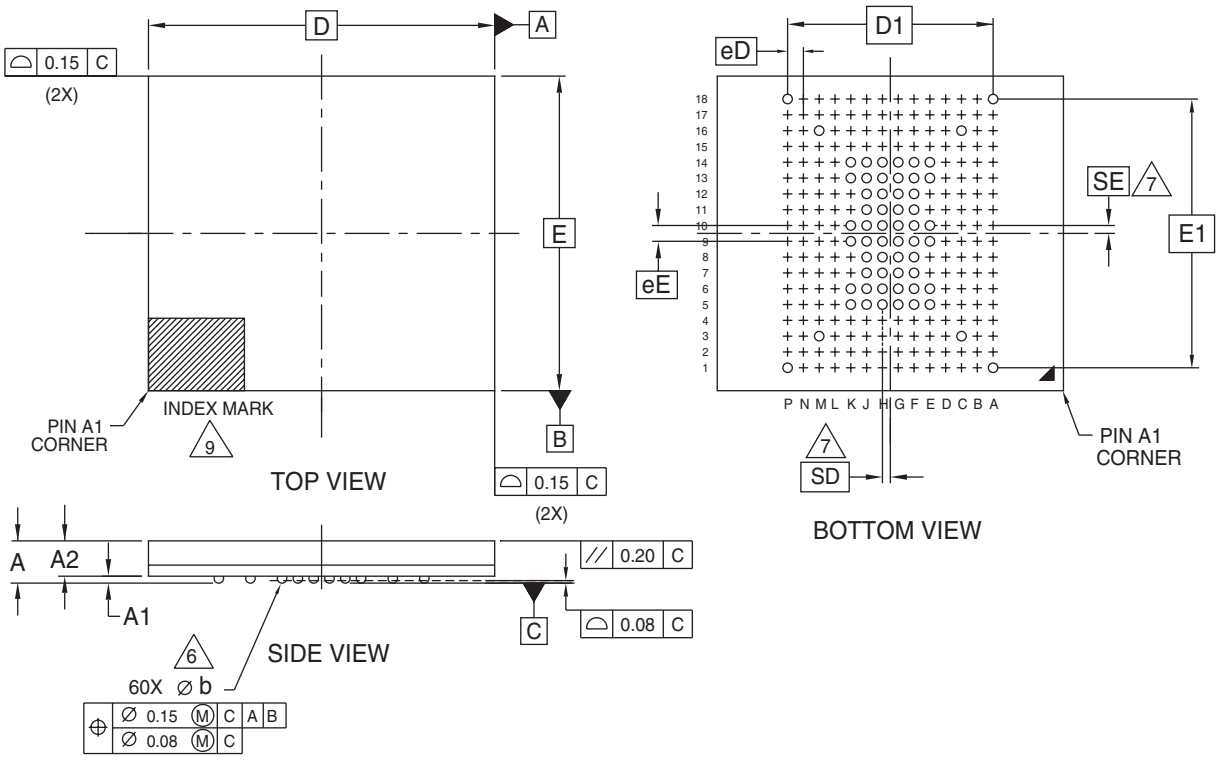
**Figure 4.4 Physical Dimensions, NLB056—56-ball VFBGA**

### 4.3.1 NLA060—11.0 x 10.0 mm, 60-ball VFBGA




| PACKAGE | NLA 060 | | | |
|---|---|---|---|---|
| JEDEC | N/A | | | |
| D x E | 10.95 mm x 9.95 mm PACKAGE | | | |
| SYMBOL | MIN | NOM | MAX | NOTE |
| A | --- | --- | 1.20 | PROFILE |
| A1 | 0.20 | --- | --- | BALL HEIGHT |
| A2 | 0.85 | --- | 0.97 | BODY THICKNESS |
| D | | 10.95 BSC. | | BODY SIZE |
| E | | 9.95 BSC. | | BODY SIZE |
| D1 | | 6.50 BSC. | | MATRIX FOOTPRINT |
| E1 | | 8.50 BSC. | | MATRIX FOOTPRINT |
| MD | | 14 | | MATRIX SIZE D DIRECTION |
| ME | | 18 | | MATRIX SIZE E DIRECTION |
| n | | 60 | | BALL COUNT |
| Øb | 0.25 | 0.30 | 0.35 | BALL DIAMETER |
| eE | | 0.50 BSC. | | BALL PITCH |
| eD | | 0.50 BSC | | BALL PITCH |
| SD / SE | | 0.25 BSC. | | SOLDER BALL PLACEMENT |
| | A2–A17,B1–B18,C1,C2,C4–C15,C17,C18 D1–D18,E1,E2,E3,E4,E7,E8,E11,E12,E15,E16,E17,E18 F1,F2,F3,F4,F15,F16,F17,F18,G1,G2,G3,G4,G15,G16,G17,G18 H1,H2,H3,H4,H15,H16,H17,H18,J1,J2,J3,J4,J15,J16,J17,J18 K1,K2,K3,K4,K7,K8,K11,K12,K15,K16,K17,K18 L1 –L18,M1,M2,M4–M15,M17,M18,N1–N18,P2–P17 | | | DEPOPULATED SOLDER BALLS |

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

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9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. OUTLINE AND DIMENSIONS PER CUSTOMER REQUIREMENT.

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**Figure 4.5 Physical Dimensions, NLA060—60-ball VFBGA**

# 5 Revisions

## Revision A0 (January 3, 2006)

Initial Release under Publication Identification Number S71NS128NC0_01

## Revision A1 (March 1, 2006)

Changed the Publication Identification Number from S71NS128NC0_01 to S71NS-N_00

Added the MCP S71NS064NA0

## Revision A2 (June 13, 2006)

Corrected the grid reference for 56-ball connection diagram

## Revision A3 (October 10, 2006)

Added the S71NS064NA0-RT - the one using pSRAM Type 2