# **S7INS-N MCP Products**

MirrorBit<sup>™</sup> I.8 Volt-only Simultaneous Read/Write, Burst-mode Multiplexed Flash Memory: 256 Mb (I6 Mb x I6-bit), I28 Mb (8 Mb x I6-bit) and 64 Mb (4 Mb x I6-bit) with Burst-mode Multiplexed pSRAM: 64 Mb (4 Mb x I6-bit), 32 Mb (2 Mb x I6-bit) and I6 Mb (I Mb x I6-bit)



Data Sheet ADVANCE INFORMATION

**Notice to Readers:** The Advance Information status indicates that this document contains information on one or more products under development at Spansion Inc. The information is intended to help you evaluate this product. Do not design in this product without contacting the factory. Spansion Inc. reserves the right to change or discontinue work on this proposed product without notice.



# **Notice On Data Sheet Designations**

Spansion Inc. issues data sheets with Advance Information or Preliminary designations to advise readers of product information or intended specifications throughout the product life cycle, including development, qualification, initial production, and full production. In all cases, however, readers are encouraged to verify that they have the latest information before finalizing their design. The following descriptions of Spansion data sheet designations are presented here to highlight their presence and definitions.

#### **Advance Information**

The Advance Information designation indicates that Spansion Inc. is developing one or more specific products, but has not committed any design to production. Information presented in a document with this designation is likely to change, and in some cases, development on the product may discontinue. Spansion Inc. therefore places the following conditions upon Advance Information content:

"This document contains information on one or more products under development at Spansion Inc. The information is intended to help you evaluate this product. Do not design in this product without contacting the factory. Spansion Inc. reserves the right to change or discontinue work on this proposed product without notice."

#### Preliminary

The Preliminary designation indicates that the product development has progressed such that a commitment to production has taken place. This designation covers several aspects of the product life cycle, including product qualification, initial production, and the subsequent phases in the manufacturing process that occur before full production is achieved. Changes to the technical specifications presented in a Preliminary document should be expected while keeping these aspects of production under consideration. Spansion places the following conditions upon Preliminary content:

"This document states the current technical specifications regarding the Spansion product(s) described herein. The Preliminary status of this document indicates that product qualification has been completed, and that initial production has begun. Due to the phases of the manufacturing process that require maintaining efficiency and quality, this document may be revised by subsequent versions or modifications due to changes in technical specifications."

#### Combination

Some data sheets will contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document will distinguish these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with DC Characteristics table and AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

#### Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or  $V_{\text{IO}}$  range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion Inc. applies the following conditions to documents in this category:

"This document states the current technical specifications regarding the Spansion product(s) described herein. Spansion Inc. deems the products to have been in sufficient production volume such that subsequent versions of this document are not expected to change. However, typographical or specification corrections, or modifications to the valid combinations offered may occur."

Questions regarding these document designations may be directed to your local AMD or Fujitsu sales office.

ii S7INS-N 00 A3 October 10, 2006

# S7INS-N MCP Products

MirrorBit<sup>™</sup> I.8 Volt-only Simultaneous Read/Write, Burst-mode Multiplexed Flash Memory: 256 Mb (I6 Mb x I6-bit), I28 Mb (8 Mb x I6-bit) and 64 Mb (4 Mb x I6-bit) with Burst-mode Multiplexed pSRAM: 64 Mb (4 Mb x I6-bit), 32 Mb (2 Mb x I6-bit) and I6 Mb (I Mb x I6-bit)



ADVANCE INFORMATION

# **General Description**

The S71NS-N Series is a product line of stacked Multi-Chip Product (MCP) packages and consists of the following items:

- One or more S29NS-N flash memory die
- Mux burst-mode pSRAM

The products covered by this document are listed in the table below. For details about their specifications, please refer to their individual datasheet for further details.

	pSRAM					
	Density	l6 Mb	32 Mb	64 Mb		
	64 Mb	S71NS064NA0				
Flash 128 Mb		S71NS128NA0	S71NS128NB0	S71NS128NC0		
	256 Mb		S71NS256NB0	S71NS256NC0		

# **Distinctive Characteristics**

**MCP Features** 

- Power supply voltage of 1.7 V to 1.95 V
- Burst Speed: 66 MHz
- Package MCP BGA: 0.5 mm ball pitch
  - 8.0 x 9.2 mm, 56 ball for NS064N and NS128N based MCPs
  - 10.0 x 11.0 mm, 60 ball for NS256N based MCPs
- Operating Temperature
  - Wireless, -25°C to +85°C

For detailed specifications, please refer to the individual data sheets:

Document	Publication Identification Number
S29NS-N	S29NS-N_00
16 M Multiplexed pSRAM Type 2	muxpsram_05
16 M Multiplexed pSRAM Type 3	muxpsram_03
32 M Multiplexed pSRAM Type 3	muxpsram_04
64 M Multiplexed pSRAM Type 3	muxpsram_01



# I Ordering Information

The ordering part number is formed by a valid combination of the following:

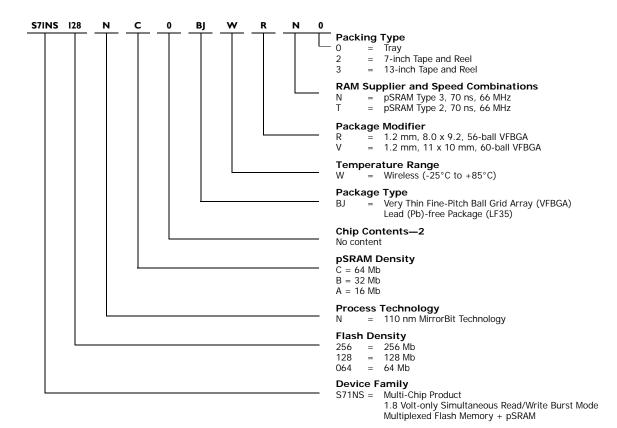


Table I.I MCP Configurations and Valid Combinations

Base Ordering Part Number (Note 2)	Package & Temperature	Model Number	Packing Type	pSRAM Type	Flash Speed Options	pSRAM Speed Options
S71NS064NA0		RT		pSRAM Type 2	66 MHz	66 MHz
37 TN3004NA0		RN		pSRAM Type 3	66 MHz	66 MHz
S71NS128NA0	BJW	RN		pSRAM Type 3	66 MHz	66 MHz
S71NS128NB0		RN	0, 1, 2	pSRAM Type 3	66 MHz	66 MHz
S71NS128NC0		RN		pSRAM Type 3	66 MHz	66 MHz
S71NS256NB0		VN		pSRAM Type 3	66 MHz	66 MHz
S71NS256NC0		VN		pSRAM Type 3	66 MHz	66 MHz

#### Package Marking Note:

The package marking omits the leading S from the ordering part number.

#### **Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

2 S7INS-N MCP Products 57INS-N 00 A3 October 10, 2006



# 2 Input/Output Descriptions

Table 2.1 identifies the input and output package connections provided on the device.

**Table 2.1 Input/Output Descriptions** 

Symbol	Description	Flash	RAM	
AMAX – A16	Address inputs	Χ	Х	
ADQ15 – ADQ0	Multiplexed Address/Data	Х	Х	
OE#	Output Enable input. Asynchronous relative to CLK for the Burst mode.	Х	Х	
WE#	Write Enable input.	Х	Х	
$V_{SS}$	Ground	Χ	Х	
NC	No Connect; not connected internally	Χ	Х	
RDY	Ready output. Indicates the status of the Burst read. The WAIT# pin of the pSRAM is tied to RDY.	Х	Х	
CLK	Clock input. In burst mode, after the initial word is output, subsequent active edges of CLK increment the internal address counter. Should be at $V_{\rm IL}$ or $V_{\rm IH}$ while in asynchronous mode	Х	Х	
AVD#	Address Valid input. Indicates to device that the valid address is present on the address inputs.  Low = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched.  High = device ignores address inputs	Х	Х	
F-RST#	Hardware reset input. Low = device resets and returns to reading array data	Х		
F-WP#	Hardware write protect input. At $V_{\rm IL}$ , disables program and erase functions in the four outermost sectors. Should be at $V_{\rm IH}$ for all other conditions.	Х		
F-ACC	Accelerated input. At $V_{HH}$ , accelerates programming; automatically places device in unlock bypass mode. At $V_{IL}$ , disables all program and erase functions. Should be at $V_{IH}$ for all other conditions.			
R-CE1#	Chip-enable input for pSRAM.		Х	
F-CE#	Chip-enable input for Flash. Asynchronous relative to CLK for Burst Mode.	Χ		
R-CRE	Control Register Enable (pSRAM).		Х	
F-VCC	Flash 1.8 Volt-only single power supply.			
R-VCC	pSRAM Power Supply.		Х	
R-UB#	Upper Byte Control (pSRAM).		Х	
R-LB#	Lower Byte Control (pSRAM)		Х	
DNU	Do Not Use			



# 3 MCP Block Diagram

F-RST# RST# F-ACC ACC NS F-WP# WP# RDY RDY/ WAIT F-CE# CE# OE# OE# AD15-AD0 AD15-AD0 WE# WE# AVD# AVD# CLK CLK Amax-A16 Amax-A16 OE# WE# AVD# CLK WAIT pSRAM R-CE# CE# CRE R-CRE AD15-AD0 UB# R-UB# R-LB# LB# Amax-A16

Figure 3.1 MCP Block Diagram

**Note:** The CLK and WAIT signals on the pSRAM are not present on the pSRAM Type 2; therefore, for those MCP's, those signals will only be connected to the NS flash, but not to the pSRAM. Also, on this pSRAM, the CRE signal will not be present at all.

4 S7INS-N MCP Products S7INS-N\_00\_A3 October 10, 2006



# 4 Connection Diagrams/Physical Dimensions

This section contains the I/O designations and package specifications for the S71NS-N.

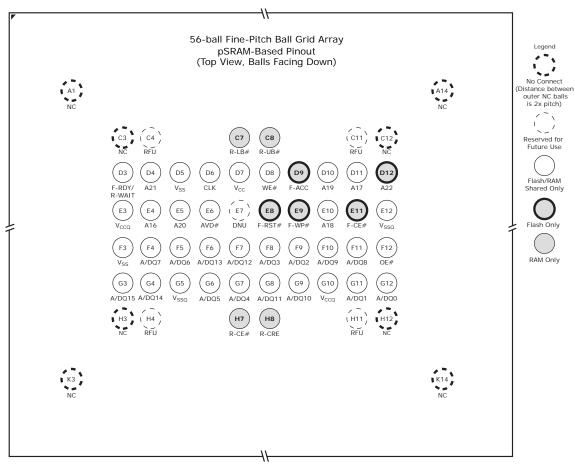
# 4.1 Special Handling Instructions for FBGA Packages

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

# 4.2 Connection Diagrams

#### 4.2.1 pSRAM Based Pinout, 56-Ball, VFBGA



#### Notes:

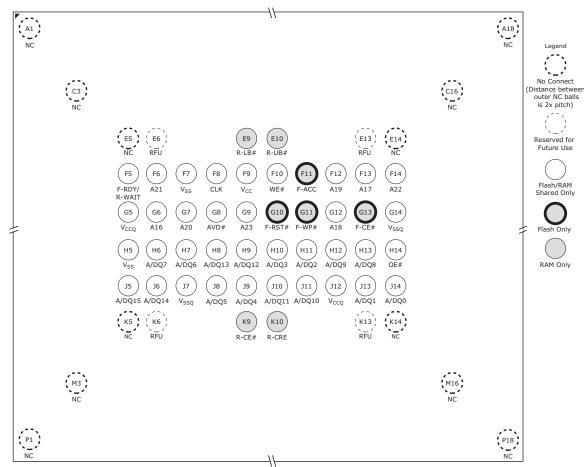
- 1. Addresses are shared between Flash and RAM depending on the density of the pSRAM.
- 2. CLK and WAIT signals are Flash only for the S71NS064NAO-RT, while on that MCP, the CRE signal won't exist.

MCP	Flash-Only Addresses	Shared Addresses	Shared ADQ Pins
S71NS128NC0	A22	A21-A16	ADQ15 – ADQ0
S71NS128NB0 A22-A21		A20-A16	ADQ15 – ADQ0
S71NS128NA0	A22-A20	A19-A16	ADQ15 – ADQ0
S71NS064NA0 A21-A20		A19-A16	ADQ15 – ADQ0

Figure 4.1 pSRAM Based Pinout, 56-Ball, VFBGA



#### 4.2.2 pSRAM Based Pinout, 60-Ball, VFBGA



Note: Addresses are shared between Flash and RAM depending on the density of the pSRAM.

MCP	Flash-Only Addresses	Shared Addresses	Shared ADQ Pins
S71NS256NC0	A23-A22	A21–A16	ADQ15 – ADQ0
S71NS256NB0 A23-A21		A20-A16	ADQ15 – ADQ0

Figure 4.2 pSRAM Based Pinout, 60-Ball, VFBGA

6 S7INS-N MCP Products S7INS-N\_00\_A3 October 10, 2006



# 4.2.3 Look Ahead Connection Diagram 112-ball x16 MUX NOR Flash + x16 MUX pSRAM on Shared Bus and x16 NAND Interface ORNAND on Bus 2

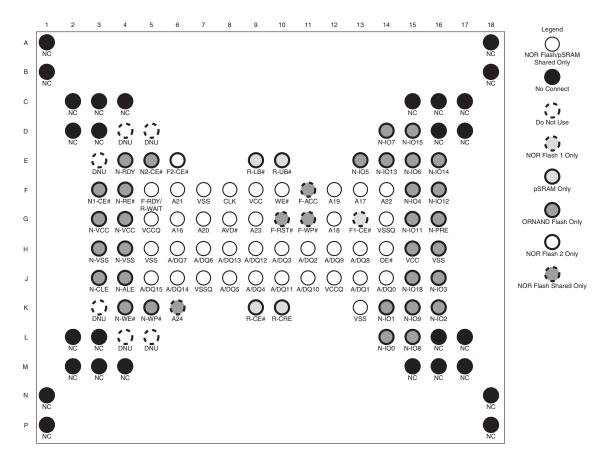
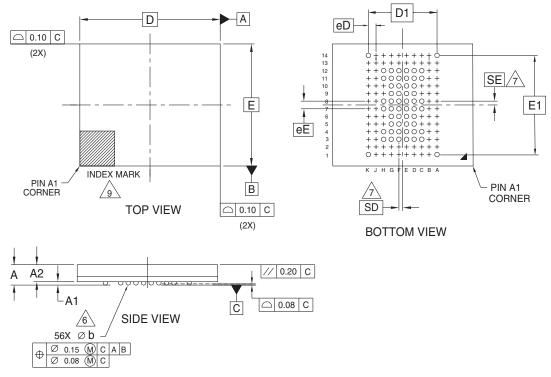


Figure 4.3 Look Ahead Connection Diagram
II2-ball xl6 MUX NOR Flash + xl6 MUX pSRAM on Shared Bus and xl6 NAND Interface
ORNAND on Bus 2



# 4.3 Physical Dimensions

#### 4.3.1 NLB056—9.2 x 8.0 mm, 56-ball VFBGA



PACKAGE		NLB 056		
JEDEC	N/A			
JEDEC		IN/A		
DxE	9.20 mm x 8.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
Α			1.20	PROFILE
A1	0.20			BALL HEIGHT
A2	0.85		0.97	BODY THICKNESS
D		9.20 BSC.		BODY SIZE
E	8.00 BSC.			BODY SIZE
D1	4.50 BSC.			MATRIX FOOTPRINT
E1	6.50 BSC.			MATRIX FOOTPRINT
MD	10			MATRIX SIZE D DIRECTION
ME		14		MATRIX SIZE E DIRECTION
n		56		BALL COUNT
Øb	0.25 0.30 0.35		0.35	BALL DIAMETER
eЕ	0.50 BSC.			BALL PITCH
eD	0.50 BSC			BALL PITCH
SD/SE	0.25 BSC.			SOLDER BALL PLACEMENT
	A2 - A13,B1 - B14 C1,C2,C5,C6,C9,C10,C13,C14 D1,D2,D13,D14,E1,E2,E13,E14,F1,F2,F13,F14 G1,G2,G13,G14,H1,H2,H5,H6,H9,H10,H13,H14 J1 - J14, K2 - K13			DEPOPULATED SOLDER BALLS

#### NOTES:

- DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
- 2. ALL DIMENSIONS ARE IN MILLIMETERS.
- 3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
- 4. e REPRESENTS THE SOLDER BALL GRID PITCH.
- 5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
  - SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
  - $\ensuremath{\mathsf{n}}$  IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
  - WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.
  - WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = 6/2
- 8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
- 41 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
- 10. OUTLINE AND DIMENSIONS PER CUSTOMER REQUIREMENT.

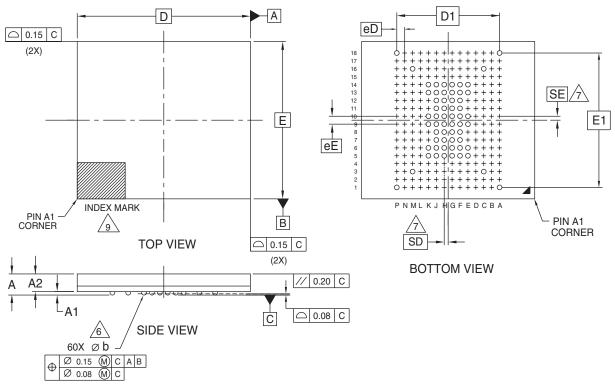
3507\ 16-038.22 \ 7.14.5

Figure 4.4 Physical Dimensions, NLB056-56-ball VFBGA

8 S7INS-N MCP Products S7INS-N 00 A3 October 10, 2006



#### 4.3.1 NLA060—11.0 x 10.0 mm, 60-ball VFBGA



PACKAGE		NLA 060		
JEDEC	N/A			
DxE	10.95 mm x 9.95 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
Α			1.20	PROFILE
A1	0.20			BALL HEIGHT
A2	0.85		0.97	BODY THICKNESS
D		10.95 BSC.		BODY SIZE
E		9.95 BSC.		BODY SIZE
D1		6.50 BSC.		MATRIX FOOTPRINT
E1	8.50 BSC.			MATRIX FOOTPRINT
MD	14			MATRIX SIZE D DIRECTION
ME		18		MATRIX SIZE E DIRECTION
n		60		BALL COUNT
Øb	0.25 0.30 0.35			BALL DIAMETER
eЕ	0.50 BSC.			BALL PITCH
eD	0.50 BSC			BALL PITCH
SD / SE	0.25 BSC.			SOLDER BALL PLACEMENT
	A2-A17,B1-B18,C1,C2,C4-C15,C17,C18 D1-D18,E1,E2,E34,E7,E8,E11,E12,E15,E16,E17,E18 F1,F2,F3,F4,F15,F16,F17,F18,G1,G2,G3,G4,G15,G16,G17,G18 H1,H2,H3,H4H15,H16,H17,H18,J1,Z13,J3,J15,J16,J17,J18 K1,K2,K3,K4,K7,K8,K11,K12,K15,K16,K17,K18 L1_H18,M1,M2,M4-M15,M17,M18,M1-N18,P2-P17			DEPOPULATED SOLDER BALLS

#### NOTES:

- DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
- 2. ALL DIMENSIONS ARE IN MILLIMETERS.
- 3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
- 4. e REPRESENTS THE SOLDER BALL GRID PITCH.
- 5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

 $\ensuremath{\mathsf{n}}$  IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED  $\wedge$  BALLS.

 A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

10. OUTLINE AND DIMENSIONS PER CUSTOMER REQUIREMENT.

3483 \ 16-038.22 \ 3.11.5

Figure 4.5 Physical Dimensions, NLA060-60-ball VFBGA



# 5 Revisions

## Revision A0 (January 3, 2006)

Initial Release under Publication Identification Number S71NS128NC0\_01

#### Revision AI (March I, 2006)

Changed the Publication Identification Number from S71NS128NCO\_01 to S71NS-N\_00 Added the MCP S71NS064NA0

## Revision A2 (June I3, 2006)

Corrected the grid reference for 56-ball connection diagram

## Revision A3 (October 10, 2006)

Added the S71NS064NA0-RT - the one using pSRAM Type 2

#### Colophon

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (I) for any use that includes fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for any use where chance of failure is intolerable (i.e., submersible repeater and artificial satellite). Please note that Spansion Inc. will not be liable to you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products. Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions. If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the US Export Administration Regulations or the applicable laws of any other country, the prior authorization by the respective government entity will be required for export of those products.

#### Trademarks and Notice

The contents of this document are subject to change without notice. This document may contain information on a Spansion Inc. product under development by Spansion Inc. Spansion Inc. reserves the right to change or discontinue work on any product without notice. The information in this document is provided as is without warranty or guarantee of any kind as to its accuracy, completeness, operability, fitness for particular purpose, merchantability, non-infringement of third-party rights, or any other warranty, express, implied, or statutory. Spansion Inc. assumes no liability for any damages of any kind arising out of the use of the information in this document.

Copyright © 2006 Spansion Inc. All Rights Reserved. Spansion, the Spansion logo, MirrorBit, ORNAND, HD-SIM, and combinations thereof are trademarks of Spansion Inc. Other names are for informational purposes only and may be trademarks of their respective owners.

10 S7INS-N MCP Products S7INS-N 00 A3 October 10, 2006