S7IPL-J Based MCPs

Stacked Multi-Chip Product (MCP) Flash Memory and RAM 256M/128/64/32 Megabit (16/8/4/2M x 16-bit) CMOS 3.0 Volt-only Simultaneous Operation Page Mode Flash Memory and 64/32/16/8/4 Megabit (4M/2M/1M/512K/256K x 16-bit) Static RAM/Pseudo Static RAM

Data Sheet

SPANSION™

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Combination

Some data sheets will contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document will distinguish these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with DC Characteristics table and AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion LLC applies the following conditions to documents in this category:

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S71PL-J Based MCPs

Stacked Multi-Chip Product (MCP) Flash Memory and RAM 256M/128/64/32 Megabit (16/8/4/2M x 16-bit) CMOS 3.0 Volt-only Simultaneous Operation Page Mode Flash Memory and 64/32/16/8/4 Megabit (4M/2M/1M/512K/256K x 16-bit) Static RAM/Pseudo Static RAM

Data Sheet

SPANSION™

Distinctive Characteristics

MCP Features

- **Power supply voltage of 2.7 V to 3.1 V**
- **High performance**
  - 65 ns (65 ns Flash, 70 ns pSRAM)

- **Packages**
  - 7 x 9 x 1.2mm 56 ball FBGA
  - 8 x 11.6 x 1.2mm 64 ball FBGA
  - 8 x 11.6 x 1.4mm 84 ball FBGA
- **Operating Temperature**
  - −25°C to +85°C
  - −40°C to +85°C

General Description

The S71PL series is a product line of stacked Multi-Chip Product (MCP) packages and consists of:

- One or more S29PL (Simultaneous Read/Write) Flash memory die

- pSRAM or SRAM (See "Referenced Data Sheets" on page 2)

The 256Mb Flash memory consists of two S29PL127J devices. In this case, CE#f2 is used to access the second Flash and no extra address lines are required.

The products covered by this document are listed in the table below:

		Flash Memory Density			
		32Mb	**64Mb**	**128Mb (Note 2)**	**256Mb (Note 2)**
pSRAM Density	4 Mb	S71PL032J40			
	8 Mb	S71PL032J80	S71PL064J80		
	16 Mb	S71PL032JA0	S71PL064JA0		
	32 Mb		S71PL064JB0	S71PL127JB0	
	64 Mb			S71PL127JC0	S71PL254JC0

		Flash Memory Density	
		32Mb	**64Mb**
SRAM Density (Note 1)	4 Mb	S71PL032J04	
	8 Mb	S71PL032J08	S71PL064J08
	16 Mb		S71PL064J0A

Notes:

1. *Not recommended for new designs; use pSRAM based MCPs instead.*

2. *Not recommended for new designs: use S71PL127N and S71PL256N instead.*

For detailed specifications, please refer to the individual data sheets listed in the following table.

Referenced Data Sheets

Document	Publication Identification Number (PID)
S29PL-J	S29PL-J_M0
pSRAM Type 1	psram_12
pSRAM Type 2	psram_15
8 Mb pSRAM Type 3	psram_25
16 Mb pSRAM Type 3	psram_06
pSRAM Type 4	psram_18
pSRAM Type 5	psram_21
pSRAM Type 6	psram_14
pSRAM Type 7	psram_13
4 Mb/8 Mb SRAM Type 1	sram_02
16 Mb SRAM Type 1	sram_06
SRAM Type 4	sram_07

Product Selector Guide

32Mb Flash Memory

Device-Model#	Flash Access time (ns)	(p)SRAM density	(p)SRAM Access time (ns)	pSRAM type	Package
S71PL032J04-0B	65	4M SRAM	70	SRAM1	TSC056
S71PL032J04-0K	65	4M SRAM	70	SRAM4	TSC056
S71PL032J40-0K	65	4M pSRAM	70	pSRAM4	TLC056
S71PL032J08-0B	65	8M SRAM	70	SRAM1	TSC056
S71PL032J80-0F	65	8M pSRAM	70	pSRAM5	TSC056
S71PL032J80-Q7	65	8M pSRAM	70	pSRAM1	TSC056
S71PL032J80-QF	65	8M pSRAM	70	pSRAM3	TSC056
S71PL032JA0-0K	65	16Mb pSRAM	70	pSRAM1	TSC056
S71PL032JA0-QF	65	16Mb pSRAM	70	pSRAM3	TSC056
S71PL032JA0-0Z	65	16M pSRAM	70	pSRAM7	TLC056

64Mb Flash Memory

| Device-Model#	Flash Access time (ns)	(p)SRAM density	(p)SRAM Access time (ns)	(p)SRAM type	Package
S71PL064J08-0B	65	8M SRAM	70	SRAM1	TLC056
S71PL064J80-0K	65	8M pSRAM	70	pSRAM1	TSC056
S71PL064J0A-0S	65	16M SRAM	70	SRAM1	TLC056
S71PL064JA0-0Z	65	16M pSRAM	70	pSRAM7	TLC056
S71PL064JA0-0B	65	16M pSRAM	70	pSRAM3	TLC056
S71PL064JA0-07	65	16M pSRAM	70	pSRAM1	TLC056
S71PL064JA0-0P	65	16M pSRAM	70	pSRAM7	TLC056
S71PL064JB0-QB	65	32M pSRAM	70	pSRAM2	TLC056
S71PL064JB0-0U	65	32M pSRAM	70	pSRAM6	TLC056

128Mb Flash Memory (Not recommended for new designs; use S7IPLI27N instead)

Device-Model#	Flash Access time (ns)	pSRAM density	pSRAM Access time (ns)	pSRAM type	Package
S71PL127JB0-9Z	65	32M pSRAM	70	pSRAM7	TLA064
S71PL127JB0-9U	65	32M pSRAM	70	pSRAM6	TLA064
S71PL127JB0-9B	65	32M pSRAM	70	pSRAM2	TLA064
S71PL127JC0-9B	65	64M pSRAM	70	pSRAM2	TLA064
S71PL127JC0-9Z	65	64M pSRAM	70	pSRAM7	TLA064
S71PL127JC0-9U	65	64M pSRAM	70	pSRAM6	TLA064

256Mb Flash Memory (2xS29PLI27J) (Not recommended for new designs: use S7IPL256N instead)

| Device-Model#	Flash Access time (ns)	pSRAM density	pSRAM Access time (ns)	pSRAM type	Package
S71PL254JC0-TB	65	64M pSRAM	70	pSRAM2	FTA084
S71PL254JC0-TZ	65	64M pSRAM	70	pSRAM7	FTA084

MCP Block Diagram
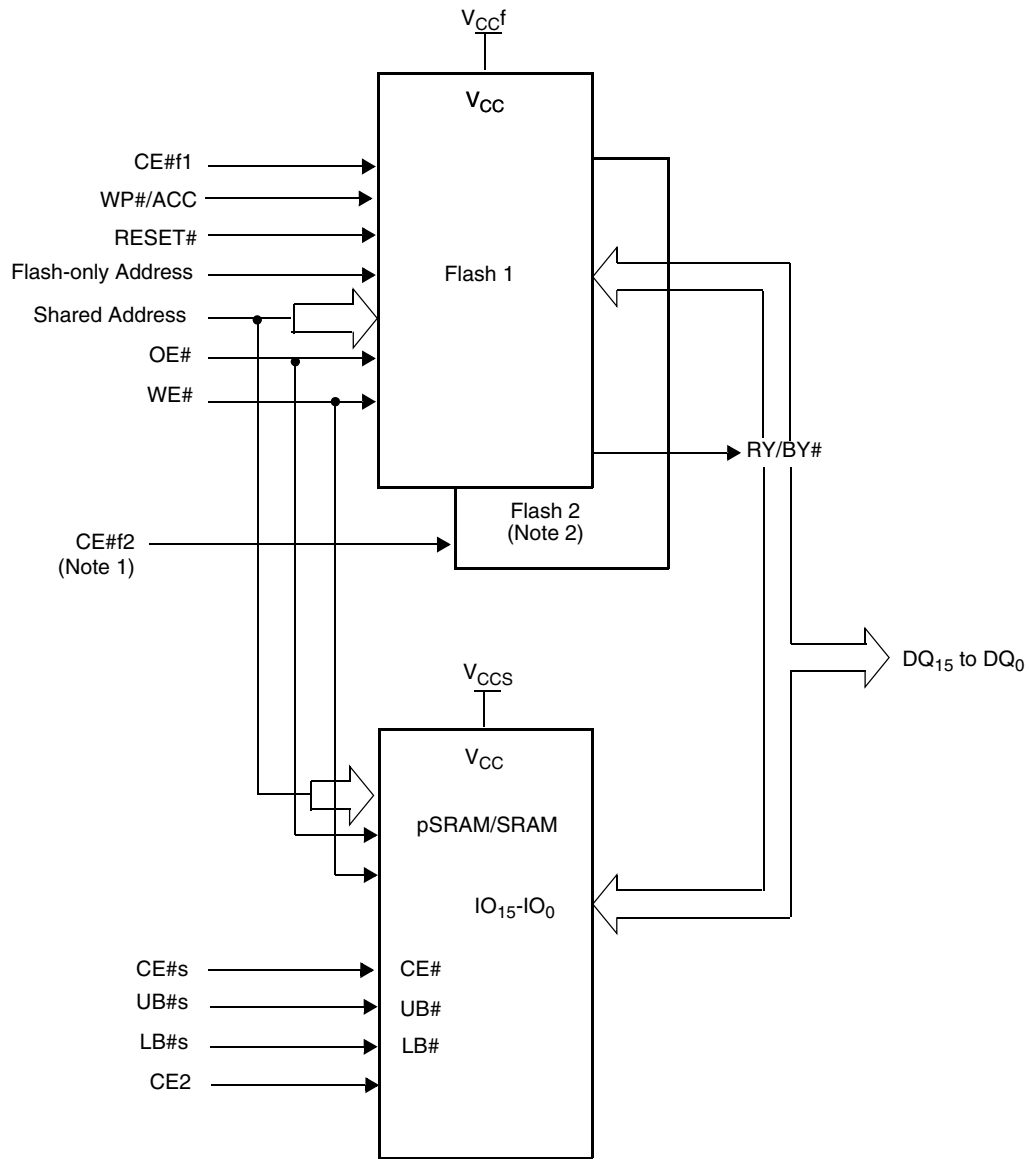
Notes:

1. For 1 Flash + pSRAM, CE#f1=CE#. For 2 Flash + pSRAM, CE#=CE#f1 and CE#f2 is the chip-enable for the second Flash.

2. For 256Mb only, Flash 1 = Flash 2 = S29PL127J.

Connection Diagram (S7IPL032J)

56-ball Fine-Pitch Ball Grid Array
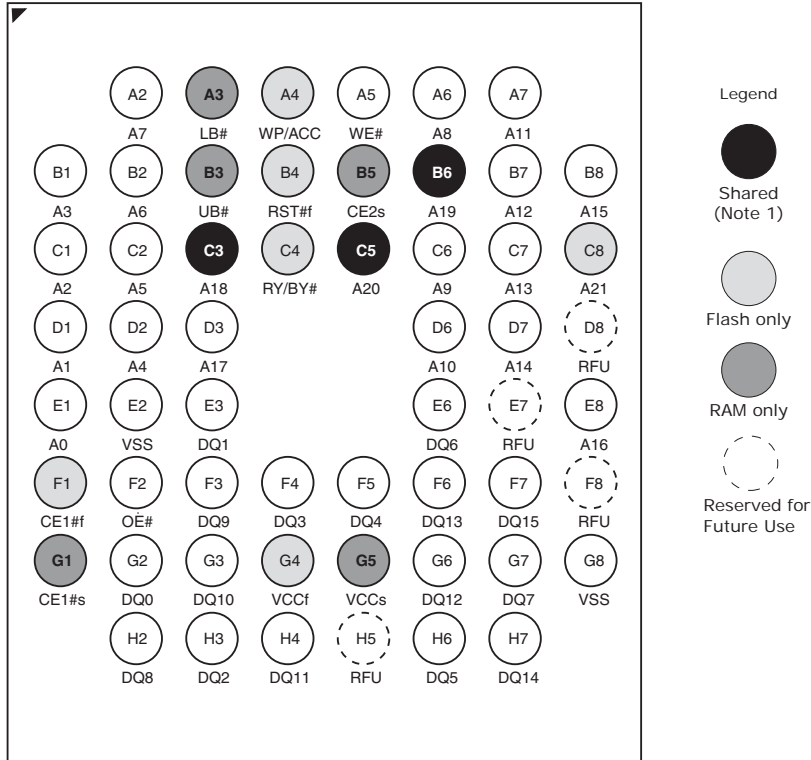(Top View, Balls Facing Down)
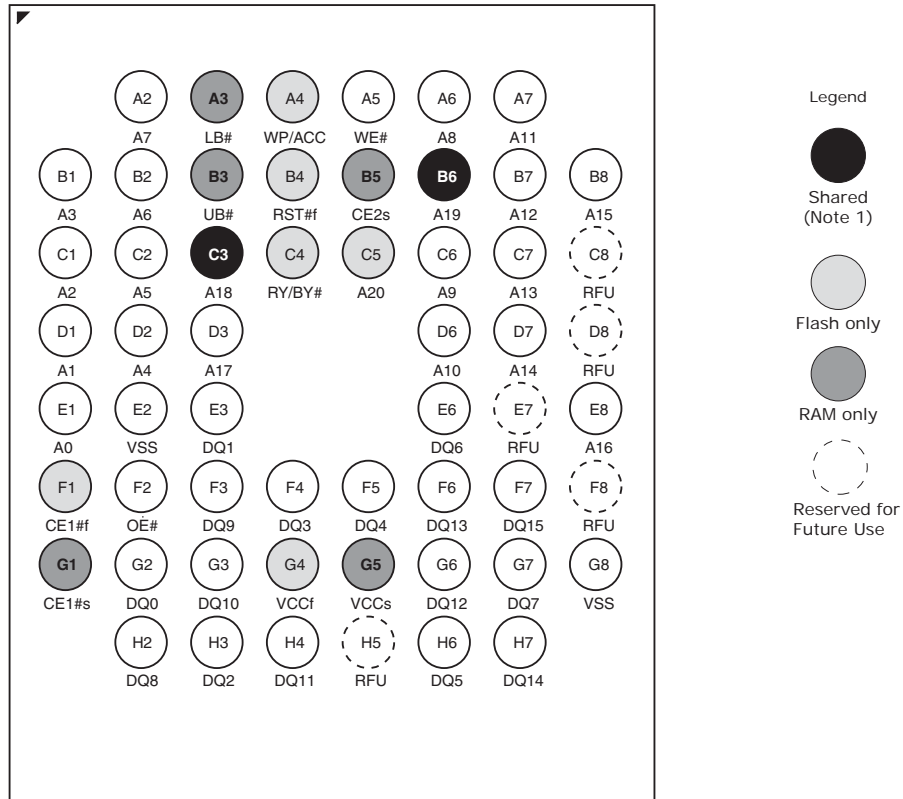
Notes:

1. *May be shared depending on density.*
   - *A19 is shared for the 16M pSRAM configuration.*
   - *A18 is shared for the 8M pSRAM and above configurations.*
2. *Connecting all V_{CC} and V_{SS} balls to V_{CC} and V_{SS} is recommended.*

MCP	Flash-only Addresses	Shared Addresses
S71PL032JA0	A20	A19-A0
S71PL032J80	A20-A19	A18-A0
S71PL032J08	A20-A19	A18-A0
S71PL032J40	A20-A18	A17-A0
S71PL032J04	A20-A18	A17-A0

Connection Diagram (S7IPL064J)

56-ball Fine-Pitch Ball Grid Array
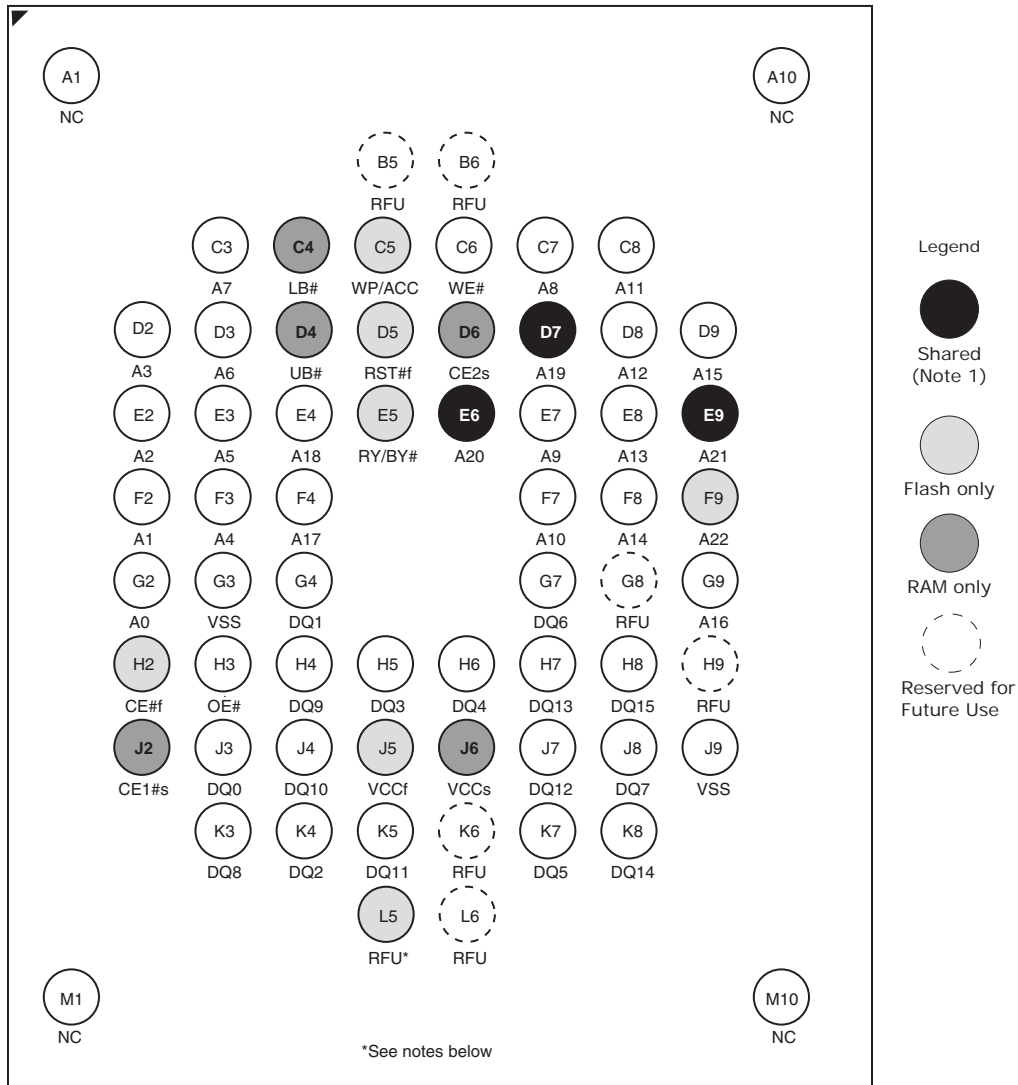(Top View, Balls Facing Down)

Notes:

1. *May be shared depending on density.*
   — *A20 is shared for the 32M pSRAM configuration.*
   — *A19 is shared for the 16M pSRAM and above configurations.*
   — *A18 is shared for the 8M pSRAM and above configurations.*
2. *Connecting all V_{CC} and V_{SS} balls to V_{CC} and V_{SS} is recommended.*

MCP	Flash-only Addresses	Shared Addresses
S71PL064JB0	A21	A20-A0
S71PL064JA0	A21-A20	A19-A0
S71PL064J0A	A21-A20	A19-A0
S71PL064J80	A21-A19	A18-A0
S71PL064J08	A21-A19	A18-A0

Connection Diagram (S7IPLI27J)

64-ball Fine-Pitch Ball Grid Array
(Top View, Balls Facing Down)

Ball	Signal
A1	NC
A10	NC
B5	RFU
B6	RFU
C3	A7
C4	LB#
C5	WP/ACC
C6	WE#
C7	A8
C8	A11
D2	A3
D3	A6
D4	UB#
D5	RST#f
D6	CE2s
D7	A19
D8	A12
D9	A15
E2	A2
E3	A5
E4	A18
E5	RY/BY#
E6	A20
E7	A9
E8	A13
E9	A21
F2	A1
F3	A4
F4	A17
F7	A10
F8	A14
F9	A22
G2	A0
G3	VSS
G4	DQ1
G7	DQ6
G8	RFU
G9	A16
H2	CE#f
H3	OE#
H4	DQ9
H5	DQ3
H6	DQ4
H7	DQ13
H8	DQ15
H9	RFU
J2	CE1#s
J3	DQ0
J4	DQ10
J5	VCCf
J6	VCCs
J7	DQ12
J8	DQ7
J9	VSS
K3	DQ8
K4	DQ2
K5	DQ11
K6	RFU
K7	DQ5
K8	DQ14
L5	RFU*
L6	RFU
M1	NC
M10	NC

Legend

● Shared (Note 1)

○ Flash only

● RAM only

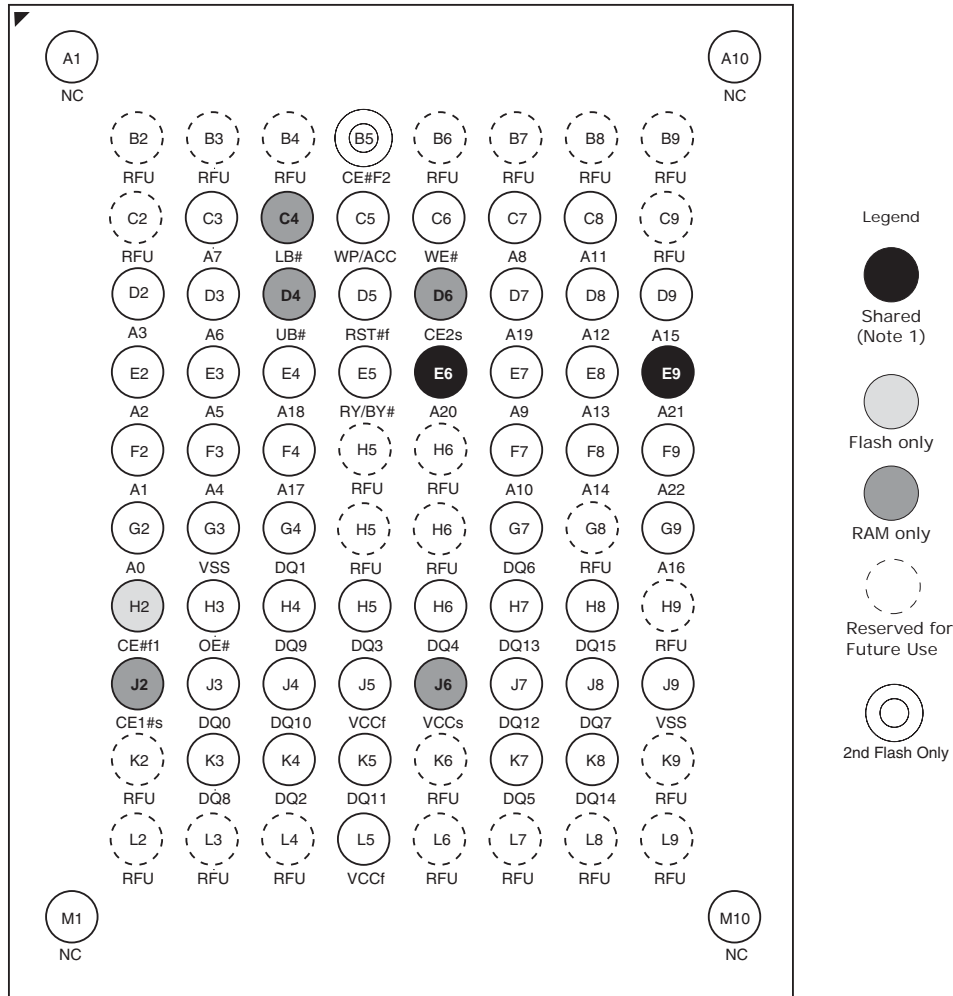⊙ Reserved for Future Use

*See notes below

Notes:

1. *May be shared depending on density.*
   - *A21 is shared for the 64M pSRAM configuration.*
   - *A20 is shared for the 32M pSRAM and above configurations.*

2. *A19 is shared for the 16M pSRAM and above configurations.*

MCP	Flash-only Addresses	Shared Addresses
S71PL127JC0	A22	A21-A0
S71PL127JB0	A22-A21	A20-A0

3. *Connecting all V_{CC} and V_{SS} balls to Vcc & Vss is recommended.*

4. *Ball L5 will be $V_{CC}F$ in the 84-ball density upgrades. Do not connect to V_{SS} or any other signal.*

Connection Diagram (S7IPL254J)

84-ball Fine-Pitch Ball Grid Array
(Top View, Balls Facing Down)

A1 NC								**A10** NC
	B2 RFU	**B3** RFU	**B4** RFU	**B5** CE#F2	**B6** RFU	**B7** RFU	**B8** RFU	**B9** RFU
	C2 RFU	**C3** A7	**C4** LB#	**C5** WP/ACC	**C6** WE#	**C7** A8	**C8** A11	**C9** RFU
	D2 A3	**D3** A6	**D4** UB#	**D5** RST#f	**D6** CE2s	**D7** A19	**D8** A12	**D9** A15
	E2 A2	**E3** A5	**E4** A18	**E5** RY/BY#	**E6** A20	**E7** A9	**E8** A13	**E9** A21
	F2 A1	**F3** A4	**F4** A17	**H5** RFU	**H6** RFU	**F7** A10	**F8** A14	**F9** A22
	G2 A0	**G3** VSS	**G4** DQ1	**H5** RFU	**H6** RFU	**G7** DQ6	**G8** RFU	**G9** A16
	H2 CE#f1	**H3** OE#	**H4** DQ9	**H5** DQ3	**H6** DQ4	**H7** DQ13	**H8** DQ15	**H9** RFU
	J2 CE1#s	**J3** DQ0	**J4** DQ10	**J5** VCCf	**J6** VCCs	**J7** DQ12	**J8** DQ7	**J9** VSS
	K2 RFU	**K3** DQ8	**K4** DQ2	**K5** DQ11	**K6** RFU	**K7** DQ5	**K8** DQ14	**K9** RFU
	L2 RFU	**L3** RFU	**L4** RFU	**L5** VCCf	**L6** RFU	**L7** RFU	**L8** RFU	**L9** RFU
M1 NC								**M10** NC

Legend

- ● Shared (Note 1)
- ◔ Flash only
- ◕ RAM only
- ◌ Reserved for Future Use
- ◎ 2nd Flash Only

Notes:

1. *May be shared depending on density.*
   - *— A21 is shared for the 64M pSRAM configuration.*
   - *— A20 is shared for the 32M pSRAM configuration.*

MCP	Flash-only Addresses	Shared Addresses
S71PL254JC0	A22	A21-A0

2. *Connecting all Vcc & Vss balls to Vcc & Vss is recommended.*

Special Handling Instructions For FBGA Package

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

Pin Description

A21–A0	=	22 Address Inputs (Common)
DQ15–DQ0	=	16 Data Inputs/Outputs (Common)
CE1#f	=	Chip Enable 1 (Flash)
CE#f2	=	Chip Enable 2 (Flash)
CE1#ps	=	Chip Enable 1 (pSRAM)
CE2ps	=	Chip Enable 2 (pSRAM)
OE#	=	Output Enable (Common)
WE#	=	Write Enable (Common)
RY/BY#	=	Ready/Busy Output (Flash 1)
UB#	=	Upper Byte Control (pSRAM)
LB#	=	Lower Byte Control (pSRAM)
RESET#	=	Hardware Reset Pin, Active Low (Flash 1)
WP#/ACC	=	Hardware Write Protect/Acceleration Pin (Flash)
$V_{CC}f$	=	Flash 3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
$V_{CC}ps$	=	pSRAM Power Supply
V_{SS}	=	Device Ground (Common)
NC	=	Pin Not Connected Internally

Logic Symbol
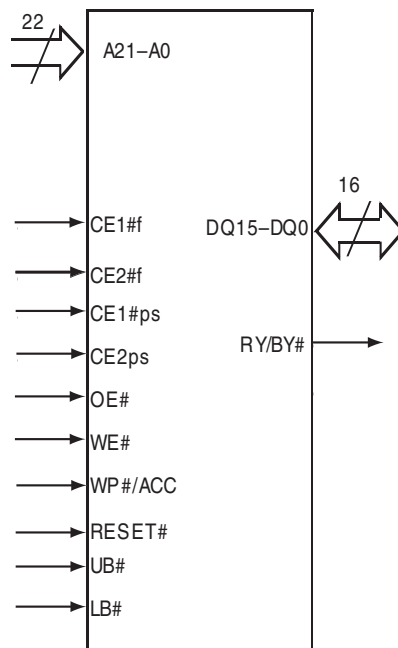
Ordering Information

The order number is formed by a valid combinations of the following:

S7IPL   I27   J   B0   BA   W   9   Z   0

PACKING TYPE

0 = Tray
2 = 7″ Tape and Reel
3 = 13″ Tape and Reel

MODEL NUMBER
See the Valid Combinations table.

PACKAGE MODIFIER

0 = 7 x 9mm, 1.2mm height, 56 balls (TLC056 or TSC065)
9 = 8 x 11.6mm, 1.2mm height, 64 balls (TLA064 or TSB064)
T = 8 x 11.6mm, 1.4mm height, 84 balls (FTA084)

TEMPERATURE RANGE

W = Wireless (-25°C to +85°C)

PACKAGE TYPE

BA = Fine-pitch BGA Lead (Pb)-free compliant package
BF = Fine-pitch BGA Lead (Pb)-free package

pSRAM DENSITY

C0 = 64Mb pSRAM
B0 = 32Mb pSRAM
A0 = 16Mb pSRAM
80 = 8Mb pSRAM
40 = 4Mb pSRAM
0A = 16Mb pSRAM
08 = 8Mb SRAM
04 = 4Mb SRAM

PROCESS TECHNOLOGY

J = 110 nm, Floating Gate Technology

FLASH DENSITY

254 = 256Mb
127 = 128Mb
064 = 64Mb
032 = 32Mb

PRODUCT FAMILY

S71PL Multi-chip Product (MCP)
3.0-volt Simultaneous Read/Write, Page Mode Flash Memory and RAM

S71PL032J Valid Combinations				Speed Options (ns)	(p)SRAM Type/Access Time (ns)	Package Marking
Base Ordering Part Number	Package & Temperature	Package Modifier/ Model Number	Packing Type			
S71PL032J04	BAW	0B	0, 2, 3 (Note 1)	65	SRAM2 / 70	(Note 2)
S71PL032J04		0K			SRAM4 / 70	
S71PL032J40		0K			pSRAM4 / 70	
S71PL032J80		0F			pSRAM5 / 70	
S71PL032J08		0B			SRAM2 / 70	
S71PL032J80		Q7			pSRAM1 / 70	
S71PL032J80		QF			pSRAM3 / 70	
S71PL032JA0		07			pSRAM1 / 70	
S71PL032JA0		QF			pSRAM3 / 70	
S71PL032JA0		0Z			pSRAM2 / 70	
S71PL032J04	BFW	0B	0, 2, 3 (Note 1)	65	SRAM2 / 70	(Note 2)
S71PL032J04		0K			SRAM4 / 70	
S71PL032J40		0K			pSRAM4 / 70	
S71PL032J80		0F			pSRAM5 / 70	
S71PL032J08		0B			SRAM2 / 70	
S71PL032J80		Q7			pSRAM1 / 70	
S71PL032J80		QF			pSRAM3 / 70	
S71PL032JA0		07			pSRAM1 / 70	
S71PL032JA0		QF			pSRAM3 / 70	
S71PL032JA0		0Z			pSRAM2 / 70	

| S71PL064J Valid Combinations				Speed Options (ns)	(p)SRAM Type/ Access Time (ns)	Package Marking
Base Ordering Part Number	Package & Temperature	Package Modifier/ Model Number	Packing Type			
S71PL064J08	BAW	0B	0, 2, 3 (Note 1)	65	SRAM1 / 70	(Note 2)
S71PL064J80		0K			pSRAM1 /70	
S71PL064J0A		0S			SRAM1 / 70	
S71PL064JA0		0B			pSRAM3 / 70	
S71PL064JA0		07			pSRAM1 / 70	
S71PL064JA0		0P			pSRAM7 / 70	
S71PL064JB0		QB			pSRAM2 / 70	
S71PL064JB0		0U			pSRAM6 / 70	
S71PL064J08	BFW	0B	0, 2, 3 (Note 1)	65	SRAM1 / 70	(Note 2)
S71PL064J80		0K			pSRAM1 /70	
S71Pl064J0A		0S			SRAM1 / 70	
S71PL064JA0		0B			pSRAM3 / 70	
S71PL064JA0		07			pSRAM1 / 70	
S71PL064JA0		0P			pSRAM7 / 70	
S71PL064JB0		QB			pSRAM2 / 70	
S71PL064JB0		0U			pSRAM6 / 70	

Notes:
1. Type 0 is standard. Specify other options as required.
2. BGA package marking omits leading "S" and packing type designator from ordering part number.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

S71PL127J Valid Combinations				Speed Options (ns)	(p)SRAM Type/ Access Time (ns)	Package Marking
Base Ordering Part Number	Package & Temperature	Package Modifier/Model Number	Packing Type			
S71PL127JB0	BAW	9Z	0, 2, 3 (Note 1)	65	pSRAM7 / 70	(Note 2)
S71PL127JB0		9U			pSRAM6 /70	
S71PL127JC0		9B			pSRAM2 /70	
S71PL127JC0		9Z			pSRAM7 / 70	
S71PL127JC0		9U			pSRAM6 / 70	
S71PL127JB0		9B			pSRAM2 / 70	
S71PL127JB0	BFW	9Z	0, 2, 3 (Note 1)	65	pSRAM7 / 70	(Note 2)
S71PL127JB0		9U			pSRAM6 / 70	
S71PL127JC0		9B			pSRAM2 /70	
S71PL127JC0		9Z			pSRAM7 / 70	
S71PL127JC0		9U			pSRAM6 / 70	
S71PL127JB0		9B			pSRAM2 / 70	

Notes:
1. *Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading "S" and packing type designator from ordering part number.*

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

S71PL254J Valid Combinations				Speed Options (ns)	(p)SRAM Type/Access Time (ns)	Package Marking
Base Ordering Part Number	Package & Temperature	Model Number	Packing Type			
S71PL254JC0	BAW	TB	0, 2, 3 (Note1)	65	pSRAM2 / 70	(Note 2)
S71PL254JC0		TZ			pSRAM7 / 70	
S71PL254JC0	BFW	TB	0, 2, 3 (Note1)	65	pSRAM2 / 70	(Note 2)
S71PL254JC0		TZ			pSRAM7 / 70	

Notes:
1. *Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading "S" and packing type designator from ordering part number.*

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Physical Dimensions

TLC056—56-ball Fine-Pitch Ball Grid Array (FBGA) 9 x 7mm Package

TOP VIEW

SIDE VIEW

BOTTOM VIEW
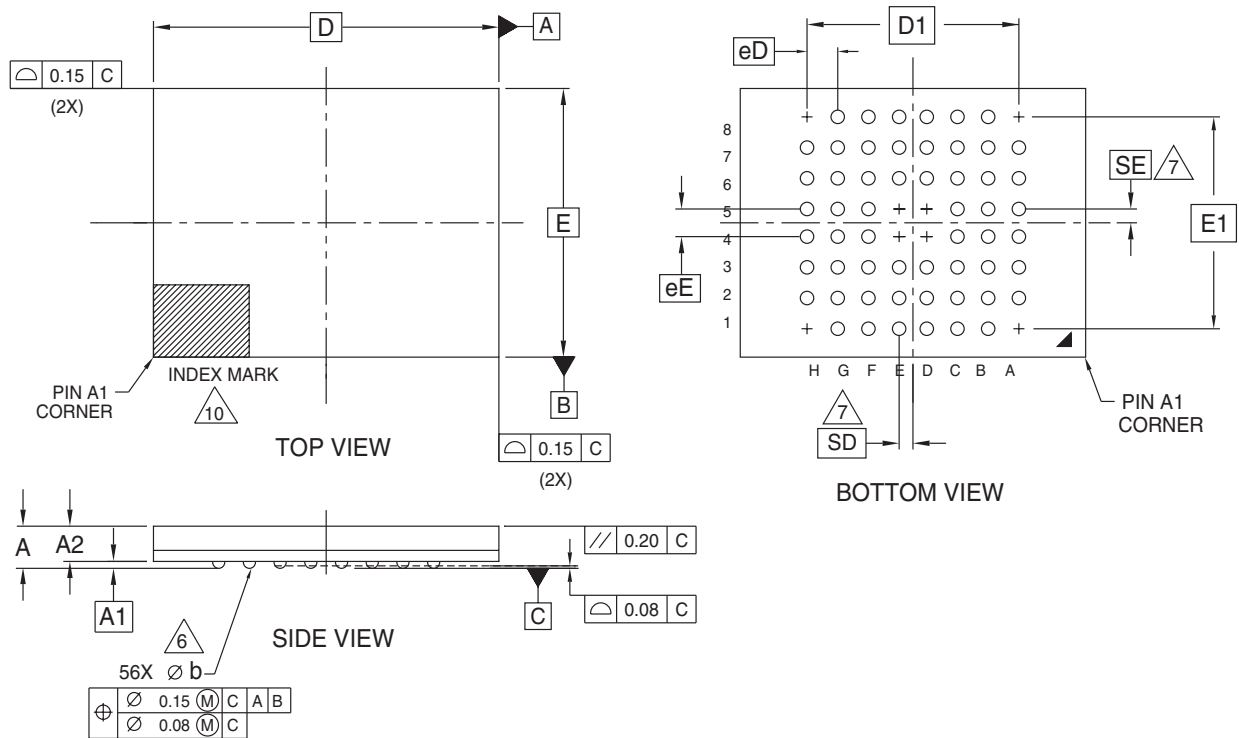
PACKAGE		TLC 056		
JEDEC		N/A		
D x E		9.00 mm x 7.00 mm PACKAGE		
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.20	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D		9.00 BSC.		BODY SIZE
E		7.00 BSC.		BODY SIZE
D1		5.60 BSC.		MATRIX FOOTPRINT
E1		5.60 BSC.		MATRIX FOOTPRINT
MD		8		MATRIX SIZE D DIRECTION
ME		8		MATRIX SIZE E DIRECTION
n		56		BALL COUNT
φb	0.35	0.40	0.45	BALL DIAMETER
eE		0.80 BSC.		BALL PITCH
eD		0.80 BSC		BALL PITCH
SD / SE		0.40 BSC.		SOLDER BALL PLACEMENT
		A1,A8,D4,D5,E4,E5,H1,H8		DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.

2. ALL DIMENSIONS ARE IN MILLIMETERS.

3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.

4. $\boxed{e}$ REPRESENTS THE SOLDER BALL GRID PITCH.

5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

    SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

    n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

    WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

    WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = $\boxed{e/2}$

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

9. N/A

10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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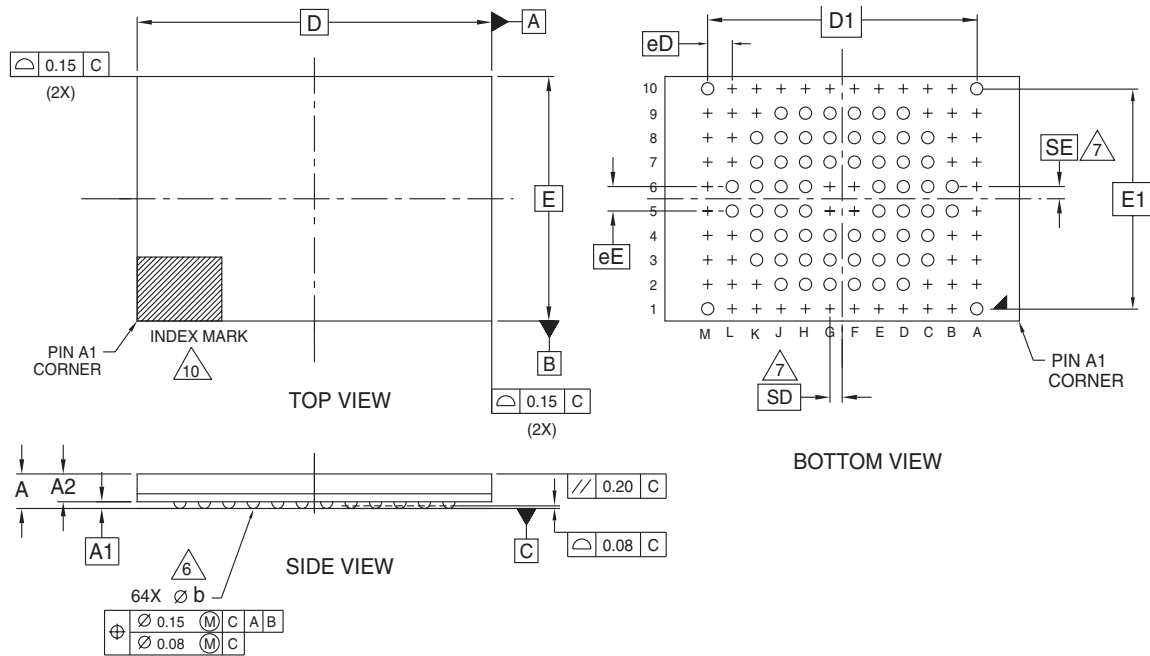## TSC056—56-ball Fine-Pitch Ball Grid Array (FBGA) 9 x 7mm Package

TOP VIEW

SIDE VIEW

BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.

2. ALL DIMENSIONS ARE IN MILLIMETERS.

3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.

4. $\boxed{e}$ REPRESENTS THE SOLDER BALL GRID PITCH.

5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = $\boxed{e/2}$

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

9. N/A

10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3427 \ 16-038.22

PACKAGE	TSC 056			
JEDEC	N/A			
D x E	9.00 mm x 7.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D	9.00 BSC.			BODY SIZE
E	7.00 BSC.			BODY SIZE
D1	5.60 BSC.			MATRIX FOOTPRINT
E1	5.60 BSC.			MATRIX FOOTPRINT
MD	8			MATRIX SIZE D DIRECTION
ME	8			MATRIX SIZE E DIRECTION
n	56			BALL COUNT
φb	0.35	0.40	0.45	BALL DIAMETER
eE	0.80 BSC.			BALL PITCH
eD	0.80 BSC			BALL PITCH
SD / SE	0.40 BSC.			SOLDER BALL PLACEMENT
	A1,A8,D4,D5,E4,E5,H1,H8			DEPOPULATED SOLDER BALLS

TLA064—64-ball Fine-Pitch Ball Grid Array (FBGA) 8 x II.6mm Package

TOP VIEW

BOTTOM VIEW

SIDE VIEW

PACKAGE		TLA 064		
JEDEC		N/A		
D x E		11.60 mm x 8.00 mm PACKAGE		
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D		11.60 BSC.		BODY SIZE
E		8.00 BSC.		BODY SIZE
D1		8.80 BSC.		MATRIX FOOTPRINT
E1		7.20 BSC.		MATRIX FOOTPRINT
MD		12		MATRIX SIZE D DIRECTION
ME		10		MATRIX SIZE E DIRECTION
n		64		BALL COUNT
φb	0.35	0.40	0.45	BALL DIAMETER
eE		0.80 BSC.		BALL PITCH
eD		0.80 BSC		BALL PITCH
SD / SE		0.40 BSC.		SOLDER BALL PLACEMENT
		A2,A3,A4,A5,A6,A7,A8,A9 B1,B2,B3,B4,B7,B8,B9,B10 C1,C2,C9,C10,D1,D10,E1,E10, F1,F5,F6,F10,G1,G5,G6,G10 H1,H10,J1,J10,K1,K2,K9,K10 L1,L2,L3,L4,L7,L8,L9,L10 M2,M3,M4,M5,M6,M7,M8,M9		DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.

2. ALL DIMENSIONS ARE IN MILLIMETERS.

3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.

4. $\boxed{e}$ REPRESENTS THE SOLDER BALL GRID PITCH.

5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

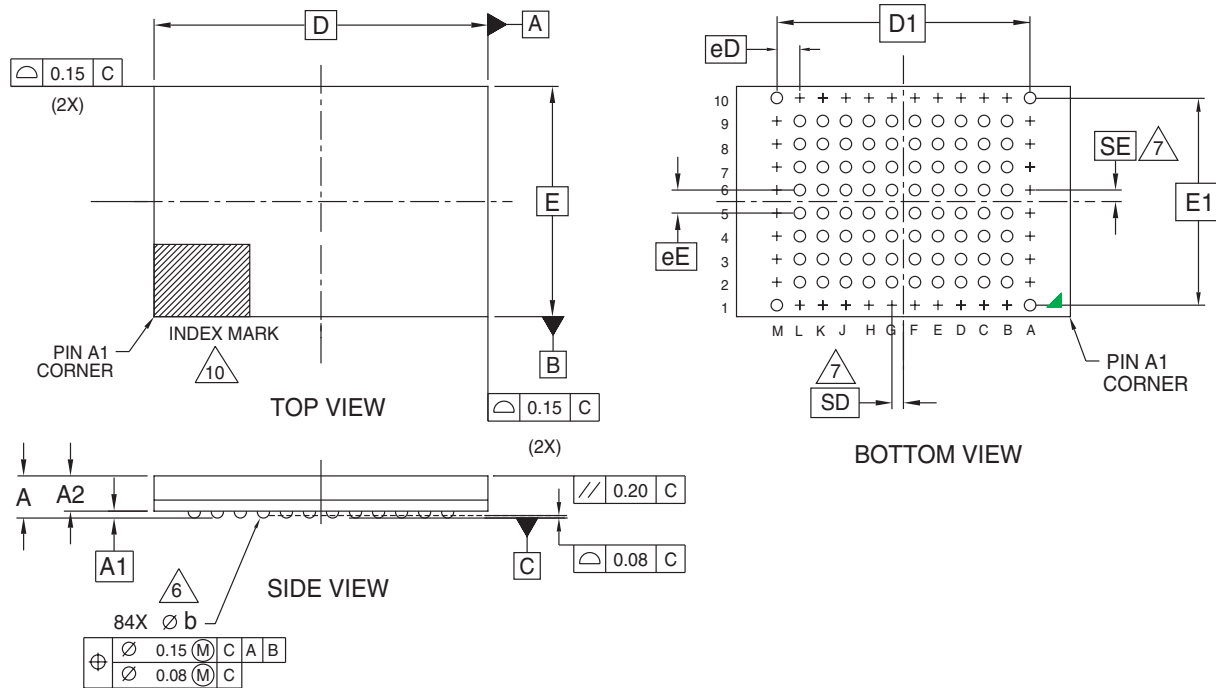   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = $\boxed{e/2}$

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

9. N/A

10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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TSB064—64-ball Fine-Pitch Ball Grid Array (FBGA) 8 x 11.6 mm Package

TOP VIEW

SIDE VIEW

BOTTOM VIEW

PACKAGE	TSB 064			
JEDEC	N/A			
D x E	11.60 mm x 8.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	017	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D	11.60 BSC.			BODY SIZE
E	8.00 BSC.			BODY SIZE
D1	8.80 BSC.			MATRIX FOOTPRINT
E1	7.20 BSC.			MATRIX FOOTPRINT
MD	12			MATRIX SIZE D DIRECTION
ME	10			MATRIX SIZE E DIRECTION
n	64			BALL COUNT
φb	0.35	0.40	0.45	BALL DIAMETER
eE	0.80 BSC.			BALL PITCH
eD	0.80 BSC			BALL PITCH
SD / SE	0.40 BSC.			SOLDER BALL PLACEMENT
	A2,A3,A4,A5,A6,A7,A8,A9 B1,B2,B3,B4,B7,B8,B9,B10 C1,C2,C9,C10,D1,D10,E1,E10 F1,F5,F6,F10,G1,G5,G6,G10 H1,H10,J1,J10,K1,K2,K9,K10 L1,L2,L3,L4,L7,L8,L9,L10 M2,M3,M4,M5,M6,M7,M8,M9			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.

2. ALL DIMENSIONS ARE IN MILLIMETERS.

3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.

4. $\boxed{e}$ REPRESENTS THE SOLDER BALL GRID PITCH.

5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = $\boxed{e/2}$

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

9. N/A

10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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FTA084—84-ball Fine-Pitch Ball Grid Array (FBGA) 8 x 11.6mm Package

TOP VIEW

SIDE VIEW

BOTTOM VIEW

PACKAGE	FTA 084			
JEDEC	N/A			
D x E	11.60 mm x 8.00 mm PACKAGE			NOTE
SYMBOL	MIN	NOM	MAX	
A	---	---	1.40	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	1.02	---	1.17	BODY THICKNESS
D	11.60 BSC.			BODY SIZE
E	8.00 BSC.			BODY SIZE
D1	8.80 BSC.			MATRIX FOOTPRINT
E1	7.20 BSC.			MATRIX FOOTPRINT
MD	12			MATRIX SIZE D DIRECTION
ME	10			MATRIX SIZE E DIRECTION
n	84			BALL COUNT
φb	0.35	0.40	0.45	BALL DIAMETER
eE	0.80 BSC.			BALL PITCH
eD	0.80 BSC			BALL PITCH
SD / SE	0.40 BSC.			SOLDER BALL PLACEMENT
	A2,A3,A4,A5,A6,A7,A8,A9 B1,B10,C1,C10,D1,D10,E1,E10 F1,F10,G1,G10,H1,H10 J1,J10,K1,K10,L1,L10 M2,M3,M4,M5,M6,M7,M8,M9			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.

2. ALL DIMENSIONS ARE IN MILLIMETERS.

3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.

4. $\boxed{e}$ REPRESENTS THE SOLDER BALL GRID PITCH.

5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = $\boxed{e/2}$

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

9. N/A

10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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MCP Revision Summary

Revision A (May 3, 2004)

Initial release.

Revision A1 (May 6, 2004)

MCP Features

Corrected the high performance access times.

Connection Diagrams

Added reference points on all diagrams.

Ordering Information

Corrected package types.

Corrected the description of product family to Page Mode Flash memory.

pSRAM Type 1

Corrected the description of the 8Mb device to 512Kb Word x 16-bit.

pSRAM Type 6

Corrected the description of the 2Mb device to 128Kb Word x 16-bit.

Corrected the description of the 4Mb device to 256Kb Word x 16-bit.

Revision A2 (May 11, 2004)

General Description

Corrected the tables to reflect accurate device configurations.

Revision A3 (June 16, 2004)

Ordering Information

Corrected the Valid Combinations tables to reflect accurate device configurations.

SRAM

New section added.

Revision A4 (July 16, 2004)

Global Changes

Global Change of FASL to Spansion.

Global change to remove space between M and Mb callouts.

"32Mb Flash Memory" on page 3

Replaced "S71PL032J08-07" with "S71PL032J08-0B".

Replaced "S71PL032JA0" with "S71PL032JA0-07".

Added row with the following content: S71PL032JA0-08; 65; 16Mb pSRAM; 70; pSRAM3; TLC056.

"64Mb Flash Memory" on page 3

Replaced "S71PL064J08-0K" with "S71PL064J08-0B".

Replaced "S71PL064J08-0P" with "S71PL064J08-0U".

Deleted "S71PL064J80-05" row.

Replaced "S71PL064JA0-07" with "S71PL064JA0-0K".

Replaced "S71PL064JA0-0Z" with

Added row with the following content:S71PL064JB0-07; 65; 32M pSRAM; 70; Psram 1; TLC056.

"32Mb Flash Memory" on page 3

Replaced "S71PL032JA0-08" with "S71PL032JA0-0F".

"64Mb Flash Memory" on page 3

Replaced "S71PL032JA0-07" with "S71PL032JA0-0K".

"I28Mb Flash Memory" on page 4

Added row with the following content: S71PL127JB0-9; 65; 32M pSRAM; 70; pSRAM; TLA064.

Replaced "S71PL127JB0-97" with "S71PL127JB0-9Z".

Added row with the following content: S71PL127JC0-97; 65; 64M pSRAM; 70; pSRAM1; TLA064.

Replaced "S71PL127JC0-9P" with "S71PL127JC0-9Z".

In the S71PI254JB0-TB row changed pSRAM type from "pSRAM3" to "pSRAM2".

"256Mb Flash Memory (2xS29PLI27J)" on page 4

Added row with the following content: S71PL254JB0-TB; 65; 32M pSRAM; 70; pSRAM3; FTA084.

Added row with the following content: S71PL254JC0-TB; 65; 64M pSRAM; 70; pSRAM2; FTA084.

"Connection Diagram (S7IPLI27J)" on page I2

Updated pins D8, D9, and L5.

Added notes 2 and 3 to drawing.

"Connection Diagram (S7IPL254J)" on page I3

Updated pins D8 and D9.

Added Note 2 to drawing.

"S7IPL032J Valid Combinations" on page I6

Changed S71PL032J08 (p)SRAM Type Access Time (ns) from "SRAM1" to "SRAM2" (4 changes made in table).

Changed S71PL032JA0 (p)SRAM Type Access Time (ns) from "SRAM3 / 70" to pSRAM3 /70".

Deleted all cells with the following collaborated text: "BAW,BFW, BAI. BFI". Merged previous place holder with cell above.

"S7IPL064J Valid Combinations" on page I7

In (p)SRAM Type/Access Time (ns) changed all instances of "stet" to "pSRAM1/ 70".

In Package Modifier/Model Number changed all instances of "stet" to "07".

Added row to BAW Package and Temperature sections with the following content: S71PL064JB0; 07; 65 (previously inclusive); pSRAM1/70.

"S7IPLI27J Valid Combinations" on page I8

Changed the S71PL127JA0 Package Modifier/Model Number from "9Z" to "9P" (4 instances).

Added 4 rows with the following content: S71PL127JC0; 97; pSRAM1/70.

"S7IPL254J Valid Combinations" on page 20

Added 4 rows with the following content: S71PL254JC0; TB; pSRAM2/70.

Added 4 rows with the following content: S71PL254JB0; TB; pSRAM2/70.

"S7IPL-J based MCPs" on page l

Added 254M to Megabit indicator.

Added 16 to CMOS indicator.

Revision A5 (September l4, 2004)

Product Selector Guide

Updated the 128Mb Flash Memory table.

Valid Combinations Table

Updated the S71PL127J Valid Combinations table.

Revision A6 (November 22, 2004)

Product Selector Guide

Updated the 32Mb and 64Mb tables.

Valid Combinations Tables

Updated the 32Mb and 64Mb combinations.

Physical Dimensions

Added the TSB064 package.

Revision A7 (February 8, 2005)

pSRAM Type 7

Updated all information in this section.

Revision A8 (April 6, 2005)

S29PL-J Flash

Updated all information in this section.

Revision A9 (May l2, 2005)

S71PL-J MCP

Added the S71PL064J0A option to cover the inclusion of the 16M SRAM

pSRAM Type 2

Added the latest revision for the pSRAM Type 2

SRAM Type 2

Added this module to the S71PL-J MCP

Revision Al0 (June 22, 2005)

S71PL-J MCP

Removed 127/16 and 254/32 pSRAM and updated OPN for 64/16SRAM

Revision All (July 29, 2005)

pSRAM Type 7

Updated module

Revision B0 (September 29, 2005)

S29PL-J

Updated module

SRAM Type 1

Updated module

Revision B1 (October 25, 2005)

pSRAM Module Type 5

Added module

Revision B2 (January 25, 2006)

Added notices for devices not recommended for new designs

Modified the *Product Selection Guide*

Modified the *S71PL032J, S71PL064J, S71PL127JValid Combinations* tables

Revision B3 (March 17, 2006)

Modified the stucture of the document. Related data sheets are referenced rather than be embedded. Added data sheet reference table to that effect.

Added the SRAM Type 4 option

Added the 8Mb pSRAM Type 3 option