DATA SHEET

SA5211
Transimpedance amplifier (180MHz)

Product specification
Replaces datasheet NE/SA5211 of 1995 Apr 26
IC19 Data Handbook

1998 Oct 07

Philips
Semiconductors

PHILIPS

Transimpedance amplifier (180MHz) SA5211

DESCRIPTION

The SA5211 is a 28kΩ transimpedance, wide-band, low noise amplifier with differential outputs, particularly suitable for signal recovery in fiber optic receivers. The part is ideally suited for many other RF applications as a general purpose gain block.

FEATURES

- Extremely low noise: $1.8\text{pA}/\sqrt{\text{Hz}}$
- Single 5V supply
- Large bandwidth: 180MHz
- Differential outputs
- Low input/output impedances
- High power supply rejection ratio
- 28kΩ differential transresistance

APPLICATIONS

- Fiber optic receivers, analog and digital
- Current-to-voltage converters
- Wide-band gain block
- Medical and scientific Instrumentation
- Sensor preamplifiers
- Single-ended to differential conversion
- Low noise RF amplifiers
- RF signal processing

PIN CONFIGURATION

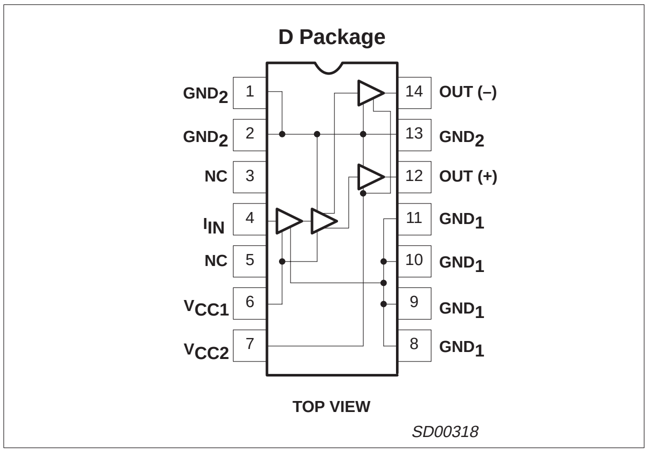


Figure 1. Pin Configuration

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Small Outline (SO) Package	-40 to +85°C	SA5211D	SOT108-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply	6	V
T_A	Operating ambient temperature range	-40 to +85	°C
T_J	Operating junction temperature range	-55 to +150	°C
T_{STG}	Storage temperature range	-65 to +150	°C
$P_{D\ MAX}$	Power dissipation, T_A=25°C (still-air)[1]	1.0	W
$I_{IN\ MAX}$	Maximum input current[2]	5	mA
θ_{JA}	Thermal resistance	125	°C/W

NOTES:

1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance: θ_{JA}=125°C/W
2. The use of a pull-up resistor to V_{CC}, for the PIN diode is recommended.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	4.5 to 5.5	V
T_A	Ambient temperature range	-40 to +85	°C
T_J	Junction temperature range	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over operating temperature range at V_{CC}=5V, unless otherwise specified. Typical data apply at V_{CC}=5V and T_A=25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	Min	Typ	Max	UNIT
V_{IN}	Input bias voltage		0.55	0.8	1.00	V
$V_{O\pm}$	Output bias voltage		2.7	3.4	3.7	V
V_{OS}	Output offset voltage			0	130	mV
I_{CC}	Supply current		20	26	31	mA
I_{OMAX}	Output sink/source current[1]		3	4		mA
I_{IN}	Input current (2% linearity)	Test Circuit 8, Procedure 2	±20	±40		µA
$I_{IN\ MAX}$	Maximum input current overload threshold	Test Circuit 8, Procedure 4	±30	±60		µA

NOTES:

1. Test condition: output quiescent voltage variation is less than 100mV for 3mA load current.

AC ELECTRICAL CHARACTERISTICS

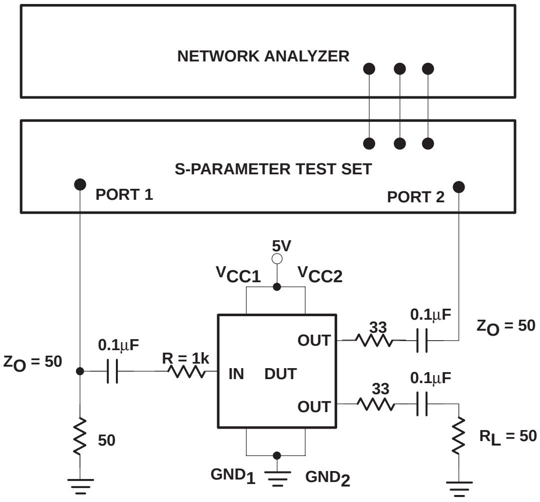
Typical data and Min and Max limits apply at V_{CC}=5V and T_A=25°C

SYMBOL	PARAMETER	TEST CONDITIONS	Min	Typ	Max	UNIT
R_T	Transresistance (differential output)	DC tested $R_L = \infty$ Test Circuit 8, Procedure 1	21	28	36	kΩ
R_O	Output resistance (differential output)	DC tested		30		Ω
R_T	Transresistance (single-ended output)	DC tested $R_L = \infty$	10.5	14	18.0	kΩ
R_O	Output resistance (single-ended output)	DC tested		15		Ω
f_{3dB}	Bandwidth (-3dB)	T_A = 25°C Test circuit 1		180		MHz
R_{IN}	Input resistance			200		Ω
C_{IN}	Input capacitance			4		pF
$\Delta R/\Delta V$	Transresistance power supply sensitivity	$V_{CC} = 5 \pm 0.5V$		3.7		%/V
$\Delta R/\Delta T$	Transresistance ambient temperature sensitivity	$\Delta T_A = T_{A\,MAX} - T_{A\,MIN}$		0.025		%/°C
I_N	RMS noise current spectral density (referred to input)	Test Circuit 2 f = 10MHz T_A = 25°C		1.8		pA/√Hz
I_T	Integrated RMS noise current over the bandwidth (referred to input)	T_A = 25°C Test Circuit 2				
	C_S=0[1]	Δf = 50MHz		13		nA
		Δf = 100MHz		20		
		Δf = 200MHz		35		
	C_S=1pF	Δf = 50MHz		13		nA
		Δf = 100MHz		21		
		Δf = 200MHz		41		
PSRR	Power supply rejection ratio[2] ($V_{CC1} = V_{CC2}$)	DC tested, ΔV_{CC} = 0.1V Equivalent AC Test Circuit 3	23	32		dB
PSRR	Power supply rejection ratio[2] (V_{CC1})	DC tested, ΔV_{CC} = 0.1V Equivalent AC Test Circuit 4	23	32		dB
PSRR	Power supply rejection ratio[2] (V_{CC2})	DC tested, ΔV_{CC} = 0.1V Equivalent AC Test Circuit 5	45	65		dB
PSRR	Power supply rejection ratio (ECL configuration)[2]	f = 0.1MHz Test Circuit 6		23		dB
V_{OMAX}	Maximum differential output voltage swing	$R_L = \infty$ Test Circuit 8, Procedure 3	1.7	3.2		V_{P-P}
$V_{IN\,MAX}$	Maximum input amplitude for output duty cycle of 50±5%[3]	Test Circuit 7	160			mV_{P-P}
t_R	Rise time for 50mV output signal[4]	Test Circuit 7		0.8	1.8	ns

NOTES:

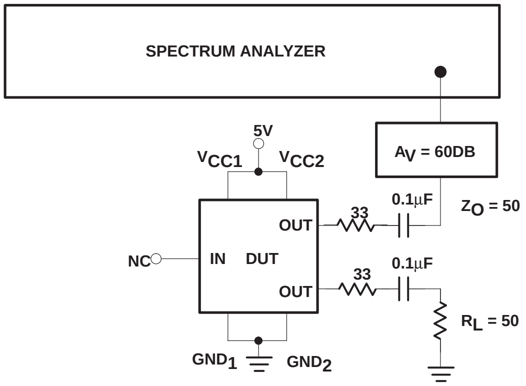
1. Package parasitic capacitance amounts to about 0.2pF
2. PSRR is output referenced and is circuit board layout dependent at higher frequencies. For best performance use RF filter in V_{CC} lines.
3. Guaranteed by linearity and overload tests.
4. t_R defined as 20-80% rise time. It is guaranteed by -3dB bandwidth test.

TEST CIRCUITS



SINGLE-ENDED	DIFFERENTIAL
$R_T \approx \frac{V_{OUT}}{V_{IN}} R = 2 \cdot S21 \cdot R$	$R_T = \frac{V_{OUT}}{V_{IN}} R = 4 \cdot S21 \cdot R$
$R_O \approx Z_O \left\lvert\frac{1 + S22}{1 - S22}\right\rvert - 33$	$R_O = 2Z_O \left\lvert\frac{1 + S22}{1 - S22}\right\rvert - 66$

Test Circuit 1

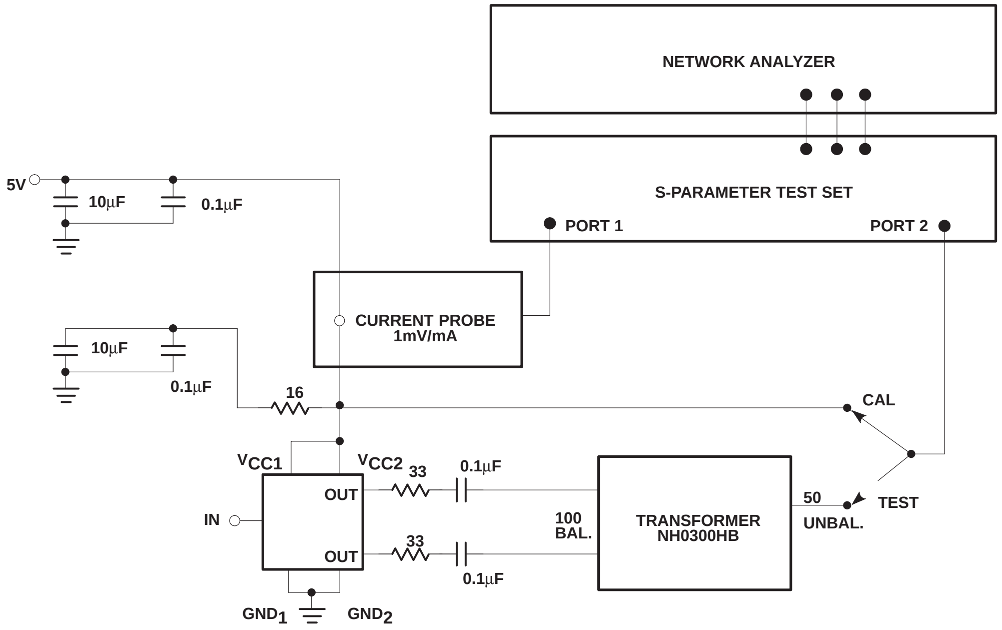


Test Circuit 2

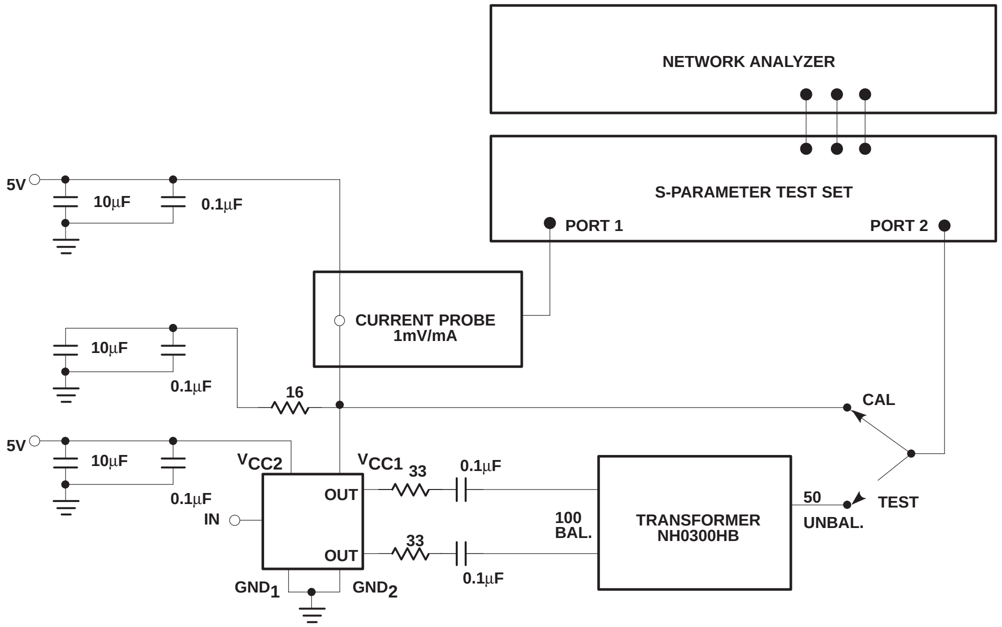
SD00319

Figure 2. Test Circuits 1 and 2

TEST CIRCUITS (Continued)



Test Circuit 3

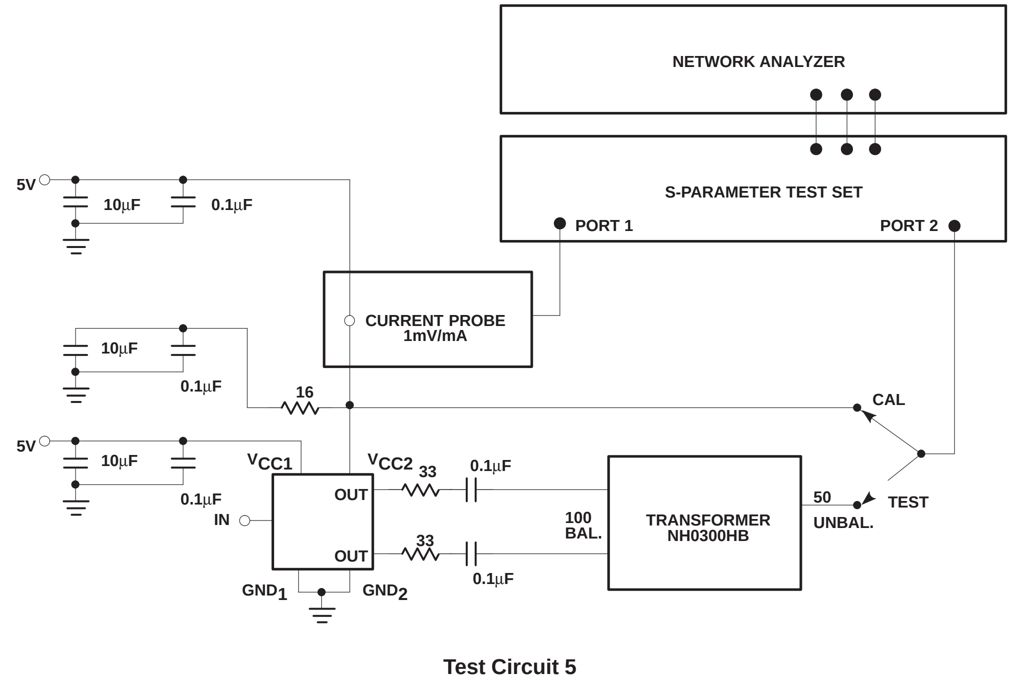


Test Circuit 4

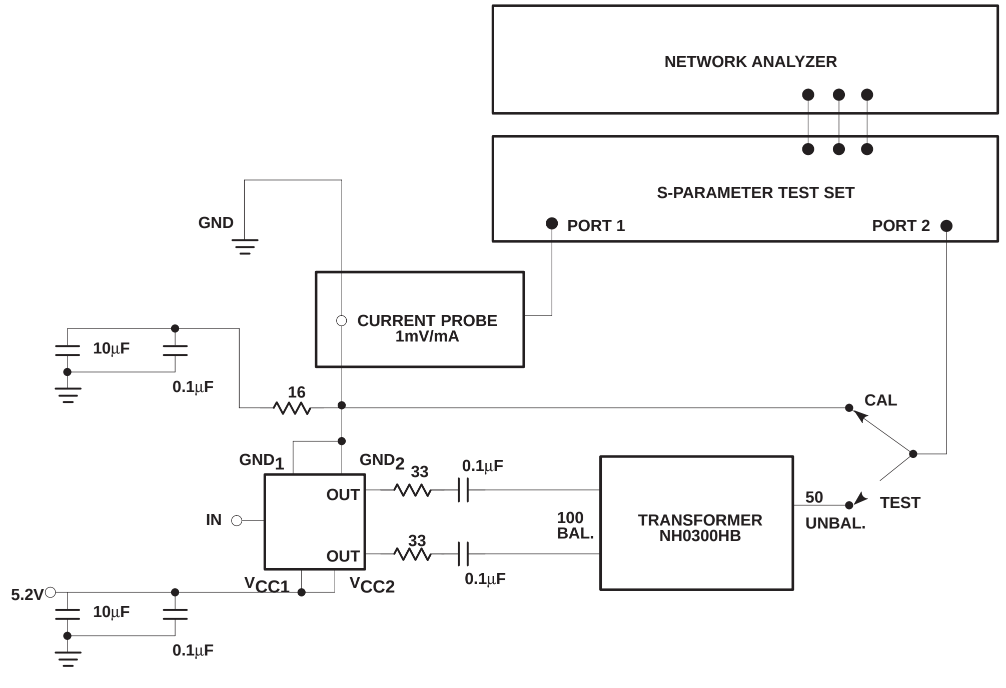
SD00320

Figure 3. Test Circuits 3 and 4

TEST CIRCUITS (Continued)



Test Circuit 5



Test Circuit 6

SD00321

Figure 4. Test Circuits 5 and 6

TEST CIRCUITS (Continued)

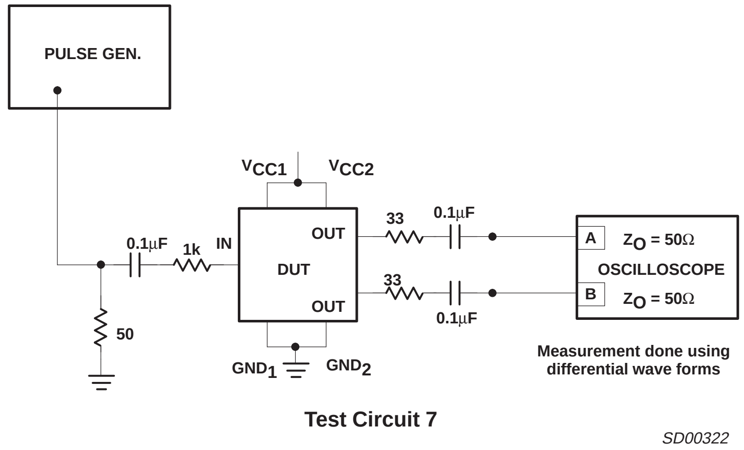
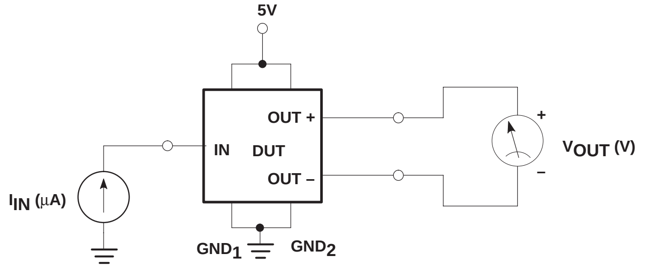
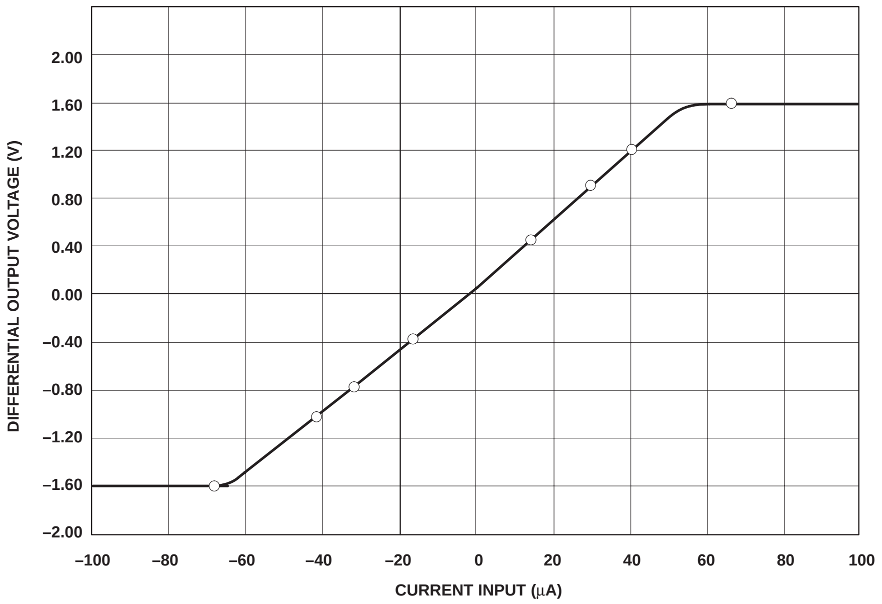


Figure 5. Test Circuit 7

TEST CIRCUITS (Continued)

Typical Differential Output Voltage vs Current Input





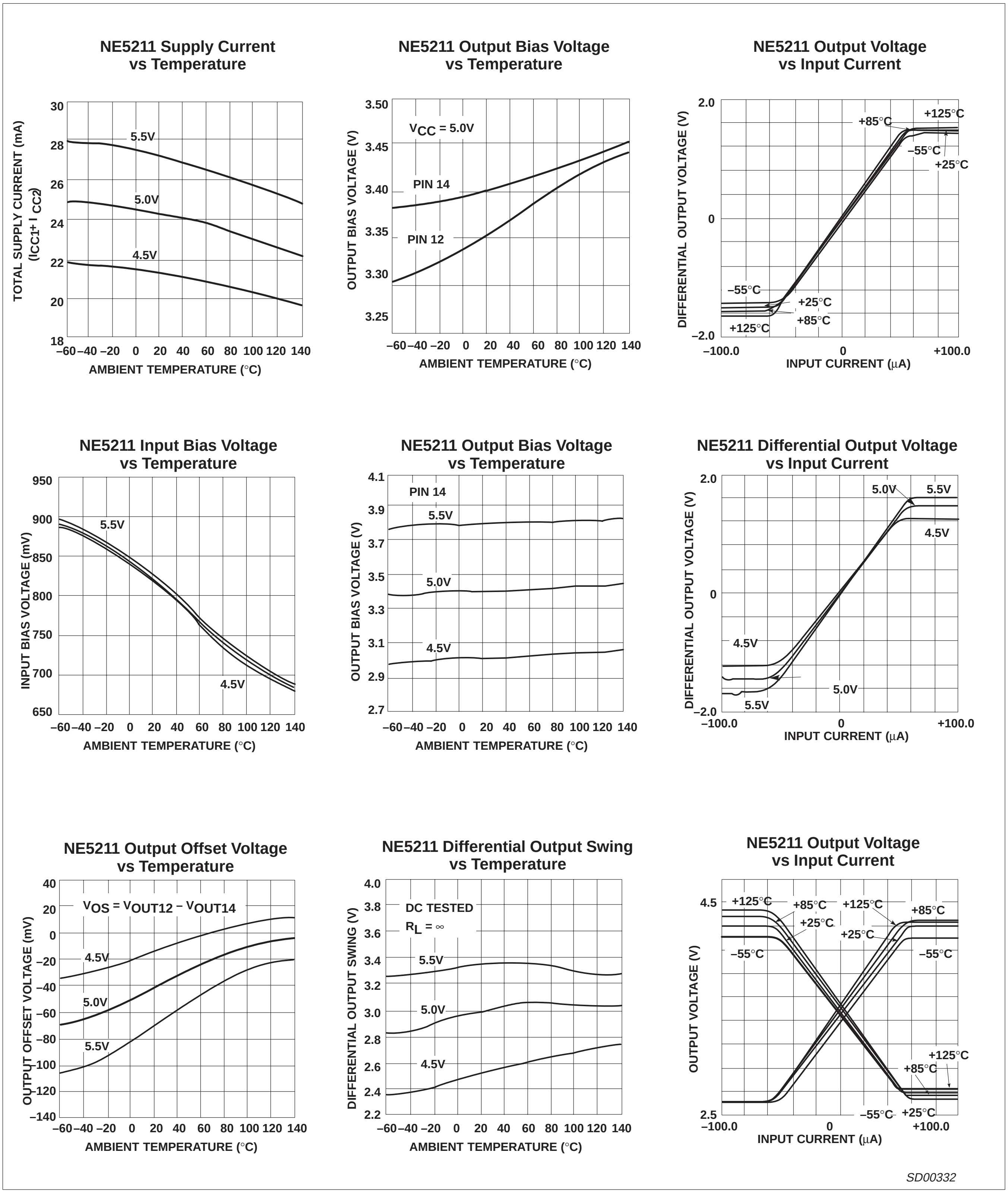
NE5211 TEST CONDITIONS

Procedure 1	R_T measured at 15µA $R_T = (V_{O1} – V_{O2})/(+15µA – (–15µA))$ Where: V_{O1} Measured at I_{IN} = +15µA V_{O2} Measured at I_{IN} = –15µA
Procedure 2	Linearity = 1 – ABS(($V_{OA} – V_{OB}$) / ($V_{O3} – V_{O4}$)) Where: V_{O3} Measured at I_{IN} = +30µA V_{O4} Measured at I_{IN} = –30µA $V_{OA} = R_T \cdot (+\ 30µA) + V_{OB}$ $V_{OB} = R_T \cdot (-\ 30µA) + V_{OB}$
Procedure 3	$V_{OMAX} = V_{O7} – V_{O8}$ Where: V_{O7} Measured at I_{IN} = +65µA V_{O8} Measured at I_{IN} = –65µA
Procedure 4	I_{IN} Test Pass Conditions: $V_{O7} – V_{O5}$ > 20mV and $V_{06} – V_{O5}$ > 50mV Where: V_{O5} Measured at I_{IN} = +40µA V_{O6} Measured at I_{IN} = –400µA V_{O7} Measured at I_{IN} = +65µA V_{O8} Measured at I_{IN} = –65µA

Test Circuit 8 *SD00331*

Figure 6. Test Circuit 8

TYPICAL PERFORMANCE CHARACTERISTICS



NE5211 Supply Current vs Temperature

NE5211 Output Bias Voltage vs Temperature

NE5211 Output Voltage vs Input Current

NE5211 Input Bias Voltage vs Temperature

NE5211 Output Bias Voltage vs Temperature

NE5211 Differential Output Voltage vs Input Current

NE5211 Output Offset Voltage vs Temperature

NE5211 Differential Output Swing vs Temperature

NE5211 Output Voltage vs Input Current

Figure 7. Typical Performance Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

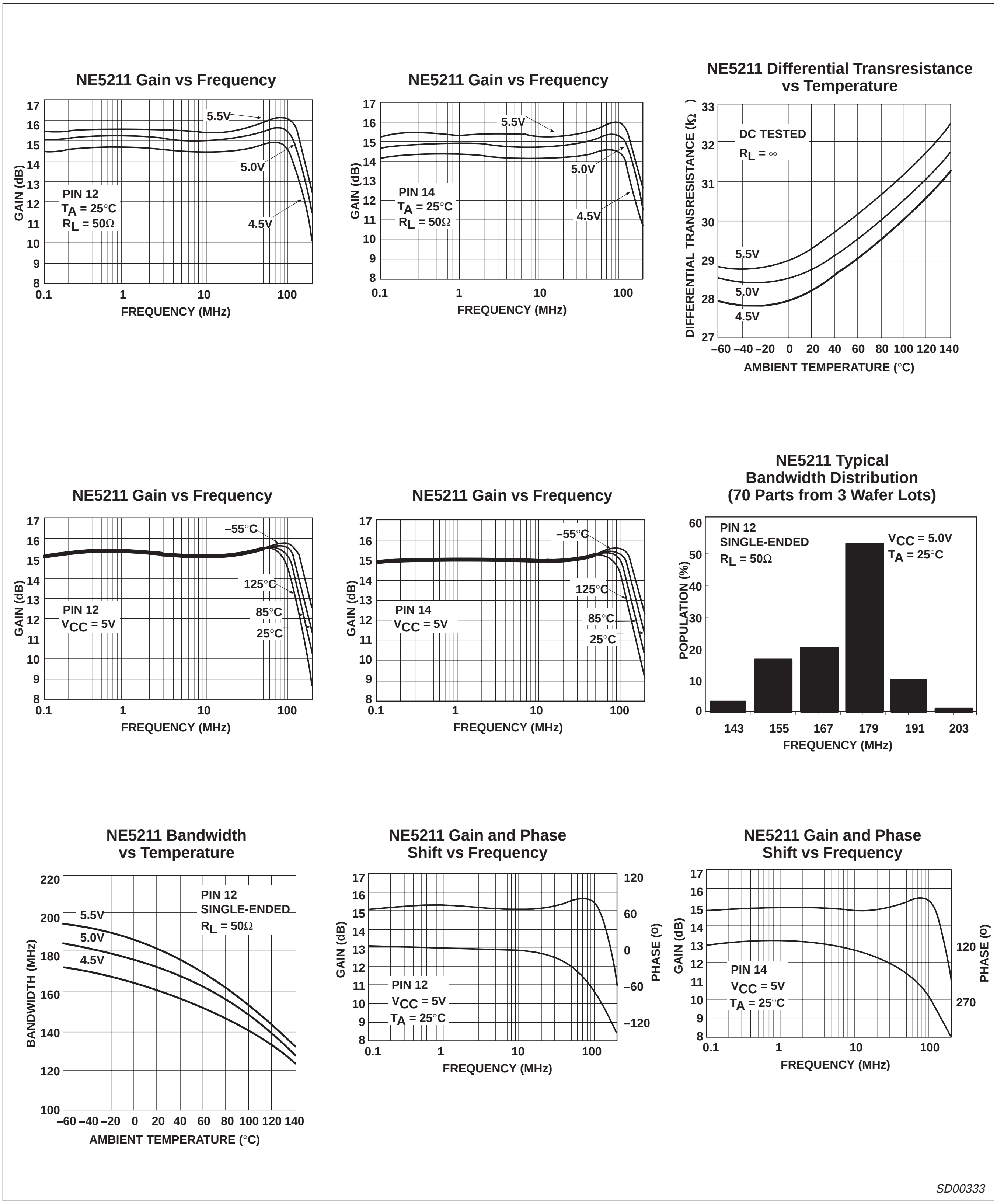
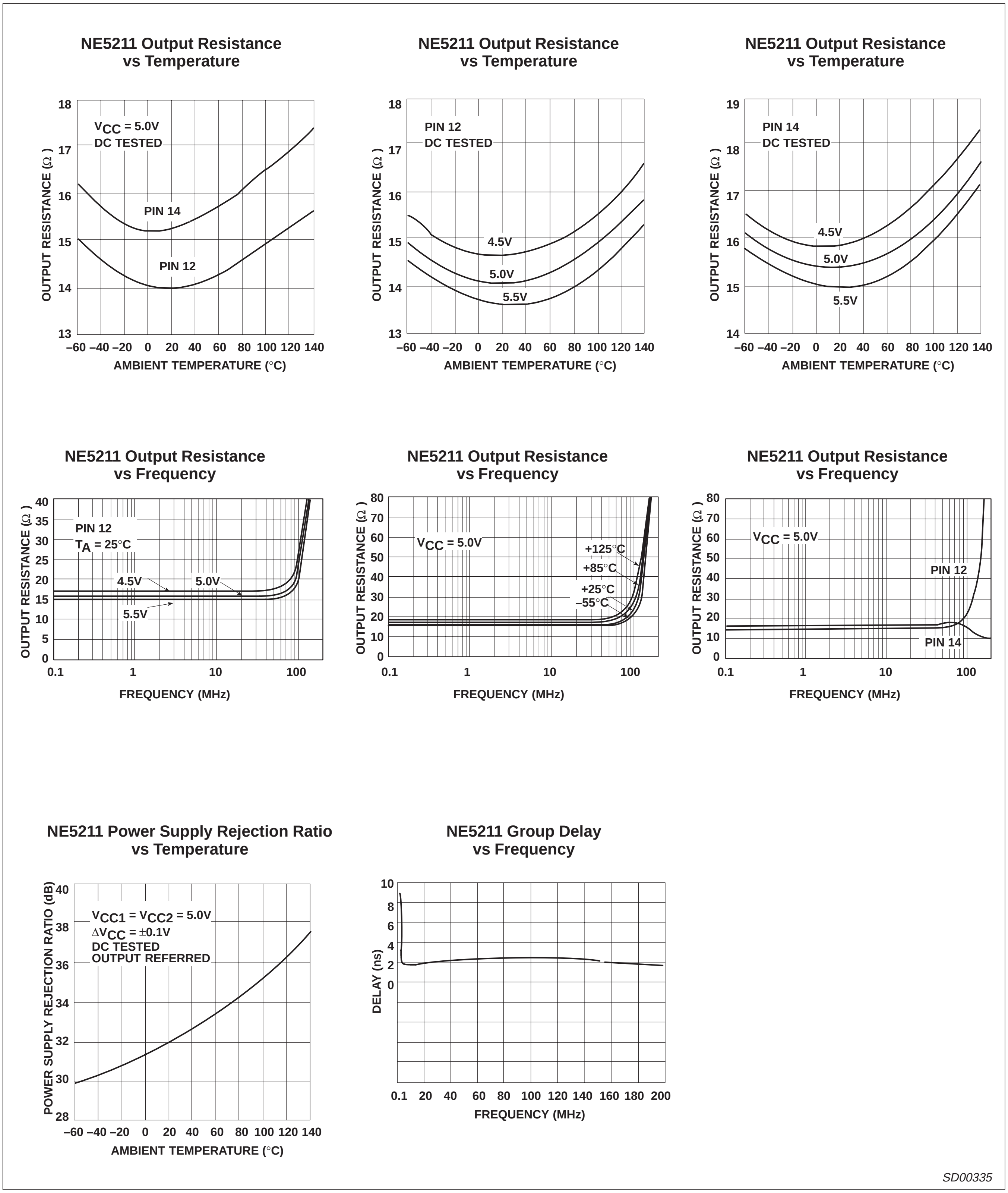


Figure 8. Typical Performance Characteristics (cont.)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



NE5211 Output Resistance vs Temperature

NE5211 Output Resistance vs Temperature

NE5211 Output Resistance vs Temperature

NE5211 Output Resistance vs Frequency

NE5211 Output Resistance vs Frequency

NE5211 Output Resistance vs Frequency

NE5211 Power Supply Rejection Ratio vs Temperature

NE5211 Group Delay vs Frequency

Figure 9. Typical Performance Characteristics (cont.)

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

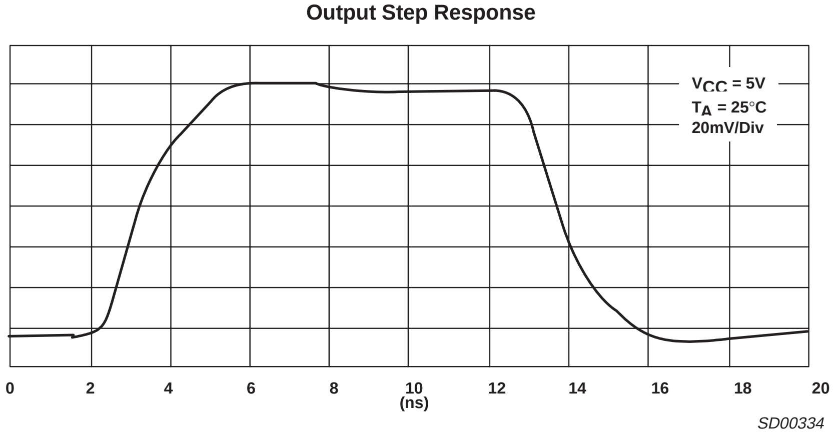

Output Step Response

Figure 10. Typical Performance Characteristics (cont.)

THEORY OF OPERATION

Transimpedance amplifiers have been widely used as the preamplifier in fiber-optic receivers. The SA5211 is a wide bandwidth (typically 180MHz) transimpedance amplifier designed primarily for input currents requiring a large dynamic range, such as those produced by a laser diode. The maximum input current before output stage clipping occurs at typically 50µA. The SA5211 is a bipolar transimpedance amplifier which is current driven at the input and generates a differential voltage signal at the outputs. The forward transfer function is therefore a ratio of the differential output voltage to a given input current with the dimensions of ohms. The main feature of this amplifier is a wideband, low-noise input stage which is desensitized to photodiode capacitance variations. When connected to a photodiode of a few picoFarads, the frequency response will not be degraded significantly. Except for the input stage, the entire signal path is differential to provide improved power-supply rejection and ease of interface to ECL type circuitry. A block diagram of the circuit is shown in Figure 11. The input stage (A1) employs shunt-series feedback to stabilize the current gain of the amplifier. The transresistance of the amplifier from the current source to the emitter of Q_3 is approximately the value of the feedback resistor, R_F=14.4kΩ. The gain from the second stage (A2) and emitter followers (A3 and A4) is about two. Therefore, the differential transresistance of the entire amplifier, R_T is

$$R_T = \frac{V_{OUT}(\text{diff})}{I_{IN}} = 2R_F = 2(14.4K) = 28.8k\Omega$$

The single-ended transresistance of the amplifier is typically 14.4kΩ.

The simplified schematic in Figure 12 shows how an input current is converted to a differential output voltage. The amplifier has a single input for current which is referenced to Ground 1. An input current from a laser diode, for example, will be converted into a voltage by the feedback resistor R_F. The transistor Q1 provides most of the open loop gain of the circuit, $A_{VOL} \approx 70$. The emitter follower Q_2 minimizes loading on Q_1. The transistor Q_4, resistor R_7, and V_{B1} provide level shifting and interface with the Q_{15} – Q_{16} differential pair of the second stage which is biased with an internal reference, V_{B2}. The differential outputs are derived from emitter followers Q_{11} – Q_{12} which are biased by constant current sources. The collectors of Q_{11} – Q_{12} are bonded to an external pin, V_{CC2}, in order to reduce the feedback to the input stage. The output impedance is about 17Ω single-ended. For ease of performance evaluation, a 33Ω resistor is used in series with each output to match to a 50Ω test system.

BANDWIDTH CALCULATIONS

The input stage, shown in Figure 13, employs shunt-series feedback to stabilize the current gain of the amplifier. A simplified analysis can determine the performance of the amplifier. The equivalent input capacitance, C_{IN}, in parallel with the source, I_S, is approximately 7.5pF, assuming that C_S=0 where C_S is the external source capacitance.

Since the input is driven by a current source the input must have a low input resistance. The input resistance, R_{IN}, is the ratio of the incremental input voltage, V_{IN}, to the corresponding input current, I_{IN} and can be calculated as:

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{R_F}{1 + A_{VOL}} = \frac{14.4K}{71} = 203\Omega$$

More exact calculations would yield a higher value of 200Ω.

Thus C_{IN} and R_{IN} will form the dominant pole of the entire amplifier;

$$f_{-3dB} = \frac{1}{2\pi\ R_{IN}\ C_{IN}}$$

Assuming typical values for R_F = 14.4kΩ, R_{IN} = 200Ω, C_{IN} = 4pF

$$f_{-3dB} = \frac{1}{2\pi\ 4pF\ 200\Omega} = 200MHz$$

The operating point of Q1, Figure 12, has been optimized for the lowest current noise without introducing a second dominant pole in the pass-band. All poles associated with subsequent stages have been kept at sufficiently high enough frequencies to yield an overall single pole response. Although wider bandwidths have been achieved by using a cascade input stage configuration, the present solution has the advantage of a very uniform, highly desensitized frequency response because the Miller effect dominates over the external photodiode and stray capacitances. For example, assuming a source capacitance of 1pF, input stage voltage gain of 70, R_{IN} =

60Ω then the total input capacitance, C_{IN} = 4 pF which will lead to only a 12% bandwidth reduction.

NOISE

Most of the currently installed fiber-optic systems use non-coherent transmission and detect incident optical power. Therefore, receiver noise performance becomes very important. The input stage achieves a low input referred noise current (spectral density) of $2.9\mathrm{pA}/\sqrt{\mathrm{Hz}}$. The transresistance configuration assures that the external high value bias resistors often required for photodiode biasing will not contribute to the total noise system noise. The equivalent input $_{RMS}$ noise current is strongly determined by the quiescent current of Q_1, the feedback resistor R_F, and the bandwidth; however, it is not dependent upon the internal Miller-capacitance. The measured wideband noise was 41nA RMS in a 200MHz bandwidth.

DYNAMIC RANGE CALCULATIONS

The electrical dynamic range can be defined as the ratio of maximum input current to the peak noise current:

Electrical dynamic range, D_E, in a 200MHz bandwidth assuming I_{INMAX} = 60μA and a wideband noise of I_{EQ}=41nA$_{RMS}$ for an external source capacitance of C_S = 1pF.

$$D_E = \frac{(\text{Max. input current})}{(\text{Peak noise current})}$$

$$D_E(\mathrm{dB}) = 20\log\frac{(60 \cdot 10^{-6})}{(\sqrt{2}\ \ 41\ \ 10^{-9})}$$

$$D_E(\mathrm{dB}) = 20\log\frac{(60\mu A)}{(58nA)} = 60\mathrm{dB}$$

In order to calculate the optical dynamic range the incident optical power must be considered.

For a given wavelength λ;

Energy of one Photon = $\frac{hc}{\lambda}$ watt sec (Joule)

Where h=Planck's Constant = 6.6×10^{-34} Joule sec.

c = speed of light = 3×10^{8} m/sec

c / λ = optical frequency

No. of incident photons/sec= $\frac{P}{\frac{hs}{\lambda}}$ where P=optical incident power

No. of generated electrons/sec = $\eta \cdot \frac{P}{\frac{hs}{\lambda}}$

where η = quantum efficiency

$$= \frac{\text{no. of generated electron hole paris}}{\text{no. of incident photons}}$$

$$\therefore I = \eta \cdot \frac{P}{\frac{hs}{\lambda}} \cdot e \ \ \text{Amps (Coulombs/sec.)}$$

where e = electron charge = 1.6×10^{-19} Coulombs

Responsivity R = $\frac{\eta \cdot e}{\frac{hs}{\lambda}}$Amp/watt

$$I = P \cdot R$$

Assuming a data rate of 400 Mbaud (Bandwidth, B=200MHz), the noise parameter Z may be calculated as:[1]

$$Z = \frac{I_{EQ}}{qB} = \frac{41 \cdot 10^{-9}}{(1.6 \cdot 10^{-19})(200 \cdot 10^{6})} = 1281$$

where Z is the ratio of $_{RMS}$ noise output to the peak response to a single hole-electron pair. Assuming 100% photodetector quantum efficiency, half mark/half space digital transmission, 850nm lightwave and using Gaussian approximation, the minimum required optical power to achieve 10^{-9} BER is:

$$P_{avMIN} = 12\frac{hc}{\lambda}B\ Z = 12 \cdot 2.3 \cdot 10^{-19}$$
$$200 \cdot 10^{6}\ (1281) = 719\mathrm{nW} = -31.5\mathrm{dBm}$$
$$= 1139\mathrm{nW} = -29.4\mathrm{dBm}$$

where h is Planck's Constant, c is the speed of light, λ is the wavelength. The minimum input current to the SA5211, at this input power is:

$$I_{avMIN} = qP_{avMIN}\frac{\lambda}{hc}\quad\frac{1}{\mathrm{Joule}} \cdot \frac{\mathrm{Joule}}{\mathrm{sec}} \cdot q = I$$

$$= \frac{707 \cdot 10^{-9} \cdot 1.6 \cdot 10^{-19}}{2.3 \cdot 10^{-19}}$$

= 500nA

Choosing the maximum peak overload current of I_{avMAX}=60μA, the maximum mean optical power is:

$$P_{avMAX} = \frac{hcI_{avMAX}}{\lambda q} = \frac{2.3 \cdot 10^{-19}}{1.6 \cdot 10^{-19}}\ 60 \cdot 10\mu A$$

$$= 86\mu W \ \text{or} \ -10.6\mathrm{dBm}\ \text{(optical)}$$

Thus the optical dynamic range, D_O is:

$D_O = P_{avMAX} - P_{avMIN} = -4.6 -(-29.4) = 24.8\mathrm{dB}.$

$$D_O = P_{avMAX} - P_{avMIN} = -31.5 - (-10.6)$$
$$= 20.8\mathrm{dB}$$

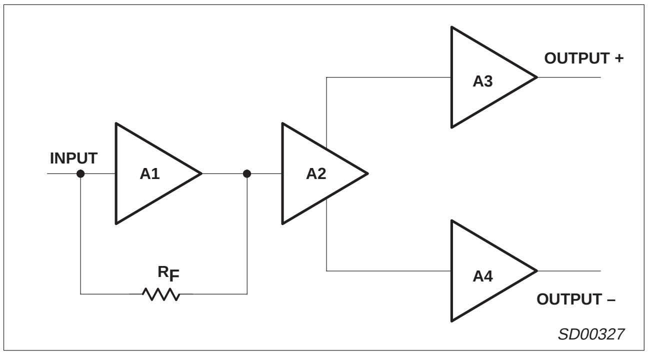


Figure 11. SA5211 – Block Diagram

This represents the maximum limit attainable with the SA5211 operating at 200MHz bandwidth, with a half mark/half space digital transmission at 850nm wavelength.

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[1] S.D. Personick, *Optical Fiber Transmission Systems*, Plenum Press, NY, 1981, Chapter 3.

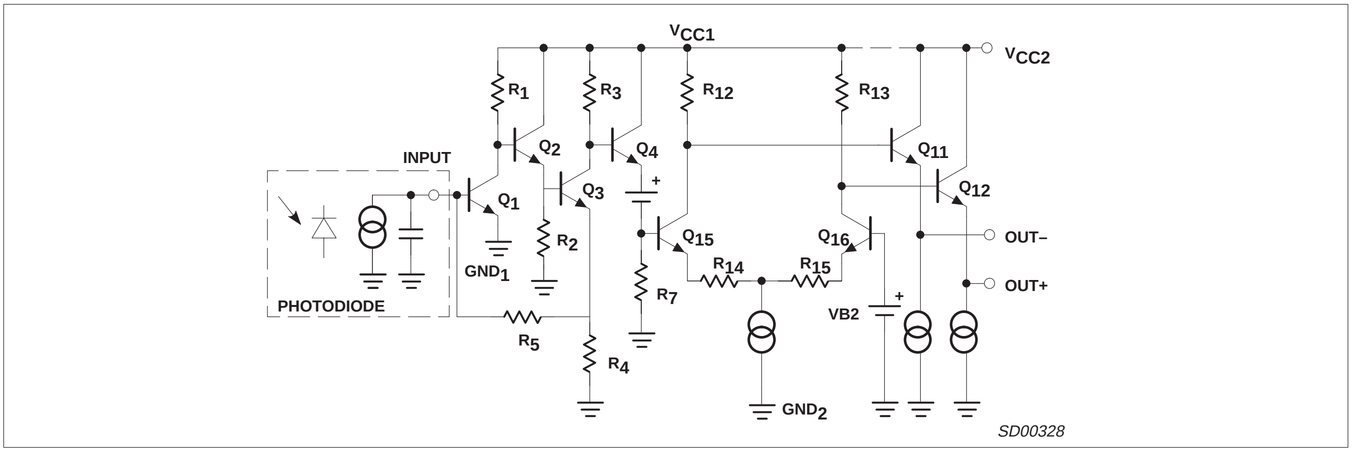


Figure 12. Transimpedance Amplifier

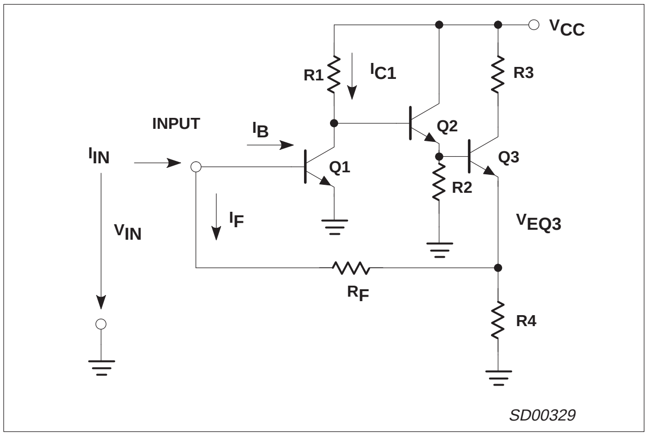


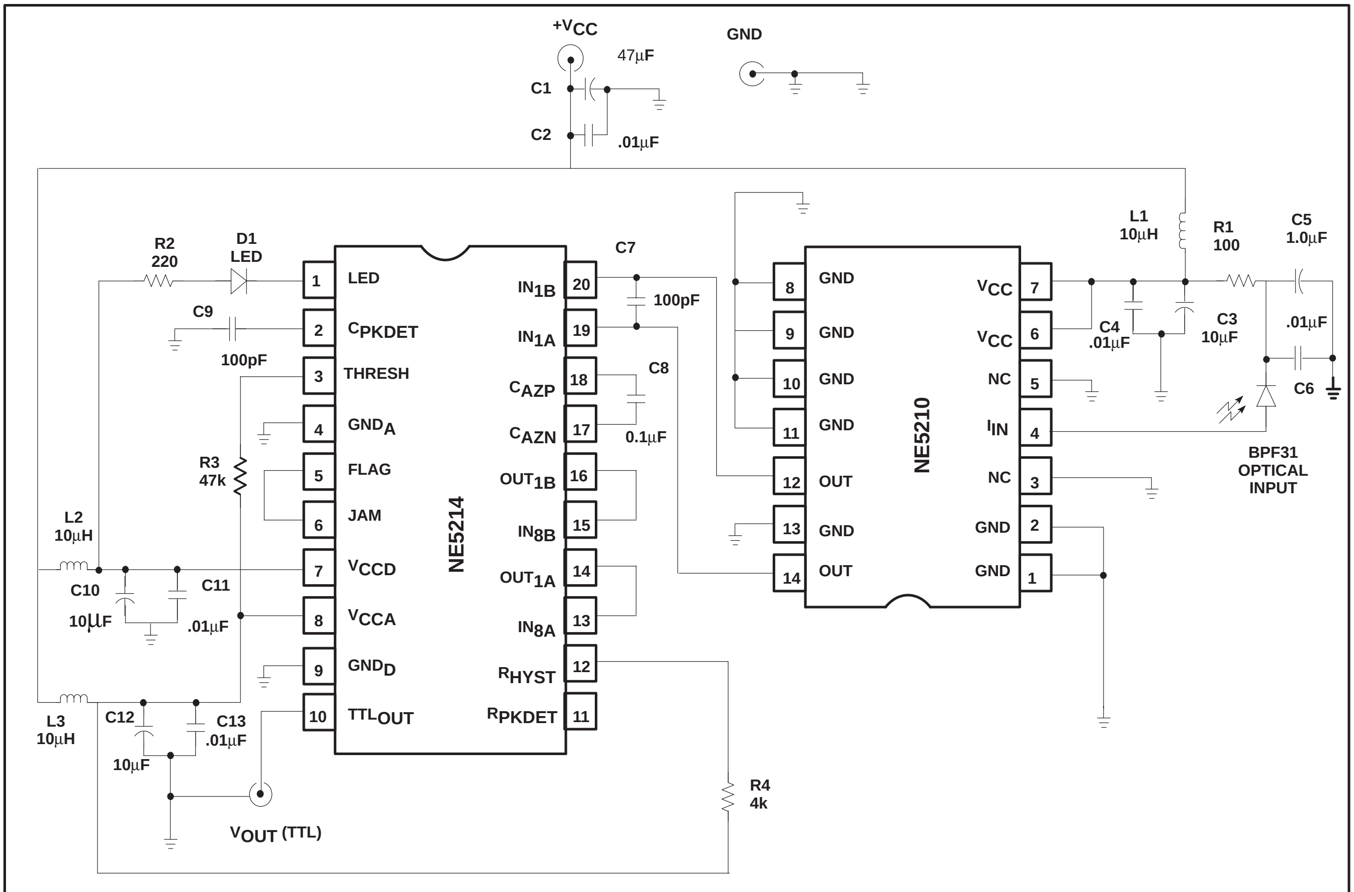
Figure 13. Shunt-Series Input Stage

APPLICATION INFORMATION

Package parasitics, particularly ground lead inductances and parasitic capacitances, can significantly degrade the frequency response. Since the SA5211 has differential outputs which can feed back signals to the input by parasitic package or board layout capacitances, both peaking and attenuating type frequency response shaping is possible. Constructing the board layout so that Ground 1 and Ground 2 have very low impedance paths has produced the best results. This was accomplished by adding a ground-plane stripe underneath the device connecting Ground 1, Pins 8–11, and Ground 2, Pins 1 and 2 on opposite ends of the SO14 package. This ground-plane stripe also provides isolation between the output return currents flowing to either V_{CC2} or Ground 2 and the input photodiode currents to flowing to Ground 1. Without this ground-plane stripe and with large lead inductances on the board, the part may be unstable and oscillate near 800MHz. The easiest way to realize that the part is not functioning normally is to measure the DC voltages at the outputs. If they are not close to their quiescent values of 3.3V (for a 5V supply), then the circuit may be oscillating. Input pin layout necessitates that the photodiode be physically very close to the input and Ground 1. Connecting Pins 3 and 5 to Ground 1 will tend to shield the input but it will also tend to increase the capacitance on the input and slightly reduce the bandwidth.

As with any high-frequency device, some precautions must be observed in order to enjoy reliable performance. The first of these is the use of a well-regulated power supply. The supply must be capable of providing varying amounts of current without significantly changing the voltage level. Proper supply bypassing requires that a good quality 0.1µF high-frequency capacitor be inserted between V_{CC1} and V_{CC2}, preferably a chip capacitor, as close to the package pins as possible. Also, the parallel combination of 0.1µF capacitors with 10µF tantalum capacitors from each supply, V_{CC1} and V_{CC2}, to the ground plane should provide adequate decoupling. Some applications may require an RF choke in series with the power supply line. Separate analog and digital ground leads must be maintained and printed circuit board ground plane should be employed whenever possible.

Figure 14 depicts a 50Mb/s TTL fiber-optic receiver using the BPF31, 850nm LED, the SA5211 and the SA5214 post amplifier.



NOTE:
The NE5210/NE5217 combination can operate at data rates in excess of 100Mb/s NRZ
The capacitor C7 decreases the NE5210 bandwidth to improve overall S/N ratio in the DC–50MHz band, but does create extra high frequency noise on the NE5210 V_{CC} pin(s).

SD00330

Figure 14. A 50Mb/s Fiber Optic Receiver

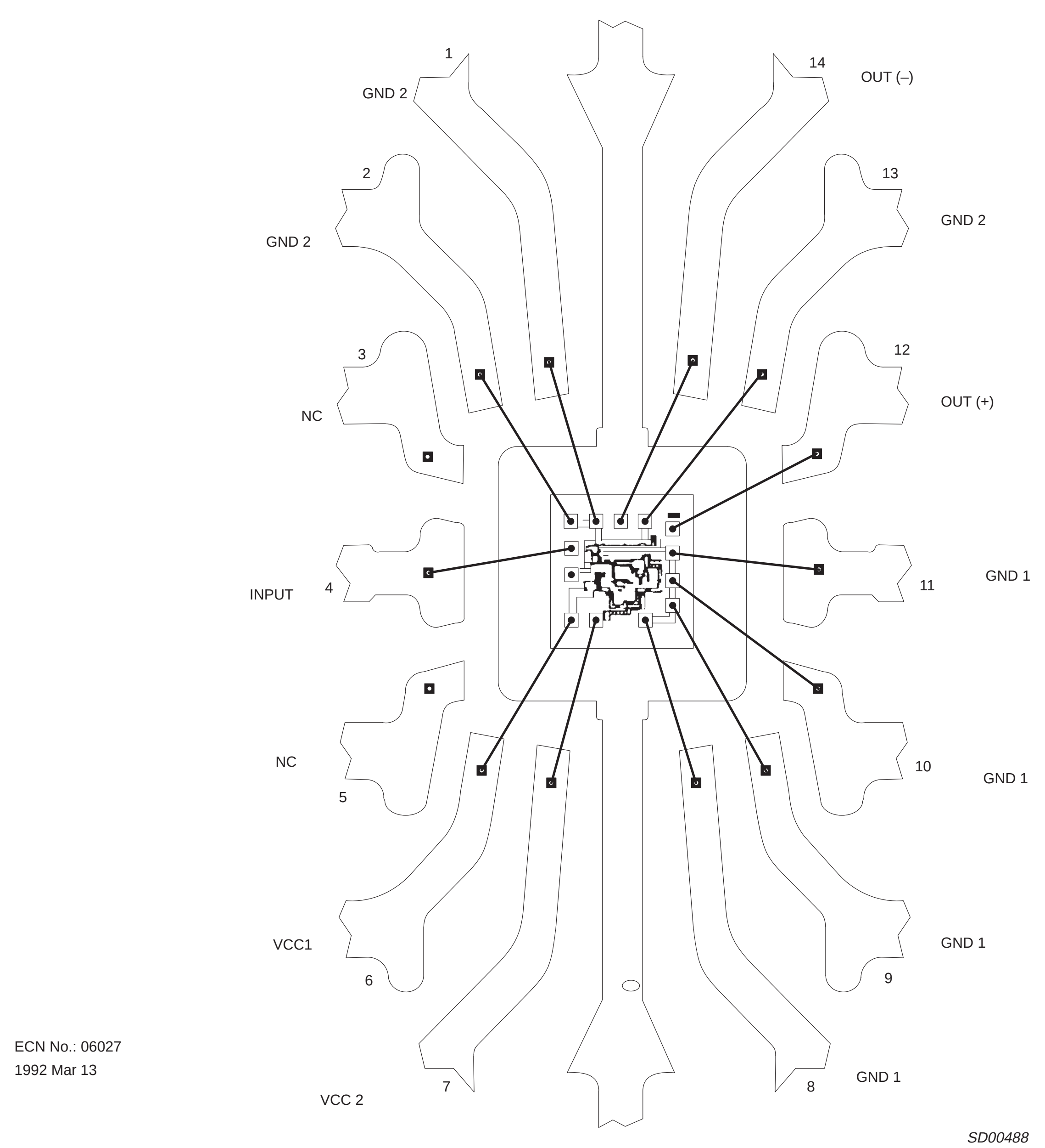


Figure 15. SA5211 Bonding Diagram

Die Sales Disclaimer

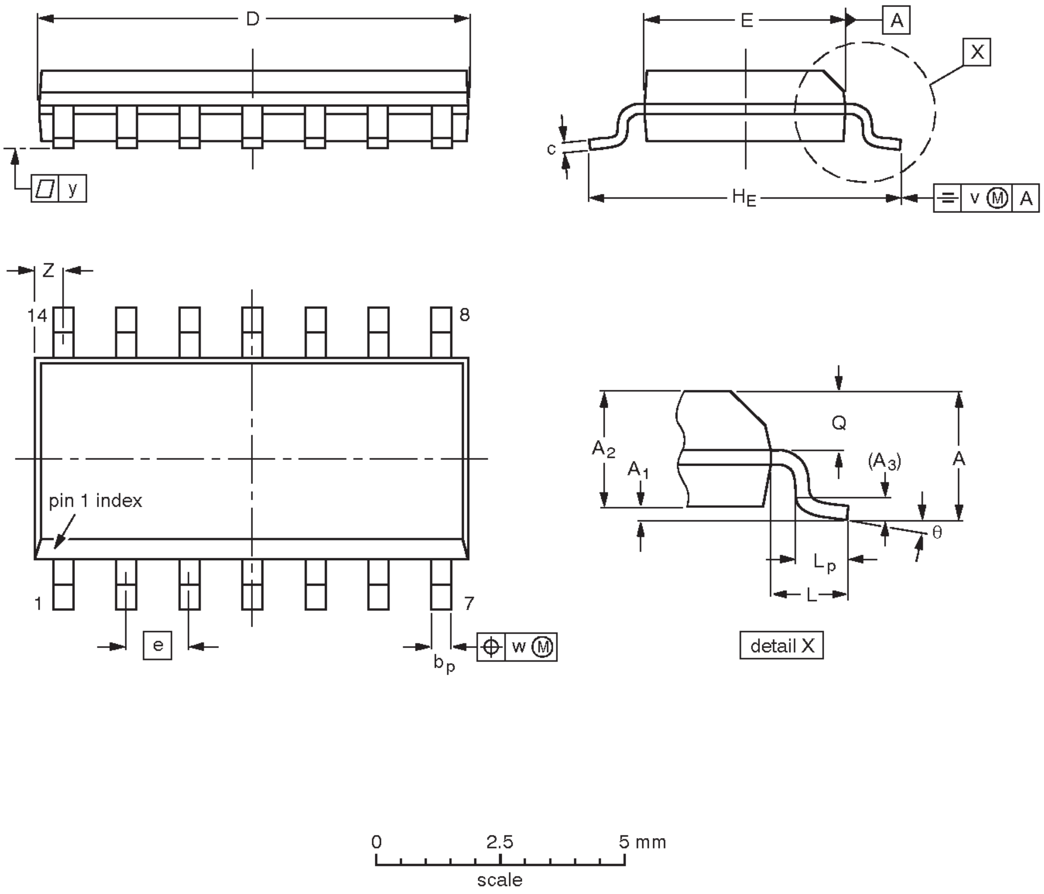
Due to the limitations in testing high frequency and other parameters at the die level, and the fact that die electrical characteristics may shift after packaging, die electrical parameters are not specified and die are not guaranteed to meet electrical characteristics (including temperature range) as noted in this data sheet which is intended only to specify electrical characteristics for a packaged device.

All die are 100% functional with various parametrics tested at the wafer level, at room temperature only (25°C), and are guaranteed to be 100% functional as a result of electrical testing to the point of wafer sawing only. Although the most modern processes are utilized for wafer sawing and die pick and place into waffle pack carriers, it is impossible to guarantee 100% functionality through this process. There is no post waffle pack testing performed on individual die.

Since Philips Semiconductors has no control of third party procedures in the handling or packaging of die, Philips Semiconductors assumes no liability for device functionality or performance of the die or systems on any die sales.

Although Philips Semiconductors typically realizes a yield of 85% after assembling die into their respective packages, with care customers should achieve a similar yield. However, for the reasons stated above, Philips Semiconductors cannot guarantee this or any other yield on any die sales.

SO14: plastic small outline package; 14 leads; body width 3.9 mm SOT108-1

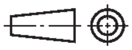


DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				~~95-01-23~~ 97-05-22

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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