National Semiconductor

November 2006

SCAN25100
2457.6, 1228.8, and 614.4 Mbps CPRI SerDes with Auto RE Sync and Precision Delay Calibration Measurement

General Description

The SCAN25100 is a 2457.6, 1228.8, and 614.4 Mbps serializer/deserializer (SerDes) for high-speed bidirectional serial data transmission over FR-4 printed circuit board backplanes, balanced cables, and optical fiber. The SCAN25100 integrates precision delay calibration measurement (DCM) circuitry that measures link delay components to better than ± 800 ps accuracy.

The SCAN25100 features independent transmit and receive PLLs, on-chip oscillator, and intelligent clock management circuitry to automatically perform remote radio head synchronization and reduce the cost and complexity of external clock networks.

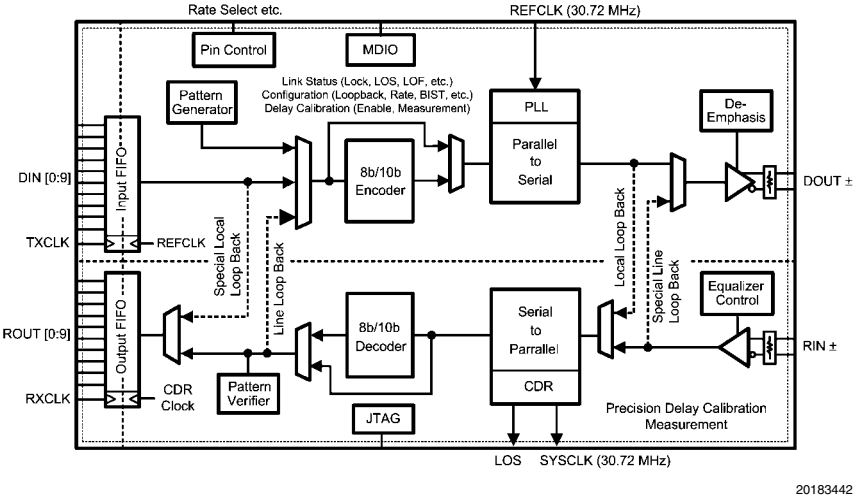
The SCAN25100 is programmable though an MDIO interface as well as through pins, featuring configurable transmitter de-emphasis, receiver equalization, speed rate selection, internal pattern generation/verification, and loop back modes. In addition to at-speed BIST, the SCAN25100 includes IEEE 1149.1 and 1149.6 testability.

Note: For a full datasheet of the SCAN25100 please contact your local National Semiconductor representitive.

Features

- Exceeds LV and HV CPRI voltage and jitter requirements
- 2457.6, 1228.8, and 614.4 Mbps operation
- Integrated delay calibration measurement (DCM) directly measures T14 and Toffset delays to ≤ ± 800 ps
- DCM also measures chip and other delays to ≤ ± 1200 ps accuracy
- Deterministic chip latency
- Automatic receiver lock and RE synchronization without reference clock or external crystal
- Independent transmit and receive PLLs for seamless RE synchronization
- Low noise recovered clock output
- Requires no jitter cleaning in single-hop applications
- >8 kV ESD on the CML IO, >7 kV on all other pins, >2 kV CDM
- Hot plug protection
- LOS, LOF, 8b/10b line code violation, comma, and receiver PLL lock reporting
- Programmable hyperframe length and start of hyperframe character
- Programmable transmit de-emphasis and receive equalization with on-chip termination
- Advanced testability features
  - IEEE 1149.1 and 1149.6
  - At-speed BIST pattern generator/verifier
  - Multiple loopback modes
- 1.8V or 3.3V compatible parallel bus interface
- 100-pin TQFP package with exposed dap
- Industrial –40 to +85° C temperature range

Block Diagram



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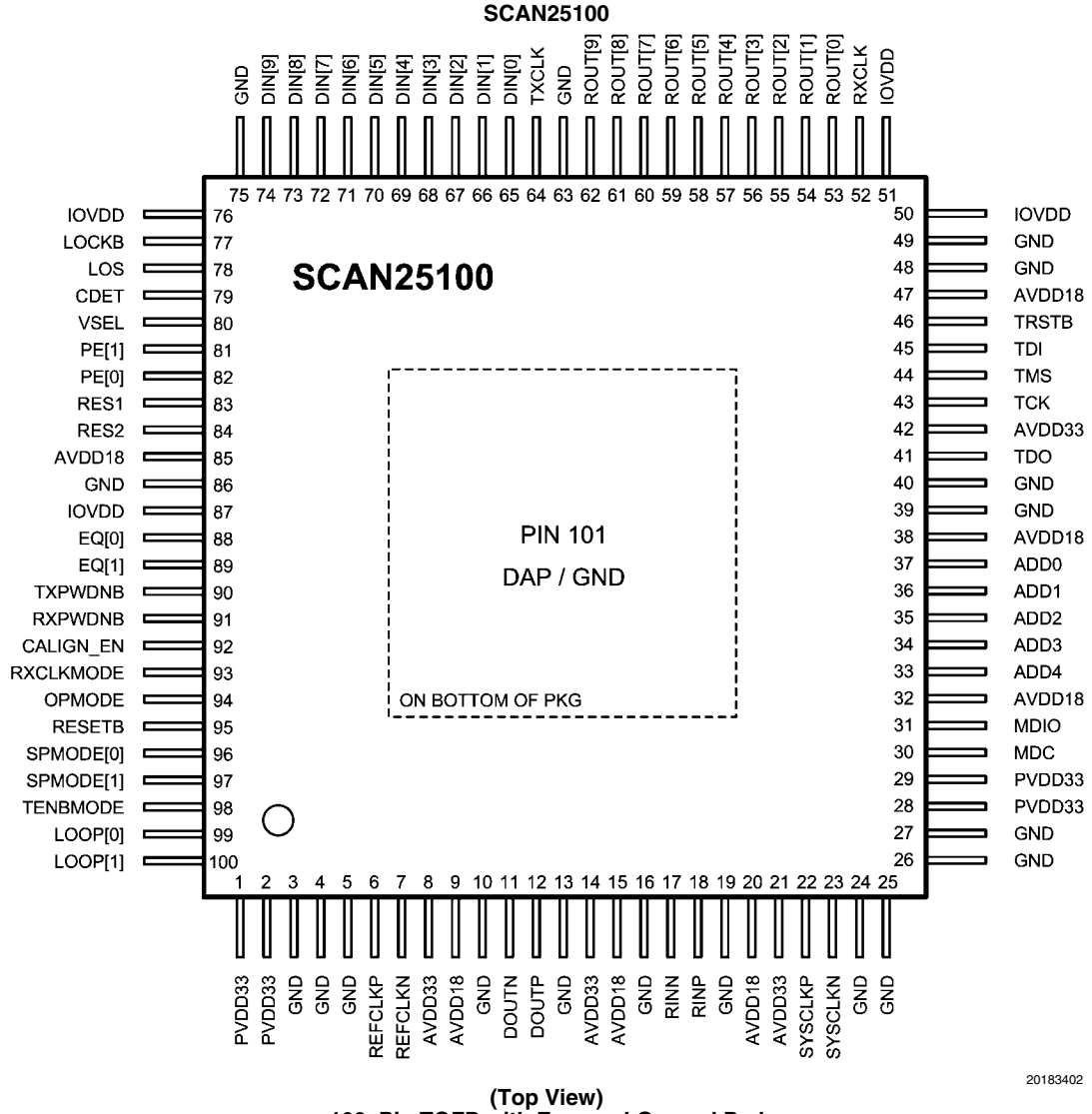
Pin Diagram



(Top View)
100–Pin TQFP with Exposed Ground Pad
Order Number SCAN25100TYA
See NS Number VXF100B

Pin Descriptions

Pin #	Pin Name	I/O, Type	Description
HIGH SPEED DIFFERENTIAL I/O			
12 11	DOUTP DOUTN	O, CML	Inverting and non-inverting high speed CML differential outputs of the serializer. On-chip termination resistors connect from DO+ and DO– to an internal reference
18 17	RINP RINN	I, CML	Inverting and non-inverting high speed differential inputs of the deseralizer. On-chip termination resistors connect from RI+ and RI– to an internal reference. On-chip termination resistors are configured for AC-coupled applications.
PARALLEL DATA BUS			
65 66 67 68 69 70 71 72 73 74	DIN [0] DIN [1] DIN [2] DIN [3] DIN [4] DIN [5] DIN [6] DIN [7] DIN [8] DIN [9]	I, LVTTL or 1.8V LVCMOS Internal pull down	Transmit data word. In 10-bit mode, the 10-bit code-group at DIN [0–9] is serialized with the internal 8b/10b encoder disabled. Bit 9 is the msb. The 8B/10B specification is defined in IEEE 802.3-2000 section 36.2.2
53 54 55 56 57 58 59 60 61 62	ROUT [0] ROUT [1] ROUT [2] ROUT [3] ROUT [4] ROUT [5] ROUT [6] ROUT [7] ROUT [8] ROUT [9]	O, LVTTL or 1.8V LVCMOS Internal pull down	Deserialized receive data word. In 10-bit mode, ROUT [0-9] is the deserialized received data word in 10-bit code group. Bit 9 is the msb. The 8B/10B specification is defined in IEEE 802.3-2000 section 36.2.2
CLOCK SIGNALS			
6 7	REFCLKP REFCLKN	I, LVDS or LVPECL	Inverting and non-inverting differential serializer reference clock. A low jitter clock source should be connected to REFCLKP & REFCLKN.
64	TXCLK	I, LVTTL or 1.8V LVCMOS Internal pull down	Transmit clock. TXCLK must be synchronous to REFCLK to avoid FIFO under/overflow though it may differ in phase.
52	RXCLK	I/O, LVTTL or 1.8V LVCMOS	Write mode: RXCLK is a recovered clock output pin. Read mode: RXCLK is an input pin. ROUT [9:0] are latched out on RXCLK rising and falling edges. RXCLK must be synchronous to the incoming serial data to avoid FIFO over/underflow, though it may differ in phase. See RXCLKMODE pin description for more details.
22 23	SYSCLKP SYSCLKN	O, LVDS	30.72 MHz output clock. (OPMODE must be low.)
LINE STATUS			
78	LOS	O, LVTTL or 1.8V LVCMOS	Receiver CPRI loss of signal (LOS) status (8-bit mode only). 0 = signal detected (per CPRI standard) 1 = signal lost (per CPRI standard) See “LOS Detection” under “Functional Description” for more details.
77	LOCKB	O, LVTTL or 1.8V LVCMOS	Receiver PLL lock status 0 = Receiver PLL locked 1 = Receiver PLL not locked

Pin #	Pin Name	I/O, Type	Description
79	CDET	O, LVTTL or 1.8V LVCMOS	Comma Detect. 0 = no comma yet detected in the incoming serial stream or receiver PLL not locked. 1 = the receiver PLL is locked and a positive or negative comma bit sequence detected in the incoming bit stream. The serial to parallel converter is aligned to the proper 10-bit word boundary when comma alignment is enabled (CALIGN_EN = 1).
CONTROL PINS			
82 81	PE [0] PE [1]	I, LVTTL or 1.8V LVCMOS Internal pull down	Transmitter de-emphasis configuration. Pulling both pins low enables MDIO control, default is no de-emphasis.
			PE1 / **PE0** /
			0 / 0 / No de-emphasis
			0 / 1 / Low de-emphasis
			1 / 0 / Medium de-emphasis
			1 / 1 / Maximum de-emphasis
88 89	EQ [0] EQ [1]	I, LVTTL or 1.8V LVCMOS Internal pull down	Receive input equalization configuration. Pulling both pins low enables MDIO control, default is no receive equalization.
			EQ1 / **EQ0** /
			0 / 0 / No receive equalization
			0 / 1 / Low receive equalization
			1 / 0 / Medium receive equalization
			1 / 1 / Maximum receive equalization
90 91	TXPWDNB RXPWDNB	I, LVTTL or 1.8V LVCMOS Internal pull down	Power down control signals. **TXPWDNB** 0 = Transmitter is powered down and DOUT± pins are high impedance. 1 = Transmitter is powered up. **RXPWDNB** 0 = Receiver is powered down and ROUT [9:0] as well as LOS, LOCKB, CDET, RXCLK, and SYSCLK are high impedance. 1 = Receiver is powered up.
92	CALIGN_EN	I, LVTTL or 1.8V LVCMOS Internal pull down	Comma alignment enable. 0 = comma alignment circuitry disabled. 1 = comma detect and alignment circuitry enabled. Receiver aligns 10-bit data to incoming comma character and flags comma detect through CDET pin.
93	RXCLKMODE	I, LVTTL or 1.8V LVCMOS Internal pull down	Receiver recovered clock mode 0 = Write mode. RXCLK pin is a recovered clock output. (RXCLK = output pin) 1 = Read mode. RXCLK pin is the ROUT [9:0] bus read input strobe. (RXCLK = input pin)
80	VSEL	I, LVTTL or 1.8V LVCMOS Internal pull down	Selects whether single-ended data and control pins are 3.3V LVTTL or 1.8V LVCMOS. 0 = 1.8V LVCMOS. Tie VSEL to ground and power IOVDD at 1.8 V. 1 = 3.3V LVTTL. Tie VSEL to IOVDD supply and power IOVDD at 3.3 V.
94	OPMODE	I, LVTTL or 1.8V LVCMOS Internal pull down	Selects SerDes mode. 0 = Base station mode 1 = Reserved for future use
95	RESETB	I, LVTTL or 1.8V LVCMOS Internal pull down	Hardware SerDes reset. Resets PLLs and MDIO registers. 0 = Hardware SerDes reset 1 = Normal operation

Pin #	Pin Name	I/O, Type	Description		
96 97	SPMODE [0] SPMODE [1]	I, LVTTL or 1.8V LVCMOS Internal pull down	Speed mode configuration. (OPMODE must be low) Pulling both pins low enables MDIO control.		
			SPMODE [1]	**SPMODE [0]**	
			0	0	Rate selected via MDIO
			0	1	614.4 Mbps rate mode
			1	0	1228.8 Mbps rate mode
			1	1	2457.6 Mbps rate mode
98	TENBMODE	I, LVTTL or 1.8V LVCMOS, Internal pull down	Enable 10-bit mode The 8B/10B specification is defined in IEEE 802.3-2000 section 36.2.2 0 = Selects 8-bit mode. Enables the internal 8b/10b encoder and decoder. 1 = Selects 10-bit mode. Bypasses internal 8b/10b encoder and decoder.		
99 100	LOOP [0] LOOP [1]	I, LVTTL or 1.8V LVCMOS, Internal pull down	Loop back configuration. Pulling both pins low enables MDIO control. Note: During Special line (remote) loop back mode, output de-emphasis control is disabled.		
			LOOP [1]	**LOOP [0]**	
			0	0	Normal mode—no loop back
			0	1	Line (remote) loop back mode
			1	0	Local loop back mode
			1	1	Special line (remote) loop back mode
MDC/MDIO					
30 31 37 36 35 34 33	MDC MDIO ADD0 ADD1 ADD2 ADD3 ADD4	3.3V LVTTL Internal pull up on ADDR pins	MDC/MDIO configuration bus. Protocol per IEEE 802.2ae-2002 MDC/MDIO Clause 45. These pins are 3.3V LVTTL compatible, not 1.2V signal compatible.		
IEEE 1149.1 (JTAG)					
45 41 44 43 46	TDI TDO TMS TCK TRSTB	3.3V LVTTL Internal pull up on TDI, TMS, and TRSTB	JTAG test bus for IEEE 1149.1 and 1149.6 support.		
RESERVED PINS					
83 84	RES1 RES2	I	Reserved. Tie with 5 KΩ resistor to ground.		
POWER					
9, 15, 20, 32, 38, 47, 85	AVDD18	I, Power	1.8V analog supply.		
8, 14, 21, 42	AVDD33	I, Power	3.3V analog supply.		
1, 2, 28, 29	PVDD33	I, Power	3.3V PLL supply (minimize supply noise to < 100 mV peak-to-peak).		
50, 51, 76, 87	IOVDD	I, Power	1.8V or 3.3V parallel I/O bus and control pin supply. See VSEL pin description for additional information.		
GROUND					
3, 4, 5, 10, 13, 16, 19, 24, 25, 26, 27, 39, 40, 48, 49, 63, 75, 86	GND	I, Ground	Device ground.		

Pin #	Pin Name	I/O, Type	Description
GROUND DAP			
101	GND	I, Ground	Device ground. Pad must be soldered and contected to GND plane with a minimum of 8 thermal vias to achieve specified thermal performance.

Note: I= input O = output Internal pull down = input pin is pulled low by an internal resistor Internal pull up = input pin is pulled high by an internal resistor

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (AV_{DD18})	−0.3V to +2.0V
Supply Voltage (PV_{DD}, IOV_{DD})	−0.3V to +3.6V
Supply Voltage (AV_{DD33})	−0.3V to +3.6V
LVCMOS Input Voltage	−0.3V to (IOV_{DD} + 0.5V)
LVCMOS Output Voltage	−0.3V to (IOV_{DD} + 0.5V)
MDC/MDIO/ADD[0:4],VSEL Input Voltage	−0.3V to (AV_{DD33} + 0.5V)
MDIO Output Voltage	−0.3V to (AV_{DD33} + 0.5V)
CML Receiver Input Voltage	−0.3V to (AV_{DD} + 0.3V)
CML Receiver Output Voltage	−0.3V to (AV_{DD} + 0.3V)
Junction Temperature	+125°C
Storage Temperature	−65°C to +150°C
Lead Temperature	
Soldering, 10–20 sec	235 °C
Lead-free +260°C flow is available	
Maximum Package Power Dissipation at 25°C	
100-pin TQFP with Exposed Pad	4.16 W

Note: This is the maximum TQFP-100 package power dissipation capability. For SCAN25100 power dissipation, see the information in the Electrical Characteristics section.

Derating above 25°C	41.6 mW/°C
Thermal Resistance , θ_{JA} (0 airflow)	24.0°C/W
ESD Rating	
CML RIN/DOUT Pins	
HBM, 1.5 kΩ, 100 pF	>8 kV
EIAJ, 0Ω, 200 pF	>250V
CDM	>2 kV
All Other Pins	
HBM, 1.5 kΩ, 100 pF	>7 kV
EIAJ, 0Ω, 200 pF	>250V
CDM	>2 kV

Recommended Operating Conditions

	Min	Typ	Max	Unit
Supply Voltage				
AV_{DD18}	1.7	1.8	1.9	V
AV_{DD33}, PV_{DD33}	3.135	3.3	3.465	V
IOV_{DD} (1.8V Mode)	1.7	1.8	1.9	V
IOV_{DD} (3.3V Mode)	3.135	3.3	3.465	V
Temperature	-40	25	85	°C
Junction temperature			125	°C
Supply Noise (Peak-to-Peak)			<100	mV

Electrical Characteristics

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Condition	Min	Typ (Note 2)	Max	Units
LVCMOS DC SPECIFICATIONS (1.8V I/O)						
V_{IH}	High level input voltage		$0.65V_{DD}$			V
V_{IL}	Low level input voltage				$0.35V_{DD}$	V
I_{IN}	Input Current	V_{IN} = 0V or 1.9V	−10		+50	µA
V_{OH}	High level output voltage	I_{OH} = −2 mA	1.2			V
V_{OL}	Low level output voltage	I_{OL} = 2 mA			0.45	V
I_{OZ}	Power Down Output Current	Power down	−20		+20	µA
C_{IO}	Input/Output Capacitance	Typical		2.8		pF
LVCMOS DC SPECIFICATIONS (3.3V I/O)						
V_{IH}	High level input voltage		2			V
V_{IL}	Low level input voltage				0.8	V
I_{IN}	Input Current	V_{IN} = 0V or 3.465V	−10		+50	µA
V_{OH}	High level output voltage	I_{OH} = −2 mA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2 mA			0.4	V
I_{OZ}	Power Down Output Current	Power down	−20		+20	µA
C_{IO}	Input/Output Capacitance	Typical		2.8		pF
JTAG DC SPECIFICATIONS (3.3V I/O)						
V_{IH}	High level input voltage		2			V
V_{IL}	Low level input voltage				0.8	V
I_{IN}	Input Current	V_{IN} = 0V or 3.465V	−35		+35	µA
V_{OH}	High level output voltage	I_{OH} = −2 mA	2.4			V

Symbol	Parameter	Condition	Min	Typ (Note 2)	Max	Units
V_{OL}	Low level output voltage	I_{OL} = 2 mA			0.4	V
C_{IO}	Input/Output Capacitance	Typical		2.8		pF
MDIO/MDC/ADD0-4 DC SPECIFICATIONS						
V_{IH}	High level input voltage		2.0		3.465	V
V_{IL}	Low level input voltage		GND		0.8	V
I_{IN}	Input Current	V_{IN} = 0V or 3.465V	-150		+150	µA
V_{OH}	High level output voltage	I_{OH} = −2 mA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2 mA			0.4	V
I_{OZ}	Power Down Output Current	Power down	−100		+100	µA
C_{IO}	Input/Output Capacitance	Typical		2.8		pF
POWER CONSUMPTION (Powerdown)						
P_{PDN}	Powerdown Mode	Rx and Tx Powerdown		25	40	mW
RECOMMENDED REFCLK INPUT SPECIFICATIONS						
$V_{IDSREFCLK}$	Differential input voltage		± 100			mV_{P-P}
V_{ICM}	Common mode voltage		0.05V		2.4V	V
f_{REF}	REFCLK frequency	OPMODE = 0 (BTS SerDes Mode)	30	30.72	31.5	MHz
df_{REF}	REFCLK frequency variation	Variation from nominal frequency	−100		100	ppm
t_{REF-DC}	REFCLK duty cycle	Between 50% of the differential voltage across REFCLKP and REFCLKN	45		55	%
t_{REF-X}	REFCLK transition time	Transition time between 20% and 80% of the differential voltage across REFCLKP and REFCLKN		300		pS
SYSCLK DC OUTPUT SPECIFICATIONS						
V_{OD}	Differential Output Voltage	R_L = 100Ω	± 250	± 330	± 450	mV
V_{OS}	Offset Voltage		1.125	1.20	1.375	V
I_{OS}	Output Short Circuit Current	Output pair shorted together and tied to GND			35	mA
I_{OZ}	Power Down Output Current	Power down	−30		+30	µA
TRANSMITTER SERIAL TIMING SPECIFICATIONS						
V_{OD}	Output differential voltage swing	PE[1]=0, PE[0]=0	± 550	± 700	± 800	mVp-p
		PE[1]=0, PE[0]=1		± 630		mVp-p
		PE[1]=1, PE[0]=0		± 500		mVp-p
		PE[1]=1, PE[0]=1	± 200	± 360	± 450	mVp-p
R_{DO}	Output differential resistance		80	100	120	Ω
R_O	Output Return Loss	Frequency = 1.229 GHz		-13.4		dB
t_R, t_F	Serial data output transition time (Notes 12, 16)	Measured between 20% and 80%	80	100	130	ps
JIT_{T-DJ}	Serial data output deterministic jitter (Notes 3, 12)	Output CJPAT with BER of 10^{-12} (Note 4)			0.14	UIp-p
JIT_{T-TJ}	Serial data output total jitter (Notes 3, 12)	Output CJPAT pattern with BER of 10^{-12} (Note 4)			0.279	UIp-p
t_{LAT-T}	Transmit latency (Notes 9, 7)	614.4 Mbps		310		ns
		1.228 Gbps		155		
		2.4576 Gbps		80		
$t_{DO-LOCK}$	Maximum lock time	K28.5 pattern at 2457.6 Mbps		110	130	us
RECEIVER SERIAL TIMING SPECIFICATIONS						
V_{ID}	Input voltage	RINP - RINN	± 100		± 1100	mVp-p
V_{CMR}	Receiver common mode voltage			0.9		V

Symbol	Parameter	Condition	Min	Typ (Note 2)	Max	Units
R_R	Differential Input Terminations		80	100	120	Ω
RLR_I	Input Return Loss (Note 12)	Frequency = 1.229 GHz		-20	-15	dB
t_{LAT-R}	Receive latency (Notes 10, 8)	614.4 Mbps		280		ns
		1.228 Gbps		140		ns
		2.4576 Gbps		75		ns
JIT_{R-TOL}	Total input jitter tolerance (Note 12)	Input CJPAT with BER of 10^{-12} (Note 4)			0.66	UIp-p
F_{R-LOCK}	Receiver lock range	Input data rate reference to local transmit data rate.	–200		+200	ppm
t_{R-LOCK}	Maximum lock time	K28.5 pattern at 2457.6 Mbps			1	ms
TRANSMITTER INPUT TIMING SPECIFICATIONS						
t_{S-T}	Setup Time	DIN [9:0] valid to TXCLK rising or falling edge	0.5			ns
t_{H-T}	Hold Time	TXCLK rising or falling edge to DIN [9:0] valid	0.5			ns
t_{DC}	Duty cycle	TXCLK duty cycle	45		55	%
f_{TXCLK}	TXCLK frequency		30		125	MHz
RECEIVER OUTPUT TIMING SPECIFICATIONS (Read Mode RXCLKMODE=1, 1228.8 and 614.4 Mbps only)						
t_{PDRX}	RXCLK Propagation Delay	RXCLK rising or falling edge to ROUT [9:0] valid	2	4	6	ns
t_{DC}	Duty cycle	RXCLK input duty cycle	45		55	%
f_{RXCLKR}	RXCLK input frequency	RXCLK input frequency	30		62.5	MHz
t_R, t_F	Output data transition time	For ROUT [0-9], LOCK, etc. pins. Measured between 20% and 80% levels		0.35		ns
RECEIVER OUTPUT TIMING SPECIFICATIONS (Write Mode RXCLKMODE=0)						
t_{S-R}	Setup Time	ROUT [9:0] valid to RXCLK rising or falling edge (Note 11)	0.9	1.5		ns
t_{H-R}	Hold Time	RXCLK rising or falling edge to ROUT [9:0] valid (Note 11)	0.9	1.5		ns
t_{DC}	Duty cycle	RXCLK duty cycle	45		55	%
f_{RXCLK}	RXCLK frequency		30		125	MHz
t_R, t_F	Output data transition time	For ROUT [0-9], LOCK, etc. pins. Measured between 20% and 80% levels		0.35		ns
CDET OUTPUT TIMING SPECIFICATIONS (Read Mode RXCLKMODE=1, 1228.8 and 614.4 Mbps only)						
t_{PDCD}	CDET Propagation Delay	RXCLK rising or falling edge to CDET	2	4	6	ns
CDET OUTPUT TIMING SPECIFICATIONS (Write Mode RXCLKMODE=0) (Note 5)						
t_{S-C}	Setup Time	CDET valid to RXCLK rising or falling edge	1			ns
t_{H-C}	Hold Time	RXCLK rising or falling edge to CDET valid	1.1			ns
SYSCLK LVDS OUTPUT TIMING SPECIFICATIONS						
$t_{SYSCLKNDC}$	Duty cycle		40		60	%
JIT_{SYSCLK}	Cycle to cycle jitter	(Note 12)		40	65	ps p-p
t_R, t_F	Output transition time	Between 20% and 80% levels (Note 12)	0.1		0.3	ns
MDC/MDIO TIMING SPECIFICATIONS (Clause 45)						
f_{MDC}	MDC Frequency		0		2.5	MHz

Symbol	Parameter	Condition	Min	Typ (Note 2)	Max	Units
t_{S-MDIO}	Setup Time	MDIO (input) valid to MDC rising clock	10			ns
t_{H-MDIO}	Hold Time	MDC rising edge to MDIO (input) invalid	10			ns
t_{D-MDIO}	Delay Time	MDIO (output) delay from MDC rising edge	0		300	ns
t_{X-MDIO}	Transition Time	Measured at MDIO when used as output, CL = 470 pF		1		ns
MINIMUM PULSE WIDTH, Hardware Reset (Note 13)						
t_{TX-RST}	Transmiter Reset	TXPWDNB = 0		1		us
t_{RX-RST}	Receiver Reset	RXPWDNB = 0		1		us
t_{RST}	SerDes Reset	RESETB = 0		1		us
JTAG TIMING SPECIFICATIONS						
f_{JTAG}	JTAG TCK Frequency	R_L= 1000Ω, C_L = 15 pF	25			MHz
t_{R-J} t_{F-J}	TDO data transition time (20% to 80%)			2		ns
t_{S-TDI}	Setup Time TDI to TCK High or Low		2			ns
t_{H-TDI}	Hold Time TDI to TCK High or Low		2			ns
t_{S-TMS}	Setup Time TMS to TCK High or Low		2			ns
t_{H-TMS}	Hold Time TMS to TCK High or Low		2			ns
t_{W-TCK}	TCK Pulse Width		10			ns
t_{W-TRST}	TRSTB Pulse Width		2.5			ns
t_{REC}	Recovery Time TRSTB to TCK		14			ns
DELAY CALIBRATION MEASUREMENT (DCM) (Notes 12, 14, 15)						
T_{14}	T_{14} Delay Accuracy	Receive and Transmit PLLs locked to valid hyperframe data.			± 800	ps
T_{offset}	T_{offset} Delay Accuracy				± 800	ps
T_{ser}	Serializer Delay Accuracy				± 1200	ps
T_{des}	Deserializer Delay Accuracy				± 1200	ps
T_{in-out}	T_{in-out} Delay Accuracy				± 1200	ps
T_{out-in}	T_{out-in} Delay Accuracy				± 1200	ps

Note 1: "Absolute Maximum Ratings" are the ratings beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.

Note 2: Typical parameters are measured at nominal supply levels and T_A = 25°C. They are for reference purposes and are not production-tested.

Note 3: Transmit Jitter testing methodology is defined in Appendix 48B of IEEE 802.2ae-2002. The SCAN25100 transmit output jitter is constant for all valid CPRI datarates. For 614.4 and 1228.8 Mbps rates, the transmit jitter is significantly less then the specified limits in terms of UI.

Note 4: CJPAT is a stress pattern defined in IEEE 802.2ae-2002 Appendix 48A

Note 5: CDET nominal valid duration is determined by the CPRI data rate. CDET timing is similar to the ROUT[0:9] timing.

Note 6: Transmit or Receive K28.5 pattern. Assumes TXCLK is stable and toggles only after all SerDes clocks become synchronous.

Note 7: Transmit latency is fixed once the link is established and is guaranteed by the Tser specification.

Note 8: Receive latency is fixed once the link is established and is guaranteed by the Tdes specification.

Note 9: Conditions: The TX PLL is locked, the TXCLK is stable and the TXCLK is synchronous.

Note 10: Conditions: The RX PLL is locked to the incoming data and the SCAN25100 is in WRITE mode.

Note 11: Receiver output timing specifications for TS-R and TH-R are tested at the CPRI rate of 2.4576 Gbps.

Note 12: Limits are guaranteed by design and characterization over process, supply voltage, and temperature variations.

Note 13: Limits are guaranteed by design.

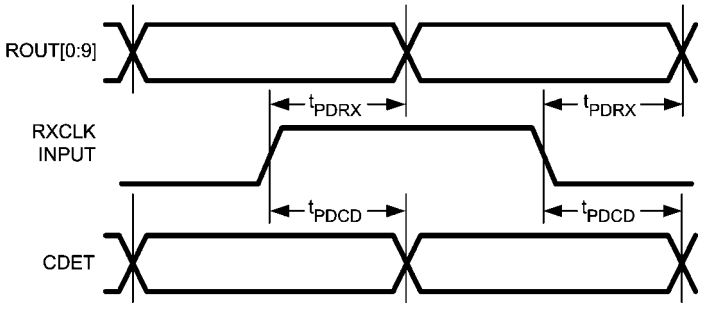
Note 14: Serial side DCM readings are referenced to the first bit of the K28.5 pattern {110000 0101 001111 1010}. Parallel side DCM readings are referenced to the TXCLK or RXCLK edge (not the data edge) that registers the K character as an input or output.

Note 15: DCM readings have been validated when the RXCLK pin on the SCAN25100 is used as an output in "WRITE" mode (RXCLKMODE = 0) and IOVDD = 3.3V.

Note 16: Edge rate characterization includes the loading effects of 1.0 uF AC-coupling capacitors and 4 inches of 100-Ohm differential microstrip.

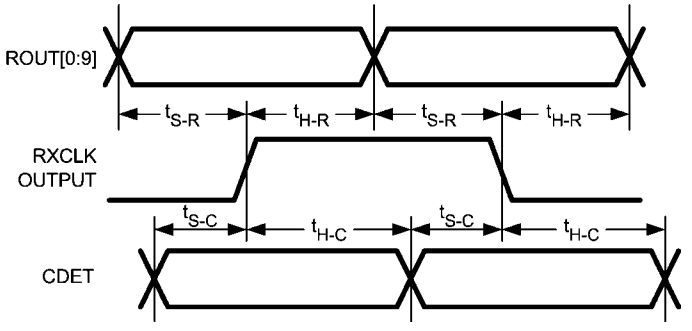
AC Timing Diagrams

READ MODE



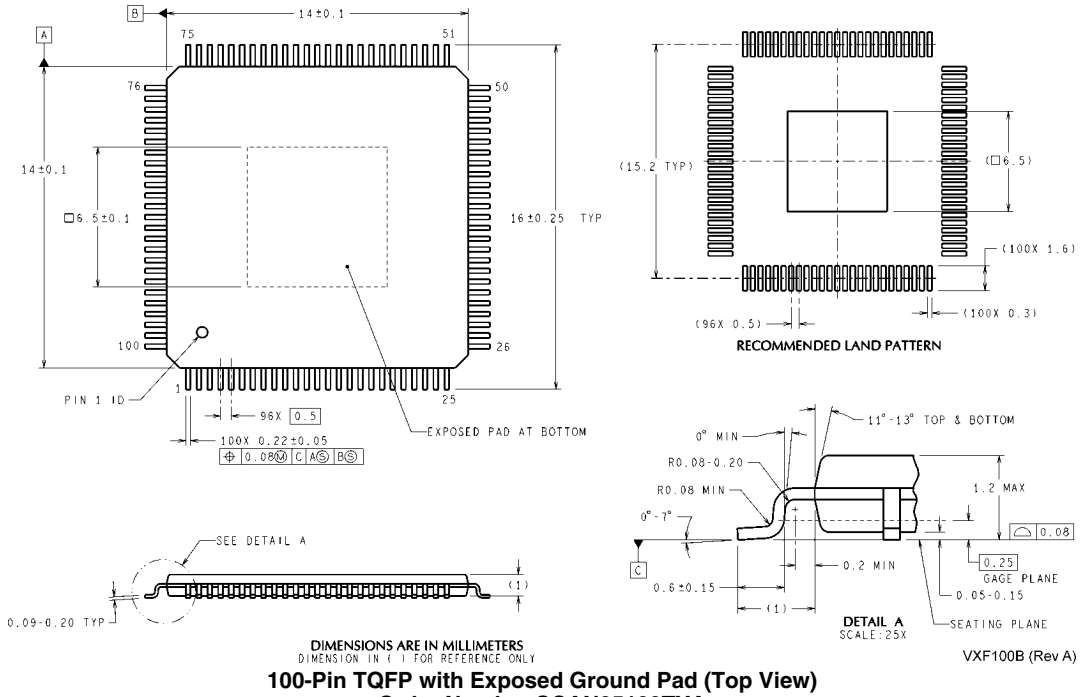
20183409

WRITE MODE



20183410

Physical Dimensions inches (millimeters) unless otherwise noted



100-Pin TQFP with Exposed Ground Pad (Top View)
Order Number SCAN25100TYA
NS Package Number VXF100B
See www.national.com/quality/marking_conventions.html for additional part marking information

Notes

Notes

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