

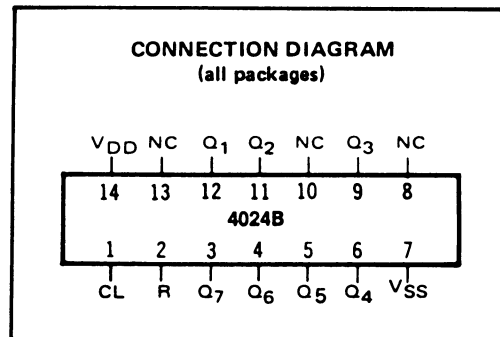
CMOS 7-STAGE BINARY COUNTER

FEATURES

- ◆ 7 Fully Static Stages
- ◆ Buffered Outputs Available from All Stages
- ◆ Common Reset Line
- ◆ 8 MHz Counting Rate @ 10Vdc
- ◆ All Inputs Buffered

DESCRIPTION

The 4024B is a single chip monolithic medium scale integrated circuit containing N-Channel and P-Channel enhancement-mode MOS transistors. Seven single-phase clocked counting stages are provided with the Q output of each stage accessible. The Counter is reset to "zero" by a high level on the Reset input. Each counter stage is a static master-slave flip-flop. The counter state is advanced one count on the negative-going transition of each input pulse.



TRUTH TABLE

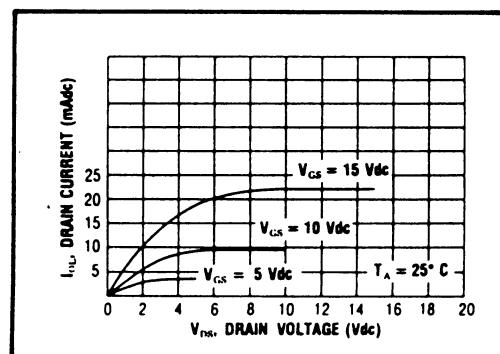
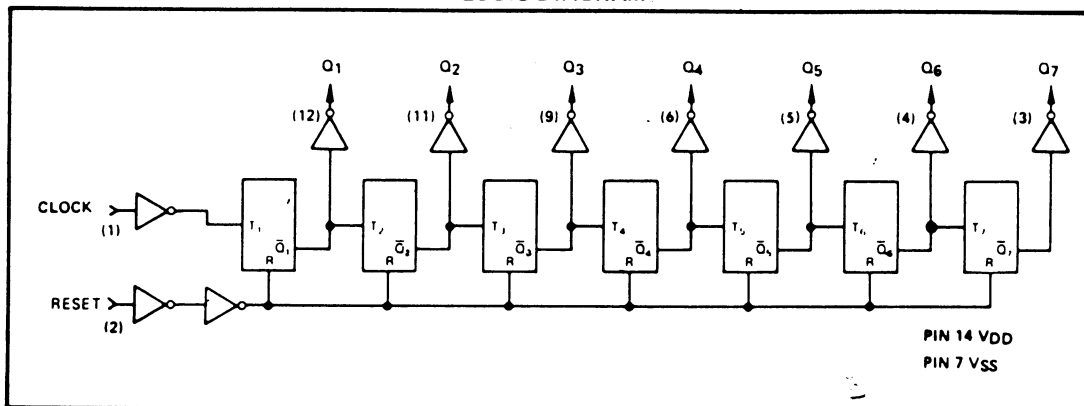
Clock	Reset	State
0	0	No Change
0	1	All Outputs Low
1	0	No Change
1	1	All Outputs Low
	0	No Change
	1	All Outputs Low
	0	Advance One Count
	1	All Outputs Low

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A	-55 to +125	°C
		-40 to +85	°C

LOGIC DIAGRAM



Typical N-Channel
Sink Current Characteristics

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS ¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} = V _{SS} or V _{DD} All valid input combinations	-	5	-	0.05	5	-	150	μA _{dc}
			-	10	-	0.1	10	-	300	
			-	15	-	0.2	20	-	600	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications"

² T_{LOW} = -55°C for C

= -40°C for E

T_{HIGH} = +125°C for C

= + 85°C for E

DYNAMIC CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

PARAMETER	V _{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION					
PROPAGATION DELAY TIME Clock to Q ₁	t _{PLH} , t _{PHL}	5	-	180	ns
		10	-	80	
		15	-	65	
Q _i to Q _{i+1}	t _{PLH} , t _{PHL}	5	-	100	ns
		10	-	40	
		15	-	30	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	-	100	ns
		10	-	50	
		15	-	40	
MINIMUM CLOCK PULSE WIDTH	PW _{CL}	5	-	120	ns
		10	-	60	
		15	-	45	
MAXIMUM CLOCK FREQUENCY	f _{CL}	5	2	4	MHz
		10	5	10	
		15	6	12	
MAXIMUM CLOCK RISE AND FALL TIME	t _{rCL} , t _{fCL}	5	15	-	μs
		10	10	-	
		15	5	-	
RESET OPERATION					
PROPAGATION DELAY TIME	t _{PHL}	5	-	200	ns
		10	-	100	
		15	-	80	
MINIMUM RESET PULSE WIDTH	PW _R	5	-	200	ns
		10	-	100	
		15	-	80	
RESET REMOVAL TIME	t _{rem}	5	-	200	ns
		10	-	100	
		15	-	80	

TYPICAL COUNTER STAGE

