

## SDA 3112 TV PLL

The SDA 3112 is produced in ASBC technology. In connection with VCO (tuner) and a fast prescaler (prescaler factor 1:64), it represents a digitally programmable PLL for a TV set with frequency synthesis tuning. The PLL enables a crystal exact adjustment of the tuner oscillator frequencies for the TV ranges band III/IV/V in 125 kHz resolution (frequency range: 128 to 2000 MHz). A serial interface enables a simple connection to a microprocessor. This microprocessor loads the prescaler and band selection outputs with the appropriate information. At the output LOCK the PLL supplies a state information (locked/released).

### Features

- No need for an external integrator
- Noise free telegram transmission
- Integration time constant controlled by software
- Microprocessor compatible

### Maximum ratings

Supply voltage	$V_S$	-0.3 to 7.5	V
<b>Inputs</b>			
Q1, Q2, $I_{ref}$	$V_I$	-0.3 to $V_S$	V
IFO, CPL, PLE	$V_I$	-0.3 to $V_S + 0.5$	V
PLE	$V_I$	-0.3 to 7.8	V
F, $\bar{F}$	$V_I$	-0.3 to $V_S + 0.5$	V
<b>Outputs</b>			
PD	$V_O$	-0.3 to $V_S$	V
UD	$V_O$	-0.3 to 33	V
	$I_{OL}$	-7	mA
BS1...BS5	$V_O$	-0.3 to 16	V
LOCK	$I_O$	-1 to 5	mA
Internal pull-up $R_L = 3\text{ k}\Omega$			
Junction temperature	$T_j$	140	°C
Storage temperature range	$T_{stg}$	-55 to 150	°C
Thermal resistance (system-air)	$R_{thSA}$	80	K/W

### Operating range

Supply voltage range	$V_S$	4.5 to 5.5	V
Input frequency	$f_F, f_{\bar{F}}$	32	MHz
Divider ratio	$N$	1024 to 16383	
Resistance for $I_{ref}$	$R_I$	80	k $\Omega$
$I_{ref} = (V_S - 0.8)R_I$			
Tuning voltage range open collector	$V_D$	0.3 to 33	V
Ambient temperature range	$T_{amb}$	0 to 85	°C

**Characteristics** ( $V_S = 5\text{ V} \pm 0.5\text{ V}$ ;  $T_{\text{amb}} = 0\text{ to }70\text{ }^\circ\text{C}$ )

		min	typ	max	
Supply current	$I_S$	15	22	35	mA
Crystal frequency Series C = 18 pf	$f_q$		4		MHz
<b>Signal inputs F/F</b>					
Input voltage	$V_{16H}$	3.92		$V_S + 0.12$	V
	$V_{16L}$	3.8		$V_S$	V
Input current	$I_{16}$			50	$\mu\text{A}$
$V_{16} = 5\text{ V}$					
Input sensitivity at sine push-pull triggering ; $f = 32\text{ MHz}$	$V_{16}$	120		1200	mV <sub>pp</sub>
<b>Inputs (IFO, CPL, PLE)</b>					
Upper threshold voltage	$V_{8H}$	2.4			V
Lower threshold voltage	$V_{8L}$			0.8	V
Input current					
$V_{8H} = 5\text{ V}$	$I_{8H}$			8	$\mu\text{A}$
$V_{8L} = 0.4\text{ V}$	$I_{8L}$			-550	$\mu\text{A}$
$V_{8L} = 0.8\text{ V}$	$I_{8L}$			-500	$\mu\text{A}$
<b>Band select outputs (BS1 . . . BS5)</b>					
Reverse current	$I_{3H}$			10	$\mu\text{A}$
$V_{3H} = 15\text{ V}$					
Current drain	$I_{3H}$	0.5		3	mA
$2\text{ V} \leq V_3 \leq 15\text{ V}$					
<b>Tuning section PD, UD, <math>I_{\text{ref}}</math>, LOCK</b>					
Charge pump current	$I_{13}$	$\pm 250$		$\pm 550$	$\mu\text{A}$
$I_{\text{pump}} = 10 \times I_{\text{ref}}$ ; $R_1 = 120\text{ k}\Omega$ ; $V_S = 5\text{ V}$					
Tuning voltage	$V_{15L}$			0.3	V
$I_{15L} = 1.5\text{ mA}$					
Reverse current	$I_{15H}$			20	$\mu\text{A}$
$V_{15H} = 33\text{ V}$					
Reference current	$I_{14}$	30		40	$\mu\text{A}$
ext. $R = 120\text{ k}\Omega$					
Output voltage	$V_{12H}$	4.5			V
int. $R_L = 3\text{ k}\Omega$					
$I_{12H} = -100\text{ }\mu\text{A}$					
$I_{12L} = 100\text{ }\mu\text{A}$	$V_{12L}$			0.7	V
<b>IFO, PLE</b>					
Set-up time for release	$t_{VE}$	2			$\mu\text{s}$
data	$t_{VD}$	2			$\mu\text{s}$
Hold time for: release	$t_{HE}$	2			$\mu\text{s}$
data	$t_{HD}$	2			$\mu\text{s}$
<b>CPL</b>					
H pulse width	$t_{CH}$	2			$\mu\text{s}$
L pulse width	$t_{CL}$	2			$\mu\text{s}$

### Circuit description

Triggered by the ECI inputs  $F\bar{F}$  a switchable 32/33 counter operates as a 14 bit synchronous prescaler in the dual modulus method by combining it with a 5 and 9 bit programmable synchronous counter. In this combination the 5 bit counter controls the switch-over from 32 to 33 (block diagram 1). Dividing ratios of  $N = 1024$  to 16383 are possible.

The 18 bit deep shift register latch is subdivided into 14 bits for storing the dividing ratio  $N$ , as well as 1 bit for selecting the pump current and 3 bits for controlling the 5 band selection outputs.

The telegram is inserted over the serial data input IFO with the H-L slope of the shift clock CPL, when the enable input is set at H. Beginning with LSB, the complement of the dividing ratio is inserted in binary code, then the select bit  $2^{14}$  for the pump current and the band selection control bits  $2^{15}$ ,  $2^{16}$ ,  $2^{17}$  (please refer to enclosed table).

An integrated control circuit checks the word length (18 bit) of the data telegram. The 18 bit latch accepts the data from the shift register during the L state of the enable input PLE.

A 4 MHz crystal controlled clock oscillator has been integrated in the IC. An internal reference divider divides the output signal of the crystal oscillator ( $f_{OSC} = 4$  MHz) by 2048 resulting in 1.953125 kHz (reference signal), providing a frequency resolution of 125 kHz by means of the asynchronous permanent prescaler (dividing factor 1:64).

In a digital phase detector the divided VCO input signal is compared with the reference signal. If the falling slope of the VCO input signal appears before the falling slope of the reference signal, the output DOWN of the phase detector will be in the H state for the duration of the phase difference. However, if above signal sequence is reversed, the output UP will be in the H state instead. The outputs UP/DOWN control the two current sources  $I+$  and  $I-$  (charge pump). In case both outputs are in the L state, the charge pump output will be in the high impedance mode (TRI-STATE). Information with respect to either the H or L state will be provided at the LOCK output by the logical "NOR" of the outputs UP/DOWN.

The output current of the charge pump (source current = drain current) is adjusted by an external resistor between pin  $I_{ref}$  and  $V_{CC}$ . In addition, this output current can be generated by the control bit for the pump current at the same value or at a value increased by a factor of 10 (refer to enclosed table).

The current pulses generated by the charge pump are integrated into the tuning voltage by means of an active low pass filter (on-chip loop amplifier and external RC circuit). The dc output signal of the low pass filter is available at  $V_D$  and is used as tuning voltage for the VCO. In order to provide tuning voltages higher than  $V_{CC} = 5$  V, the output stage of the amplifier consists of a transistor with an open collector. The external collector resistor can be connected to voltages up to 33 V.

To switch voltages higher than  $V_S = 5$  V, the band selection outputs (BS1, BS2, BS3, BS4, BS5) include current drains with open collectors. It is therefore possible to directly connect transistors operating as band selection switches without the use of current limiting resistors (please refer to enclosed application current).

**Pin configuration**

Pin No.	Symbol	Function
1	Q1	Crystal
2	Q2	Crystal
3	BS1	Standard switchover output
4	BS2	Band selection output BS
5	BS3	Band selection output VHF
6	BS4	Band selection output UHF
7	BS5	Band selection output I/III
8	PLE	Release input for shift register
9	GND	Ground
10	CPL	Shift clock pulse input
11	IFO	Data input
12	LOCK	Lock output
13	PD	Amplifier input/charge pump output
14	$I_{ref}$	Current adjustment for charge pump
15	$V_D$	Tuning voltage output
16	F	Signal input
17	F	Signal input
18	$V_S$	Supply voltage

**Loop-filter calculations**

Loop bandwidth:  $\sqrt{\frac{I_p \times K_{VCO}}{C_1 \times P \times N}} = \omega_R$

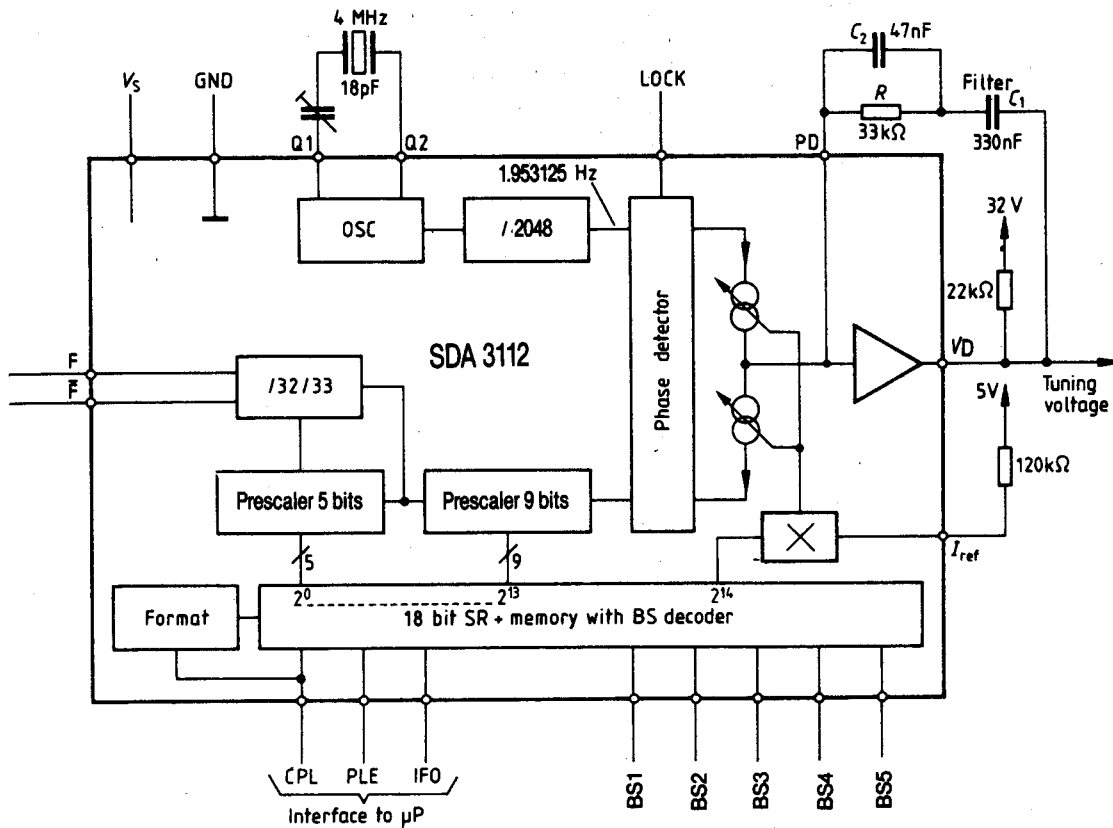
Attenuation  $1/2 \times \omega_R \times R \times C_1 = \xi$

- P = prescaler
- N = programmable divider ratio
- $I_p$  = pump current
- $S_{VCO}$  = tuner voltage characteristic
- $R_1 C_1$  = loop filter

Example for channel 47:

P = 64 N = 11520  $I_p = 200 \mu A$   $S_{VCO} = 18.7 \text{ MHz/V}$  R = 33 k $\Omega$   $C_1 = 330 \text{ nF}$   
 $\omega_R = 124 \text{ Hz}$   $f_R = 20 \text{ Hz}$   $\xi = 0.675$  Standard dimensioning:  $C_2 \approx C_1/5$

**Block diagram**



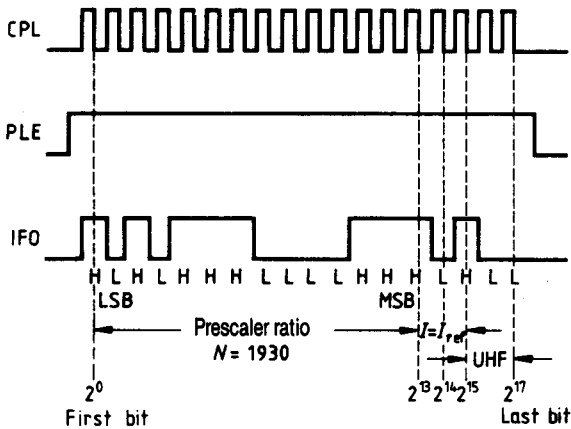
**Truth Table**

"IFO" bit 2 <sup>14</sup>			Pump Current $I_p$				
L			$I_{ref}$				
H			$10 \times I_{ref}$				

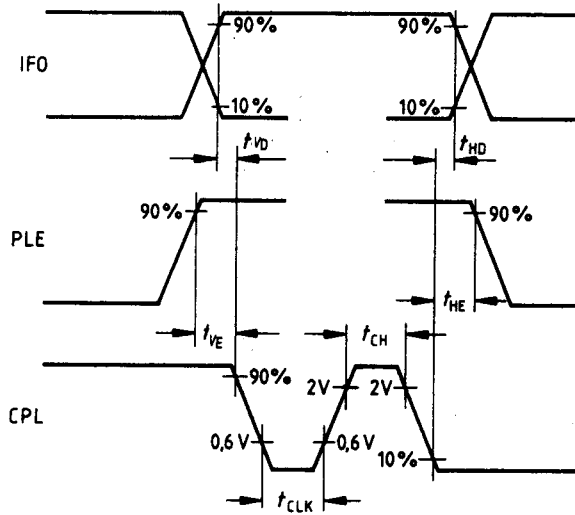
  

"IFO" bit			Band selection outputs (L = conducting, H = blocking)				
2 <sup>15</sup>	2 <sup>16</sup>	2 <sup>17</sup>	BS1	BS2	BS3	BS4	BS5
L	L	L	L	L	L	L	H
L	L	H	L	L	H	H	H
L	H	L	L	H	L	H	L
L	H	H	L	H	H	H	H
H	L	L	H	L	L	L	H
H	L	H	H	L	H	H	H
H	H	L	H	H	L	H	L
H	H	H	H	H	H	H	H

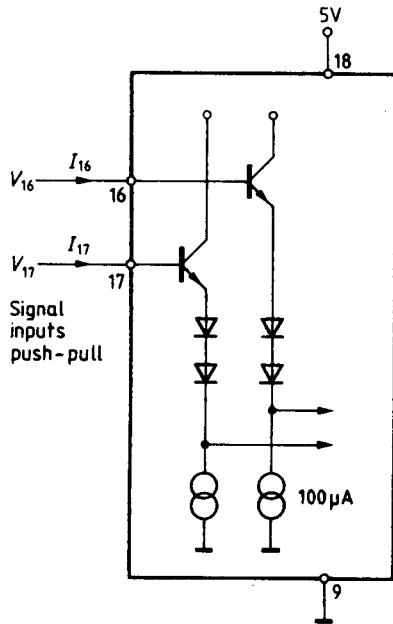
**Pulse diagram**



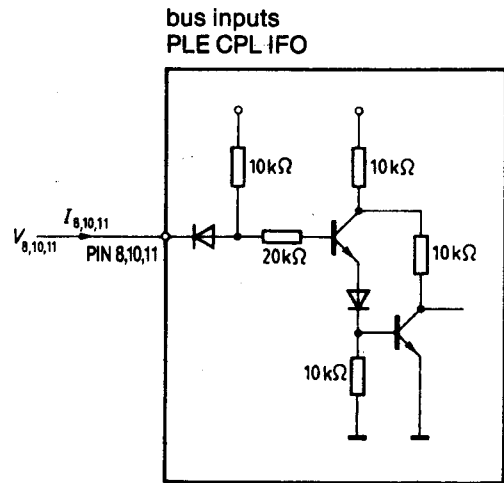
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**Pulse diagram****Set-up and hold times**

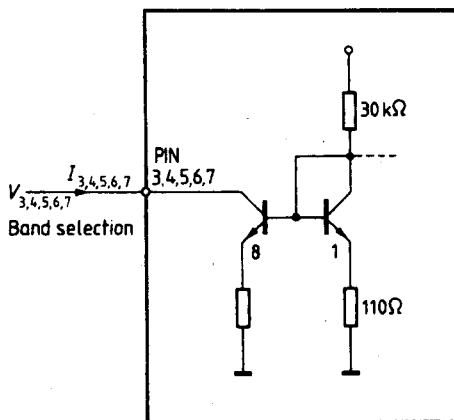
Test and measurement circuits



Test circuit 1



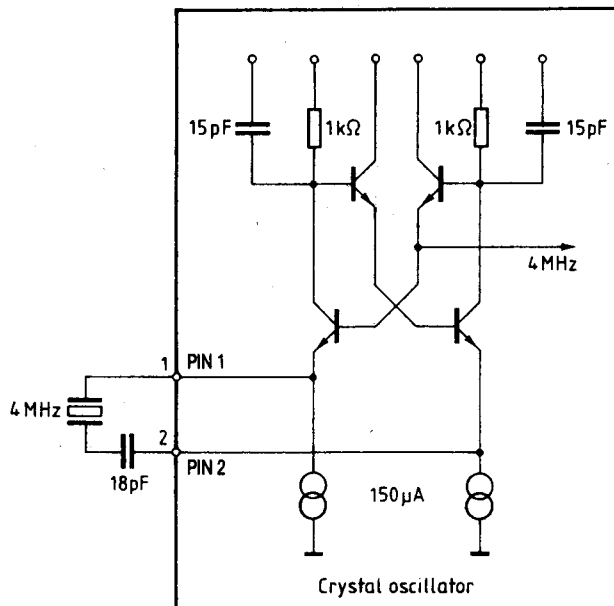
Test circuit 2



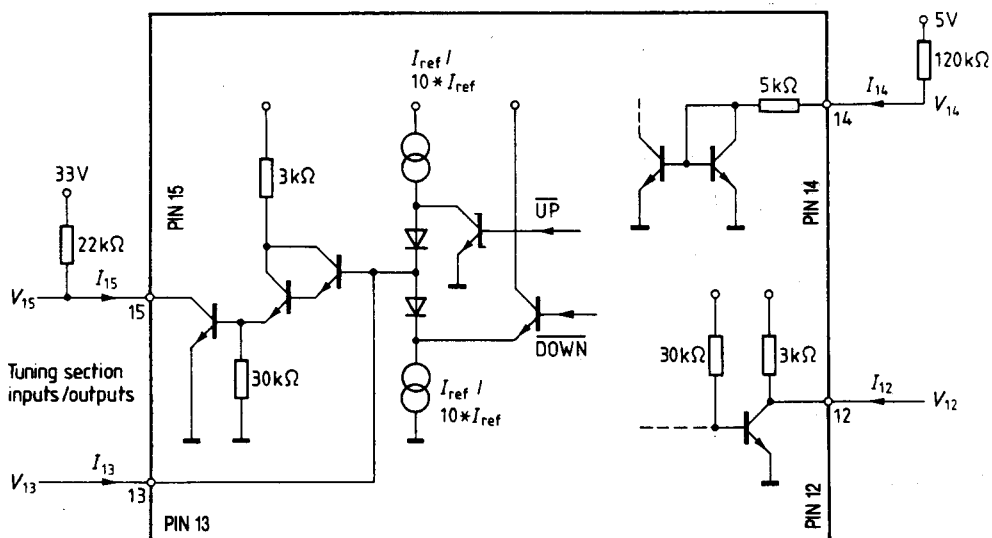
Test circuit 3



Test and measurement circuits



Test circuit 4



Test circuit 5

**Application circuit**

**Design proposal**

$R_1 = 120 \text{ k}\Omega$  ( $I_p = 35/350 \mu\text{A}$ )

$R_L = 22 \text{ k}\Omega$ ,  $R_2 \dots R_4 = 22 \text{ k}\Omega$

Loop filter:  $R = 33 \text{ k}\Omega$ ,  $C_1 = 330 \text{ nF}$ ,  $C_2 = 47 \text{ nF}$

Post filter (in the tuner):  $R_T = 10 \text{ k}\Omega$ ,  $C_T = 47 \text{ nF}$

