

SF1133A

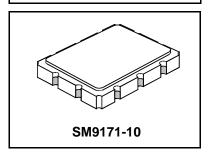
- Designed for GSM BTS Receiver IF Applications
- Compatible with National Semiconductor Chip Set
- Very Flexible Impedance Matching
- Unbalanced or Balanced Input or Output
- Complies with Directive 2002/95/EC (RoHS)



Absolute Maximum Ratings

Rating	Value	Units
Maximum Incident Power in Passband	+15	dBm
Max. DC voltage between any 2 terminals	30	VDC
Storage Temperature Range	-40 to +85	°C
Suitable for lead-free soldering - Max. Soldering Profile	260°C for 30 s	

246 MHz SAW Filter



Electrical Characteristics

Characteristic			Notes	Min	Тур	Max	Units
Nominal Center Frequency		f _C	1		246.000		MHz
Passband	Insertion Loss at fc	IL	1			7.0	dB
	1 db Passband	BW ₁		±100			kHz
	Amplitude Ripple over fc±100 kHz		1, 2			1.0	dB _{P-P}
	Group Delay Variation over fc ±100 kHz	GDV	1			500	ns _{P-P}
Rejection	fc-800 to fc-600 and fc+600 to fc+800 kHz			20			
	fc-30 MHz to fc-800 kHz		1	30			
	fc+800 kHz to fc+17 MHz		1, 2, 3	30			dB
	fc-80 MHz to fc-30 MHz		1	35			
	fc+17 Mhz to fc+80 MHz		İ	35			
Operating Temperature Range		T _A	1	-35		+85	°C

Impedance Matching to 50 Ω Unbalanced	External L-C
Impedance Matching to 200 Ω Balanced	External L-C
Case Style	SMP9171-10 9.1 x 7.1 mm Nominal Footprint
Lid Symbolization (YY = year, WW = week)	RFM SF1133A YYWW

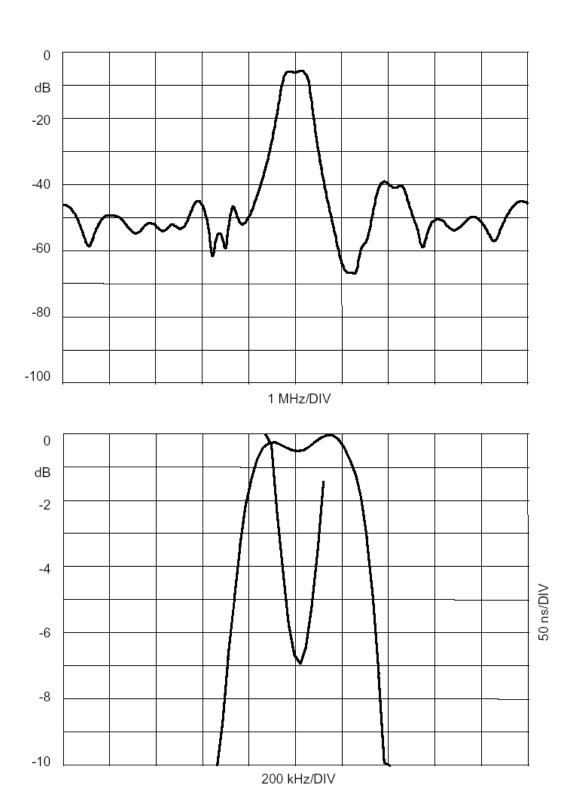
Notes:

- 1. Unless noted otherwise, all specifications apply over the operating temperature range with filter soldered to the specified demonstration board with impedance matching to $50~\Omega$ and measured with $50~\Omega$ network analyzer.
- 2. Unless noted otherwise, all frequency specifications are referenced to the nominal center frequency, fc.
- Rejection is measured as attenuation below the minimum IL point in the passband.
 Rejection in final user application is dependent on PCB layout and external impedance matching design. See Application Note No. 42 for details.
- "LRIP" or "L" after the part number indicates "low rate initial production" and "ENG" or "E" indicates "engineering prototypes."
- 5. The design, manufacturing process, and specifications of this filter are subject to change.
- 6. Either Port 1 or Port 2 may be used for either input or output in the design. However, impedances and impedance matching may vary between Port 1 and Port 2, so that the filter must always be installed in one direction per the circuit design.
- 7. US and international patents may apply.
- 8. Electrostatic Sensitive Device. Observe precautions for handling.



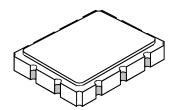
Electrical Connections

Connection	Terminals
Port 1 Hot	10
Port 1 Gnd Return	1
Port 2 Hot	5
Port 2 Gnd Return	6
Case Ground	All others



SM9171-10 Case

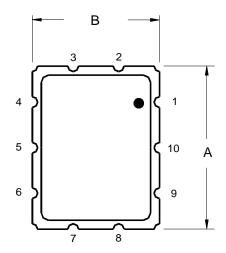
10-Terminal Ceramic Surface-Mount Case 9.1 x 7.1 mm Nominal Footprint

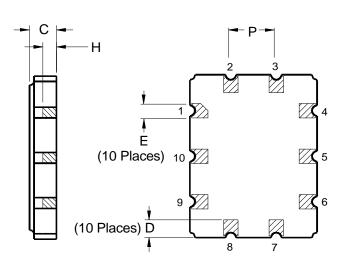


Case Dimensions						
Dimension	mm			Inches		
Dilliension	Min	Nom	Max	Min	Nom	Max
Α	8.86	9.09	9.40	0.349	0.358	0.370
В	6.88	7.11	7.40	0.271	0.280	0.291
С		1.91	2.00		0.075	0.079
D		0.99			0.039	
E		0.79			0.031	
Н		1.0			0.039	
Р		2.54			0.100	

Materials				
Solder Pad Termination	Au plating 30 - 60 μinches (76.2-152 μm) over 80-200 μinches (203-508 μm) Ni.			
Lid	Fe-Ni-Co Alloy Electroless Nickel Plate (8-11% Phosphorus) 100-200 µinches Thick			
Body	Al ₂ O ₃ Ceramic			
Pb Free				

Electrical Connections				
	Connection	Terminals		
Port 1	Input or Return	6		
	Return or Input	5		
Port 2	Output or Return	1		
	Return or Output	10		
	Ground	All others		
Single	Ended Operation	Return is ground		
Differe	ntial Operation	Return is hot		





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