



SILICON LABORATORIES

Si3210/Si3211/Si3212

PROSLIC™ PROGRAMMABLE CMOS SLIC/CODEC WITH RINGING/BATTERY VOLTAGE GENERATION

Features

- Performs all BORSCHT Functions
- Ideal for Short Loop Applications (5 REN at 2 kft, 3 REN at 4 kft)
- Low Voltage CMOS
- Package: 38-Pin TSSOP
- Compliant with Relevant LSSGR and CCITT Specifications
- Battery Voltage Generated Dynamically with On-Chip DC-DC Converter Controller (Si3210 only)
- 5 REN Ringing Generator
 - Programmable Frequency, Amplitude, Waveshape, and Cadence
- Programmable AC Impedance
- A-Law/ μ -Law, Linear PCM Companding
- On-Hook Transmission
- Programmable Constant Current Feed (20–41 mA)
- Programmable Loop Closure and Ring Trip Thresholds with Debouncing
- Loop or Ground Start Operation and Polarity Battery Reversal
- Continuous Line Voltage and Current Monitoring
- DTMF Decoder
- Dual Tone Generator
- SPI and PCM Bus Digital Interfaces with Programmable Interrupt for Control and Data
- 3.3 V or 5 V Operation
- Multiple Loopback Modes for Testing
- Pulse Metering
- FSK Caller ID Generation

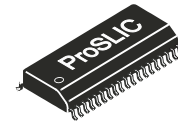
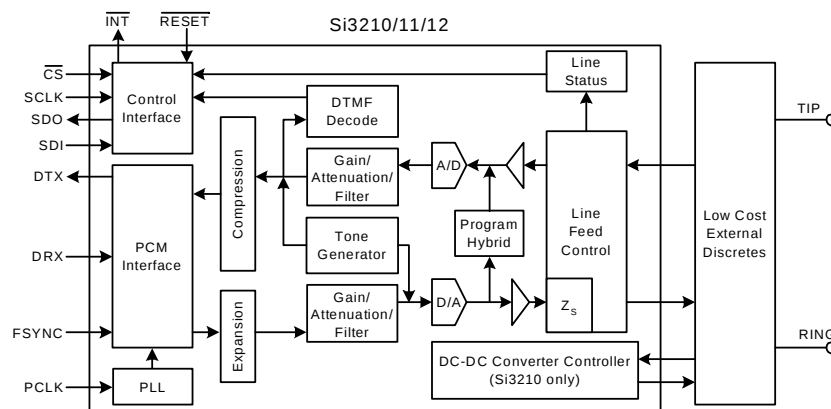
Applications

- Terminal Adaptors
- Cable Telephony
- PBX/Key Systems
- Wireless Local Loop
- Voice Over IP
- Integrated Access Devices

Description

The ProSLIC™ is a low-voltage CMOS device that integrates SLIC, codec, and battery generation functionality into a complete analog telephone interface. The device is ideal for short loop applications such as terminal adaptors, cable telephony, and wireless local loop. The ProSLIC is powered with a single 3.3 V or 5 V supply. The Si3210 generates battery voltages dynamically using a software programmable dc-dc converter from a 3.3 V to 35 V supply; negative high-voltage supplies are not needed. All high voltage functions are performed locally with a few low cost discrete components. The device is available in a 38-pin TSSOP and interfaces directly to standard SPI and PCM bus digital interfaces.

Functional Block Diagram



Ordering Information

See page 118.

Pin Assignments

Si3210/11/12

CS	1	38	SCLK
INT	2	37	SDI
PCLK	3	36	SDO
DRX	4	35	SDITHRU
DTX	5	34	DCDRV/DCSW
FSYNC	6	33	DCFF/DOUT
RESET	7	32	TEST
SDCH/DIO1	8	31	GNDD
SDCL/DIO2	9	30	VDDD
VDDA1	10	29	ITIPN
IREF	11	28	ITIPP
CAPP	12	27	VDDA2
QGND	13	26	IRINGP
CAPM	14	25	IRINGN
STIPDC	15	24	IGMP
SRINGDC	16	23	GNDA
STIPE	17	22	IGMN
SVBAT	18	21	SRINGAC
SRINGE	19	20	STIPAC

Patents pending

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Si3210/Si3211/Si3212

Electrical Specifications

Table 1. Absolute Maximum Ratings and Thermal Information*

Parameter	Symbol	Value	Unit
DC Supply Voltage	$V_{DD}, V_{DDA1}, V_{DDA2}$	-0.5 to 6.0	V
Input Current, Digital Input Pins	I_{IN}	± 10	mA
Digital Input Voltage	V_{IND}	-0.3 to ($V_{DD} + 0.3$)	V
ESD, Si3210/11/12 (Human Body Model)		2000	V
Operating Temperature Range	T_A	-40 to 100	°C
Storage Temperature Range	T_{STG}	-40 to 150	°C
TSSOP-38 Thermal Resistance, Typical	θ_{JA}	50	°C/W
*Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.			

Table 2. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min*	Typ	Max*	Unit
Ambient Temperature	T_A	K-grade	0	25	70	°C
Ambient Temperature	T_A	B-grade	-40	25	85	°C
Si3210/11/12 Supply Voltage	$V_{DD}, V_{DDA1}, V_{DDA2}$		3.13	3.3/5.0	5.25	V
*Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated. Product specifications are only guaranteed when the typical application circuit (including component tolerances) is used.						

Table 3. AC Characteristics(V_{DDA}, V_{DDD} = 3.13 to 5.25 V, T_A = 0 to 70°C for K-Grade, –40 to 85°C for B-Grade)

Parameter	Test Condition	Min	Typ	Max	Unit
TX/RX Performance					
Overload Level	THD = 1.5%	2.5	—	—	V _{PK}
Single Frequency Distortion ¹	2-wire – PCM or PCM – 2-wire: 200 Hz–3.4 kHz	—	—	–45	dB
Signal-to-(Noise + Distortion) Ratio ²	200 Hz to 3.4 kHz D/A or A/D 8-bit Active off-hook, and OHT, any ZAC	Figure 1	—	—	
Audio Tone Generator Signal-to-Distortion Ratio ²	0 dBm0, Active off-hook, and OHT, any Zac	45	—	—	dB
Intermodulation Distortion		—	—	–41	dB
Gain Accuracy ²	2-wire to PCM, 1014 Hz	–0.5	0	0.5	dB
	PCM to 2-wire, 1014 Hz	–0.5	0	0.5	dB
Gain Accuracy Over Frequency		Figure 3,4	—	—	
Group Delay Over Frequency		Figure 5,6	—	—	
Gain Tracking ³	1014 Hz sine wave, refer- ence level –10 dBm signal level:				
	3 dB to –37 dB	–0.25	—	0.25	dB
	–37 dB to –50 dB	–0.5	—	0.5	dB
	–50 dB to –60 dB	–1.0	—	1.0	dB
Round-Trip Group Delay	at 1000 Hz	—	1100	—	μs
Gain Step Accuracy	–6 dB to 6 dB	–0.017	—	0.017	dB
Gain Variation with Temperature	All gain settings	–0.25	—	0.25	dB
Gain Variation with Supply	V _{DDA} = V _{DDA} = 3.3/5 V ± 5%	–0.1	—	0.1	dB
2-Wire Return Loss	200 Hz to 3.4 kHz	30	35	—	dB
Transhybrid Balance	300 Hz to 3.4 kHz	30	—	—	dB
Noise Performance					
Idle Channel Noise ⁴	C-Message Weighted	—	—	15	dBrnC
	Psophometric Weighted	—	—	–75	dBmP
	3 kHz flat	—	—	18	dBrn
PSRR from VDDA	RX and TX, DC to 3.4 kHz	40	—	—	dB
PSRR from VDDD	RX and TX, DC to 3.4 kHz	40	—	—	dB
PSRR from VBAT	RX and TX, DC to 3.4 kHz	40	—	—	dB

Table 3. AC Characteristics (Continued)

(V_{DDA} , $V_{DDD} = 3.13$ to 5.25 V, $T_A = 0$ to 70°C for K-Grade, -40 to 85°C for B-Grade)

Parameter	Test Condition	Min	Typ	Max	Unit
Longitudinal Performance					
Longitudinal to Metallic or PCM Balance	200 Hz to 3.4 kHz, $\beta_{Q1,Q2} \geq 150$, 1% mismatch	56	60	—	dB
	$\beta_{Q1,Q2} = 60$ to 240^5	43	60	—	dB
	$\beta_{Q1,Q2} = 300$ to 800^5	53	60	—	dB
Metallic to Longitudinal Balance	200 Hz to 3.4 kHz	40	—	—	dB
Longitudinal Impedance	200 Hz to 3.4 kHz at TIP or RING Register selectable ETBO/ETBA				
	00	—	33	—	Ω
	01	—	17	—	Ω
	10	—	17	—	Ω
Longitudinal Current per Pin	Active off-hook 200 Hz to 3.4 kHz Register selectable ETBO/ETBA				
	00	—	4	—	mA
	01	—	8	—	mA
	10	—	8	—	mA
Notes: 1. The input signal level should be 0 dBm0 for frequencies greater than 100 Hz. For 100 Hz and below, the level should be -10 dBm0. The output signal magnitude at any other frequency will be smaller than the maximum value specified. 2. Analog signal measured as $V_{TIP} - V_{RING}$. Assumes ideal line impedance matching. 3. The quantization errors inherent in the μ/A-law companding process can generate slightly worse gain tracking performance in the signal range of 3 dB to -37 dB for signal frequencies that are integer divisors of the 8 kHz PCM sampling rate. 4. The level of any unwanted tones within the bandwidth of 0 to 4 kHz does not exceed -55 dBm. 5. Assumes normal distribution of betas.					

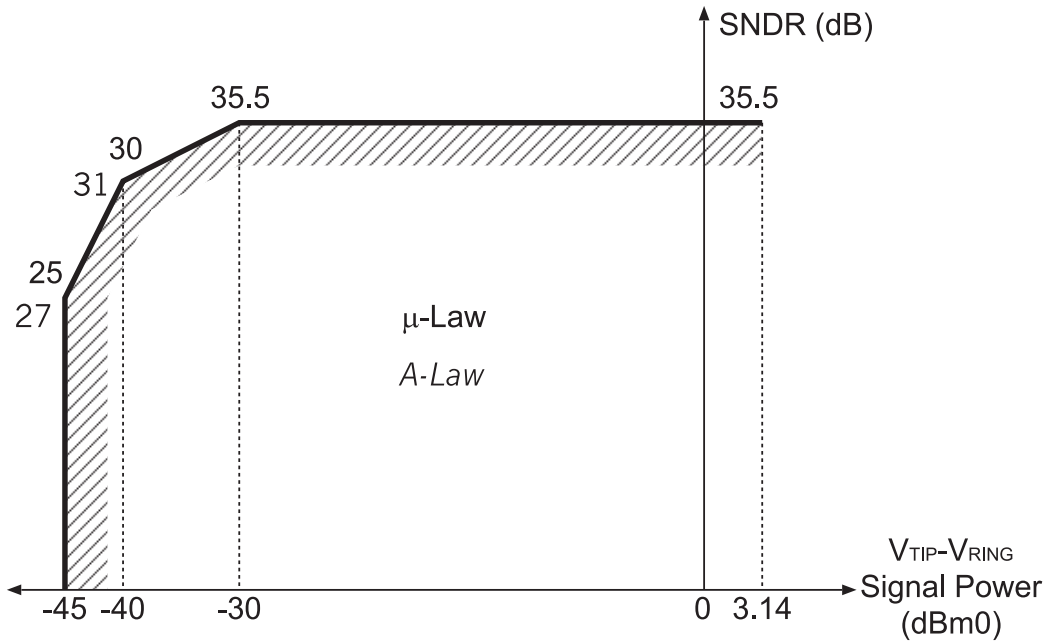


Figure 1. Transmit and Receive Path SNDR

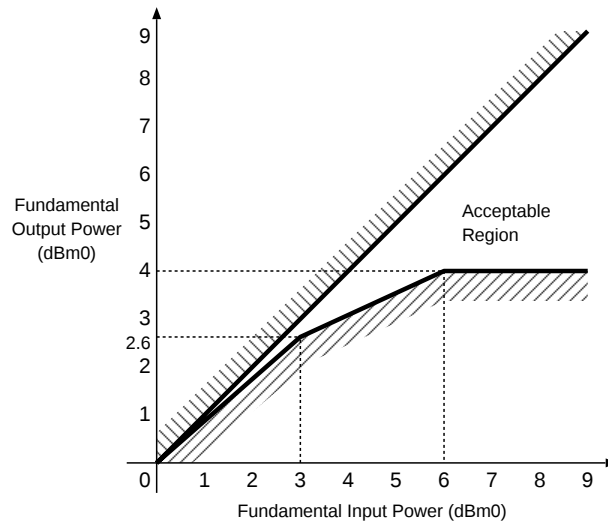


Figure 2. Overload Compression Performance

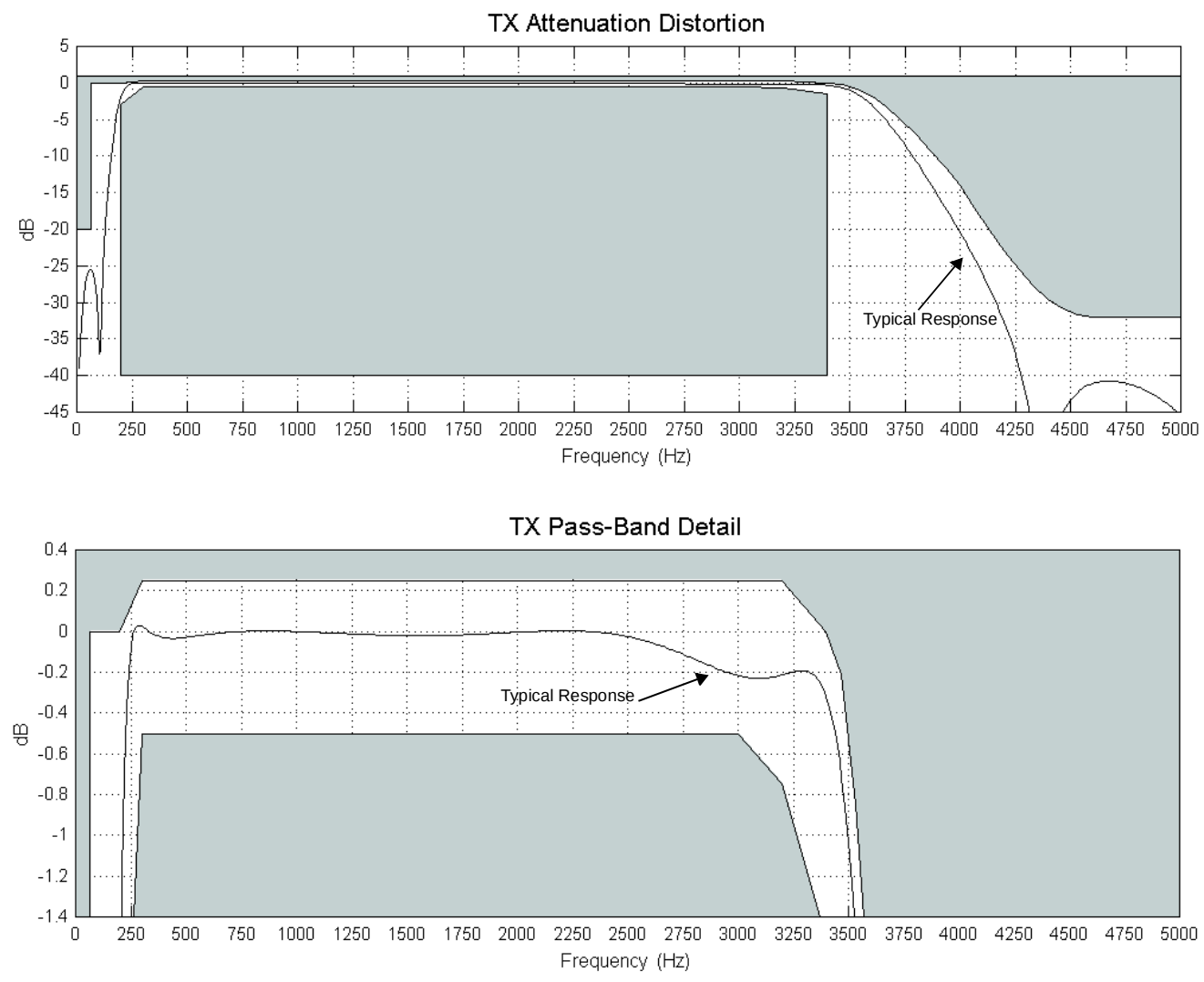


Figure 3. Transmit Path Frequency Response

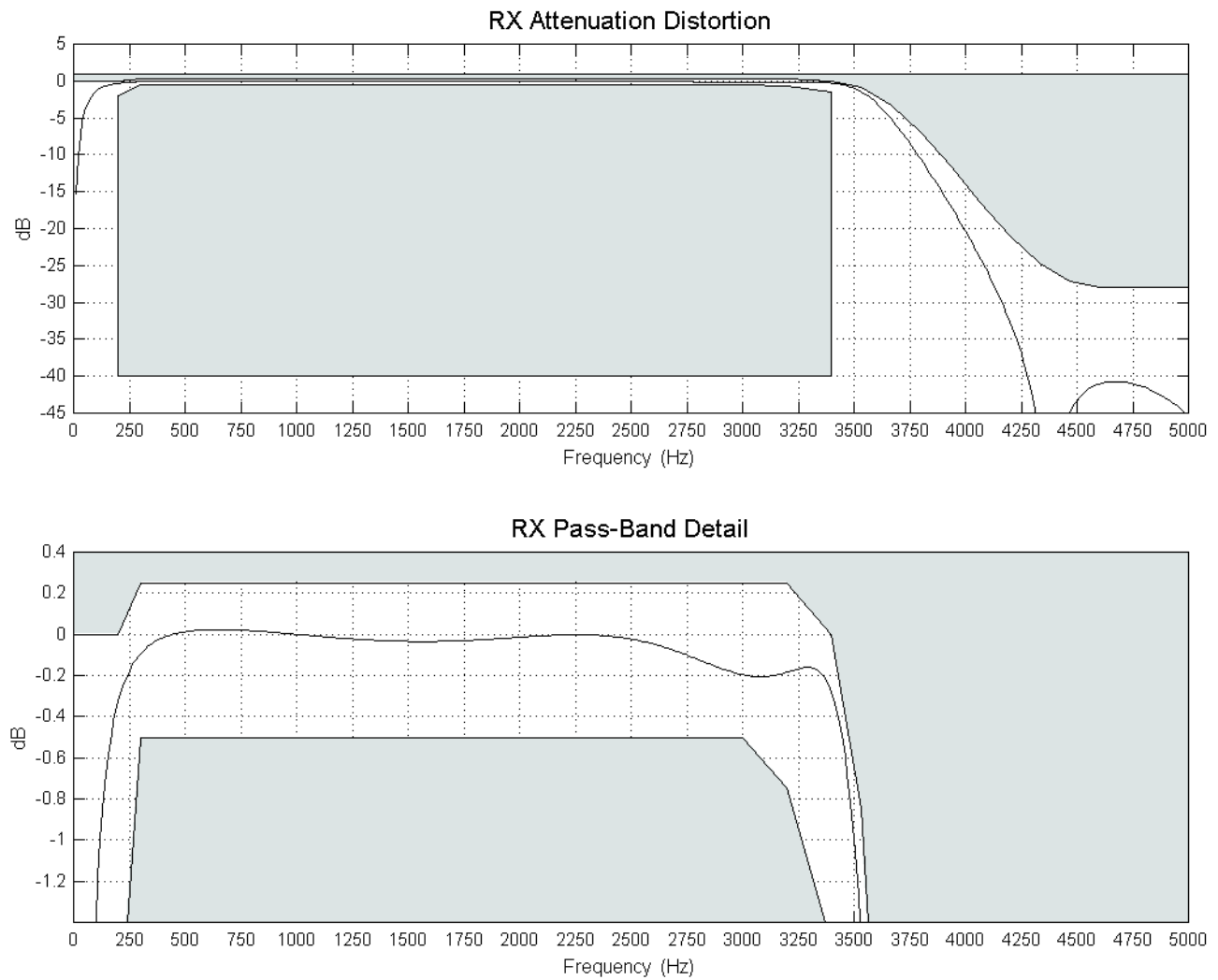


Figure 4. Receive Path Frequency Response

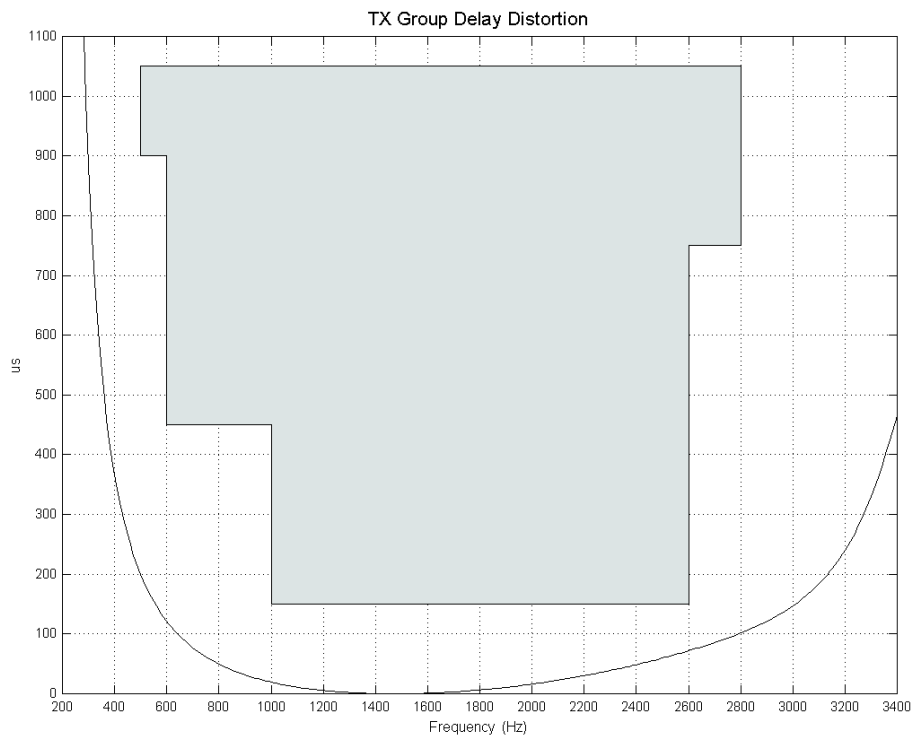


Figure 5. Transmit Group Delay Distortion

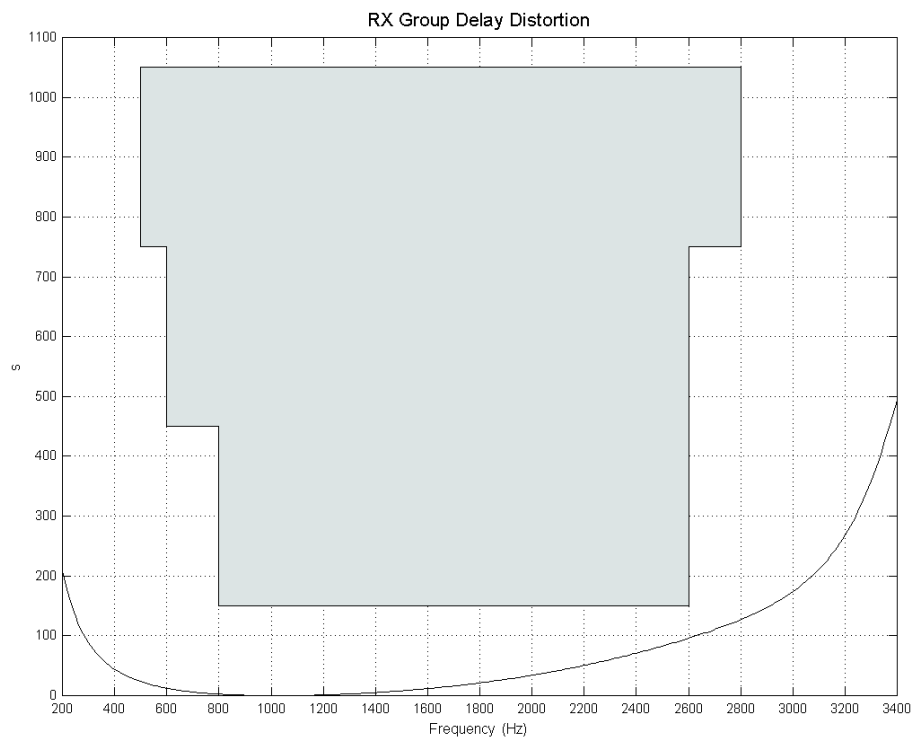


Figure 6. Receive Group Delay Distortion

Table 4. Linefeed Characteristics(V_{DDA}, V_{DDD} = 3.13 to 5.25 V, T_A = 0 to 70°C for K-Grade, –40 to 85°C for B-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Loop Resistance Range	R _{LOOP}	See note.*	0	—	160	Ω
DC Loop Current Accuracy		I _{LIM} = 29 mA, ETBA = 4 mA	–10	—	10	%
DC Open Circuit Voltage Accuracy		Active Mode; V _{OC} = 48 V, V _{TIP} – V _{RING}	–4	—	4	V
DC Differential Output Resistance	R _{DO}	I _{LOOP} < I _{LIM}	—	160	—	Ω
DC Open Circuit Voltage—Ground Start	V _{OCTO}	I _{RING} < I _{LIM} ; V _{RING} wrt ground V _{OC} = 48 V	–4	—	4	V
DC Output Resistance—Ground Start	R _{ROTO}	I _{RING} < I _{LIM} ; RING to ground	—	160	—	Ω
DC Output Resistance—Ground Start	R _{TOTO}	TIP to ground	150	—	—	kΩ
Loop Closure/Ring Ground Detect Threshold Accuracy		I _{THR} = 11.43 mA	–20	—	20	%
Ring Trip Threshold Accuracy		R _{THR} = 1100 Ω	–20	—	20	%
Ring Trip Response Time		User Programmable Register 70 and Indirect Register 36	—	—	—	
Ring Amplitude	V _{TR}	5 REN load; sine wave; R _{LOOP} = 160 Ω, V _{BAT} = –75 V	44	—	—	V _{RMS}
Ring DC Offset	R _{OS}	Programmable in Indirect Register 19	0	—	—	V
Trapezoidal Ring Crest Factor Accuracy		Crest factor = 1.3	–.05	—	.05	
Sinusoidal Ring Crest Factor	R _{CF}		1.35	—	1.45	
Ringing Frequency Accuracy		f = 20 Hz	–1	—	1	%
Ringing Cadence Accuracy		Accuracy of ON/OFF Times	–50	—	50	msec
Calibration Time		↑CAL to ↓CAL Bit	—	—	600	msec
Power Alarm Threshold Accuracy		At Power Threshold = 300 mW	–25	—	25	%
*Note: DC resistance round trip; 160 Ω corresponds to 2 kft 26 gauge AWG.						

Si3210/Si3211/Si3212

Table 5. Monitor ADC Characteristics

($V_{DDA}, V_{DDD} = 3.13$ to 5.25 V, $T_A = 0$ to 70°C for K-Grade, -40 to 85°C for B-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential Nonlinearity (6-bit resolution)	DNLE		-1/2	—	1/2	LSB
Integral Nonlinearity (6-bit resolution)	INLE		-1	—	1	LSB
Gain Error (voltage)			—	—	10	%
Gain Error (current)			—	—	20	%

Table 6. Si321x DC Characteristics, $V_{DDA} = V_{DDD} = 5.0$ V

($V_{DDA}, V_{DDD} = 4.75$ V to 5.25 V, $T_A = 0$ to 70°C for K-Grade, -40 to 85°C for B-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		$0.7 \cdot V_{DDD}$	—	—	V
Low Level Input Voltage	V_{IL}		—	—	$0.3 \cdot V_{DDD}$	V
High Level Output Voltage	V_{OH}	DIO1,DIO2,SDITHRU: $I_O = -4$ mA SDO, DTX: $I_O = -8$ mA	$V_{DDD} - 0.6$	—	—	V
		DOUT: $I_O = -40$ mA	$V_{DDD} - 0.8$	—	—	V
Low Level Output Voltage	V_{OL}	DIO1,DIO2,DOUT,SDITHRU: $I_O = 4$ mA SDO,INT,DTX: $I_O = 8$ mA	—	—	0.4	V
Input Leakage Current	I_L		-10	—	10	μA

Table 7. Si321x DC Characteristics, $V_{DDA} = V_{DDD} = 3.3$ V

($V_{DDA}, V_{DDD} = 3.13$ V to 3.47 V, $T_A = 0$ to 70°C for K-Grade, -40 to 85°C for B-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		$0.7 \cdot V_{DDD}$	—	—	V
Low Level Input Voltage	V_{IL}		—	—	$0.3 \cdot V_{DDD}$	V
High Level Output Voltage	V_{OH}	DIO1,DIO2,SDITHRU: $I_O = -2$ mA SDO, DTX: $I_O = -4$ mA	$V_{DDD} - 0.6$	—	—	V
		DOUT: $I_O = -40$ mA	$V_{DDD} - 0.8$	—	—	V
Low Level Output Voltage	V_{OL}	DIO1,DIO2,DOUT,SDITHRU: $I_O = 2$ mA SDO,INT,DTX: $I_O = 4$ mA	—	—	0.4	V
Input Leakage Current	I_L		-10	—	10	μA

Table 8. Power Supply Characteristics(V_{DDA}, V_{DDD} = 3.13 V to 5.25 V, T_A = 0 to 70°C for K-Grade, –40 to 85°C for B-Grade)

Parameter	Symbol	Test Condition	Typ ¹	Typ ²	Max	Unit
Power Supply Current, Analog and Digital	I _A + I _D	Sleep ($\overline{\text{RESET}} = 0$)	0.1	0.25	0.42	mA
		Open	33	42.8	49	mA
		Active on-hook ETBO = 4 mA	46	57	68	mA
		Active OHT ETBO = 4 mA	57	72	83	mA
		Active off-hook ETBA = 4 mA, I _{LIM} = 20 mA	73	88	99	mA
		Ground-start	36	47	55	mA
		Ringing Sinewave, REN = 1, V _{PK} = 56 V	45	55	65	mA
Power Supply Current, V _{BAT} ³	I _{BAT}	Sleep ($\overline{\text{RESET}} = 0$)	—	0	—	mA
		Open (DCOF = 1)	—	0	—	mA
		Active on-hook V _{OC} = 48 V, ETBO = 4 mA	—	3	—	mA
		Active OHT ETBO = 4 mA	—	11	—	mA
		Active off-hook ETBA = 4 mA, I _{LIM} = 20 mA	—	30	—	mA
		Ground-start	—	2	—	mA
		Ringing V _{PK_RING} = 56 V _{PK} , sinewave ringing, REN = 1	—	5.5	—	mA

Notes:

1. V_{DDD}, V_{DDA} = 3.3 V.
2. V_{DDD}, V_{DDA} = 5.25 V.
3. I_{BAT} = current from V_{BAT} (the large negative supply). For a switched-mode power supply regulator efficiency of 71%, the user can calculate the regulator current consumption as I_{BAT} • V_{BAT} / (0.71 • V_{DC}).

Table 9. Switching Characteristics—General InputsV_{DDA} = V_{DDA} = 3.13 to 5.25 V, T_A = 0 to 70°C for K-Grade, –40 to 85°C for B-Grade, C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Rise Time, $\overline{\text{RESET}}$	t _r	—	—	20	ns
RESET Pulse Width	t _{rl}	100	—	—	ns

Note: All timing (except Rise and Fall time) is referenced to the 50% level of the waveform. Input test levels are V_{IH} = V_D – 0.4 V, V_{IL} = 0.4 V. Rise and Fall times are referenced to the 20% and 80% levels of the waveform.

Table 10. Switching Characteristics—SPI

$V_{DDA} = V_{DDA} = 3.13$ to 5.25 V, $T_A = 0$ to 70°C for K-Grade, -40 to 85°C for B-Grade, $C_L = 20$ pF

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Cycle Time SCLK	t_c		0.062	—	—	μsec
Rise Time, SCLK	t_r		—	—	25	ns
Fall Time, SCLK	t_f		—	—	25	ns
Delay Time, SCLK Fall to SDO Active	t_{d1}		—	—	20	ns
Delay Time, SCLK Fall to SDO Transition	t_{d2}		—	—	20	ns
Delay Time, $\overline{\text{CS}}$ Rise to SDO Tri-state	t_{d3}		—	—	20	ns
Setup Time, $\overline{\text{CS}}$ to SCLK Fall	t_{su1}		25	—	—	ns
Hold Time, $\overline{\text{CS}}$ to SCLK Rise	t_{h1}		20	—	—	ns
Setup Time, SDI to SCLK Rise	t_{su2}		25	—	—	ns
Hold Time, SDI to SCLK Rise	t_{h2}		20	—	—	ns
Delay Time between Chip Selects	t_{cs}		220	—	—	ns
SDI to SDITHRU Propagation Delay	t_{cs}		—	4	—	ns

Note: All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_{DDA} - 0.4$ V, $V_{IL} = 0.4$ V

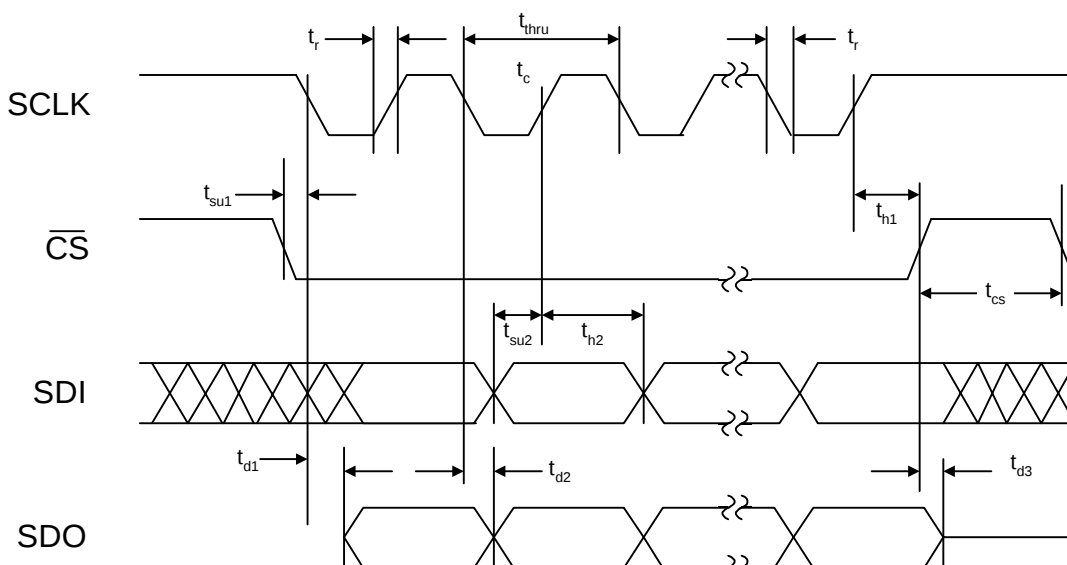


Figure 7. SPI Timing Diagram

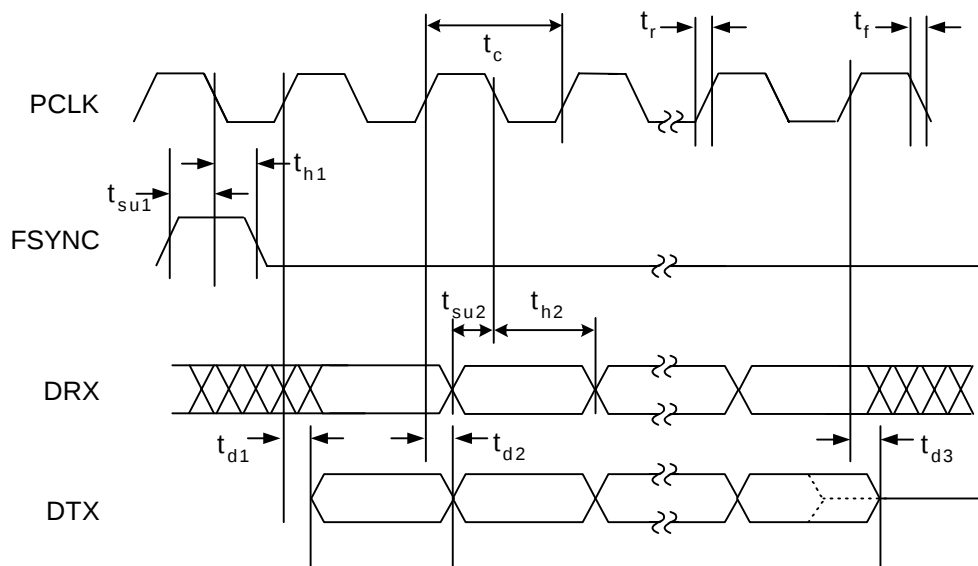
Table 11. Switching Characteristics—PCM Highway Serial Interface

$V_D = 3.13$ to 5.25 V, $T_A = 0$ to 70°C for K-Grade, -40 to 85°C for B-Grade, $C_L = 20$ pF

Parameter	Symbol	Test Conditions	Min ¹	Typ ¹	Max ¹	Units
PCLK Frequency	$1/t_c$		—	0.256	—	MHz
			—	0.512	—	MHz
			—	0.768	—	MHz
			—	1.024	—	MHz
			—	1.536	—	MHz
			—	2.048	—	MHz
			—	4.096	—	MHz
			—	8.192	—	MHz
PCLK Duty Cycle Tolerance	t_{dty}		40	50	60	%
PCLK Period Jitter Tolerance	t_{jitter}		-120	—	120	ns
Rise Time, PCLK	t_r		—	—	25	ns
Fall Time, PCLK	t_f		—	—	25	ns
Delay Time, PCLK Rise to DTX Active	t_{d1}		—	—	20	ns
Delay Time, PCLK Rise to DTX Transition	t_{d2}		—	—	20	ns
Delay Time, PCLK Rise to DTX Tri-state ²	t_{d3}		—	—	20	ns
Setup Time, FSYNC to PCLK Fall	t_{su1}		25	—	—	ns
Hold Time, FSYNC to PCLK Fall	t_{h1}		20	—	—	ns
Setup Time, DRX to PCLK Fall	t_{su2}		25	—	—	ns
Hold Time, DRX to PCLK Fall	t_{h2}		20	—	—	ns

Notes:

1. All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} - V_{I/O} - 0.4\text{V}$, $V_{IL} = 0.4\text{V}$
2. Spec applies to PCLK fall to DTX tri-state when that mode is selected ($TRI = 0$).

**Figure 8. PCM Highway Interface Timing Diagram**

Si3210/Si3211/Si3212

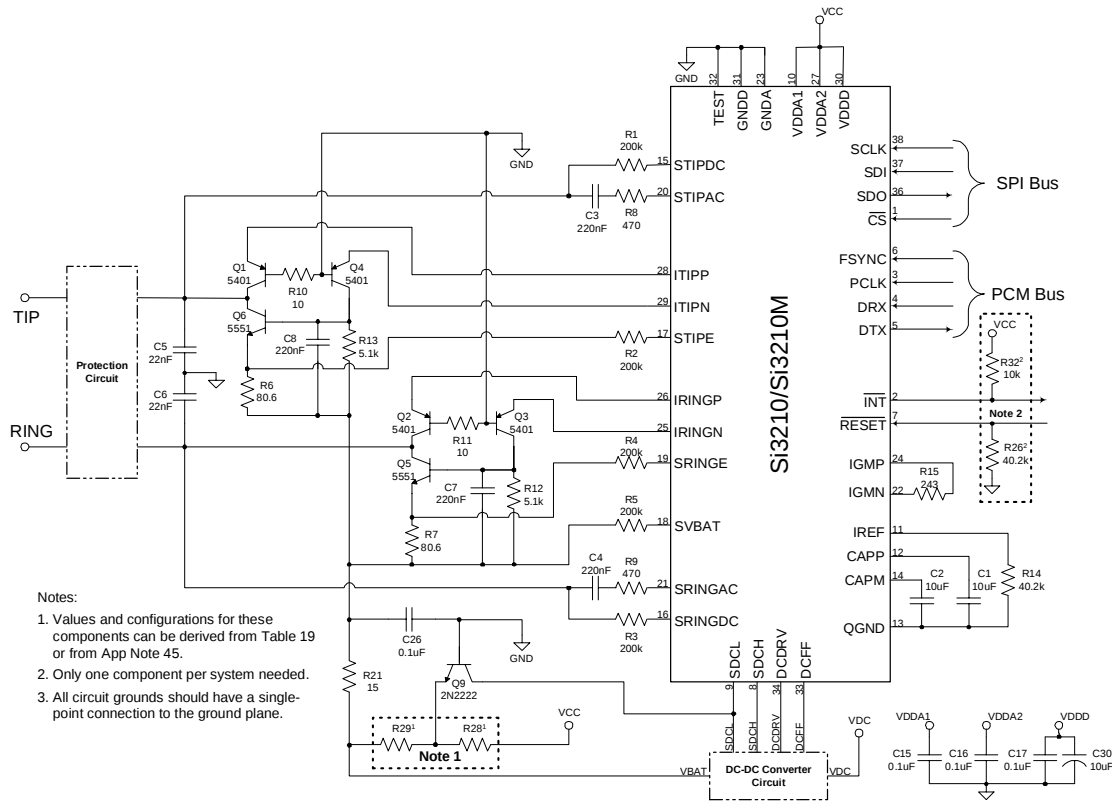
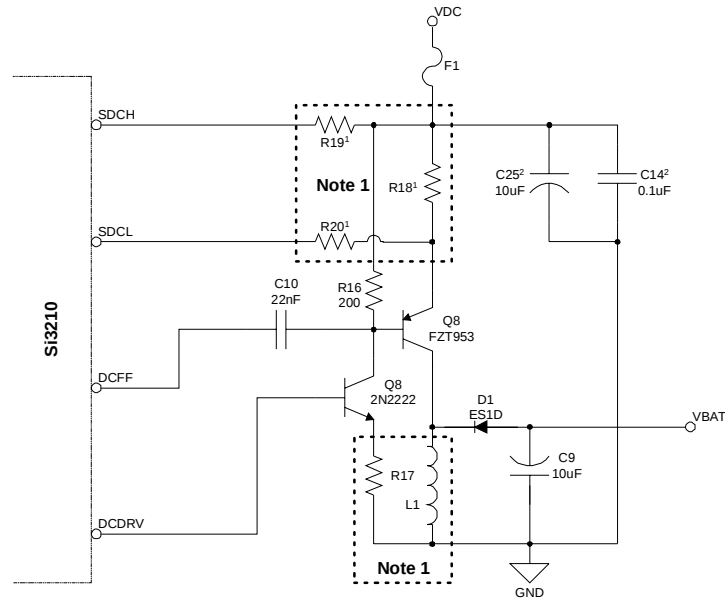


Figure 9. Si3210/Si3210M Typical Application Circuit Using Integrated DC-DC Converter

Table 12. Si3210/Si3210M External Component Values

Component	Value	Supplier/Part Number
C1,C2	10 μ F, 6 V Ceramic/Tantalum or 16 V Low Leakage Electrolytic, $\pm 20\%$	Murata, Panasonic, Nichicon URL16100MD, Panasonic Z Series
C3,C4	220 nF, 100 V, X7R, $\pm 20\%$	Murata, Johanson, Novacap, Venkel
C5,C6	22 nF, 100 V, X7R, $\pm 20\%$	Murata, Johanson, Novacap, Venkel
C7,C8	220 nF, 50 V, X7R, $\pm 20\%$	Murata, Johanson, Novacap, Venkel
C15,C16,C17	0.1 μ F, 6 V, Y5V, $\pm 20\%$	Murata, Johanson, Novacap, Venkel
C26	0.1 μ F, 100 V, X7R, $\pm 20\%$	Murata, Johanson, Novacap, Venkel
C30	10 μ F, 16 V, Electrolytic, $\pm 20\%$	Panasonic
Q1,Q2,Q3,Q4	100 V, PNP, BJT	Central Semi CMPT5401; ON Semi MMBT5401LT1, 2N5401; Zetex FMPT5401
Q5,Q6	100 V, NPN, BJT	Central Semi CZT5551, ON Semi 2N5551
Q9	NPN General Purpose BJT	ON Semi MMBT2222ALT1, MPS2222A; Central Semi CMPT2222A; Zetex FMPT2222
R1,R2,R3,R4,R5	200 k Ω , 1/10 W, $\pm 1\%$	
R6,R7	80.6 Ω , 1/4 W, $\pm 1\%$	
R8,R9	470 Ω , 1/10 W, $\pm 1\%$	
R10,R11	10 Ω , 1/10 W, $\pm 5\%$	
R12,R13	5.1 k Ω , 1/10 W, $\pm 5\%$	
R14,R26*	40.2 k Ω , 1/10 W, $\pm 1\%$	
R15	243 Ω , 1/10 W, $\pm 1\%$	
R21	15 Ω , 1/4 W, $\pm 1\%$	
R28,R29	1/10 W, $\pm 1\%$ (See AN45 or Table 17 for value selection)	
R32*	10 k Ω , 1/10 W, $\pm 5\%$	

***Note:** Only one component per system needed.



Notes:

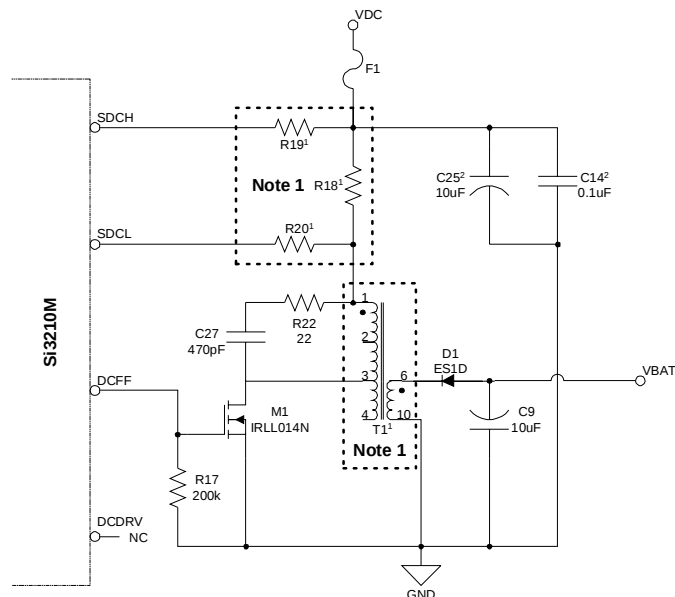
1. Values and configurations for these components can be derived from Table 21 or from App Note 45.
2. Voltage rating for C14 and C25 must be greater than VDC.

Figure 10. Si3210 BJT/Inductor DC-DC Converter Circuit

Table 13. Si3210 BJT/Inductor DC-DC Converter Component Values

Component (s)	Value	Supplier
C9	10 μ F, 100 V, Electrolytic, $\pm 20\%$	Panasonic
C10	22 nF, 50 V, X7R, $\pm 20\%$	Murata, Johanson, Novacap, Venkel
C14*	0.1 μ F, X7R, $\pm 20\%$	Murata, Johanson, Novacap, Venkel
C25*	10 μ F, Electrolytic, $\pm 20\%$	Panasonic
R16	200 Ω , 1/10 W, $\pm 5\%$	
R17	1/10 W, $\pm 5\%$ (See AN45 or Table 19 for value selection)	
R18	1/4 W, $\pm 5\%$ (See AN45 or Table 19 for value selection)	
R19,R20	1/10 W, $\pm 1\%$ (See AN45 or Table 19 for value selection)	
F1	Fuse	Belfuse SSQ Series
D1	Ultra Fast Recovery 200 V, 1A Rectifier	General Semi ES1D; Central Semi CMR1U-02
L1	1A, Shielded Inductor (See AN45 or Table 19 for value selection)	API Delevan SPD127 series, Sumida CDRH127 series, Datatronics DR340-1 series, Coilcraft DS5022, TDK SLF12565
Q7	120 V, High Current Switching PNP	Zetex FZT953, FZT955, ZTX953, ZTX955
Q8	60 V, General Purpose Switching NPN	ON Semi MMBT2222ALT1, MPS2222A; Central Semi CMPT2222A; Zetex FMMT2222

***Note:** Voltage rating of this device must be greater than V_{DC} .



Notes:

1. Values and configurations for these components can be derived from Table 20 or from App Note 45.
2. Voltage rating for C14 and C25 must be greater than VDC.

Figure 11. Si3210M MOSFET/Transformer DC-DC Converter Circuit

Table 14. Si3210M MOSFET/Transformer DC-DC Converter Component Values

Component (s)	Value	Supplier
C9	10 μ F, 100 V, Electrolytic, $\pm 20\%$	Panasonic
C14*	0.1 μ F, X7R, $\pm 20\%$	Murata, Johanson, Novacap, Venkel
C25*	10 μ F, Electrolytic, $\pm 20\%$	Panasonic
C27	470 pF, 100 V, X7R, $\pm 20\%$	Murata, Johanson, Novacap, Venkel
R17	200 k Ω , 1/10 W, $\pm 5\%$	
R18	1/4 W, $\pm 5\%$ (See AN45 or Table 18 for value selection)	
R19,R20	1/10 W, $\pm 1\%$ (See AN45 or Table 18 for value selection)	
R22	22 Ω , 1/10 W, $\pm 5\%$	
F1	Fuse	Belfuse SSQ Series
D1	Ultra Fast Recovery 200 V, 1A Rectifier	General Semi ES1D; Central Semi CMR1U-02
T1	Power Transformer	Coiltronic CTX01-15275; Datatronics SM76315; Midcom 31353R-02
M1	100 V, Logic Level Input MOSFET	Intl Rect. IRL014N; Intersil HUF76609D3S; ST Micro STD5NE10L, STN2NE10L
*Note: Voltage rating of this device must be greater than V _{DC} .		

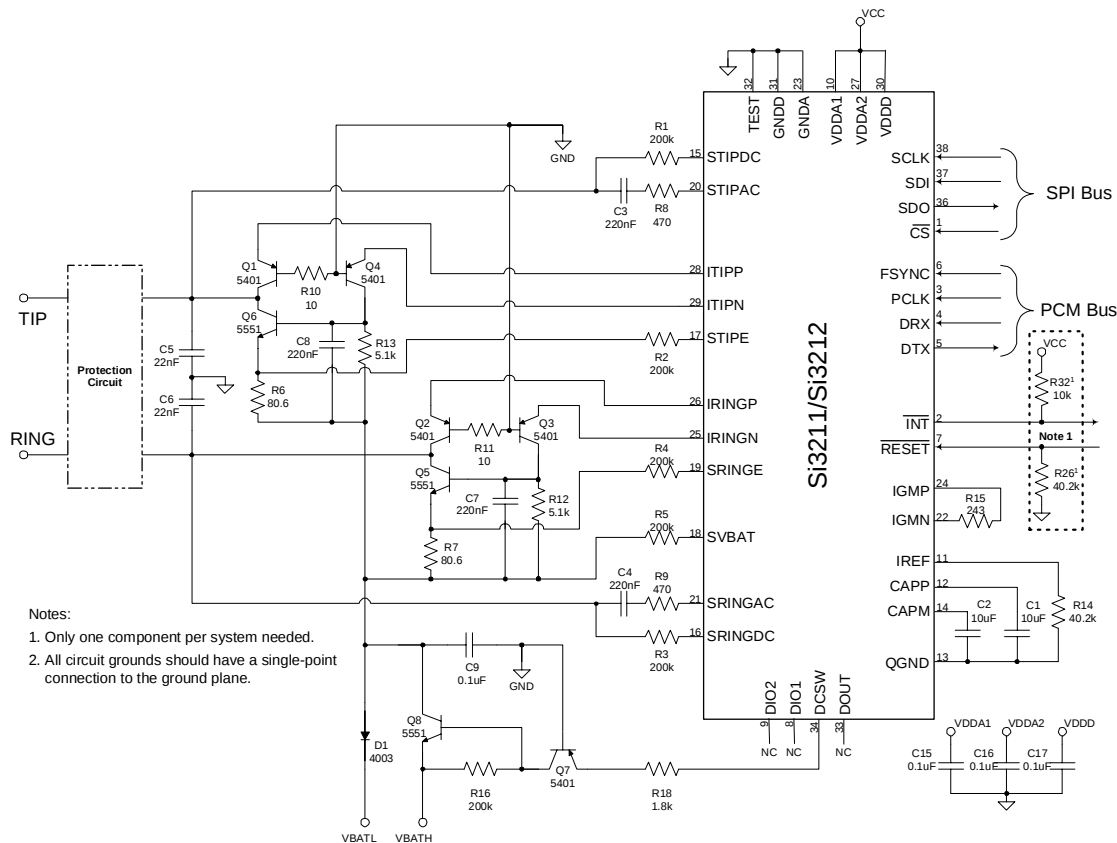


Figure 12. Si3211/12 Typical Application Circuit Using Extended Battery

Table 15. Si3211/12 External Component Values

Component	Value	Supplier/Part Number
C1,C2	10 μ F, 6 V Ceramic/Tantalum or 16 V Low Leakage Electrolytic, $\pm 20\%$	Murata, Panasonic, Nichicon URL16100MD, Panasonic Z Series
C3,C4	220 nF, 100 V, X7R, $\pm 20\%$	Murata, Johanson, Novacap, Venkel
C5,C6	22 nF, 100 V, X7R, $\pm 20\%$	Murata, Johanson, Novacap, Venkel
C7,C8	220 nF, 50 V, X7R, $\pm 20\%$	Murata, Johanson, Novacap, Venkel
C9	0.1 μ F, 100 V, Electrolytic, $\pm 20\%$	Panasonic
C15,C16,C17	0.1 μ F, 6 V, Y5V, $\pm 20\%$	Murata, Johanson, Novacap, Venkel
R1,R2,R3,R4,R5,R16	200 k Ω , 1/10 W, $\pm 1\%$	
R6,R7	80.6 Ω , 1/4 W, $\pm 1\%$	
R8,R9	470 Ω , 1/10 W, $\pm 1\%$	
R10,R11	10 Ω , 1/10 W, $\pm 5\%$	
R12,R13	5.1 k Ω , 1/10 W, $\pm 5\%$	
R14,R26*	40.2 k Ω , 1/10 W, $\pm 1\%$	
R15	243 Ω , 1/10 W, $\pm 1\%$	
R18	1.8 k Ω , 1/10 W, $\pm 5\%$	
R32*	10 k Ω , 1/10 W, $\pm 5\%$	
D1	200 V 1A Rectifier	ON Semi MRA4003, 1N4003
Q1,Q2,Q3,Q4,Q7	100 V, PNP, BJT	Central Semi CMPT5401; ON Semi MMBT5401LT1, 2N5401; Zetex FMMT5401
Q5,Q6	100 V, NPN, BJT	Central Semi CZT5551, ON Semi 2N5551
Q8	100 V, NPN, BJT	Central Semi CMPT5551, ON Semi 2N5551

***Note:** Only one component per system needed.

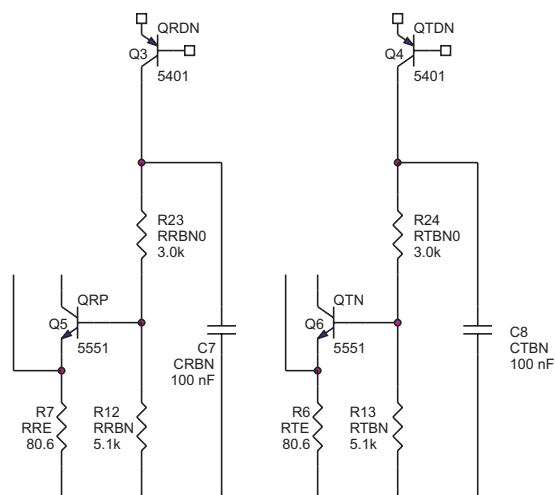


Figure 13. Si321x Optional Equivalent Q5, Q6 Bias Circuit

Table 16. Si321x Optional Bias Component Values

Component	Value	Supplier/Part Number
C7,C8	100 nF, 100 V, X7R, $\pm 20\%$	Murata, Johanson, Venkel
R23,R24	3.0 k Ω , 1/10 W, $\pm 5\%$	

The subcircuit above can be substituted into any of the ProSLIC solutions as an optional bias circuit for Q5, Q6. For this optional subcircuit, C7 and C8 are different in voltage and capacitance to the standard circuit. R23 and R24 are additional components.

Table 17. Component Value Selection for Si3210/Si3210M

Component	Value	Comments
R28	1/10 W, 1% resistor For $V_{DD} = 3.3$ V: 26.1 k Ω For $V_{DD} = 5.0$ V: 37.4 k Ω	$R28 = (V_{DD} + V_{BE})/148 \mu A$ where V_{BE} is the nominal VBE for Q9
R29	1/10 W, 1% resistor For $V_{CLAMP} = 80$ V: 541 k Ω For $V_{CLAMP} = 85$ V: 574 k Ω For $V_{CLAMP} = 100$ V: 676 k Ω	$R29 = V_{CLAMP}/148 \mu A$ where V_{CLAMP} is the clamping voltage for V_{BAT}

Table 18. Component Value Selection Examples for Si3210M MOSFET/Transformer DC-DC Converter

VDC	Ringing Load/Loop Resistance	Transformer Ratio	R18	R19, R20
3.3 V	3 REN/117 Ω	1 - 2	0.56 Ω	7.15 k Ω
5.0 V	5 REN/117 Ω	1 - 2	0.10 Ω	16.5 k Ω
12 V	5 REN/117 Ω	1 - 3	0.68 Ω	56.2 k Ω
24 V	5 REN/117 Ω	1 - 4	2.20 Ω	121 k Ω
Note: There are other system and software conditions that influence component value selection, so please refer to AN45 "Design Guide for the Si3210 DC-DC Converter for detailed guidance.				

Table 19. Component Value Selection Examples for Si3210 BJT/Inductor DC-DC Converter

VDC	Ringing Load/Loop Length	L1	R17	R18	R19, R20
5 V	3 REN/117 Ω	33 μH	100 Ω	0.12 Ω	16.5 k Ω
12 V	5 REN/117 Ω	150 μH	162 Ω	0.56 Ω	56.2 k Ω
24 V	5 REN/117 Ω	560 μH	274 Ω	2.2 Ω	121 k Ω
Note: There are other system and software conditions that influence component value selection, so please refer to AN45 "Design Guide for the Si3210 DC-DC Converter for detailed guidance.					

Functional Description

The ProSLIC™ is a single low-voltage CMOS device that provides all the SLIC, codec, DTMF detection, and signal generation functions needed for a complete analog telephone interface. The ProSLIC performs all battery, overvoltage, ringing, supervision, codec, hybrid, and test (BORSCHT) functions. Unlike most monolithic SLICs, the Si3210 does not require externally supplied high-voltage battery supplies. Instead, it generates all necessary battery voltages from a positive dc supply using its own dc-dc converter controller. Two fully programmable tone generators can produce DTMF tones, phase continuous FSK (caller ID) signaling, and call progress tones. DTMF decoding and pulse metering signal generation are also integrated.

The ProSLIC is ideal for short loop applications, such as terminal adapters, cable telephony, PBX/key systems, wireless local loop (WLL), and voice over IP solutions. The device meets all relevant LSSGR and CCITT standards.

The linefeed provides programmable on-hook voltage, programmable off-hook loop current, reverse battery operation, loop or ground start operation, and on-hook transmission ringing voltage. Loop current and voltage are continuously monitored using an integrated A/D converter. Balanced 5 REN ringing with or without a programmable dc offset is integrated. The available offset, frequency, waveshape, and cadence options are designed to ring the widest variety of terminal devices and to reduce external controller requirements.

A complete audio transmit and receive path is integrated, including DTMF decoding, ac impedance, and hybrid gain. These features are software programmable, allowing for a single hardware design to meet international requirements. Digital voice data transfer occurs over a standard PCM bus. Control data is transferred using a standard SPI. The device is available in a 38-pin TSSOP.

Linefeed Interface

The ProSLIC's linefeed interface offers a rich set of features and programmable flexibility to meet the broadest applications requirements. The dc linefeed characteristics are software programmable; key current, voltage, and power measurements are acquired in realtime and provided in software registers.

DC Feed Characteristics

The ProSLIC has programmable constant voltage and constant current zones as depicted in Figure 14. Open circuit TIP-to-RING voltage (V_{OC}) defines the constant voltage zone and is programmable from 0 V to 94.5 V in

1.5 V steps. The loop current limit (I_{LIM}) defines the constant current zone and is programmable from 20 mA to 41 mA in 3 mA steps. The ProSLIC has an inherent dc output resistance (R_O) of 160 Ω .

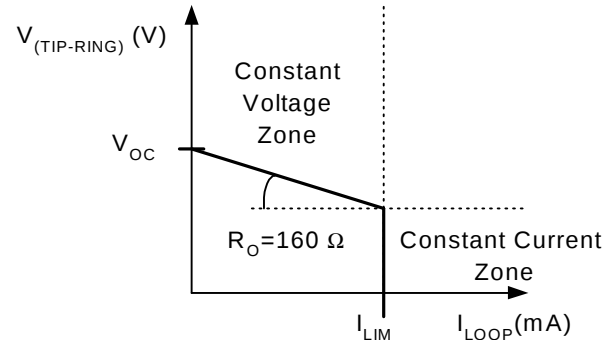


Figure 14. Simplified DC Current/Voltage Linefeed Characteristic

The TIP-to-RING voltage (V_{OC}) is offset from ground by a programmable voltage (V_{CM}) to provide voltage headroom to the positive-most terminal (TIP in forward polarity states and RING in reverse polarity states) for carrying audio signals. Table 20 summarizes the parameters to be initialized before entering an active state.

Table 20. Programmable Ranges of DC Linefeed Characteristics

Parameter	Programmable Range	Default Value	Register Bits	Location*
I_{LIM}	20 to 41 mA	20 mA	ILIM[2:0]	Direct Register 71
V_{OC}	0 to 94.5 V	48 V	VOC[5:0]	Direct Register 72
V_{CM}	0 to 94.5 V	3 V	VCM[5:0]	Direct Register 73
*Note: The ProSLIC uses registers that are both directly and indirectly mapped. A "direct" register is one that is mapped directly.				

Linefeed Architecture

The ProSLIC is a low-voltage CMOS device that uses low-cost external components to control the high voltages required for subscriber line interfaces. Figure 15 is a simplified illustration of the linefeed control loop circuit for TIP or RING and the external components used.

The ProSLIC uses both voltage and current sensing to control TIP and RING. DC and AC line voltages on TIP and RING are measured through sense resistors R_{DC} and R_{AC} , respectively. The ProSLIC uses linefeed transistors Q_P and Q_N to drive TIP and RING. Q_{DN} isolates the high-voltage base of Q_N from the ProSLIC.

The ProSLIC measures voltage at various nodes in order to monitor the linefeed current. R_{DC} , R_{SE} , and R_{BAT} provide access to these measuring points. The sense circuitry is calibrated on-chip to guarantee measurement accuracy with standard external component tolerances. See "Linefeed Calibration" on page 26 for details.

Linefeed Operation States

The ProSLIC linefeed has eight states of operation as shown in Table 21. The state of operation is controlled using the Linefeed Control register (direct Register 64).

The open state turns off all currents into the external bipolar transistors and can be used in the presence of fault conditions on the line and to generate Open Switch Intervals (OSIs). TIP and RING are effectively tri-stated with a dc output impedance of about 150 k Ω . The ProSLIC can also automatically enter the open state if it detects excessive power being consumed in the external bipolar transistors. See "Power Monitoring and Line Fault Detection" on page 24 for more details.

In the forward active and reverse active states, linefeed circuitry is on and the audio signal paths are powered down.

In the forward and reverse on-hook transmission states audio signal paths are powered up to provide data transmission during an on-hook loop condition.

The TIP Open state turns off all control currents to the external bipolar devices connected to TIP and provides an active linefeed on RING for ground start operation.

The RING Open state provides similar operation with the RING drivers off and TIP active.

The ringing state drives programmable ringing waveforms onto the line.

Loop Voltage and Current Monitoring

The ProSLIC continuously monitors the TIP and RING voltages and external BJT currents. These values are available in registers 78–89. Table 22 on page 24 lists the values that are measured and their associated registers. An internal A/D converter samples the measured voltages and currents from the analog sense circuitry and translates them into the digital domain. The A/D updates the samples at an 800 Hz rate. Two derived values are also reported—loop voltage and loop current. The loop voltage, $V_{TIP} - V_{RING}$, is reported as a 1-bit sign, 6-bit magnitude format. For ground start operation the reported value is the RING voltage. The loop current, $(I_{Q1} - I_{Q2} + I_{Q5} - I_{Q6})/2$, is reported in a 1-bit sign, 6-bit magnitude format. In RING open and TIP open states the loop current is reported as $(I_{Q1} - I_{Q2}) + (I_{Q5} - I_{Q6})$.

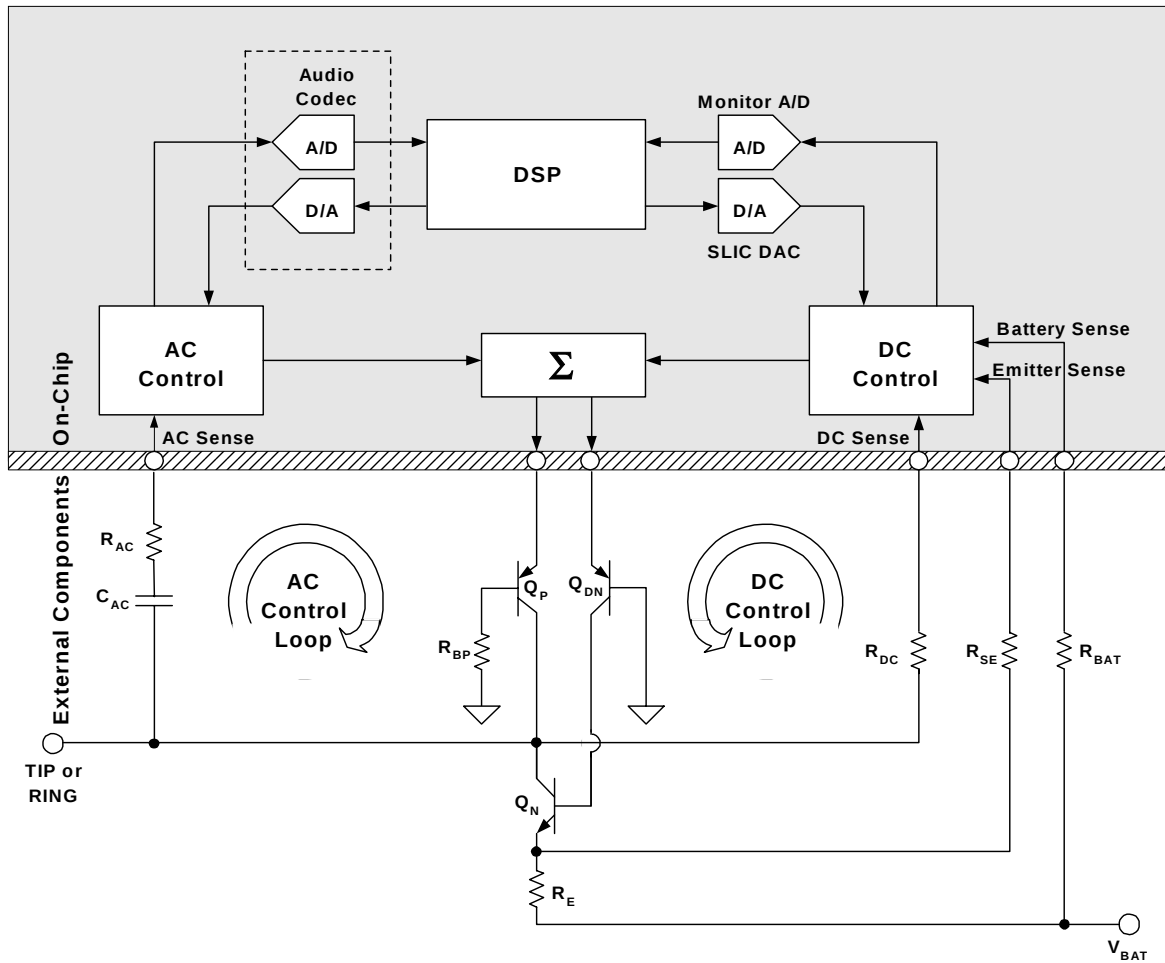


Figure 15. Simplified ProSLIC Linefeed Architecture for TIP and RING Leads (One Shown)

Table 21. ProSLIC Linefeed Operations

LF[2:0]*	Linefeed State	Description
000	Open	TIP and RING tri-stated.
001	Forward Active	$V_{TIP} > V_{RING}$.
010	Forward On-Hook Transmission	$V_{TIP} > V_{RING}$; audio signal paths powered on.
011	TIP Open	TIP tri-stated, RING active; used for ground start.
100	Ringing	Ringing waveform applied to TIP and RING.
101	Reverse Active	$V_{RING} > V_{TIP}$.
110	Reverse On-Hook Transmission	$V_{RING} > V_{TIP}$; audio signal paths powered on.
111	Ring Open	RING tri-stated, TIP active.

Note: The Linefeed register (LF) is located in direct Register 64.

Table 22. Measured Realtime Linefeed Interface Characteristics

Parameter	Measurement Range	Resolution	Register Bits	Location*
Loop Voltage Sense ($V_{TIP} - V_{RING}$)	–94.5 to +94.5 V	1.5 V	LVSP, LVS[6:0]	Direct Register 78
Loop Current Sense	–80 to +80 mA	1.27 mA	LCSP, LCS[5:0]	Direct Register 79
TIP Voltage Sense	0 to –95.88 V	0.376 V	VTIP[7:0]	Direct Register 80
RING Voltage Sense	0 to –95.88 V	0.376 V	VRING[7:0]	Direct Register 81
Battery Voltage Sense 1 (V_{BAT})	0 to –95.88 V	0.376 V	VBATS1[7:0]	Direct Register 82
Battery Voltage Sense 2 (V_{BAT})	0 to –95.88 V	0.376 V	VBATS2[7:0]	Direct Register 83
Transistor 1 Current Sense	0 to 81.35 mA	0.319 mA	IQ1[7:0]	Direct Register 84
Transistor 2 Current Sense	0 to 81.35 mA	0.319 mA	IQ2[7:0]	Direct Register 85
Transistor 3 Current Sense	0 to 9.59 mA	37.6 μ A	IQ3[7:0]	Direct Register 86
Transistor 4 Current Sense	0 to 9.59 mA	37.6 μ A	IQ4[7:0]	Direct Register 87
Transistor 5 Current Sense	0 to 80.58 mA	0.316 mA	IQ5[7:0]	Direct Register 88
Transistor 6 Current Sense	0 to 80.58 mA	0.316 mA	IQ6[7:0]	Direct Register 89
*Note: The ProSLIC uses registers that are both directly and indirectly mapped. A “direct” register is one that is mapped directly.				

Power Monitoring and Line Fault Detection

In addition to reporting voltages and currents, the ProSLIC continuously monitors the power dissipated in each external bipolar transistor. Realtime output power of any one of the six linefeed transistors can be read by setting the Power Monitor Pointer (direct Register 76) to point to the desired transistor and then reading the Line Power Output Monitor (direct Register 77).

The realtime power measurements are low-pass filtered and compared to a maximum power threshold. Maximum power thresholds and filter time constants are software programmable and should be set for each transistor pair based on the characteristics of the transistors used. Table 23 describes the registers associated with this function. If the power in any external transistor exceeds the programmed threshold, a power alarm event is triggered. The ProSLIC sets the Power Alarm register bit, generates an interrupt (if enabled), and automatically enters the Open state (if AOPN = 1). This feature protects the external transistors from fault conditions and, combined with the loop voltage and current monitors, allows diagnosis of

the type of fault condition present on the line.

The value of each thermal low-pass filter pole is set according to the equation:

$$\text{thermal LPF register} = \frac{4096}{800 \cdot \tau} \cdot 2^3$$

where τ is the thermal time constant of the transistor package, 4096 is the full range of the 12-bit register, and 800 is the sample rate in hertz. Generally $\tau = 3$ seconds for SOT223 packages and $\tau = 0.16$ seconds for SOT23, but check with the manufacturer for the package thermal constant of a specific device. For example, the power alarm threshold and low-pass filter values for Q5 and Q6 using a SOT223 package transistor are computed as follows:

$$\text{PPT56} = \frac{P_{\text{MAX}}}{\text{Resolution}} \cdot 2^7 = \frac{1.28}{0.0304} \cdot 2^7 = 5389 = 150\text{Dh}$$

Thus, indirect Register 34 should be set to 150Dh.

Note: The power monitor resolution for Q3 and Q4 is different from that of Q1, Q2, Q5, and Q6.

Table 23. Associated Power Monitoring and Power Fault Registers

Parameter	Description/ Range	Resolution	Register Bits	Location*
Power Monitor Pointer	0 to 5 points to Q1 to Q6, respectively	n/a	PWRMP[2:0]	Direct Register 76
Line Power Monitor Output	0 to 7.8 W for Q1, Q2, Q5, Q6 0 to 0.9 W for Q3, Q4	30.4 mW 3.62 mW	PWROM[7:0]	Direct Register 77
Power Alarm Threshold, Q1 & Q2	0 to 7.8 W	30.4 mW	PPT12[7:0]	Indirect Register 32
Power Alarm Threshold, Q3 & Q4	0 to 0.9 W	3.62 mW	PPT34[7:0]	Indirect Register 33
Power Alarm Threshold, Q5 & Q6	0 to 7.8 W	30.4 mW	PPT56[7:0]	Indirect Register 34
Thermal LPF Pole, Q1 & Q2	see equation above		NQ12[7:0]	Indirect Register 37
Thermal LPF Pole, Q3 & Q4	see equation above		NQ34[7:0]	Indirect Register 38
Thermal LPF Pole, Q5 & Q6	see equation above		NQ56[7:0]	Indirect Register 39
Power Alarm Interrupt Pending	Bits 2 to 7 correspond to Q1 to Q6, respectively	n/a	QnAP[n+1], where n = 1 to 6	Direct Register 19
Power Alarm Interrupt Enable	Bits 2 to 7 correspond to Q1 to Q6, respectively	n/a	QnAE[n+1], where n = 1 to 6	Direct Register 22
Power Alarm Automatic/Manual Detect	0 = manual mode 1 = enter open state upon power alarm	n/a	AOPN	Direct Register 67
*Note: The ProSLIC uses registers that are both directly and indirectly mapped. A “direct” register is one that is mapped directly. An “indirect” register is one that is accessed using the indirect access registers (direct registers 28 through 31).				

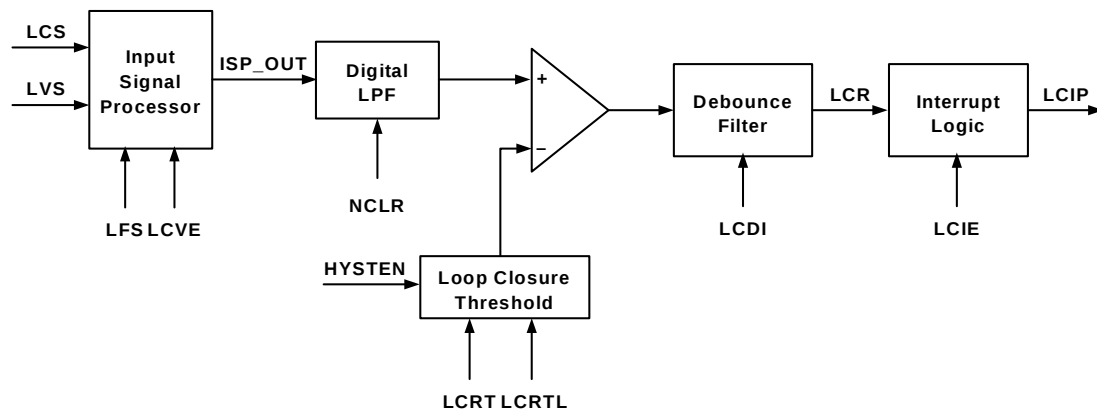


Figure 16. Loop Closure Detection

Loop Closure Detection

A loop closure event signals that the terminal equipment has gone off-hook during on-hook transmission or on-hook active states. The ProSLIC performs loop closure detection digitally using its on-chip monitor A/D converter. The functional blocks required to implement loop closure detection are shown in Figure 16. The primary input to the system is the Loop Current Sense value provided in the LCS register (direct Register 79). The LCS value is processed in the Input Signal Processor when the ProSLIC is in the on-hook transmission or on-hook active linefeed state, as indicated by the Linefeed Shadow register, LFS[2:0] (direct Register 64). The data then feeds into a programmable digital low-pass filter, which removes unwanted ac signal components before threshold detection.

The output of the low-pass filter is compared to a programmable threshold, LCRT (indirect register 28). The threshold comparator output feeds a programmable debouncing filter. The output of the debouncing filter remains in its present state unless the input remains in the opposite state for the entire period of time programmed by the loop closure debounce interval, LCDI (direct Register 69). If the debounce interval has been satisfied, the LCR bit will be set to indicate that a valid loop closure has occurred. A loop closure interrupt is generated if enabled by the LCIE bit (direct Register 22). Table 24 lists the registers that must be written or monitored to correctly detect a loop closure condition.

Loop Closure Threshold Hysteresis

Silicon revisions C and higher support the addition of programmable hysteresis to the loop closure threshold, which can be enabled by setting HYSTEN = 1 (direct Register 108, bit 0). The hysteresis is defined by LCRT (indirect Register 28) and LCRTL (indirect Register 43),

which set the upper and lower bounds, respectively.

Voltage-Based Loop Closure Detection

Silicon revisions C and higher also support an optional voltage-based loop closure detection mode, which is enabled by setting LCVE = 1 (direct Register 108, bit 2). In this mode the loop voltage is compared to the loop closure threshold register (LCRT) which represents a minimum voltage threshold instead of a maximum current threshold. If hysteresis is also enabled, then LCRT represents the upper voltage boundary and LCRTL represents the lower voltage boundary for hysteresis. Although voltage-based loop closure detection is an option, the default current-based loop closure detection is recommended.

Table 24. Register Set for Loop Closure Detection

Parameter	Register	Location
Loop Closure Interrupt Pending	LCIP	Direct Reg. 19
Loop Closure Interrupt Enable	LCIE	Direct Reg. 22
Loop Closure Threshold	LCRT[5:0]	Indirect Reg. 28
Loop Closure Threshold—Lower	LCRTL[5:0]	Indirect Reg. 43
Loop Closure Filter Coefficient	NCLR[12:0]	Indirect Reg. 35
Loop Closure Detect Status (monitor only)	LCR	Direct Reg. 68
Loop Closure Detect Debounce Interval	LCDI[6:0]	Direct Reg. 69
Hysteresis Enable	HYSTEN	Direct Reg. 108
Voltage-Based Loop Closure	LCVE	Direct Reg. 108

Linefeed Calibration

An internal calibration algorithm corrects for internal and external component errors. The calibration is initiated by setting the CAL bit in direct Register 96. Upon completion of the calibration cycle, this bit is automatically reset.

It is recommended that a calibration be executed following system power-up. Upon release of the chip reset, the Si3210 will be in the open state. After powering up the dc-dc converter and allowing it to settle for time (t_{settle}) the calibration can be initiated. Additional calibrations may be performed, but only one calibration should be necessary as long as the system remains powered up.

During calibration, V_{BAT} , V_{TIP} and V_{RING} voltages are controlled by the calibration engine to provide the correct external voltage conditions for the algorithm. Calibration should be performed in the on-hook state. RING or TIP must not be connected to ground during the calibration.

Battery Voltage Generation and Switching

The ProSLIC supports two modes of battery supply operation. First, the Si3210 integrates a dc-dc converter controller that dynamically regulates a single output voltage. This mode eliminates the need to supply large external battery voltages. Instead, it converts a single positive input voltage into the real-time battery voltage needed for any given state according to programmed linefeed parameters. Second, the Si3211 and Si3212 support switching between high and low battery voltage supplies, as would a traditional monolithic SLIC.

For single to low channel count applications, the Si3210 proves to be an economical choice, as the dc-dc converter eliminates the need to design and build high-voltage power supplies. For higher channel count applications where centralized battery voltage supply is economical, or for modular legacy systems where battery voltage is already available, the Si3211 and Si3212 are recommended.

DC-DC Converter General Description (Si3210/Si3210M Only)

The dc-dc converter dynamically generates the large negative voltages required to operate the linefeed interface. The Si3210 acts as the controller for a buck-boost dc-dc converter that converts a positive dc voltage into the desired negative battery voltage. In addition to eliminating external power supplies, this allows the Si3210 to dynamically control the battery voltage to the minimum required for any given mode of operation.

Two different dc-dc circuit options are offered: a BJT/inductor version and a MOSFET/transformer version.

Due to the differences on the driving circuits, there are two different versions of the Si3210. The Si3210 supports the BJT/inductor circuit option, and the Si3210M version supports the MOSFET solution. The only difference between the two versions is the polarity of the DCFF pin with respect to the DCDRV pin. For the Si3210, DCDRV and DCFF are opposite polarity. For the Si3210M, DCDRV and DCFF are the same polarity. Table 25 summarizes these differences.

Table 25. Si3210 and Si3210M Differences

Device	DCFF Signal Polarity	DCPOL
Si3210	= $\overline{\text{DCDRV}}$	0
Si3210M	= DCDRV	1
Notes: 1. DCFF signal polarity with respect to DCDRV signal. 2. Direct Register 93, bit 5; This is a read-only bit.		

Extensive design guidance on each of these circuits can be obtained from Application Note 45 (AN45) and from an interactive dc-dc converter design spreadsheet. Both of these documents are available on the Silicon Laboratories website (www.silabs.com).

BJT/Inductor Circuit Option Using Si3210

The BJT/Inductor circuit option, as defined in Figure 9, offers a flexible, low-cost solution. Depending on selected L1 inductance value and the switching frequency, the input voltage (V_{DC}) can range from 5 V to 30 V. By nature of a dc-dc converter's operation, peak and average input currents can become large with small input voltages. Consider this when selecting the appropriate input voltage and power rating for the V_{DC} power supply.

For this solution, a PNP power BJT (Q7) switches the current flow through low ESR inductor L1. The Si3210 uses the DCDRV and DCFF pins to switch Q7 on and off. DCDRV controls Q7 through NPN BJT Q8. DCFF is ac coupled to Q7 through capacitor C10 to assist R16 in turning off Q7. Therefore, DCFF must have opposite polarity to DCDRV, and the Si3210 (not Si3210M) must be used.

MOSFET/Transformer Circuit Option Using Si3210M

The MOSFET/transformer circuit option, as defined in Figure 11, offers higher power efficiencies across a larger input voltage range. Depending on the transformers primary inductor value and the switching frequency, the input voltage (V_{DC}) can range from 3.3 V to 35 V. Therefore, it is possible to power the entire ProSLIC solution from a single 3.3 V or 5 V power supply. By nature of a dc-dc converter's operation, peak

Si3210/Si3211/Si3212

and average input currents can become large with small input voltages. Consider this when selecting the appropriate input voltage and power rating for the V_{DC} power supply (number of REN supported).

For this solution, an n-channel power MOSFET (M1) switches the current flow through a power transformer T1. T1 is specified in Application Note 45 (AN45), and includes several taps on the primary side to facilitate a wide range of input voltages. The Si3210M version of the Si3210 must be used for the application circuit depicted in Figure 9 because the DCFF pin is used to drive M1 directly and therefore must be the same polarity as DCDRV. DCDRV is not used in this circuit option; connecting DCFF and DCDRV together is not recommended.

DC-DC Converter Architecture (Si3210/Si3210M Only)

The control logic for a pulse width modulated (PWM) dc-dc converter is incorporated in the Si3210. Output pins, DCDRV and DCFF, are used to switch a bipolar transistor or MOSFET. The polarity of DCFF is opposite to that of DCDRV.

The dc-dc converter circuit is powered on when the DCOF bit in the Power Down Register (direct Register 14, bit 4) is cleared to 0. The switching regulator circuit within the Si3210 is a high performance, pulse-width modulation controller. The control pins are driven by the PWM controller logic in the Si3210. The regulated output voltage (V_{BAT}) is sensed by the SVBAT pin and is used to detect whether the output voltage is above or below an internal reference for the desired battery voltage. The dc monitor pins SDCH and SDCL monitor input current and voltage to the dc-dc converter external circuitry. If an overload condition is detected, the PWM controller will turn off the switching transistor for the remainder of a PWM period to prevent damage to external components. It is important that the proper value of R18 be selected to ensure safe operation. Guidance is given in Application Note 45 (AN45).

The PWM controller operates at a frequency set by the dc-dc Converter PWM register (direct Register 92). During a PWM period the outputs of the control pins DCDRV and DCFF are asserted for a time given by the read-only PWM Pulse Width register (direct Register 94).

The dc-dc converter must be off for some time in each cycle to allow the inductor or transformer to transfer its stored energy to the output capacitor, C9. This minimum off time can be set through the dc-dc Converter Switching Delay register, (direct Register 93). The number of 16.384 MHz clock cycles that the controller is off is equal to DCTOF (bits 0 through 4) plus 4. If the dc

Monitor pins detect an overload condition, the dc-dc converter interrupts its conversion cycles regardless of the register settings to prevent component damage. These inputs should be calibrated by writing the DCCAL bit (bit 7) of the dc-dc Converter Switching Delay register, direct Register 93, after the dc-dc converter has been turned on.

Because the Si3210 dynamically regulates its own battery supply voltage using the dc-dc converter controller, the battery voltage (V_{BAT}) is offset from the negative-most terminal by a programmable voltage (V_{OV}) to allow voltage headroom for carrying audio signals.

As mentioned previously, the Si3210 dynamically adjusts V_{BAT} to suit the particular circuit requirement. To illustrate this, the behavior of V_{BAT} in the active state is shown in Figure 17. In the active state, the TIP-to-RING open circuit voltage is kept at V_{OC} in the constant voltage region while the regulator output voltage, $V_{BAT} = V_{CM} + V_{OC} + V_{OV}$.

When the loop current attempts to exceed I_{LIM} , the dc line driver circuit enters constant current mode allowing the TIP to RING voltage to track R_{LOOP} . As the TIP terminal is kept at a constant voltage, it is the RING terminal voltage that tracks R_{LOOP} and, as a result, the $|V_{BAT}|$ voltage will also track R_{LOOP} . In this state, $|V_{BAT}| = I_{LIM} \cdot R_{LOOP} + V_{CM} + V_{OV}$. As R_{LOOP} decreases below the V_{OC}/I_{LIM} mark, the regulator output voltage can continue to track R_{LOOP} (TRACK = 1), or the R_{LOOP} tracking mechanism is stopped when $|V_{BAT}| = |V_{BATL}|$ (TRACK = 0). The former case is the more common application and provides the maximum power dissipation savings. In principle, the regulator output voltage can go as low as $|V_{BAT}| = V_{CM} + V_{OV}$, offering significant power savings.

When TRACK = 0, $|V_{BAT}|$ will not decrease below V_{BATL} . The RING terminal voltage, however, continues to decrease with decreasing R_{LOOP} . The power dissipation on the NPN bipolar transistor driving the RING terminal can become large and may require a higher power rating device. The non-tracking mode of operation is required by specific terminal equipment which, in order to initiate certain data transmission modes, goes briefly on-hook to measure the line voltage to determine whether there is any other off-hook terminal equipment on the same line. TRACK = 0 mode is desired since the regulator output voltage has long settling time constants (on the order of tens of milliseconds) and cannot change rapidly for TRACK = 1 mode. Therefore, the brief on-hook voltage measurement would yield approximately the same voltage as the off-hook line voltage and would cause the terminal equipment to incorrectly sense another off-hook terminal.

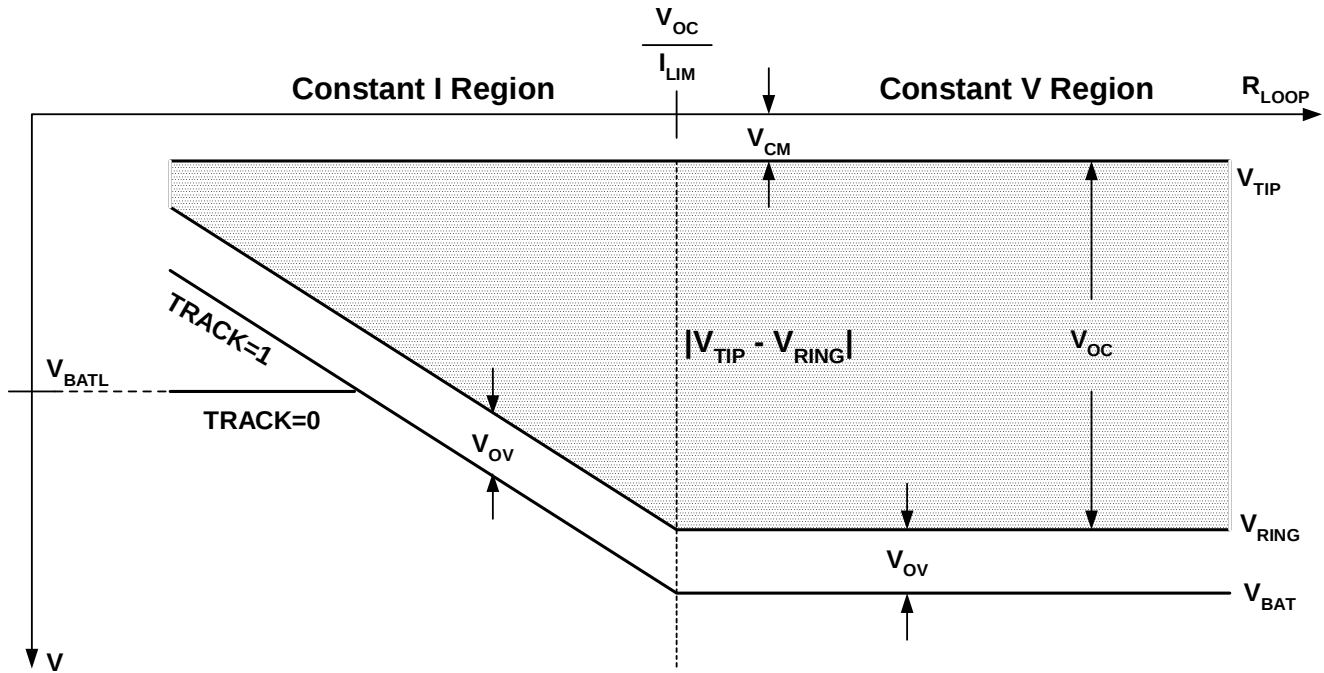
Figure 17. V_{TIP} , V_{RING} , and V_{BAT} in the Forward Active State

Table 26. Associated Relevant DC-DC Converter Registers

Parameter	Range	Resolution	Register Bit	Location
DC-DC Converter Power-off Control	n/a	n/a	DCOF	Direct Register 14
DC-DC Converter Calibration Enable/Status	n/a	n/a	DCCAL	Direct Register 93
DC-DC Converter PWM Period	0 to 15.564 μ s	61.035 ns	DCN[7:0]	Direct Register 92
DC-DC Converter Min. Off Time	(0 to 1.892 μ s) + 4 ns	61.035 ns	DCTOF[4:0]	Direct Register 93
High Battery Voltage— V_{BATH}	0 to -94.5 V	1.5 V	VBATH[5:0]	Direct Register 74
Low Battery Voltage— V_{BATL}	0 to -94.5 V	1.5 V	VBATL[5:0]	Direct Register 75
V_{OV}	0 to -9 V or 0 to -13.5 V	1.5 V	VMIND[3:0] VOV	Indirect Register 41 Direct Register 66

Note: The ProSLIC uses registers that are both directly and indirectly mapped. A “direct” register is one that is mapped directly. An “indirect” register is one that is accessed using the indirect access registers (direct registers 28 through 31).

DC-DC Converter Enhancements

Silicon revisions C and higher support two enhancements to the dc-dc converter. The first is a multi-threshold error control algorithm that enables the dc-dc converter to adjust more quickly to voltage changes. This option is enabled by setting DCSU = 1 (direct Register 108, bit 5). The second enhancement is an audio band filter that removes audio band noise from the dc-dc converter control loop. This option is enabled by setting DCFIL = 1 (direct Register 108, bit 1).

DC-DC Converter During Ringing

When the ProSLIC enters the ringing state, it requires voltages well above those used in the active mode. The voltage to be generated and regulated by the dc-dc converter during a ringing burst is set using the VBATH register (direct Register 74). VBATH can be set between 0 and -94.5 V in 1.5 V steps. To avoid clipping the ringing signal, V_{BATH} must be set larger than the ringing amplitude. At the end of each ringing burst the dc-dc converter adjusts back to active state regulation as described above.

External Battery Switching (Si3211 and Si3212 Only)

The Si3211 and Si3212 support switching between two battery voltages. The circuit for external battery switching is defined in Figure 12. Typically a high voltage battery (e.g., -70 V) is used for on-hook and ringing states, and a low voltage battery (e.g., -24 V) is used for the off-hook condition. The ProSLIC uses an external transistor to switch between the two supplies.

When the ProSLIC changes operating states, it automatically switches battery supplies if the automatic/manual control bit ABAT (direct Register 67, bit 3) is set. For example, the ProSLIC will switch from high battery to low battery when it detects an off-hook event through either a ring trip or loop closure event. If automatic battery selection is disabled (ABAT = 0), the battery is selected by the Battery Feed Select bit, BATSL (direct Register 66, bit 1).

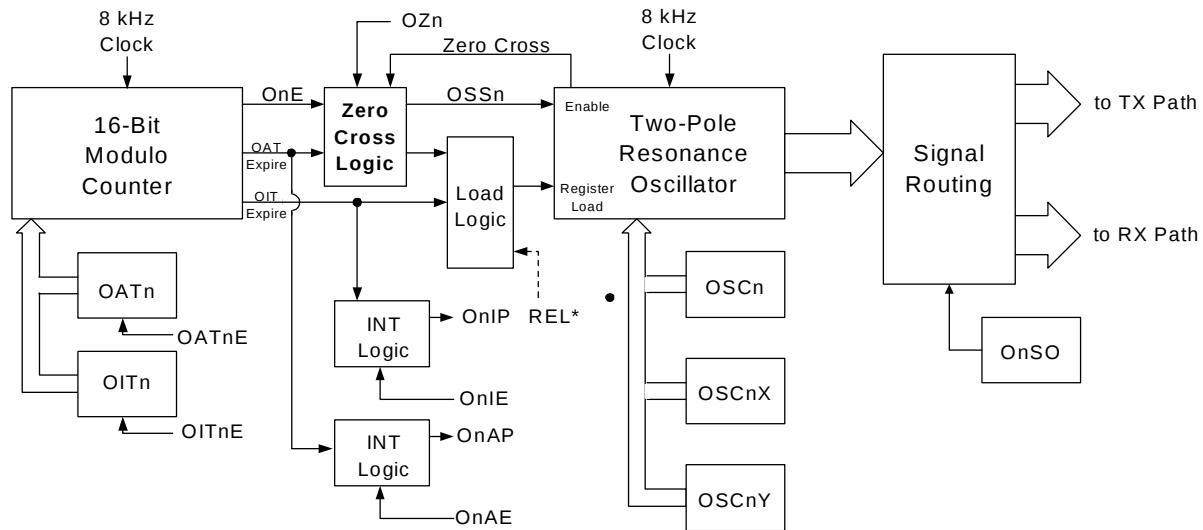
Silicon revisions C and higher support the option to add a 60 ms debounce period to the battery switching circuit when transitioning from high battery to low battery. This option is enabled by setting SWDB = 1 (direct Register 108, bit 3). This debounce minimizes battery transitions in the case of pulse dialing or other quick on-hook to off-hook transitions.

Tone Generation

Two digital tone generators are provided in the ProSLIC. They allow the generation of a wide variety of single or dual tone frequency and amplitude combinations and spare the user the effort of generating the required POTS signaling tones on the PCM highway. DTMF, FSK (caller ID), call progress, and other tones can all be generated on-chip. The tones can be sent to either the receive or transmit paths (see Figure 23 on page 40).

Tone Generator Architecture

A simplified diagram of the tone generator architecture is shown in Figure 18. The oscillator, active/inactive timers, interrupt block, and signal routing block are connected to give the user flexibility in creating audio signals. Control and status register bits are placed in the figure to indicate their association with the tone generator architecture. These registers are described in more detail in Table 27.



*Tone Generator 1 Only
n = "1" or "2" for Tone Generator 1 and 2, respectively

Figure 18. Simplified Tone Generator Diagram

Oscillator Frequency and Amplitude

Each of the two tone generators contains a two-pole resonate oscillator circuit with a programmable frequency and amplitude, which are programmed via indirect registers OSC1, OSC1X, OSC1Y, OSC2, OSC2X, and OSC2Y. The sample rate for the two oscillators is 8000 Hz. The equations are as follows:

$$\text{coeff}_n = \cos(2\pi f_n / 8000 \text{ Hz}),$$

where f_n is the frequency to be generated;

$$\text{OSCn} = \text{coeff}_n \cdot (2^{15});$$

$$\text{OSCnX} = \frac{1}{4} \cdot \frac{\sqrt{1 - \text{coeff}}}{\sqrt{1 + \text{coeff}}} \cdot (2^{15} - 1) \cdot \frac{\text{Desired } V_{\text{RMS}}}{1.11 V_{\text{RMS}}}$$

where desired V_{rms} is the amplitude to be generated;

$$\text{OSCnY} = 0,$$

n = 1 or 2 for oscillator 1 or oscillator 2, respectively.

For example, in order to generate a DTMF digit of 8, the two required tones are 852 Hz and 1336 Hz. Assuming the generation of half-scale values (ignoring twist) is desired, the following values are calculated:

$$\text{coeff}_1 = \cos\left(\frac{2\pi 852}{8000}\right) = 0.78434$$

$$\text{OSC1} = 0.78434(2^{15}) = 25701 = 6465\text{h}$$

$$\text{OSC1X} = \frac{1}{4} \cdot \frac{\sqrt{0.21556}}{\sqrt{1.78434}} \cdot (2^{15} - 1) \cdot 0.5 = 1424 = 590\text{h}$$

$$\text{OSC1Y} = 0$$

$$\text{coeff}_2 = \cos\left(\frac{2\pi 1336}{8000}\right) = 0.49819$$

$$\text{OSC2} = 0.49819(2^{15}) = 16324 = 3\text{FC4h}$$

$$\text{OSC2X} = \frac{1}{4} \cdot \frac{\sqrt{0.50181}}{\sqrt{1.49819}} \cdot (2^{15} - 1) \cdot 0.5 = 2370 = 942\text{h}$$

$$\text{OSC2Y} = 0$$

The computed values above would be written to the corresponding registers to initialize the oscillators. Once the oscillators are initialized, the oscillator control registers can be accessed to enable the oscillators and direct their outputs.

Tone Generator Cadence Programming

Each of the two tone generators contains two timers, one for setting the active period and one for setting the inactive period. The oscillator signal is generated during the active period and suspended during the inactive period. Both the active and inactive periods can be programmed from 0 to 8 seconds in 125 μs steps. The active period time interval is set using OAT1 (direct registers 36 and 37) for tone generator 1 and OAT2 (direct registers 40 and 41) for tone generator 2.

To enable automatic cadence for tone generator 1, define the OAT1 and OIT1 registers and then set the O1TAE bit (direct Register 32, bit 4) and O1TIE bit (direct Register 32, bit 3). This enables each of the timers to control the state of the Oscillator Enable bit, O1E (direct Register 32, bit 2). The 16-bit counter will begin counting until the active timer expires, at which

time the 16-bit counter will reset to zero and begin counting until the inactive timer expires. The cadence continues until the user clears the O1TAE and O1TIE control bits. The zero crossing detect feature can be implemented by setting the OZ1 bit (direct Register 32, bit 5). This ensures that each oscillator pulse ends without a dc component. The timing diagram in Figure 19 is an example of an output cadence using the zero crossing feature.

One-shot oscillation can be achieved by enabling O1E and O1TAE. Direct control over the cadence can be achieved by controlling the O1E bit (direct Register 32, bit 2) directly if O1TAE and O1TIE are disabled.

The operation of tone generator 2 is identical to that of tone generator 1 using its respective control registers.

Note: Tone Generator 2 should not be enabled simultaneously with the ringing oscillator due to resource sharing within the hardware.

Continuous phase frequency-shift keying (FSK) waveforms may be created using tone generator 1 (not available on tone generator 2) by setting the REL bit (direct Register 32, bit 6), which enables reloading of the OSC1, OSC1X, and OSC1Y registers at the expiration of the active timer (OAT1).

Table 27. Associated Tone Generator Registers

Tone Generator 1			
Parameter	Description / Range	Register Bits	Location
Oscillator 1 Frequency Coefficient	Sets oscillator frequency	OSC1[15:0]	Indirect Register 13
Oscillator 1 Amplitude Coefficient	Sets oscillator amplitude	OSC1X[15:0]	Indirect Register 14
Oscillator 1 initial phase coefficient	Sets initial phase	OSC1Y[15:0]	Indirect Register 15
Oscillator 1 Active Timer	0 to 8 sec	OAT1[15:0]	Direct Registers 36 & 37
Oscillator 1 Inactive Timer	0 to 8 sec	OIT1[15:0]	Direct Register 38 & 39
Oscillator 1 Control	Status and control registers	OSS1, REL, OZ1, O1TAE, O1TIE, O1E, O1SO[1:0]	Direct Register 32
Tone Generator 2			
Parameter	Description / Range	Register	Location
Oscillator 2 Frequency Coefficient	Sets oscillator frequency	OSC2[15:0]	Indirect Register 16
Oscillator 2 Amplitude Coefficient	Sets oscillator amplitude	OSC2X[15:0]	Indirect Register 17
Oscillator 2 initial phase coefficient	Sets initial phase	OSC2Y[15:0]	Indirect Register 18
Oscillator 2 Active Timer	0 to 8 sec	OAT2[15:0]	Direct Registers 40 & 41
Oscillator 2 Inactive Timer	0 to 8 sec	OIT2[15:0]	Direct Register 42 & 43
Oscillator 2 Control	Status and control registers	OSS2, OZ2, O2TAE, O2TIE, O2E, O2SO[1:0]	Direct Register 33

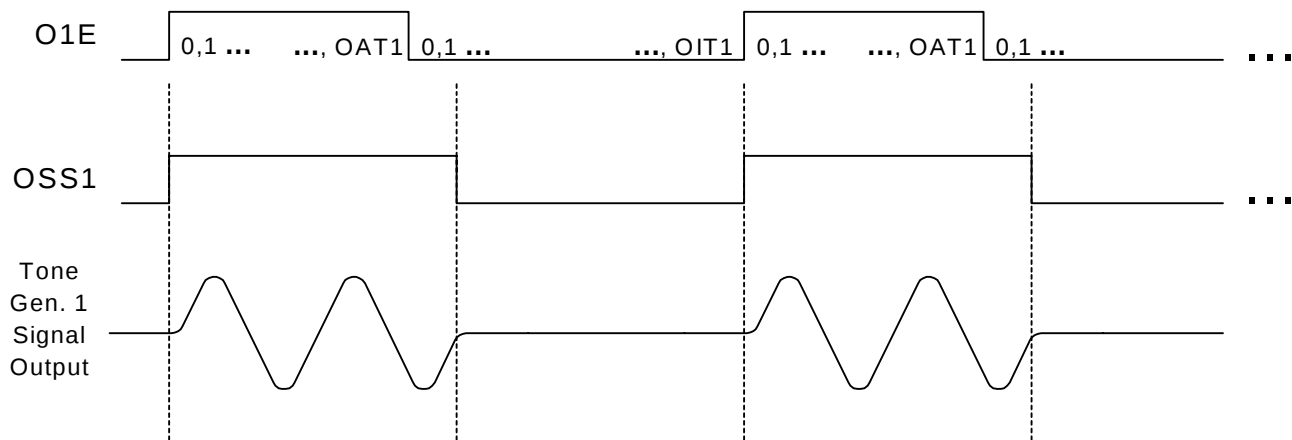


Figure 19. Tone Generator Timing Diagram

Enhanced FSK Waveform Generation

Silicon revisions C and higher support enhanced FSK generation capabilities, which can be enabled by setting FSKEN = 1 (direct Register 108, bit 6) and REN = 1 (direct Register 32, bit 6). In this mode, the user can define mark (1) and space (0) attributes once during initialization by defining indirect registers 99–104. The user need only indicate 0-to-1 and 1-to-0 transitions in the information stream. By writing to FSKDAT (direct Register 52), this mode applies a 24 kHz sample rate to tone generator 1 to give additional resolution to timers and frequency generation. Application Note 32 gives detailed instructions on how to implement FSK in this mode. Additionally, sample source code is available from Silicon Laboratories upon request.

Tone Generator Interrupts

Both the active and inactive timers can generate their own interrupt to signal “on/off” transitions to the software. The timer interrupts for tone generator 1 can be individually enabled by setting the O1AE and O1IE bits (direct Register 21, bits 0 and 1, respectively). Timer interrupts for tone generator two are O2AE and O2IE (direct Register 21, bits 2 and 3, respectively). A pending interrupt for each of the timers is determined by reading the O1AP, O1IP, O2AP, and O2IP bits in the Interrupt Status 1 register (direct Register 18, bits 0 through 3, respectively).

Ring Generation

The ProSLIC provides fully programmable internal balanced ringing with or without a dc offset to ring a wide variety of terminal devices. All parameters associated with ringing are software programmable: ringing frequency, waveform, amplitude, dc offset, and

ringing cadence. Both sinusoidal and trapezoidal ringing waveforms are supported, and the trapezoidal crest factor is programmable. Ringing signals of up to 88 V peak or more can be generated, enabling the ProSLIC to drive a 5 REN (1380 Ω + 40 μ F) ringer load across loop lengths of 2000 feet (160 Ω) or more.

Ring Architecture

The ringing generator architecture is nearly identical to that of the tone generator. The sinusoid ringing waveform is generated using an internal two-pole resonance oscillator circuit with programmable frequency and amplitude. However, since ringing frequencies are very low compared to the audio band signaling frequencies, the ringing waveform is generated at a 1 kHz rate instead of 8 kHz.

The ringing generator has two timers that function the same as for the tone generator timers. They allow on/off cadence settings up to 8 sec on/ 8 sec off. In addition to controlling ringing cadence, these timers control the transition into and out of the ringing state. Table 28 summarizes the list of registers used for ringing generation.

Note: Tone generator 2 should not be enabled concurrently with the ringing generator due to resource sharing within the hardware.

Table 28. Registers for Ringing Generation

Parameter	Range/ Description	Register Bits	Location
Ringing Waveform	Sine/Trapezoid	TSWS	Direct Register 34
Ringing Voltage Offset Enable	Enabled/ Disabled	RVO	Direct Register 34
Ringing Active Timer Enable	Enabled/ Disabled	RTAE	Direct Register 34
Ringing Inactive Timer Enable	Enabled/ Disabled	RTIE	Direct Register 34
Ringing Oscillator Enable	Enabled/ Disabled	ROE	Direct Register 34
Ringing Oscillator Active Timer	0 to 8 sec	RAT[15:0]	Direct Registers 48 and 49
Ringing Oscillator Inactive Timer	0 to 8 sec	RIT[15:0]	Direct Registers 50 and 51
Linefeed Control (Initiates Ringing State)	Ringing State = 100b	LF[2:0]	Direct Register 64
High Battery Voltage	0 to -94.5 V	VBATH[5:0]	Direct Register 74
Ringing dc voltage offset	0 to 94.5 V	ROFF[15:0]	Indirect Register 19
Ringing frequency	15 to 100 Hz	RCO[15:0]	Indirect Register 20
Ringing amplitude	0 to 94.5 V	RNGX[15:0]	Indirect Register 21
Ringing initial phase	Sets initial phase for sinewave and period for trapezoid	RNGY[15:0]	Indirect Register 22
Common Mode Bias Adjust During Ringing	0 to 22.5 V	VCMR[3:0]	Indirect Register 40
Note: The ProSLIC uses registers that are both directly and indirectly mapped. A "direct" register is one that is mapped directly. An "indirect" register is one that is accessed using the indirect access registers (direct registers 28 through 31).			

When the ringing state is invoked by writing LF[2:0] = 100 (direct Register 64), the ProSLIC will go into the ringing state and start the first ring. At the expiration of RAT, the ProSLIC will turn off the ringing waveform and will go to the on-hook transmission state. At the expiration of RIT, ringing will again be initiated. This process will continue as long as the two timers are enabled and the Linefeed Control register is set to the ringing state.

Sinusoidal Ringing

To configure the ProSLIC for sinusoidal ringing, the frequency and amplitude are initialized by writing to the following indirect registers: RCO, RNGX, and RNGY. The equations for RCO, RNGX, RNGY are as follows:

$$RCO = \text{coeff} \cdot (2^{15})$$

where

$$\text{coeff} = \cos\left(\frac{2\pi f}{1000 \text{ Hz}}\right)$$

and f = desired ringing frequency in hertz.

$$RNGX = \frac{1}{4} \cdot \frac{\sqrt{1 - \text{coeff}}}{\sqrt{1 + \text{coeff}}} \cdot 2^{15} \cdot \frac{\text{Desired } V_{PK}(0 \text{ to } 94.5 \text{ V})}{96 \text{ V}}$$

$$RNGY = 0$$

In selecting a ringing amplitude, the peak TIP-to-RING ringing voltage must be greater than the selected on-hook line voltage setting (VOC, direct Register 72). For example, to generate a 70 V_{PK} 20 Hz ringing signal, the equations are as follows:

$$\text{coeff} = \cos\left(\frac{2\pi \cdot 20}{1000 \text{ Hz}}\right) = 0.99211$$

$$RCO = 0.99211 \cdot (2^{15}) = 32509 = 7EFDh$$

$$RNGX = \frac{1}{4} \cdot \frac{\sqrt{0.00789}}{1.99211} \cdot 2^{15} \cdot \frac{70}{96} = 376 = 0177h$$

$$RNGY = 0$$

In addition, the user must select the sinusoidal ringing waveform by writing TSWS = 0 (direct Register 34, bit 0).

Trapezoidal Ringing

In addition to the sinusoidal ringing waveform, the ProSLIC supports trapezoidal ringing. Figure 20 illustrates a trapezoidal ringing waveform with offset V_{ROFF} .

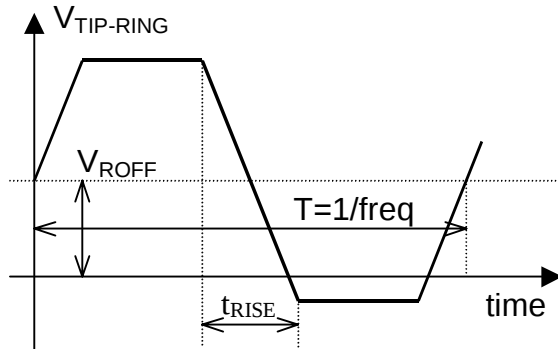


Figure 20. Trapezoidal Ringing Waveform

To configure the ProSLIC for trapezoidal ringing, the user should follow the same basic procedure as in the Sinusoidal Ringing section, but using the following equations:

$$RNGY = \frac{1}{2} \cdot \text{Period} \cdot 8000$$

$$RNGX = \frac{\text{Desired } V_{PK}}{96 \text{ V}} \cdot (2^{15})$$

$$RCO = \frac{2 \cdot RNGX}{t_{RISE} \cdot 8000}$$

RCO is a value which is added or subtracted from the waveform to ramp the signal up or down in a linear fashion. This value is a function of rise time, period, and amplitude, where rise time and period are related through the following equation for the crest factor of a trapezoidal waveform.

$$t_{RISE} = \frac{3}{4} T \left(1 - \frac{1}{CF^2} \right)$$

where T = ringing period, and CF = desired crest factor. For example, to generate a 71 V_{PK} , 20 Hz ringing signal, the equations are as follows:

$$RNGY(20 \text{ Hz}) = \frac{1}{2} \cdot \frac{1}{20 \text{ Hz}} \cdot 8000 = 200 = \text{C8h}$$

$$RNGX(71 \text{ V}_{PK}) = \frac{71}{96} \cdot 2^{15} = 24235 = 5\text{EABh}$$

For a crest factor of 1.3 and a period of 0.05 sec (20 Hz), the rise time requirement is 0.0153 sec.

$$RCO(20 \text{ Hz}, 1.3 \text{ crest factor})$$

$$= \frac{2 \cdot 24235}{0.0153 \cdot 8000} = 396 = 018\text{Ch}$$

In addition, the user must select the trapezoidal ringing waveform by writing TSWS = 1 in direct Register 34.

Ringing DC voltage Offset

A dc offset can be added to the ac ringing waveform by defining the offset voltage in ROFF (indirect Register 19). The offset, V_{ROFF} , is added to the ringing signal when RVO is set to 1 (direct Register 34, bit 1). The value of ROFF is calculated as follows:

$$ROFF = \frac{V_{ROFF}}{96} \cdot 2^{15}$$

Linefeed Considerations During Ringing

Care must be taken to keep the generated ringing signal within the ringing voltage rails (GNDA and V_{BAT}) to maintain proper biasing of the external bipolar transistors. If the ringing signal nears the rails, a distorted ringing signal and excessive power dissipation in the external transistors will result.

To prevent this invalid operation, set the VBATH value (direct Register 74) to a value higher than the maximum peak ringing voltage. The discussion below outlines the considerations and equations that govern the selection of the VBATH setting for a particular desired peak ringing voltage.

First, the required amount of ringing overhead voltage, V_{OVR} , is calculated based on the maximum value of current through the load, $I_{LOAD,PK}$, the minimum current gain of Q5 and Q6, and a reasonable voltage required to keep Q5 and Q6 out of saturation. For ringing signals up to $V_{PK} = 87 \text{ V}$, $V_{OVR} = 7.5 \text{ V}$ is a safe value. However, to determine V_{OVR} for a specific case, use the equations below.

$$I_{LOAD,PK} = \frac{V_{AC,PK}}{R_{LOAD}} + I_{OS} = V_{AC,PK} \cdot \frac{N_{REN}}{6.9 \text{ k}\Omega} + I_{OS}$$

where:

N_{REN} is the ringing REN load (max value = 5),

I_{OS} is the offset current flowing in the line driver circuit (max value = 2 mA), and

$V_{AC,PK}$ = amplitude of the ac ringing waveform.

It is good practice to provide a buffer of a few more milliamperes for $I_{LOAD,PK}$ to account for possible line

leakages, etc. The total $I_{LOAD,PK}$ current should be smaller than 80 mA.

$$V_{OVR} = I_{LOAD,PK} \cdot \frac{\beta + 1}{\beta} \cdot 80.6 \, \Omega + 1 \, V$$

where β is the minimum expected current gain of transistors Q5 and Q6.

The minimum value for VBATH is therefore given by the following:

$$VBATH = V_{AC,PK} + V_{ROFF} + V_{OVR}$$

The ProSLIC is designed to create a fully balanced ringing waveform, meaning that the TIP and RING common mode voltage, $(V_{TIP} + V_{RING})/2$, is fixed. This voltage is referred to as VCM_RING and is automatically set to the following:

$$VCM_RING = \frac{VBATH - VCMR}{2}$$

VCMR is an indirect register which provides the headroom by the ringing waveform with respect to the VBATH rail. The value is set as a 4-bit setting in indirect Register 40 with an LSB voltage of 1.5 V/LSB.

Register 40 should be set with the calculated V_{OVR} to provide voltage headroom during ringing.

Silicon revisions C and higher support the option to briefly increase the maximum differential current limit between the voltage transition of TIP and RING from ringing to a dc linefeed state. This mode is enabled by setting ILIMEN = 1 (direct Register 108, bit 7).

Ring Trip Detection

A ring trip event signals that the terminal equipment has gone off-hook during the ringing state. The ProSLIC performs ring trip detection digitally using its on-chip monitor A/D converter. The functional blocks required to implement ring trip detection is shown in Figure 21. The primary input to the system is the Loop Current Sense value provided by the current monitoring circuitry and reported in direct Register 79. LCS data is processed by the input signal processor when the ProSLIC is in the ringing state as indicated by the Linefeed Shadow register (direct Register 64). The data then feeds into a programmable digital low pass filter, which removes unwanted ac signal components before threshold detection.

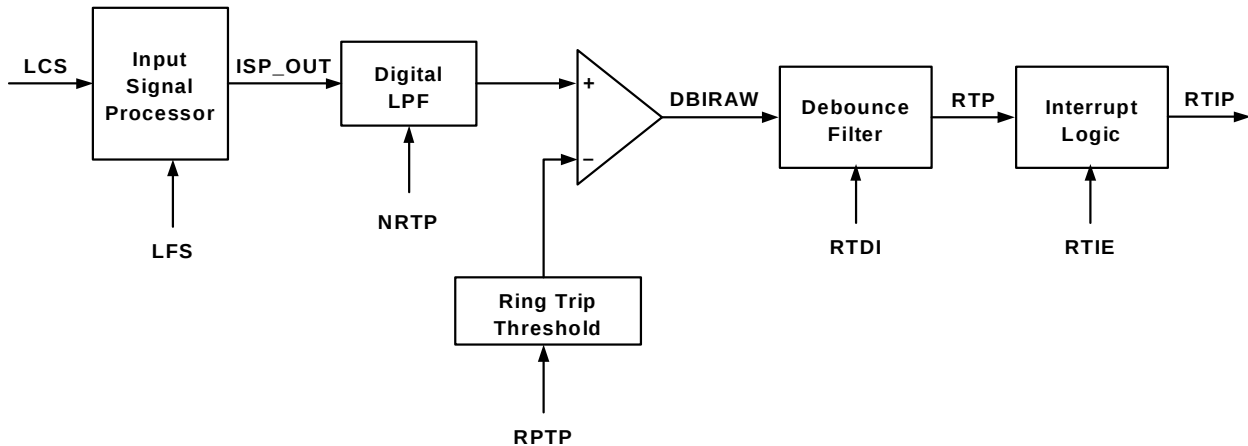


Figure 21. Ring Trip Detector

The output of the low pass filter is compared to a programmable threshold, RPTP (indirect Register 29). The threshold comparator output feeds a programmable debouncing filter. The output of the debouncing filter remains in its present state unless the input remains in the opposite state for the entire period of time programmed by the ring trip debounce interval, RTDI[6:0] (direct Register 70). If the debounce interval has been satisfied, the RTP bit of direct Register 68 will be set to indicate that a valid ring trip has occurred. A ring trip interrupt is generated if enabled by the RTIE bit (direct Register 22). Table 29 lists the registers that must be written or monitored to correctly detect a ring

trip condition.

The recommended values for RPTP, NRTP, and RTDI vary according to the programmed ringing frequency. Register values for various ringing frequencies are given in Table 30.

Table 29. Associated Registers for Ring Trip Detection

Parameter	Register	Location
Ring Trip Interrupt Pending	RTIP	Direct Register 19
Ring Trip Interrupt Enable	RTIE	Direct Register 22
Ring Trip Detect Debounce Interval	RTDI[6:0]	Direct Register 70
Ring Trip Threshold	RPTP[5:0]	Indirect Register 29
Ring Trip Filter Coefficient	NRTP[12:0]	Indirect Register 36
Ring Trip Detect Status (monitor only)	RTP	Direct Register 68
Note: The ProSLIC uses registers that are both directly and indirectly mapped. A “direct” register is one that is mapped directly. An “indirect” register is one that is accessed using the indirect access registers (direct registers 28 through 31).		

Table 30. Recommended Ring Trip Values for Ringing

Ringing Frequency	NRTP		RPTP		RTDI	
	decimal	hex	decimal	hex	decimal	hex
Hz						
16.667	64	0200	34 mA	3600	15.4 ms	0F
20	100	0320	34 mA	3600	12.3 ms	0B
30	112	0380	34 mA	3600	8.96 ms	09
40	128	0400	34 mA	3600	7.5 ms	07
50	213	06A8	34 mA	3600	5 ms	05
60	256	0800	34 mA	3600	4.8 ms	05

Pulse Metering Generation

There is an additional tone generator suitable for generating tones above the audio frequency. This oscillator is provided for the generation of billing tones which are typically 12 kHz or 16 kHz. The generator follows the same algorithm as described in "Tone Generation" on page 30 with the exception that the sample rate for computation is 64 kHz instead of 8 kHz. The equations are as follows:

$$\text{coeff} = \cos\left(\frac{2\pi f}{64000 \text{ Hz}}\right)$$

$$\text{PLSCO} = \text{coeff} \cdot (2^{15} - 1)$$

$$\text{PLSX} = \frac{1}{4} \sqrt{\frac{1 - \text{coeff}}{1 + \text{coeff}}} \cdot (2^{15} - 1) \cdot \frac{\text{Desired } V_{\text{RMS}}}{\text{Full Scale } V_{\text{RMS}}}$$

where full scale $V_{\text{RMS}} = 0.85 V_{\text{RMS}}$ for a matched load.

The initial phase of the pulse metering signal is set to 0 internally so there is no register to serve this purpose.

The pulse metering generator timers and associated pulse metering timer registers are similar to that of the tone generators. These timers count 8 kHz sample periods like the other tones even though the sinusoid is generated at 64 kHz.

Table 31. Associated Pulse Metering Generator Registers

Parameter	Description / Range	Register Bits	Location
Pulse Metering Frequency Coefficient	Sets oscillator frequency	PLSCO[15:0]	Indirect Register 25
Pulse Metering Amplitude Coefficient	Sets oscillator amplitude	PLSX[15:0]	Indirect Register 24
Pulse Metering Attack/Decay Ramp Rate	0 to PLSX (full amplitude)	PLSD[15:0]	Indirect Register 23
Pulse Metering Active Timer	0 to 8 sec	PAT[15:0]	Direct Registers 44 & 45
Pulse Metering Inactive Timer	0 to 8 sec	PIT[15:0]	Direct Register 46 & 47
Pulse Metering Control	Status and control registers	PSTAT, PMAE, PMIE, PMOE	Direct Register 35

Note: The ProSLIC uses registers that are both directly and indirectly mapped. A “direct” register is one that is mapped directly. An “indirect” register is one that is accessed using the indirect access registers (direct registers 28 through 31).

The pulse metering oscillator has a volume envelope (linear ramp) on the on/off transitions of the oscillator. The volume value is incremented by the value in the PLSD register (indirect Register 23) at an 8 kHz rate. The sinusoidal generator output is multiplied by this volume before being sent to the DAC. The volume will ramp from 0 to 7FFF in increments of PLSD so the value of PLSD will set the slope of the ramp. When the pulse metering signal is turned off, the volume will ramp to 0 by decrementing according to the value of PLSD.

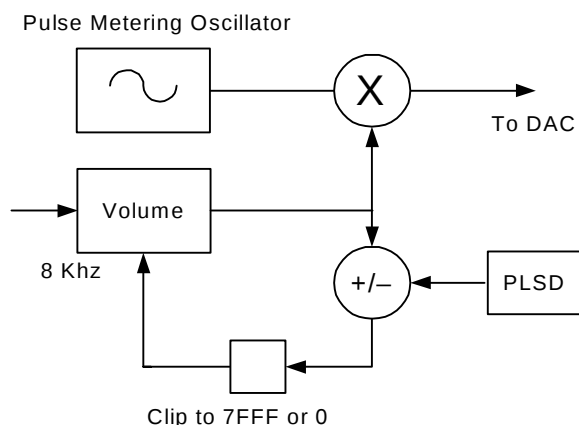


Figure 22. Pulse Metering Volume Envelope

DTMF Detection

The dual-tone multi-frequency (DTMF) tone signaling standard is also known as touch tone. It is an in-band signaling system used to replace the pulse-dial signaling standard. In DTMF, two tones are used to generate a DTMF digit. One tone is chosen from four possible row tones, and one tone is chosen from four possible column tones. The sum of these tones constitutes one of 16 possible DTMF digits.

DTMF Detection Architecture

DTMF detection is performed using a modified Goertzel algorithm to compute the dual frequency tone (DFT) for each of the eight DTMF frequencies as well as their second harmonics. At the end of the DFT computation, the squared magnitudes of the DFT results for the eight DTMF fundamental tones are computed. The row results are sorted to determine the strongest row frequency; the column frequencies are sorted as well. At the completion of this process, a number of checks are made to determine whether the strongest row and column tones constitute a DTMF digit.

The detection process is performed twice within the 45 ms minimum tone time. A digit must be detected on two consecutive tests following a pause to be recognized as a new digit. If all tests pass, an interrupt is generated, and the DTMF digit value is loaded into the DTMF register. If tones are occurring at the maximum rate of 100 ms per digit, the interrupt must be serviced within 85 ms so that the current digit is not

overwritten by a new one. There is no buffering of the digit information.

Audio Path

Unlike traditional SLICs, the codec function is integrated into the ProSLIC. The 16-bit codec offers programmable gain/attenuation blocks and several loop-back modes. The signal path block diagram is shown in Figure 23.

Transmit Path

In the transmit path, the analog signal fed by the external ac coupling capacitors is amplified by the analog transmit amplifier, ATX, prior to the A/D converter. The gain of the ATX is user selectable to one of mute/−3.5/0/3.5 dB options. The main role of ATX is to coarsely adjust the signal swing to be as close as possible to the full-scale input of the A/D converter in order to maximize the signal-to-noise ratio of the transmit path. After passing through an anti-aliasing filter, the analog signal is processed by the A/D converter, producing an 8 kHz, 16-bit wide, linear PCM data stream. The standard requirements for transmit path attenuation for signals above 3.4 kHz are implemented as part of the combined decimation filter characteristic of the A/D converter. One more digital filter is available in the transmit path: THPF. THPF implements the high-pass attenuation requirements for signals below 65 Hz. The linear PCM data stream output from THPF is amplified by the transmit-path programmable gain amplifier, ADCG, which can be programmed from $-\infty$ dB to 6 dB. The DTMF decoder can receive the linear PCM data stream at this point to perform the digit extraction when enabled by the user. The final step in the transmit path signal processing is the user selectable A-law or μ -law compression which can reduce the data stream word width to 8 bits. Depending on the PCM_Mode register selection, every 8-bit compressed serial data word will occupy one time slot on the PCM highway, or every 16-bit uncompressed serial data word will occupy two time slots on the PCM highway.

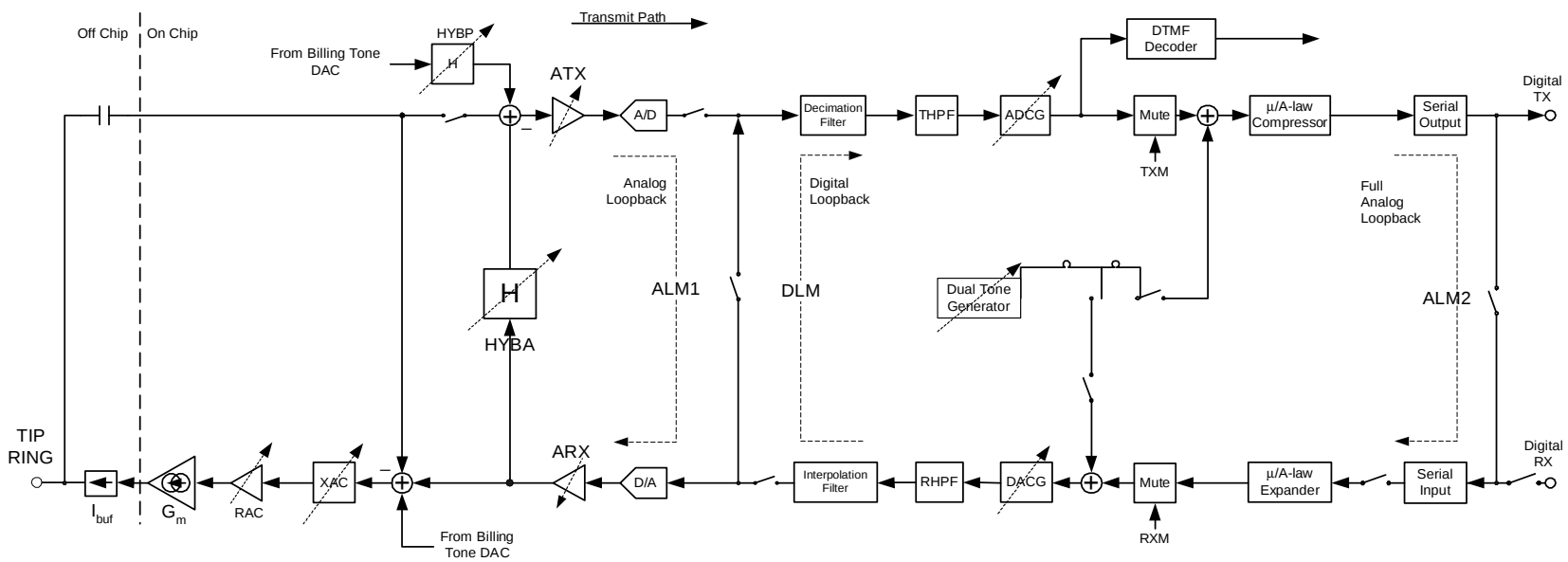


Figure 23. AC Signal Path Block Diagram

Receive Path

In the receive path, the optionally compressed 8-bit data is first expanded to 16-bit words. The PCMF register bit can bypass the expansion process, in which case two 8-bit words are assembled into one 16-bit word. DACG is the receive path programmable gain amplifier which can be programmed from $-\infty$ dB to 6 dB. An 8 kHz, 16-bit signal is then provided to a D/A converter. The resulting analog signal is amplified by the analog receive amplifier, ARX, which is user selectable to one of mute/-3.5/0/3.5 dB options. It is then applied at the input of the transconductance amplifier (Gm) which drives the off-chip current buffer (I_{BUF}).

Audio Characteristics

The dominant source of distortion and noise in both the transmit and receive paths is the quantization noise introduced by the μ -law or the A-law compression process. Figure 1 on page 7 specifies the minimum signal-to-noise-and-distortion ratio for either path for a sine wave input of 200 Hz to 3400 Hz.

Both the μ -law and the A-law speech encoding allow the audio codec to transfer and process audio signals larger than 0 dBm0 without clipping. The maximum PCM code is generated for a μ -law encoded sine wave of 3.17 dBm0 or an A-law encoded sine wave of 3.14 dBm0. The ProSLIC overload clipping limits are driven by the PCM encoding process. Figure 2 on page 7 shows the acceptable limits for the analog-to-analog fundamental power transfer-function, which bounds the behavior of ProSLIC.

The transmit path gain distortion versus frequency is shown in Figure 3 on page 8. The same figure also presents the minimum required attenuation for any out-of-band analog signal that may be applied on the line. Note the presence of a high-pass filter transfer-function, which ensures at least 30 dB of attenuation for signals below 65 Hz. The low-pass filter transfer function which attenuates signals above 3.4 kHz has to exceed the requirements specified by the equations in Figure 3 on page 8 and it is implemented as part of the A-to-D converter.

The receive path transfer function requirement, shown in Figure 4 on page 9, is very similar to the transmit path transfer function. The most notable difference is the absence of the high-pass filter portion. The only other differences are the maximum 2 dB attenuation at 200 Hz (as opposed to 3 dB for the transmit path) and the 28 dB of attenuation for any frequency above 4.6 kHz. The PCM data rate is 8 kHz and thus, no frequencies greater than 4 kHz can be digitally encoded in the data stream. From this point of view, at frequencies greater than 4 kHz, the plot in Figure 4

should be interpreted as the maximum allowable magnitude of any spurious signals that are generated when a PCM data stream representing a sine wave signal in the range of 300 Hz to 3.4 kHz at a level of 0 dBm0 is applied at the digital input.

The group delay distortion in either path is limited to no more than the levels indicated in Figure 5 on page 10. The reference in Figure 5 is the smallest group delay for a sine wave in the range of 500 Hz to 2500 Hz at 0 dBm0.

The block diagram for the voice-band signal processing paths are shown in Figure 23. Both the receive and the transmit paths employ the optimal combination of analog and digital signal processing to provide the maximum performance while, at the same time, offering sufficient flexibility to allow users to optimize for their particular application of the ProSLIC. All programmable signal-processing blocks are symbolically indicated in Figure 23 by a dashed arrow across them. The two-wire (TIP/RING) voice-band interface to the ProSLIC is implemented using a small number of external components. The receive path interface consists of a unity-gain current buffer, I_{BUF} , while the transmit path interface is simply an ac coupling capacitor. Signal paths, although implemented differentially, are shown as single-ended for simplicity.

Transhybrid Balance

The ProSLIC provides programmable transhybrid balance with gain block H. (See Figure 23.) In the ideal case where the synthesized SLIC impedance matches exactly the subscriber loop impedance, the transhybrid balance should be set to subtract a -6 dB level from the transmit path signal. The transhybrid balance gain can be adjusted from -2.77 dB to +4.08 dB around the ideal setting of -6 dB by programming the HYBA[2:0] bits of the Hybrid Control register (direct Register 11). Note that adjusting any of the analog or digital gain blocks will not require any modification of the transhybrid balance gain block, as the transhybrid gain is subtracted from the transmit path signal prior to any gain adjustment stages. The transhybrid balance can also be disabled, if desired, using the appropriate register setting.

Loopback Testing

Four loopback test options are available in the ProSLIC:

- The full analog loopback (ALM2) tests almost all the circuitry of both the transmit and receive paths. The compressed 8-bit word transmit data stream is fed back serially to input of the receive path expander. (See Figure 23.) The signal path starts with the analog signal at the input of the transmit path and ends with an analog signal at the output of the

receive path.

- An additional analog loopback (ALM1) takes the digital stream at the output of the A/D converter and feeds it back to the D/A converter. (See Figure 23.) The signal path starts with the analog signal at the input of the transmit path and ends with an analog signal at the output of the receive path. This loopback option allows the testing of the analog signal processing circuitry of the Si3210 completely independent from any activity in the DSP.
- The full digital loopback tests almost all the circuitry of both the transmit and receive paths. The analog signal at the output of the receive path is fed back to the input of the transmit path by way of the hybrid filter path. (See Figure 23.) The signal path starts with 8-bit PCM data input to the receive path and ends with 8-bit PCM data at the output of the transmit path. The user can bypass the companding process and interface directly to the 16-bit data.
- An additional digital loopback (DLM) takes the digital stream at the input of the D/A converter in the receive path and feeds it back to the transmit A/D digital filter. The signal path starts with 8-bit PCM data input to the receive path and ends with 8-bit PCM data at the output of the transmit path. This loopback option allows the testing of the digital signal processing circuitry of the Si3210 completely independent from any analog signal processing activity. The user can bypass the companding process and interface directly to the 16-bit data.

Two-Wire Impedance Matching

The ProSLIC provides on-chip programmable two-wire impedance settings to meet a wide variety of worldwide two-wire return loss requirements. The two-wire impedance is programmed by loading one of the eight available impedance values into the TISS[2:0] bits of the Two-Wire Impedance Synthesis Control register (direct Register 10). If direct Register 10 is not user-defined, the default setting of 600 Ω will be loaded into the TISS register.

Real and complex two-wire impedances are realized by internal feedback of a programmable amplifier (RAC) a switched capacitor network (XAC) and a transconductance amplifier (G_m). (See Figure 23.) RAC creates the real portion and XAC creates the imaginary portion of G_m 's input. G_m then creates a current that models the desired impedance value to the subscriber loop. The differential ac current is fed to the subscriber loop via the ITIPP and IRINGP pins through an off-chip current buffer (I_{BUF}), which is implemented using transistor Q1 and Q2 (see Figure on page 16). G_m is referenced to an off-chip resistor (R_{15}).

The ProSLIC also provides a means to compensate for degraded subscriber loop conditions involving excessive line capacitance (leakage). The CLC[1:0] bits of direct Register 10 increase the ac signal magnitude to compensate for the additional loss at the high end of the audio frequency range. The default setting of CLC[2:0] assumes no line capacitance.

Silicon revisions C and higher support the option to remove the internal reference resistor used to synthesize ac impedances for 600 + 2.16 μ F and 900 + 2.16 μ F settings so that an external resistor reference may be used. This option is enabled by setting ZSEXT = 1 (direct Register 108, bit 4).

Clock Generation

The ProSLIC will generate the necessary internal clock frequencies from the PCLK input. PCLK must be synchronous to the 8 kHz FSYNC clock and run at one of the following rates: 256 kHz, 512 kHz, 768 kHz, 1.024 MHz, 1.536 MHz, 2.048 MHz, 4.096 MHz or 8.192 MHz. The ratio of the PCLK rate to the FSYNC rate is determined via a counter clocked by PCLK. The three-bit ratio information is automatically transferred into an internal register, PLL_MULT, following a reset of the ProSLIC. The PLL_MULT is used to control the internal PLL which multiplies PCLK as needed to generate 16.384 MHz rate needed to run the internal filters and other circuitry.

The PLL clock synthesizer settles very quickly following power up. However, the settling time depends on the PCLK frequency and it can be approximately predicted by the following equation:

$$T_{SETTLE} = \frac{64}{F_{PCLK}}$$

Interrupt Logic

The ProSLIC is capable of generating interrupts for the following events:

- Loop current/ring ground detected
- Ring trip detected
- Power alarm
- DTMF digit detected (Si3210 and Si3211 only)
- Active timer 1 expired
- Inactive timer 1 expired
- Active timer 2 expired
- Inactive timer 2 expired
- Ringing active timer expired
- Ringing inactive timer expired
- Pulse metering active timer expired
- Pulse metering inactive timer expired

■ Indirect register access complete

The interface to the interrupt logic consists of six registers. Three interrupt status registers contain 1 bit for each of the above interrupt functions. These bits will be set when an interrupt is pending for the associated resource. Three interrupt enable registers also contain 1 bit for each interrupt function. In the case of the interrupt enable registers, the bits are active high. Refer to the appropriate functional description section for operational details of the interrupt functions.

When a resource reaches an interrupt condition, it will signal an interrupt to the interrupt control block. The interrupt control block will then set the associated bit in the interrupt status register if the enable bit for that interrupt is set. The INT pin is a NOR of the bits of the interrupt status registers. Therefore, if a bit in the interrupt status registers is asserted, IRQ will assert low. Upon receiving the interrupt, the interrupt handler should read interrupt status registers to determine which resource is requesting service. To clear a pending interrupt, write the desired bit in the appropriate interrupt status register to 1. Writing a 0 has no effect. This provides a mechanism for clearing individual bits when multiple interrupts occur simultaneously. While the interrupt status registers are non-zero, the INT pin will remain asserted.

Serial Peripheral Interface

The control interface to the ProSLIC is a 4-wire interface modeled after commonly available micro-controller and serial peripheral devices. The interface consists of a clock (SCLK), chip select ($\overline{CS}$), serial data input (SDI), and serial data output (SDO). Data is transferred a byte at a time with each register access consisting of a pair of byte transfers. Figures 24 and 25 illustrate read and write operation in the SPI bus.

The first byte of the pair is the command/address byte. The MSB of this byte indicates register read when 1 and a register write when 0. The remaining seven bits of the command/address byte indicate the address of the register to be accessed. The second byte of the pair is the data byte. During a read operation, the SDO becomes active and the 8-bit contents of the register are driven out MSB first. The SDO will be high impedance on either the falling edge of SCLK following the LSB, or the rising of $\overline{CS}$ whichever comes first. SDI is a “don’t care” during the data portion of read operations. During write operations, data is driven into the ProSLIC via the SDI pin MSB first. The SDO pin will remain high impedance during write operations. Data always transitions with the falling edge of the clock and is latched on the rising edge. The clock should return to a logic high when no transfer is in progress.

Indirect registers are accessed through direct registers 29 through 30. Instructions on how to access them is described in “Control Registers” beginning on page 50.

There are a number of variations of usage on this four-wire interface:

- **Continuous clocking.** During continuous clocking, the data transfers are controlled by the assertion of the $\overline{CS}$ pin. $\overline{CS}$ must assert before the falling edge of SCLK on which the first bit of data is expected during a read cycle, and must remain low for the duration of the 8 bit transfer (command/address or data).
- **SDI/SDO wired operation.** Independent of the clocking options described, SDI and SDO can be treated as two separate lines or wired together if the master is capable of tristating its output during the data byte transfer of a read operation.
- **Daisy chain mode.** This mode allows communication with banks of up to eight ProSLIC devices using one chip select signal. When the SPIDC bit in the SPI Mode Select register is set, data transfer mode changes to a 3-byte operation: a chip select byte, an address/control byte, and a data byte. Using the circuit shown in Figure 26, a single device may select from the bank of devices by setting the appropriate chip select bit to a one. Each device uses the LSB of the chip select byte, shifts the data right by one bit, and passes the chip select byte using the SDITHRU pin to the next device in the chain. Address/control and data bytes are unaltered.

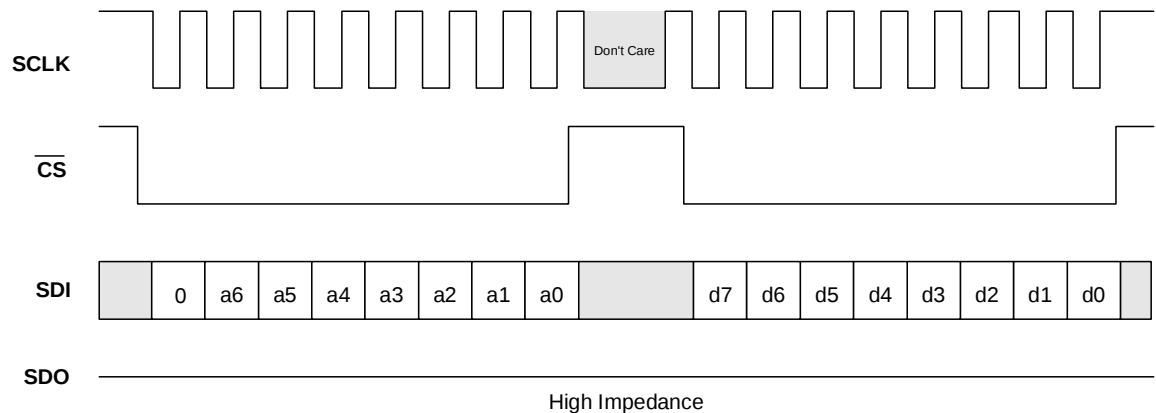


Figure 24. Serial Write 8-Bit Mode

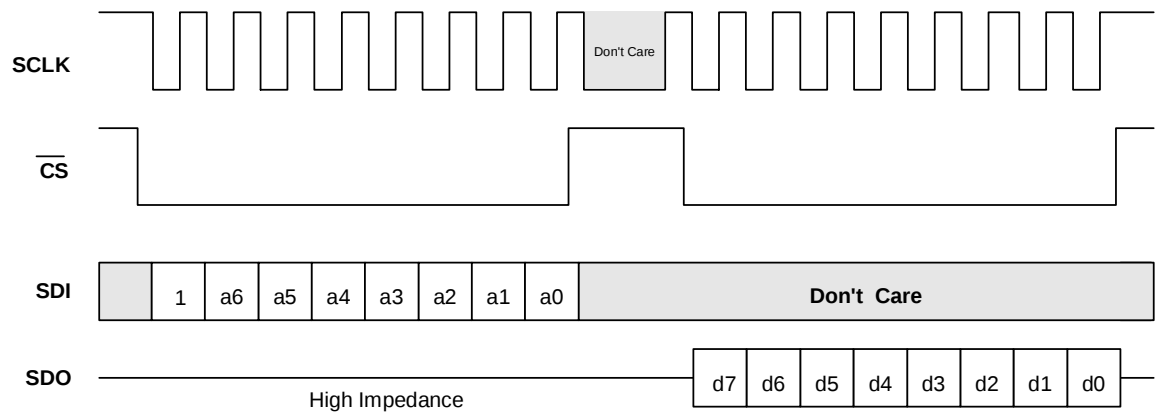
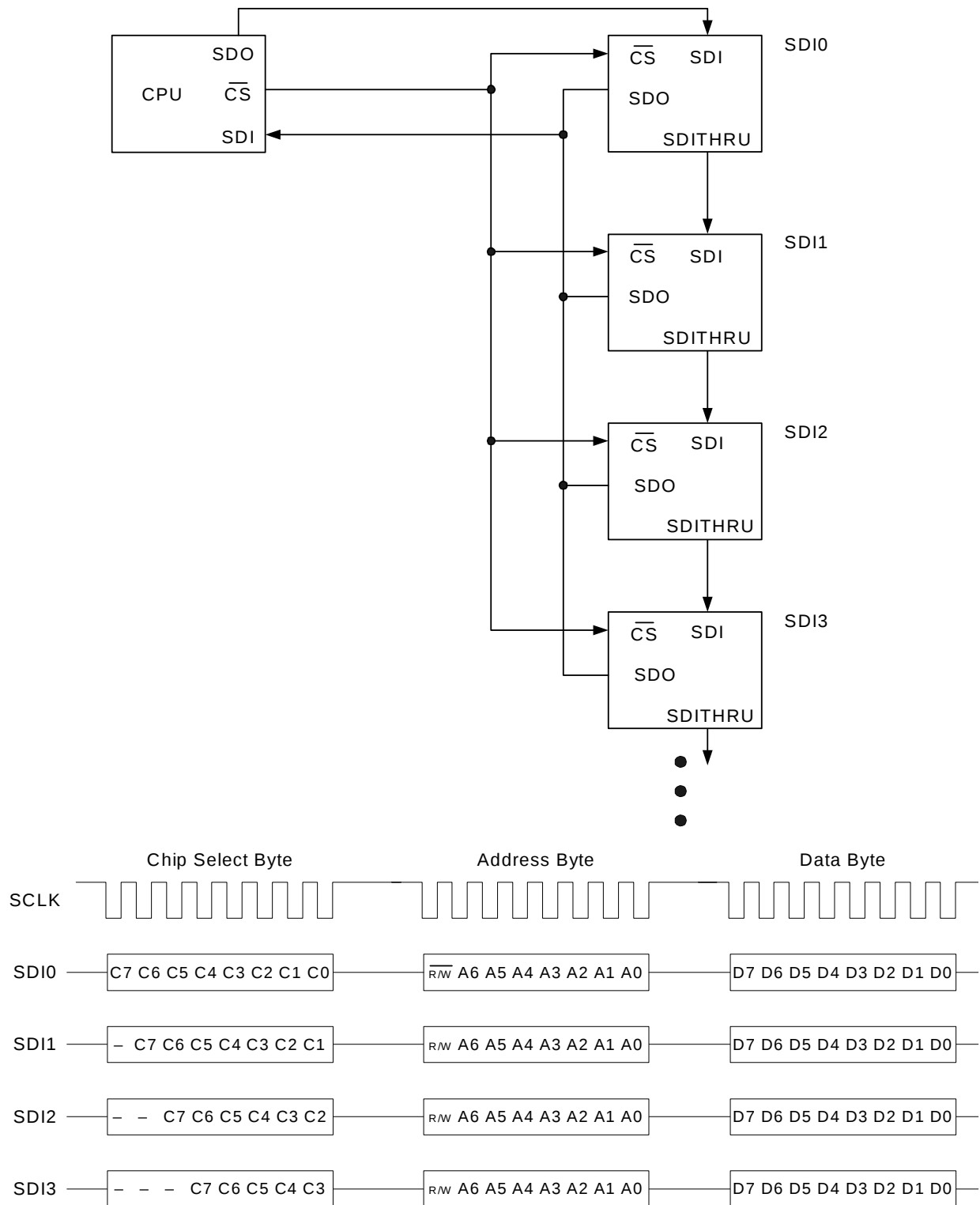


Figure 25. Serial Read 8-Bit Mode



Note: During chip select byte, SDITHRU = SDI delayed by one SCLK. Each device daisy-chained looks at the LSB of the chip select byte for its chip select.

Figure 26. SPI Daisy Chain Mode

PCM Interface

The ProSLIC contains a flexible programmable interface for the transmission and reception of digital PCM samples. PCM data transfer is controlled via the PCLK and FSYNC inputs as well as the PCM Mode Select (direct Register 1), PCM Transmit Start Count (direct registers 2 and 3), and PCM Receive Start Count (direct registers 4 and 5) registers. The interface can be configured to support from 4 to 128 8-bit timeslots in each frame. This corresponds to PCLK frequencies of 256 kHz to 8.192 MHz in power of 2 increments. (768 kHz and 1.536 MHz are also available.) Timeslots for data transmission and reception are independently configured using the TXS and RXS registers. By setting the correct starting point of the data, the ProSLIC can be configured to support long FSYNC and short FSYNC variants as well as IDL2 8-bit, 10-bit, B1 and B2 channel time slots. DTX data is high impedance except for the duration of the 8-bit PCM transmit. DTX will return to

high impedance either on the negative edge of PCLK during the LSB, or on the positive edge of PCLK following the LSB. This is based on the setting of the TRI bit of the PCM Mode Select register. Tristating on the negative edge allows the transmission of data by multiple sources in adjacent timeslots without the risk of driver contention. In addition to 8-bit data modes, there is a 16-bit mode provided. This mode can be activated via the PCMT bit of the PCM Mode Select register. GCI timing is also supported in which the duration of a data bit is two PCLK cycles. This mode is also activated via the PCM Mode Select register. Setting the TXS or RXS register greater than the number of PCLK cycles in a sample period will stop data transmission because TXS or RXS will never equal the PCLK count. Figures 27–30 illustrate the usage of the PCM highway interface to adapt to common PCM standards.

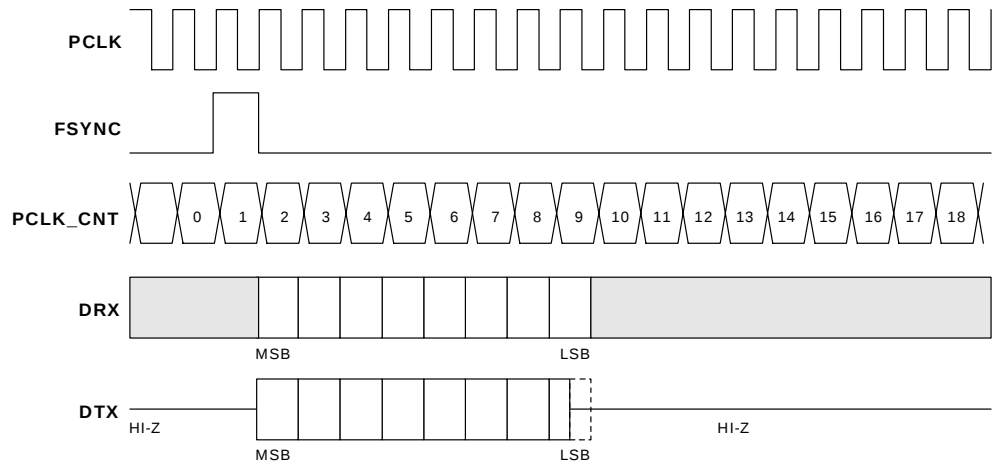


Figure 27. Example, Timeslot 1, Short FSYNC (TXS/RXS = 1)

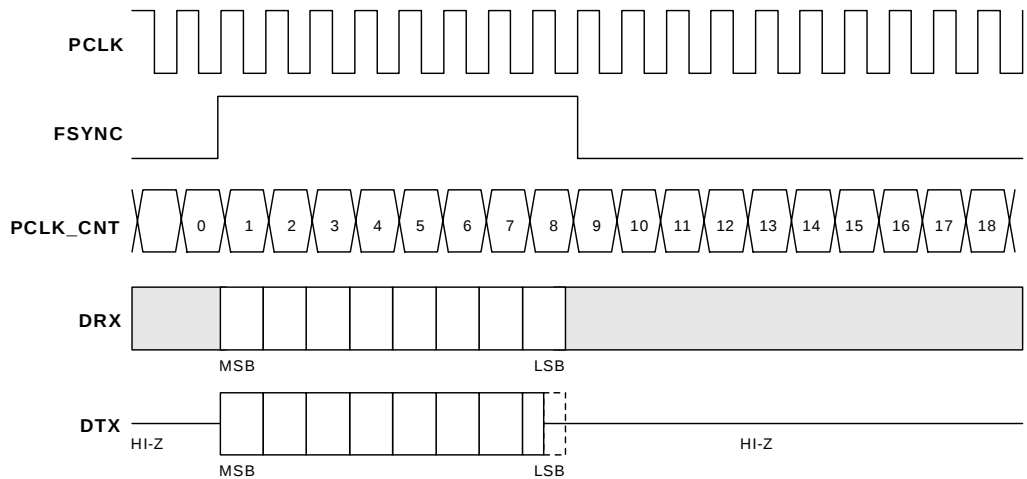


Figure 28. Example, Timeslot 1, Long FSYNC (TXS/RXS = 0)

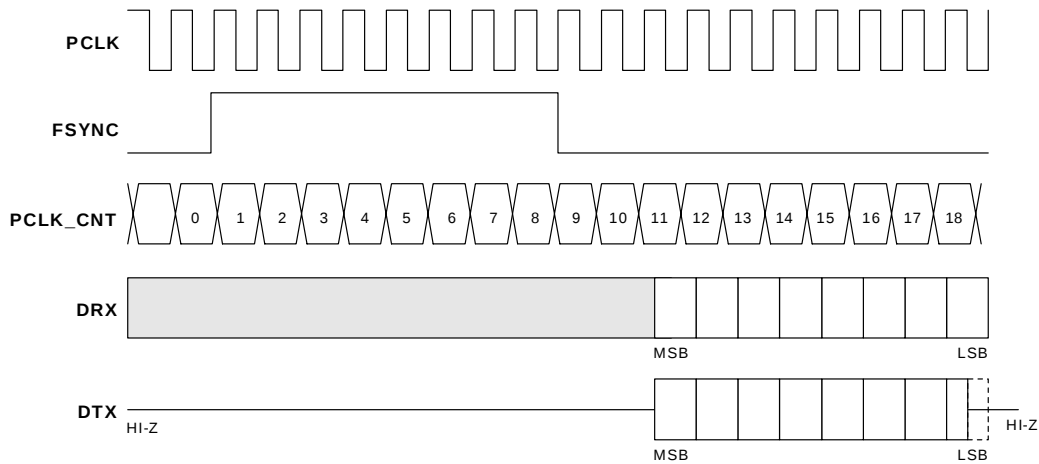


Figure 29. Example, IDL2 Long FSYNC, B2, 10-Bit Mode (TXS/RXS = 10)

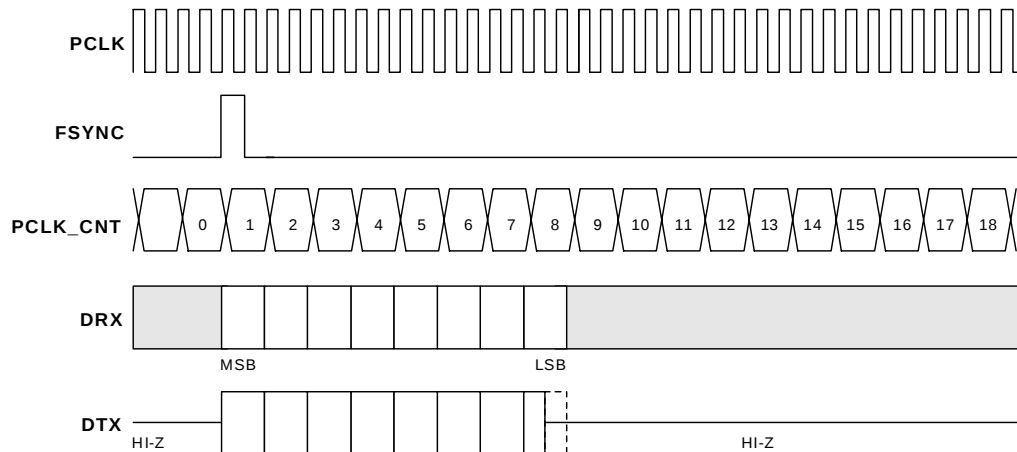


Figure 30. GCI Example, Timeslot 1 (TXS/RXS = 0)

Companding

The ProSLIC supports both μ -255 Law and A-Law companding formats in addition to linear data. These 8-bit companding schemes follow a segmented curve formatted as sign bit, three chord bits, and four step bits. μ -255 Law is more commonly used in North America and Japan, while A-Law is primarily used in Europe. Data format is selected via the PCMF register. Tables 32 and 33 define the μ -Law and A-Law encoding formats.

Table 32. μ -Law Encode-Decode Characteristics^{1,2}

Segment Number	#Intervals X Interval Size	Value at Segment Endpoints	Digital Code	Decode Level
8	16 X 256	8159 . . . 4319 4063	10000000b 10001111b	8031 4191
7	16 X 128	. . . 2143 2015	 10011111b	 2079
6	16 X 64	. . . 1055 991	 10101111b	 1023
5	16 X 32	. . . 511 479	 10111111b	 495
4	16 X 16	. . . 239 223	 11001111b	 231
3	16 X 8	. . . 103 95	 11011111b	 99
2	16 X 4	. . . 35 31	 11101111b	 33
1	15 X 2	. . . 3 1	 11111110b	 2
	1 X 1	0	11111111b	0

Notes:

1. Characteristics are symmetrical about analog zero with sign bit = 0 for negative analog values.
2. Digital code includes inversion of all magnitude bits.

Table 33. A-Law Encode-Decode Characteristics^{1,2}

Segment Number	#intervals X interval size	Value at segment endpoints	Digital Code	Decode Level
7	16 X 128	4096 3968 . . 2176 2048	10101010b 10100101b	4032 2112
6	16 X 64	. . . 1088 1024	 10110101b	 1056
5	16 X 32	. . . 544 512	 10000101b	 528
4	16 X 16	. . . 272 256	 10010101b	 264
3	16 X 8	. . . 136 128	 11100101b	 132
2	16 X 4	. . . 68 64	 11110101b	 66
1	32 X 2	. . . 2 0	 11010101b	 1

Notes:

1. Characteristics are symmetrical about analog zero with sign bit = 0 for negative values.
2. Digital code includes inversion of all even numbered bits.

Si3210/Si3211/Si3212

Control Registers

Note: Any register not listed here is reserved and must not be written.

Table 34. Direct Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Setup									
0	SPI Mode Select	SPIDC	SPIM	PNI[1:0]		RNI[3:0]			
1	PCM Mode Select			PCME	PCMF[1:0]		PCMT	GCI	TRI
2	PCM Transmit Start Count—Low Byte	TXS[7:0]							
3	PCM Transmit Start Count—High Byte							TXS[9:8]	
4	PCM Receive Start Count—Low Byte	RXS[7:0]							
5	PCM Receive Start Count—High Byte							RXS[9:8]	
6	Digital Input/Output Control				DOUT ¹	DIO2 ¹	DIO1 ¹	PD2 ¹	PD1 ¹
Audio									
8	Audio Path Loopback Control						ALM2	DLM	ALM1
9	Audio Gain Control	RXHP	TXHP	TXM	RXM	ATX[1:0]		ARX[1:0]	
10	Two-Wire Impedance Synthesis Control			CLC[1:0]		TISE	TISS[2:0]		
11	Hybrid Control		HYBP[2:0]				HYBA[2:0]		
Powerdown									
14	Power Down Control 1			PMON	DCOF ²	MOF		BIASOF	SLICOF
15	Power Down Control 2			ADCM	ADCON	DACM	DACON	GMM	GMON
Interrupts									
18	Interrupt Status 1	PMIP	PMAP	RGIP	RGAP	O2IP	O2AP	O1IP	O1AP
19	Interrupt Status 2	Q6AP	Q5AP	Q4AP	Q3AP	Q2AP	Q1AP	LCIP	RTIP
20	Interrupt Status 3						CMCP	INDP	DTMFP ³
21	Interrupt Enable 1	PMIE	PMAE	RGIE	RGAE	O2IE	O2AE	O1IE	O1AE
22	Interrupt Enable 2	Q6AE	Q5AE	Q4AE	Q3AE	Q2AE	Q1AE	LCIE	RTIE
23	Interrupt Enable 3						CMCE	INDE	DTMFE ³
24	Decode Status				VAL ³	DIG[3:0] ³			
Indirect Register Access									
Notes: 1. Si3211 and Si3212 only. 2. Si3210 only. 3. Si3210 and Si3211 only.									

Table 34. Direct Register Summary (Continued)

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
28	Indirect Data Access—Low Byte	IDA[7:0]							
29	Indirect Data Access—High Byte	IDA[15:8]							
30	Indirect Address	IAA[7:0]							
31	Indirect Address Status								IAS
Oscillators									
32	Oscillator 1 Control	OSS1	REL	OZ1	O1TAE	O1TIE	O1E	O1SO[1:0]	
33	Oscillator 2 Control	OSS2		OZ2	O2TAE	O2TIE	O2E	O2SO[1:0]	
34	Ringing Oscillator Control	RSS		RDAC	RTAE	RTIE	ROE	RVO	TSWS
35	Pulse Metering Oscillator Control	PSTAT			PMAE	PMIE	PMOE		
36	Oscillator 1 Active Timer—Low Byte	OAT1[7:0]							
37	Oscillator 1 Active Timer—High Byte	OAT1[15:8]							
38	Oscillator 1 Inactive Timer—Low Byte	OIT1[7:0]							
39	Oscillator 1 Inactive Timer—High Byte	OIT1[15:8]							
40	Oscillator 2 Active Timer—Low Byte	OAT2[7:0]							
41	Oscillator 2 Active Timer—High Byte	OAT2[15:8]							
42	Oscillator 2 Inactive Timer—Low Byte	OIT2[7:0]							
43	Oscillator 2 Inactive Timer—High Byte	OIT2[15:8]							
44	Pulse Metering Oscillator Active Timer—Low Byte	PAT[7:0]							
45	Pulse Metering Oscillator Active Timer—High Byte	PAT[15:8]							
46	Pulse Metering Oscillator Inactive Timer—Low Byte	PIT[7:0]							

Notes:

1. Si3211 and Si3212 only.
2. Si3210 only.
3. Si3210 and Si3211 only.

Table 34. Direct Register Summary (Continued)

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
47	Pulse Metering Oscillator Inactive Timer—High Byte	PIT[15:8]							
48	Ringing Oscillator Active Timer—Low Byte	RAT[7:0]							
49	Ringing Oscillator Active Timer—High Byte	RAT[15:8]							
50	Ringing Oscillator Inactive Timer—Low Byte	RIT[7:0]							
51	Ringing Oscillator Inactive Timer—High Byte	RIT[15:8]							
52	FSK Data								FSKDAT
SLIC									
63	Loop Closure Debounce Interval for Automatic Ringing	LCD[7:0]							
64	Linefeed Control		LFS[2:0]				LF[2:0]		
65	External Bipolar Transistor Control		SQH	CBY	ETBE	ETBO[1:0]		ETBA[1:0]	
66	Battery Feed Control				VOV ²	FVBAT ²		BATSL ¹	TRACK ²
67	Automatic/Manual Control		MNCM	MNDIF	SPDS	ABAT	AORD	AOLD	AOPN
68	Loop Closure/Ring Trip Detect Status						DBIRAW	RTP	LCR
69	Loop Closure Debounce Interval		LCDI[6:0]						
70	Ring Trip Detect Debounce Interval		RTDI[6:0]						
71	Loop Current Limit						ILIM[2:0]		
72	On-Hook Line Voltage		VSGN	VOC[5:0]					
73	Common Mode Voltage			VCM[5:0]					
74	High Battery Voltage			VBATH[5:0]					
75	Low Battery Voltage			VBATL[5:0]					
76	Power Monitor Pointer						PWRMP[2:0]		
77	Line Power Output Monitor	PWROM[7:0]							
78	Loop Voltage Sense		LVSP	LVS[5:0]					

Notes:

1. Si3211 and Si3212 only.
2. Si3210 only.
3. Si3210 and Si3211 only.

Table 34. Direct Register Summary (Continued)

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
79	Loop Current Sense		LCSP	LCS[5:0]					
80	TIP Voltage Sense	VTIP[7:0]							
81	RING Voltage Sense	VRING[7:0]							
82	Battery Voltage Sense 1	VBATS1[7:0]							
83	Battery Voltage Sense 2	VBATS2[7:0]							
84	Transistor 1 Current Sense	IQ1[7:0]							
85	Transistor 2 Current Sense	IQ2[7:0]							
86	Transistor 3 Current Sense	IQ3[7:0]							
87	Transistor 4 Current Sense	IQ4[7:0]							
88	Transistor 5 Current Sense	IQ5[7:0]							
89	Transistor 6 Current Sense	IQ6[7:0]							
92	DC-DC Converter PWM Period	DCN[7:0] ³							
93	DC-DC Converter Switching Delay	DCCAL ²		DCPOL ²	DCTOF[4:0] ²				
94	PWM Pulse Width	DCPW[7:0] ²							
95	Reserved								
96	Calibration Control/ Status Register 1		CAL	CALSP	CALR	CALT	CALD	CALC	CALIL
97	Calibration Control/ Status Register 2				CALM1	CALM2	CALDAC	CALADC	CALCM
98	RING Gain Mismatch Calibration Result				CALGMR[R4:0]				
99	TIP Gain Mismatch Calibration Result				CALGMT[4:0]				
100	Differential Loop Current Gain Calibration Result				CALGD[4:0]				
101	Common Mode Loop Current Gain Calibration Result				CALGC[4:0]				

Notes:

1. Si3211 and Si3212 only.
2. Si3210 only.
3. Si3210 and Si3211 only.

Table 34. Direct Register Summary (Continued)

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
102	Current Limit Calibration Result					CALGIL[3:0]			
103	Monitor ADC Offset Calibration Result	CALMG1[3:0]				CALMG2[3:0]			
104	Analog DAC/ADC Offset					DACP	DACN	ADCP	ADCN
105	DAC Offset Calibration Result	DACOF[7:0]							
106	Common Mode Balance Calibration Result			CMBAL[5:0]					
107	DC Peak Voltage Calibration Result					CMDCPK[3:0]			
108	Enhancement Enable	ILIMEN	FSKEN	DCEN ²	ZSEXT	SWDB	LCVE	DCFIL ²	HYSTEN

Notes:

1. Si3211 and Si3212 only.
2. Si3210 only.
3. Si3210 and Si3211 only.

Register 0. SPI Mode Select

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SPIDC	SPIM	PNI[1:0]		RNI[3:0]			
Type	R/W	R/W	R		R			

Reset settings = 00xx_xxxx

Bit	Name	Function
7	SPIDC	SPI Daisy Chain Mode Enable. 0 = Disable SPI daisy chain mode. 1 = Enable SPI daisy chain mode.
6	SPIM	SPI Mode. 0 = Causes SDO to tri-state on rising edge of SCLK of $\overline{\text{LSB}}$. 1 = Normal operation; SDO tri-states on rising edge of $\overline{\text{CS}}$.
5:4	PNI[1:0]	Part Number Identification. 00 = Si3210 01 = Si3211 10 = Si3212 11 = Si3210M
3:0	RNI[3:0]	Revision Number Identification. 0001 = Revision A, 0010 = Revision B, 0011 = Revision C, etc.

Si3210/Si3211/Si3212

Register 1. PCM Mode Select

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			PCME	PCMF[1:0]		PCMT	GCI	TRI
Type	R/W		R/W		R/W		R/W	R/W

Reset settings = 0000_1000

Bit	Name	Function
7:6	Reserved	Read returns zero.
5	PCME	PCM Enable. 0 = Disable PCM transfers. 1 = Enable PCM transfers.
4:3	PCMF[1:0]	PCM Format. 00 = A-Law 01 = μ -Law 10 = Reserved 11 = Linear
2	PCMT	PCM Transfer Size. 0 = 8-bit transfer. 1 = 16-bit transfer.
1	GCI	GCI Clock Format. 0 = 1 PCLK per data bit. 1 = 2 PCLKs per data bit.
0	TRI	Tri-state Bit 0. 0 = Tri-state bit 0 on positive edge of PCLK. 1 = Tri-state bit 0 on negative edge of PCLK.

Register 2. PCM Transmit Start Count—Low Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TXS[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	TXS[7:0]	PCM Transmit Start Count. PCM transmit start count equals the number of PCLKs following FSYNC before data transmission begins. See Figure 27 on page 46.

Register 3. PCM Transmit Start Count—High Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							TXS[9:8]	
Type		R/W						

Reset settings = 0000_0000

Bit	Name	Function
7:2	Reserved	Read returns zero.
1:0	TXS[9:8]	PCM Transmit Start Count. PCM transmit start count equals the number of PCLKs following FSYNC before data transmission begins. See Figure 27 on page 46.

Register 4. PCM Receive Start Count—Low Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RXS[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	RXS[7:0]	PCM Receive Start Count. PCM receive start count equals the number of PCLKs following FSYNC before data reception begins. See Figure 27 on page 46.

Register 5. PCM Receive Start Count—High Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							RXS[9:8]	
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:2	Reserved	Read returns zero.
1:0	RXS[9:8]	PCM Receive Start Count. PCM receive start count equals the number of PCLKs following FSYNC before data reception begins. See Figure 27 on page 46.

Si3210/Si3211/Si3212

Register 6. Digital Input/Output Control

Si3210								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = 0000_0000

Si3211/Si3212								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				DOUT	DIO2	DIO1	PD2	PD1
Type			R/W		R/W	R/W	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7:5	Reserved	Read returns zero.
4	DOUT	DOUT Pin Output Data (Si3211/Si3212 only). 0 = DOUT pin driven low. 1 = DOUT pin driven high. Si3210 = Reserved.
3	DIO2	DIO2 Pin Input/Output Direction. 0 = DIO2 pin is an input. 1 = DIO2 pin is an output and driven to value of the PD2 bit. Si3210 = Reserved.
2	DIO1	DIO1 Pin Input/Output Direction. 0 = DIO1 pin is an input. 1 = DIO1 pin is an output and driven to value of the PD1 bit. Si3210 = Reserved.
1	PD2	DIO2 Pin Data. When DIO2 = 1: 0 = DIO2 pin driven low. 1 = DIO2 pin driven high. Si3210 = Reserved. When DIO2 = 0, PD2 value equals the logic input of DIO2 pin.
0	PD1	DIO1 Pin Data. When DIO1 = 1: 0 = DIO1 pin driven low. 1 = DIO1 pin driven high. Si3210 = Reserved. When DIO1 = 0, PD1 value equals the logic input of DIO1 pin.

Register 8. Audio Path Loopback Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						ALM2	DLM	ALM1
Type						R/W	R/W	R/W

Reset settings = 0000_0010

Bit	Name	Function
7:3	Reserved	Read returns zero.
2	ALM2	Analog Loopback Mode 2. (See Figure 23 on page 40.) 0 = Full analog loopback mode disabled. 1 = Full analog loopback mode enabled.
1	DLM	Digital Loopback Mode. (See Figure 23 on page 40.) 0 = Digital loopback disabled. 1 = Digital loopback enabled.
0	ALM1	Analog Loopback Mode 1. (See Figure 23 on page 40.) 0 = Analog loopback disabled. 1 = Analog loopback enabled.

Si3210/Si3211/Si3212

Register 9. Audio Gain Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RXHP	TXHP	TXM	RXM	ATX[1:0]		ARX[1:0]	
Type	R/W	R/W	R/W	R/W	R/W		R/W	

Reset settings = 0000_0000

Bit	Name	Function
7	RXHP	Receive Path High Pass Filter Disable. 0 = HPF enabled in receive path, RHDF. 1 = HPF bypassed in receive path, RHDF.
6	TXHP	Transmit Path High Pass Filter Disable. 0 = HPF enabled in transmit path, THPF. 1 = HPF bypassed in transmit path, THPF.
5	TXM	Transmit Path Mute. Refer to position of digital mute in Figure 23 on page 40. 0 = Transmit signal passed. 1 = Transmit signal muted.
4	RXM	Receive Path Mute. Refer to position of digital mute in Figure 23 on page 40. 0 = Receive signal passed. 1 = Receive signal muted.
3:2	ATX[1:0]	Analog Transmit Path Gain. 00 = 0 dB 01 = -3.5 dB 10 = 3.5 dB 11 = ATX gain = 0 dB; analog transmit path muted.
1:0	ARX[1:0]	Analog Receive Path Gain. 00 = 0 dB 01 = -3.5 dB 10 = 3.5 dB 11 = Analog receive path muted.

Register 10. Two-Wire Impedance Synthesis Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			CLC[1:0]		TISE	TISS[2:0]		
Type	R/W				R/W	R/W		

Reset settings = 0000_1000

Bit	Name	Function
7:6	Reserved	Read returns zero.
5:4	CLC[1:0]	Line Capacitance Compensation. 00 = Off 01 = 4.7 nF 10 = 10 nF 11 = Reserved
3	TISE	Two-Wire Impedance Synthesis Enable. 0 = Two-wire impedance synthesis disabled. 1 = Two-wire impedance synthesis enabled.
2:0	TISS[2:0]	Two-Wire Impedance Synthesis Selection. 000 = 600 Ω 001 = 900 Ω 010 = 600 Ω + 2.16 μ F 011 = 900 Ω + 2.16 μ F 100 = CTR21 (270 Ω + 750 Ω 150 nF) 101 = Australia/New Zealand #1 (220 Ω + 820 Ω 120 nF) 110 = Slovakia/Slovenia/South Africa (220 Ω + 820 Ω 115 nF) 111 = New Zealand #2 (370 Ω + 620 Ω 310 nF)

Si3210/Si3211/Si3212

Register 11. Hybrid Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		HYBP[2:0]				HYBA[2:0]		
Type	R/W				R/W			

Reset settings = 0011_0011

Bit	Name	Function
7	Reserved	Read returns zero.
6:4	HYBP[2:0]	Pulse Metering Hybrid Adjustment. 000 = 4.08 dB 001 = 2.5 dB 010 = 1.16 dB 011 = 0 dB 100 = -1.02 dB 101 = -1.94 dB 110 = -2.77 dB 111 = Off
3	Reserved	Read returns zero.
2:0	HYBA[2:0]	Audio Hybrid Adjustment. 000 = 4.08 dB 001 = 2.5 dB 010 = 1.16 dB 011 = 0 dB 100 = -1.02 dB 101 = -1.94 dB 110 = -2.77 dB 111 = Off

Register 14. Power Down Control 1

Si3210								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			PMON	DCOF	MOF		BIASOF	SLICOF
Type	R/W		R/W	R/W			R/W	R/W

Reset settings = 0001_0000

Si3211/Si3212								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			PMON		MOF		BIASOF	SLICOF
Type	R/W				R/W		R/W	R/W

Reset settings = 0001_0000

Bit	Name	Function
7:6	Reserved	Read returns zero.
5	PMON	Pulse Metering DAC Power-On Control. 0 = Automatic power control. 1 = Override automatic control and force pulse metering DAC circuitry on.
4	DCOF	DC-DC Converter Power-Off Control (Si3210 only). 0 = Automatic power control. 1 = Override automatic control and force dc-dc circuitry off. Si3211/Si3212 = Read returns 1; it cannot be written.
3	MOF	Monitor ADC Power-Off Control. 0 = Automatic power control. 1 = Override automatic control and force monitor ADC circuitry off.
2	Reserved	Read returns zero.
1	BIASOF	DC Bias Power-Off Control. 0 = Automatic power control. 1 = Override automatic control and force dc bias circuitry off.
0	SLICOF	SLIC Power-Off Control. 0 = Automatic power control. 1 = Override automatic control and force SLIC circuitry off.

Register 15. Power Down Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			ADCM	ADCON	DACM	DACON	GMM	GMON
Type	R/W		R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7:6	Reserved	Read returns zero.
5	ADCM	Analog to Digital Converter Manual/Automatic Power Control. 0 = Automatic power control. 1 = Manual power control; ADCON controls on/off state.
4	ADCON	Analog to Digital Converter On/Off Power Control. When ADCM = 1: 0 = Analog to digital converter powered off. 1 = Analog to digital converter powered on. ADCON has no effect when ADCM = 0.
3	DACM	Digital to Analog Converter Manual/Automatic Power Control. 0 = Automatic power control. 1 = Manual power control; DACON controls on/off state.
2	DACON	Digital to Analog Converter On/Off Power Control. When DACM = 1: 0 = Digital to analog converter powered off. 1 = Digital to analog converter powered on. DACON has no effect when DACM = 0.
1	GMM	Transconductance Amplifier Manual/Automatic Power Control. 0 = Automatic power control. 1 = Manual power control; GMON controls on/off state.
0	GMON	Transconductance Amplifier On/Off Power Control. When GMM = 1: 0 = Analog to digital converter powered off. 1 = Analog to digital converter powered on. GMON has no effect when GMM = 0.

Register 18. Interrupt Status 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PMIP	PMAP	RGIP	RGAP	O2IP	O2AP	O1IP	O1AP
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7	PMIP	Pulse Metering Inactive Timer Interrupt Pending. Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.
6	PMAP	Pulse Metering Active Timer Interrupt Pending. Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.
5	RGIP	Ringing Inactive Timer Interrupt Pending. Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.
4	RGAP	Ringing Active Timer Interrupt Pending. Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.
3	O2IP	Oscillator 2 Inactive Timer Interrupt Pending. Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.
2	O2AP	Oscillator 2 Active Timer Interrupt Pending. Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.
1	O1IP	Oscillator 1 Inactive Timer Interrupt Pending. Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.
0	O1AP	Oscillator 1 Active Timer Interrupt Pending. Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.

Register 19. Interrupt Status 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Q6AP	Q5AP	Q4AP	Q3AP	Q2AP	Q1AP	LCIP	RTIP
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7	Q6AP	Power Alarm Q6 Interrupt Pending. Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.
6	Q5AP	Power Alarm Q5 Interrupt Pending. Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.
5	Q4AP	Power Alarm Q4 Interrupt Pending. Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.
4	Q3AP	Power Alarm Q3 Interrupt Pending. Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.
3	Q2AP	Power Alarm Q2 Interrupt Pending. Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.
2	Q1AP	Power Alarm Q1 Interrupt Pending. Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.
1	LCIP	Loop Closure Transition Interrupt Pending. Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.
0	RTIP	Ring Trip Interrupt Pending. Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.

Register 20. Interrupt Status 3

Si3210/Si3211								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						CMCP	INDP	DTMFP
Type				R/W			R/W	R/W

Reset settings = 0000_0000

Si3212								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						CMCP	INDP	
Type				R/W			R/W	

Reset settings = 0000_0000

Bit	Name	Function
7:3	Reserved	Read returns zero.
2	CMCP	Common Mode Calibration Error Interrupt. This bit is set when off-hook/on-hook status changes during the common mode balance calibration. Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.
1	INDP	Indirect Register Access Serviced Interrupt. This bit is set once a pending indirect register service request has been completed. Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending.
0	DTMFP	DTMF Tone Detected Interrupt (Si3210 and Si3211 only). Writing 1 to this bit clears a pending interrupt. 0 = No interrupt pending. 1 = Interrupt pending. Si3212 = Reserved; read returns 0.

Register 21. Interrupt Enable 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PMIE	PMAE	RGIE	RGAE	O2IE	O2AE	O1IE	O1AE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7	PMIE	Pulse Metering Inactive Timer Interrupt Enable. 0 = Interrupt masked. 1 = Interrupt enabled.
6	PMAE	Pulse Metering Active Timer Interrupt Enable. 0 = Interrupt masked. 1 = Interrupt enabled.
5	RGIE	Ringing Inactive Timer Interrupt Enable. 0 = Interrupt masked. 1 = Interrupt enabled.
4	RGAE	Ringing Active Timer Interrupt Enable. 0 = Interrupt masked. 1 = Interrupt enabled.
3	O2IE	Oscillator 2 Inactive Timer Interrupt Enable. 0 = Interrupt masked. 1 = Interrupt enabled.
2	O2AE	Oscillator 2 Active Timer Interrupt Enable. 0 = Interrupt masked. 1 = Interrupt enabled.
1	O1IE	Oscillator 1 Inactive Timer Interrupt Enable. 0 = Interrupt masked. 1 = Interrupt enabled.
0	O1AE	Oscillator 1 Active Timer Interrupt Enable. 0 = Interrupt masked. 1 = Interrupt enabled.

Register 22. Interrupt Enable 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Q6AE	Q5AE	Q4AE	Q3AE	Q2AE	Q1AE	LCIE	RTIE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7	Q6AE	Power Alarm Q6 Interrupt Enable. 0 = Interrupt masked. 1 = Interrupt enabled.
6	Q5AE	Power Alarm Q5 Interrupt Enable. 0 = Interrupt masked. 1 = Interrupt enabled.
5	Q4AE	Power Alarm Q4 Interrupt Enable. 0 = Interrupt masked. 1 = Interrupt enabled.
4	Q3AE	Power Alarm Q3 Interrupt Enable. 0 = Interrupt masked. 1 = Interrupt enabled.
3	Q2AE	Power Alarm Q2 Interrupt Enable. 0 = Interrupt masked. 1 = Interrupt enabled.
2	Q1AE	Power Alarm Q1 Interrupt Enable. 0 = Interrupt masked. 1 = Interrupt enabled.
1	LCIE	Loop Closure Transition Interrupt Enable. 0 = Interrupt masked. 1 = Interrupt enabled.
0	RTIE	Ring Trip Interrupt Enable. 0 = Interrupt masked. 1 = Interrupt enabled.

Si3210/Si3211/Si3212

Register 23. Interrupt Enable 3

Si3210/Si3211								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						CMCE	INDE	DTMFE
Type				R/W			R/W	R/W

Reset settings = 0000_0000

Si3212								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						CMCE	INDE	
Type				R/W			R/W	

Reset settings = 0000_0000

Bit	Name	Function
7:3	Reserved	Read returns zero.
2	CMCE	Common Mode Calibration Error Interrupt Enable. 0 = Interrupt masked. 1 = Interrupt enabled.
1	INDE	Indirect Register Access Serviced Interrupt Enable. 0 = Interrupt masked. 1 = Interrupt enabled.
0	DTMFE	DTMF Tone Detected Interrupt Enable (Si3210 and Si3211 only). 0 = Interrupt masked. 1 = Interrupt enabled. Si3212 = Reserved.

Register 24. DTMF Decode Status

Si3210/Si3211								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				VAL	DIG[3:0]			
Type	R					R		

Reset settings = 0000_0000

Si3212								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = 0000_0000

Bit	Name	Function
7:5	Reserved	Read returns zero.
4	VAL	DTMF Valid Digit Decoded. 0 = Not currently detecting digit. 1 = Currently detecting digit. Si3212 = Reserved; read returns 0.
3:0	DIG[3:0]	DTMF Digit (Si3210 and Si3211 only). 0001 = "1" 0010 = "2" 0011 = "3" 0100 = "4" 0101 = "5" 0110 = "6" 0111 = "7" 1000 = "8" 1001 = "9" 1010 = "0" 1011 = "*" 1100 = "#" 1101 = "A" 1110 = "B" 1111 = "C" 0000 = "D" Si3212 = Reserved; read returns 0.

Si3210/Si3211/Si3212

Register 28. Indirect Data Access—Low Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	IDA[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	IDA[7:0]	Indirect Data Access—Low Byte. A write to IDA followed by a write to IAA will place the contents of IDA into an indirect register at the location referenced by IAA at the next indirect register update (16 kHz update rate—a write operation). Writing IAA only will load IDA with the value stored at IAA at the next indirect memory update (a read operation).

Register 29. Indirect Data Access—High Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	IDA[15:8]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	IDA[15:8]	Indirect Data Access—High Byte. A write to IDA followed by a write to IAA will place the contents of IDA into an indirect register at the location referenced by IAA at the next indirect register update (16 kHz update rate—a write operation). Writing IAA only will load IDA with the value stored at IAA at the next indirect memory update (a read operation).

Register 30. Indirect Address

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	IAA[7:0]							
Type	R/W							

Reset settings = xxxx_xxxx

Bit	Name	Function
7:0	IAA[7:0]	Indirect Address Access. A write to IDA followed by a write to IAA will place the contents of IDA into an indirect register at the location referenced by IAA at the next indirect register update (16 kHz update rate—a write operation). Writing IAA only will load IDA with the value stored at IAA at the next indirect memory update (a read operation).

Register 31. Indirect Address Status

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								IAS
Type	R							

Reset settings = 0000_0000

Bit	Name	Function
7:1	Reserved	Read returns zero.
0	IAS	Indirect Access Status. 0 = No indirect memory access pending. 1 = Indirect memory access pending.

Register 32. Oscillator 1 Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OSS1	REL	OZ1	O1TAE	O1TIE	O1E	O1SO[1:0]	
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	

Reset settings = 0000_0000

Bit	Name	Function
7	OSS1	Oscillator 1 Signal Status. 0 = Output signal inactive. 1 = Output signal active.
6	REL	Oscillator 1 Automatic Register Reload. This bit should be set for FSK signaling. 0 = Oscillator 1 will stop signaling after inactive timer expires. 1 = Oscillator 1 will continue to read register parameters and output signals.
5	OZ1	Oscillator 1 Zero Cross Enable. 0 = Signal terminates after active timer expires. 1 = Signal terminates at zero crossing after active timer expires.
4	O1TAE	Oscillator 1 Active Timer Enable. 0 = Disable timer. 1 = Enable timer.
3	O1TIE	Oscillator 1 Inactive Timer Enable. 0 = Disable timer. 1 = Enable timer.
2	O1E	Oscillator 1 Enable. 0 = Disable oscillator. 1 = Enable oscillator.
1:0	O1SO[1:0]	Oscillator 1 Signal Output Routing. 00 = Unassigned path (output not connected). 01 = Assign to transmit path. 10 = Assign to receive path. 11 = Assign to both paths.

Register 33. Oscillator 2 Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OSS2		OZ2	O2TAE	O2TIE	O2E	O2SO[1:0]	
Type	R		R/W	R/W	R/W	R/W	R/W	

Reset settings = 0000_0000

Bit	Name	Function
7	OSS2	Oscillator 2 Signal Status. 0 = Output signal inactive. 1 = Output signal active.
6	Reserved	Read returns zero.
5	OZ2	Oscillator 2 Zero Cross Enable. 0 = Signal terminates after active timer expires. 1 = Signal terminates at zero crossing.
4	O2TAE	Oscillator 2 Active Timer Enable. 0 = Disable timer. 1 = Enable timer.
3	O2TIE	Oscillator 2 Inactive Timer Enable. 0 = Disable timer. 1 = Enable timer.
2	O2E	Oscillator 2 Enable. 0 = Disable oscillator. 1 = Enable oscillator.
1:0	O2SO[1:0]	Oscillator 2 Signal Output Routing. 00 = Unassigned path (output not connected) 01 = Assign to transmit path. 10 = Assign to receive path. 11 = Assign to both paths.

Register 34. Ringing Oscillator Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RSS		RDAC	RTAE	RTIE	ROE	RVO	TSWS
Type	R		R	R/W	R/W	R	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7	RSS	Ringing Signal Status. 0 = Ringing oscillator output signal inactive. 1 = Ringing oscillator output signal active.
6	Reserved	Read returns zero.
5	RDAC	Ringing Signal DAC/Linefeed Cross Indicator. For ringing signal start and stop, output to TIP and RING is suspended to ensure continuity with dc linefeed voltages. RDAC indicates that ringing signal is actually present at TIP and RING. 0 = Ringing signal not present at TIP and RING. 1 = Ringing signal present at TIP and RING.
4	RTAE	Ringing Active Timer Enable. 0 = Disable timer. 1 = Enable timer.
3	RTIE	Ringing Inactive Timer Enable. 0 = Disable timer. 1 = Enable timer.
2	ROE	Ringing Oscillator Enable. 0 = Ringing oscillator disabled. 1 = Ringing oscillator enabled.
1	RVO	Ringing Voltage Offset. 0 = No dc offset added to ringing signal. 1 = DC offset added to ringing signal.
0	TSWS	Trapezoid/Sinusoid Waveshape Select. 0 = Sinusoid 1 = Trapezoid

Register 35. Pulse Metering Oscillator Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PSTAT			PMAE	PMIE	PMOE		
Type	R			R/W	R/W	R/W		

Reset settings = 0000_0000

Bit	Name	Function
7	PSTAT	Pulse Metering Signal Status. 0 = Output signal inactive. 1 = Output signal active.
6:5	Reserved	Read returns zero.
4	PMAE	Pulse Metering Active Timer Enable. 0 = Disable timer. 1 = Enable timer.
3	PMIE	Pulse Metering Inactive Timer Enable. 0 = Disable timer. 1 = Enable timer.
2	PMOE	Pulse Metering Oscillator Enable. 0 = Disable oscillator. 1 = Enable oscillator.
1:0	Reserved	Read returns zero.

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Register 36. Oscillator 1 Active Timer—Low Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OAT1[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	OAT1[7:0]	Oscillator 1 Active Timer. LSB = 125 μ s

Register 37. Oscillator 1 Active Timer—High Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OAT1[15:8]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	OAT1[15:8]	Oscillator 1 Active Timer.

Register 38. Oscillator 1 Inactive Timer—Low Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OIT1[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	OIT1[7:0]	Oscillator 1 Inactive Timer. LSB = 125 μ s

Register 39. Oscillator 1 Inactive Timer—High Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OIT1[15:8]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	OIT1[15:8]	Oscillator 1 Inactive Timer.

Register 40. Oscillator 2 Active Timer—Low Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OAT2[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	OAT2[7:0]	Oscillator 2 Active Timer. LSB = 125 μ s

Register 41. Oscillator 2 Active Timer—High Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OAT2[15:8]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	OAT2[15:8]	Oscillator 2 Active Timer.

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Register 42. Oscillator 2 Inactive Timer—Low Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OIT2[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	OIT2[7:0]	Oscillator 2 Inactive Timer. LSB = 125 μ s

Register 43. Oscillator 2 Inactive Timer—High Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	OIT2[15:8]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	OIT2[15:8]	Oscillator 2 Inactive Timer.

Register 44. Pulse Metering Oscillator Active Timer—Low Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PAT[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	PAT[7:0]	Pulse Metering Active Timer. LSB = 125 μ s

Register 45. Pulse Metering Oscillator Active Timer—High Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PAT[15:8]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	PAT[15:8]	Pulse Metering Active Timer.

Register 46. Pulse Metering Oscillator Inactive Timer—Low Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PIT[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	PIT[7:0]	Pulse Metering Inactive Timer. LSB = 125 μ s

Register 47. Pulse Metering Oscillator Inactive Timer—High Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PIT[15:8]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	PIT[15:8]	Pulse Metering Inactive Timer.

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Register 48. Ringing Oscillator Active Timer—Low Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RAT[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	RAT[7:0]	Ringing Active Timer. LSB = 125 μ s

Register 49. Ringing Oscillator Active Timer—High Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RAT[15:8]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	RAT[15:8]	Ringing Active Timer.

Register 50. Ringing Oscillator Inactive Timer—Low Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RIT[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	RIT[7:0]	Ringing Inactive Timer. LSB = 125 μ s

Register 51. Ringing Oscillator Inactive Timer—High Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RIT[15:8]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	RIT[15:8]	Ringing Inactive Timer.

Register 52. FSK Data

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								FSKDAT
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:1	Reserved	Read returns zero.
0	FSKDAT	FSK Data. When FSKEN = 1 (direct Register 108, bit 6) and REL = 1 (direct Register 32, bit 6), this bit serves as the buffered input for FSK generation bit stream data.

Register 63. Loop Closure Debounce Interval

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	LCD[7:0]							
Type								

Reset settings = 0011_0010 (revision C); 0101_0100 (subsequent revisions)

Bit	Name	Function
7:0	LCD[7:0]	Loop Closure Debounce Interval for Automatic Ringing. This register sets the loop closure debounce interval for the ringing silent period when using automatic ringing cadences. The value may be set between 0 ms (0x00) and 159 ms (0x7F) in 1.25 ms steps.

Register 64. Linefeed Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		LFS[2:0]				LF[2:0]		
Type	R				R/W			

Reset settings = 0000_0000

Bit	Name	Function
7	Reserved	Read returns zero.
6:4	LFS[2:0]	Linefeed Shadow. This register reflects the actual realtime linefeed state. Automatic operations may cause actual linefeed state to deviate from the state defined by linefeed register (e.g., when linefeed equals ringing state, LFS will equal on-hook transmission state during ringing silent period and ringing state during ring burst). 000 = Open 001 = Forward active 010 = Forward on-hook transmission 011 = TIP open 100 = Ringing 101 = Reverse active 110 = Reverse on-hook transmission 111 = RING open
3	Reserved	Read returns zero.
2:0	LF[2:0]	Linefeed. Writing to this register sets the linefeed state. 000 = Open 001 = Forward active 010 = Forward on-hook transmission 011 = TIP open 100 = Ringing 101 = Reverse active 110 = Reverse on-hook transmission 111 = RING open

Register 65. External Bipolar Transistor Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		SQH	CBY	ETBE	ETBO[1:0]		ETBA[1:0]	
Type	R/W		R/W	R/W	R/W		R/W	

Reset settings = 0110_0001

Bit	Name	Function
7	Reserved	Read returns zero.
6	SQH	Audio Squelch. 0 = No squelch. 1 = STIPAC and SRINGAC pins squelched.
5	CBY	Capacitor Bypass. 0 = Capacitors CP (C1) and CM (C2) in circuit. 1 = Capacitors CP (C1) and CM (C2) bypassed.
4	ETBE	External Transistor Bias Enable. 0 = Bias disabled. 1 = Bias enabled.
3:2	ETBO[1:0]	External Transistor Bias Levels—On-Hook Transmission State. DC bias current which flows through external BJTs in the on-hook transmission state. Increasing this value increases the compliance of the ac longitudinal balance circuit. 00 = 4 mA 01 = 8 mA 10 = 12 mA 11 = Reserved
1:0	ETBA[1:0]	External Transistor Bias Levels—Active Off-Hook State. DC bias current which flows through external BJTs in the active off-hook state. Increasing this value increases the compliance of the ac longitudinal balance circuit. 00 = 4 mA 01 = 8 mA 10 = 12 mA 11 = Reserved

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Register 66. Battery Feed Control

Si3210								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				VOV	FVBAT			TRACK
Type	R/W			R/W		R/W		

Reset settings = 0000_0011

Si3211/Si3212								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							BATSL	
Type	R/W							

Reset settings = 0000_0110

Bit	Name	Function
7:5	Reserved	Read returns zero.
4	VOV	Overhead Voltage Range Increase. (Si3210 only; See Figure 17 on page 29.) This bit selects the programmable range for V_{OV} , which is defined in indirect Register 41. 0 = V_{OV} = 0 V to 9 V 1 = V_{OV} = 0 V to 13.5 V Si3211/Si3212 = Reserved.
3	FVBAT	V_{BAT} Manual Setting (Si3210 only). 0 = Normal operation 1 = V_{BAT} tracks VBATH register. Si3211/Si3212 = Read returns 0; it cannot be written.
2	Reserved	Si3210 = Read returns zero. Si3211/Si3212 = Read returns one.
1	BATSL	Battery Feed Select (Si3211/Si3212 only). This bit selects between high and low battery supplies. 0 = Low battery selected (DCSW pin low). 1 = High battery selected (DCSW pin high). Si3210 = Read returns zero.
0	TRACK	DC-DC Converter Tracking Mode (Si3210 only). 0 = $ V_{BAT} $ will not decrease below VBATL. 1 = V_{BAT} tracks V_{RING} . Si3211/Si3212 = Reserved.

Register 67. Automatic/Manual Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MNCM	MNDIF	SPDS	ABAT	AORD	AOLD	AOPN
Type		R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0001_1111

Bit	Name	Function
7	Reserved	Read returns zero.
6	MNCM	Common Mode Manual/Automatic Select. 0 = Automatic control. 1 = Manual control, in which TIP (forward) or RING (reverse) forces voltage to follow VCM value.
5	MNDIF	Differential Mode Manual/Automatic Select. 0 = Automatic control. 1 = Manual control (forces differential voltage to follow VOC value).
4	SPDS	Speed-Up Mode Enable. 0 = Speed-up disabled. 1 = Automatic speed-up.
3	ABAT	Battery Feed Automatic/Manual Select. 0 = Automatic mode disabled. 1 = Automatic mode enabled (automatic switching to low battery in off-hook state).
2	AORD	Automatic/Manual Ring Trip Detect. 0 = Manual mode. 1 = Enter off-hook active state automatically upon ring trip detect.
1	AOLD	Automatic/Manual Loop Closure Detect. 0 = Manual mode. 1 = Enter off-hook active state automatically upon loop closure detect.
0	AOPN	Power Alarm Automatic/Manual Detect. 0 = Manual mode. 1 = Enter open state automatically upon power alarm.

Register 68. Loop Closure/Ring Trip Detect Status

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						DBIRAW	RTP	LCR
Type						R	R	R

Reset settings = 0000_0000

Bit	Name	Function
7:3	Reserved	Read returns zero.
2	DBIRAW	Ring Trip/Loop Closure Unfiltered Output. State of this bit reflects the realtime output of ring trip and loop closure detect circuits before debouncing. 0 = Ring trip/loop closure threshold exceeded. 1 = Ring trip/loop closure threshold not exceeded.
1	RTP	Ring Trip Detect Indicator (Filtered Output). 0 = Ring trip detect has not occurred. 1 = Ring trip detect occurred.
0	LCR	Loop Closure Detect Indicator (Filtered Output). 0 = Loop closure detect has not occurred. 1 = Loop closure detect has occurred.

Register 69. Loop Closure Debounce Interval

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		LCDI[6:0]						
Type	R/W							

Reset settings = 0000_1010

Bit	Name	Function
7	Reserved	Read returns zero.
6:0	LCDI[6:0]	Loop Closure Debounce Interval. The value written to this register defines the minimum steady state debounce time. Value may be set between 0 ms (0x00) to 159 ms (0x7F) in 1.25 ms steps. Default value = 12.5 ms.

Register 70. Ring Trip Detect Debounce Interval

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		RTDI[6:0]						
Type	R/W							

Reset settings = 0000_1010

Bit	Name	Function
7	Reserved	Read returns zero.
6:0	RTDI[6:0]	Ring Trip Detect Debounce Interval. The value written to this register defines the minimum steady state debounce time. The value may be set between 0 ms (0x00) to 159 ms (0x7F) in 1.25 ms steps. Default value = 12.5 ms.

Register 71. Loop Current Limit

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						ILIM[2:0]		
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:3	Reserved	Read returns zero.
2:0	ILIM[2:0]	Loop Current Limit. The value written to this register sets the constant loop current. The value may be set between 20 mA (0x00) and 41 mA (0x07) in 3 mA steps.

Register 72. On-Hook Line Voltage

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		VSGN	VOC[5:0]					
Type	R/W				R/W			

Reset settings = 0010_0000

Bit	Name	Function
7	Reserved	Read returns zero.
6	VSGN	On-Hook Line Voltage. The value written to this bit sets the on-hook line voltage polarity ($V_{TIP}-V_{RING}$). 0 = $V_{TIP}-V_{RING}$ is positive 1 = $V_{TIP}-V_{RING}$ is negative
5:0	VOC[5:0]	On-Hook Line Voltage. The value written to this register sets the on-hook line voltage ($V_{TIP}-V_{RING}$). Value may be set between 0 V (0x00) and 94.5 V (0x3F) in 1.5 V steps. Default value = 48 V.

Register 73. Common Mode Voltage

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			VCM[5:0]					
Type	R/W							

Reset settings = 0000_0010

Bit	Name	Function
7:6	Reserved	Read returns zero.
5:0	VCM[5:0]	Common Mode Voltage. The value written to this register sets V_{TIP} for forward active and forward on-hook transmission states and V_{RING} for reverse active and reverse on-hook transmission states. The value may be set between 0 V (0x00) and -94.5 V (0x3F) in 1.5 V steps. Default value = -3 V.

Register 74. High Battery Voltage

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			VBATH[5:0]					
Type	R/W							

Reset settings = 0011_0010

Bit	Name	Function
7:6	Reserved	Read returns zero.
5:0	VBATH[5:0]	High Battery Voltage. The value written to this register sets high battery voltage. VBATH must be greater than or equal to VBATL. The value may be set between 0 V (0x00) and –94.5 V (0x3F) in 1.5 V steps. Default value = –75 V. For Si3211 and Si3212, VBATH must be set equal to externally supplied V _{BATH} input voltage.

Register 75. Low Battery Voltage

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			VBATL[5:0]					
Type	R/W							

Reset settings = 0001_0000

Bit	Name	Function
7:6	Reserved	Read returns zero.
5:0	VBATL[5:0]	Low Battery Voltage. The value written to this register sets low battery voltage. VBATH must be greater than or equal to VBATL. The value may be set between 0 V (0x00) and –94.5 V (0x3F) in 1.5 V steps. Default value = –24 V. For Si3211 and Si3212, VBATL must be set equal to externally supplied V _{BATL} input voltage.

Register 76. Power Monitor Pointer

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						PWRMP[2:0]		
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:3	Reserved	Read returns zero.
2:0	PWRMP[2:0]	Power Monitor Pointer. Selects the external transistor from which to read power output. The power of the selected transistor is read in the PWRMP register. 000 = Q1 001 = Q2 010 = Q3 011 = Q4 100 = Q5 101 = Q6 110 = Undefined 111 = Undefined

Register 77. Line Power Output Monitor

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PWRMP[7:0]							
Type	R							

Reset settings = 0000_0000

Bit	Name	Function
7:0	PWRMP[7:0]	Line Power Output Monitor. This register reports the realtime power output of the transistor selected using PWRMP. The range is 0 W (0x00) to 7.8 W (0xFF) in 30.4 mW steps for Q1, Q2, Q5, and Q6. The range is 0 W (0x00) to 0.9 W (0xFF) in 3.62 mW steps for Q3 and Q4.

Register 78. Loop Voltage Sense

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		LVSP	LVS[5:0]					
Type		R	R					

Reset settings = 0000_0000

Bit	Name	Function
7	Reserved	Read returns zero.
6	LVSP	Loop Voltage Sense Polarity. This register reports the polarity of the differential loop voltage ($V_{TIP} - V_{RING}$). 0 = Positive loop voltage ($V_{TIP} > V_{RING}$). 1 = Negative loop voltage ($V_{TIP} < V_{RING}$).
5:0	LVS[5:0]	Loop Voltage Sense Magnitude. This register reports the magnitude of the differential loop voltage ($V_{TIP} - V_{RING}$). The range is 0 V to 94.5 V in 1.5 V steps.

Register 79. Loop Current Sense

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		LCSP	LCS[5:0]					
Type		R	R					

Reset settings = 0000_0000

Bit	Name	Function
7	Reserved	Read returns zero.
6	LCSP	Loop Current Sense Polarity. This register reports the polarity of the loop current. 0 = Positive loop current (forward direction). 1 = Negative loop current (reverse direction).
5:0	LCS[5:0]	Loop Current Sense Magnitude. This register reports the magnitude of the loop current. The range is 0 mA to 80 mA in 1.27 mA steps.

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Register 80. TIP Voltage Sense

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VTIP[7:0]							
Type	R							

Reset settings = 0000_0000

Bit	Name	Function
7:0	VTIP[7:0]	TIP Voltage Sense. This register reports the realtime voltage at TIP with respect to ground. The range is 0 V (0x00) to –95.88 V (0xFF) in .376 V steps.

Register 81. RING Voltage Sense

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VRING[7:0]							
Type	R							

Reset settings = 0000_0000

Bit	Name	Function
7:0	VRING[7:0]	RING Voltage Sense. This register reports the realtime voltage at RING with respect to ground. The range is 0 V (0x00) to –95.88 V (0xFF) in .376 V steps.

Register 82. Battery Voltage Sense 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VBATS1[7:0]							
Type	R							

Reset settings = 0000_0000

Bit	Name	Function
7:0	VBATS1[7:0]	Battery Voltage Sense 1. This register is one of two registers that reports the realtime voltage at V_{BAT} with respect to ground. The range is 0 V (0x00) to –95.88 V (0xFF) in .376 V steps.

Register 83. Battery Voltage Sense 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	VBATS2[7:0]							
Type	R							

Reset settings = 0000_0000

Bit	Name	Function
7:0	VBATS2[7:0]	Battery Voltage Sense 2. This register is one of two registers that reports the realtime voltage at V_{BAT} with respect to ground. The range is 0 V (0x00) to -95.88 V (0xFF) in .376 V steps.

Register 84. Transistor 1 Current Sense

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	IQ1[7:0]							
Type	R							

Reset settings = xxxx_xxxx

Bit	Name	Function
7:0	IQ1[7:0]	Transistor 1 Current Sense. This register reports the realtime current through Q1. The range is 0 A (0x00) to 81.35 mA (0xFF) in .319 mA steps. If ETBE = 1, the reported value does not include the additional ETBO/A current.

Register 85. Transistor 2 Current Sense

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	IQ2[7:0]							
Type	R							

Reset settings = xxxx_xxxx

Bit	Name	Function
7:0	IQ2[7:0]	Transistor 2 Current Sense. This register reports the realtime current through Q2. The range is 0 A (0x00) to 81.35 mA (0xFF) in .319 mA steps. If ETBE = 1, the reported value does not include the additional ETBO/A current.

Register 86. Transistor 3 Current Sense

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	IQ3[7:0]							
Type	R							

Reset settings = xxxx_xxxx

Bit	Name	Function
7:0	IQ3[7:0]	Transistor 3 Current Sense. This register reports the realtime current through Q3. The range is 0 A (0x00) to 9.59 mA (0xFF) in 37.6 μ A steps.

Register 87. Transistor 4 Current Sense

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	IQ4[7:0]							
Type	R							

Reset settings = xxxx_xxxx

Bit	Name	Function
7:0	IQ4[7:0]	Transistor 4 Current Sense. This register reports the realtime current through Q4. The range is 0 A (0x00) to 9.59 mA (0xFF) in 37.6 μ A steps.

Register 88. Transistor 5 Current Sense

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	IQ5[7:0]							
Type	R							

Reset settings = xxxx_xxxx

Bit	Name	Function
7:0	IQ5[7:0]	Transistor 5 Current Sense. This register reports the realtime current through Q5. The range is 0 A (0x00) to 80.58 mA (0xFF) in .316 mA steps.

Register 89. Transistor 6 Current Sense

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	IQ6[7:0]							
Type	R							

Reset settings = xxxx_xxxx

Bit	Name	Function
7:0	IQ6[7:0]	Transistor 6 Current Sense. This register reports the realtime current through Q6. The range is 0 A (0x00) to 80.58 mA (0xFF) in .316 mA steps.

Register 92. DC-DC Converter PWM Period

Si3210								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DCN[7]	1	DCN[5:0]					
Type	R/W	R	R/W					

Reset settings = 1111_1111

Si3211/Si3212								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = xxxx_xxxx

Bit	Name	Function
7:0	DCN[7:0]	DC-DC Converter Period. This bit sets the PWM period for the dc-dc converter. The range is 3.906 μ s (0x40) to 15.564 μ s (0xFF) in 61.035 ns steps. Si3211/Si3212 = Reserved. Bit 6 is fixed to one and read-only, so there are two ranges of operation: 3.906 μ s–7.751 μ s, used for MOSFET transistor switching. 11.719 μ s–15.564 μ s, used for BJT transistor switching.

Si3210/Si3211/Si3212

Register 93. DC-DC Converter Switching Delay

Si3210								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DCCAL		DCPOL	DCTOF[4:0]				
Type	R/W		R			R/W		

Reset settings = 0001_0100 (Si3210)

Reset settings = 0011_0100 (Si3210M)

Si3211/Si3212								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = xxxx_xxxx

Bit	Name	Function
7	DCCAL	DC-DC Converter Peak Current Monitor Calibration Status (Si3210 only). Writing a one to this bit starts the dc-dc converter peak current monitor calibration routine. 0 = Normal operation. 1 = Calibration being performed. Si3211/Si3212 = Reserved.
6	Reserved	Read returns zero.
5	DCPOL	DC-DC Converter Feed Forward Pin (DCFF) Polarity (Si3210 only). This read-only register bit indicates the polarity relationship of the DCFF pin to the DCDRV pin. Two versions of the Si3210 are offered to support the two relationships. 0 = DCFF pin polarity is opposite of DCDRV pin (Si3210). 1 = DCFF pin polarity is same as DCDRV pin (Si3210M). Si3211/Si3212 = Reserved.
4:0	DCTOF[4:0]	DC-DC Converter Minimum Off Time (Si3210 only). This register sets the minimum off time for the pulse width modulated dc-dc converter control. $T_{OFF} = (DCTOF + 4) \cdot 61.035 \text{ ns}$. Si3211/Si3212 = Reserved.

Register 94. DC-DC Converter PWM Pulse Width

Si3210								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DCPW[7:0]							
Type	R							

Reset settings = 0000_0000

Si3211/Si3212								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = 0000_0000

Bit	Name	Function
7:0	DCPW[7:0]	DC-DC Converter Pulse Width (Si3210 only). Pulse width of DCDRV is given by $PW = (DCPW - DCTOF - 4) \cdot 61.035 \text{ ns}$. Si3211/Si3212 = Reserved.

Register 96. Calibration Control/Status Register 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		CAL	CALSP	CALR	CALT	CALD	CALC	CALIL
Type		R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0001_1111

Bit	Name	Function
7	Reserved	Read returns zero.
6	CAL	Calibration Control/Status Bit. Setting this bit begins calibration of the entire system. 0 = Normal operation or calibration complete. 1 = Calibration in progress.
5	CALSP	Calibration Speedup. Setting this bit shortens the time allotted for V_{BAT} settling at the beginning of the calibration cycle. 0 = 300 ms 1 = 30 ms
4	CALR	RING Gain Mismatch Calibration. 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.
3	CALT	TIP Gain Mismatch Calibration. 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.
2	CALD	Differential DAC Gain Calibration. 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.
1	CALC	Common Mode DAC Gain Calibration. 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.
0	CALIL	I_{LIM} Calibration. 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.

Register 97. Calibration Control/Status Register 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				CALM1	CALM2	CALDAC	CALADC	CALCM
Type	R/W			R/W	R/W	R/W	R/W	R/W

Reset settings = 0001_1111

Bit	Name	Function
7:5	Reserved	Read returns zero.
4	CALM1	Monitor ADC Calibration 1. 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.
3	CALM2	Monitor ADC Calibration 2. 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.
2	CALDAC	DAC Calibration. Setting this bit begins calibration of the audio DAC offset. 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.
1	CALADC	ADC Calibration. Setting this bit begins calibration of the audio ADC offset. 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.
0	CALCM	Common Mode Balance Calibration. Setting this bit begins calibration of the ac longitudinal balance. 0 = Normal operation or calibration complete. 1 = Calibration enabled or in progress.

Register 98. RING Gain Mismatch Calibration Result

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				CALGMR[4:0]				
Type	R/W							

Reset settings = 0001_0000

Bit	Name	Function
7:5	Reserved	Read returns zero.
4:0	CALGMR[4:0]	Gain Mismatch of IE Tracking Loop for RING Current.

Register 99. TIP Gain Mismatch Calibration Result

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				CALGMT[4:0]				
Type	R/W							

Reset settings = 0001_0000

Bit	Name	Function
7:5	Reserved	Read returns zero.
4:0	CALGMT[4:0]	Gain Mismatch of IE Tracking Loop for TIP Current.

Register 100. Differential Loop Current Gain Calibration Result

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				CALGD[4:0]				
Type	R/W							

Reset settings = 0001_0001

Bit	Name	Function
7:5	Reserved	Read returns zero.
4:0	CALGD[4:0]	Differential DAC Gain Calibration Result.

Register 101. Common Mode Loop Current Gain Calibration Result

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				CALGC[4:0]				
Type	R/W							

Reset settings = 0001_0001

Bit	Name	Function
7:5	Reserved	Read returns zero.
4:0	CALGC[4:0]	Common Mode DAC Gain Calibration Result.

Register 102. Current Limit Calibration Result

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					CALGIL[3:0]			
Type	R/W							

Reset settings = 0000_1000

Bit	Name	Function
7:5	Reserved	Read returns zero.
3:0	CALGIL[3:0]	Current Limit Calibration Result.

Register 103. Monitor ADC Offset Calibration Result

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CALMG1[3:0]				CALMG2[3:0]			
Type	R/W				R/W			

Reset settings = 1000_1000

Bit	Name	Function
7:4	CALMG1[3:0]	Monitor ADC Offset Calibration Result 1.
3:0	CALMG2[3:0]	Monitor ADC Offset Calibration Result 2.

Si3210/Si3211/Si3212

Register 104. Analog DAC/ADC Offset

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					DACP	DACN	ADCP	ADCN
Type	R/W				R/W		R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7:4	Reserved	Read returns zero.
3	DACP	Positive Analog DAC Offset.
2	DACN	Negative Analog DAC Offset.
1	ADCP	Positive Analog ADC Offset.
0	ADCN	Negative Analog ADC Offset.

Register 105. DAC Offset Calibration Result

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DACOF[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	DACOF[7:0]	DAC Offset Calibration Result.

Register 106. Common Mode Calibration Result

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			CMBAL[5:0]					
Type								

Reset settings = 0010_0000

Bit	Name	Function
7:6	Reserved	Read returns zero.
5:0	CMBAL[5:0]	Common Mode Calibration Result.

Register 107. DC Peak Current Monitor Calibration Result

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					CMDCPK[3:0]			
Type	R/W							

Reset settings = 0000_1000

Bit	Name	Function
7:4	Reserved	Read returns zero.
3:0	CMDCPK[3:0]	DC Peak Current Monitor Calibration Result.

Si3210/Si3211/Si3212

Register 108. Enhancement Enable

Note: The Enhancement Enable register and associated features are available in silicon revisions C and later.

Si3210								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ILIMEN	FSKEN	DCSU	ZSEXT		LCVE	DCFIL	HYSTEN
Type	R/W	R/W	R/W	R/W		R/W	R/W	R/W

Reset settings = 0000_0000

Si3211/Si3212								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ILIMEN	FSKEN		ZSEXT	SWDB	LCVE		HYSTEN
Type	R/W	R/W		R/W	R/W	R/W		R/W

Reset settings = 0000_0000

Bit	Name	Function
7	ILIMEN	Current Limit Increase. When enabled, this bit temporarily increases the maximum differential current limit at the end of a ring burst to enable a faster settling time to a dc linefeed state. 0 = The value programmed in ILIM (direct Register 71) is used. 1 = The maximum differential loop current limit is temporarily increased to 41 mA.
6	FSKEN	FSK Generation Enhancement. When enabled, this bit will increase the clocking rate of tone generator 1 to 24 kHz only when the REL bit (direct Register 32, bit 6) is set. Also, dedicated oscillator registers are used for FSK generation (indirect registers 99–104). Audio tones are generated using this new higher frequency, and oscillator 1 active and inactive timers have a finer bit resolution of 41.67 μ s. This provides greater resolution during FSK caller ID signal generation. 0 = Tone generator always clocked at 8 kHz; OSC1, OSC1X., and OSC1Y are always used. 1 = Tone generator module clocked at 24 kHz and dedicated FSK registers used only when REL = 1; otherwise clocked at 8 kHz.
5	DCSU	DC-DC Converter Control Speedup (Si3210 only). When enabled, this bit invokes a multi-threshold error control algorithm which allows the dc-dc converter to adjust more quickly to voltage changes. 0 = Normal control algorithm used. 1 = Multi-threshold error control algorithm used.

Bit	Name	Function
4	ZSEXT	Impedance Internal Reference Resistor Disable. When enabled, this bit removes the internal reference resistor used to synthesize ac impedances for $600 + 2.1 \mu\text{F}$ and $900 + 2.16 \mu\text{F}$ so that an external resistor reference may be used. 0 = Internal resistor used to generate $600 + 2.1 \mu\text{F}$ and $900 + 2.16 \mu\text{F}$ impedances. 1 = Internal resistor removed from circuit.
3	SWDB	Battery Switch Debounce (Si3211 and Si3212 only). When enabled, this bit allows debouncing of the battery switching circuit only when transitioning from V_{BATH} to V_{BATL} external battery supplies ($\text{EXTBAT} = 1$). 0 = No debounce used. 1 = 60 ms debounce period used. Si3210 = Reserved.
2	LCVE	Voltage-Based Loop Closure. Enables loop closure to be determined by the TIP-to-RING voltage rather than loop current. 0 = Loop closure determined by loop current. 1 = Loop closure determined by TIP-to-RING voltage.
1	DCFIL	DC-DC Converter Squelch (Si3210 only). When enabled, this bit squelches noise in the audio band from the dc-dc converter control loop. 0 = Voice band squelch disabled. 1 = Voice band squelch enabled.
0	HYSTEN	Loop Closure Hysteresis Enable. When enabled, this bit allows hysteresis to the loop closure calculation. The upper and lower hysteresis thresholds are defined by indirect registers 28 and 43, respectively. 0 = Loop closure hysteresis disabled. 1 = Loop closure hysteresis enabled.

Indirect Registers

Indirect registers are not directly mapped into memory but are accessible through the IDA and IAA registers. A write to IDA followed by a write to IAA is interpreted as a write request to an indirect register. In this case, the contents of IDA are written to indirect memory at the location referenced by IAA at the next indirect register update. A write to IAA without first writing to IDA is interpreted as a read request from an indirect register. In this case, the value located at IAA is written to IDA at the next indirect register update. Indirect registers are updated at a rate of 16 kHz. For pending indirect register transfers, IAS (direct Register 31) will be one until serviced. In addition an interrupt, IND (Register 20), can be generated upon completion of the indirect transfer.

DTMF Decoding (Si3210 and Si3211 only)

All values are represented in twos-complement format.

Note: The values of all indirect registers are undefined following the reset state.

Table 35. DTMF Indirect Registers Summary

Addr.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	ROW0[15:0]															
1	ROW1[15:0]															
2	ROW2[15:0]															
3	ROW3[15:0]															
4	COL[15:0]															
5	FWDTW[15:0]															
6	REVTW[15:0]															
7	ROWREL[15:0]															
8	COLREL[15:0]															
9	ROW2[15:0]															
10	COL2[15:0]															
11	PWRMIN[15:0]															
12	HOTL[15:0]															

Table 36. DTMF Indirect Registers Description

Addr.	Description	Reference Page
0	DTMF Row 0 Peak Magnitude Pass Ratio Threshold. This register sets the minimum power ratio threshold for row 0 DTMF detection. If the ratio of power in row 0 to total power in the row band is greater than ROW0, then a row 0 signal is detected. A value of 0x7FF0 corresponds to a 1.0 ratio.	38
1	DTMF Row 1 Peak Magnitude Pass Ratio Threshold. This register sets the minimum power ratio threshold for row 1 DTMF detection. If the ratio of power in row 1 to total power in the row band is greater than ROW1, then a row 1 signal is detected. A value of 0x7FF0 corresponds to a 1.0 ratio.	38

Table 36. DTMF Indirect Registers Description (Continued)

Addr.	Description	Reference Page
2	DTMF Row 2 Peak Magnitude Pass Ratio Threshold. This register sets the minimum power ratio threshold for row 2 DTMF detection. If the ratio of power in row 2 to total power in the row band is greater than ROW2, then a row 2 signal is detected. A value of 0x7FF0 corresponds to a 1.0 ratio.	38
3	DTMF Row 3 Peak Magnitude Pass Ratio Threshold. This register sets the minimum power ratio threshold for row 3 DTMF detection. If the ratio of power in row 3 to total power in the row band is greater than ROW3, then a row 3 signal is detected. A value of 0x7FF0 corresponds to a 1.0 ratio.	38
4	DTMF Column Peak Magnitude Pass Threshold. This register sets the minimum power ratio threshold for column DTMF detection; all columns use the same threshold. If the ratio of power in a particular column to total power in the column band is greater than COL, then a column detect for that particular column signal is detected. A value of 0x7FF0 corresponds to a 1.0 ratio.	38
5	DTMF Forward Twist Threshold. This register sets the threshold for the power ratio of row power to column power. A value of 0x7F0 corresponds to a 1.0 ratio.	38
6	DTMF Reverse Twist Threshold. This register sets the threshold for the power ratio of column power to row power. A value of 0x7F0 corresponds to a 1.0 ratio.	38
7	DTMF Row Ratio Threshold. This register sets the threshold for the power ratio of highest power row to the other rows. A value of 0x7F0 corresponds to a 1.0 ratio.	38
8	DTMF Column Ratio Threshold. This register sets the threshold for the power ratio of highest power column to the other columns. A value of 0x7F0 corresponds to a 1.0 ratio.	38
9	DTMF Row Second Harmonic Threshold. This register sets the threshold for the power ratio of peak row tone to its second harmonic. A value of 0x7F0 corresponds to a 1.0 ratio.	38
10	DTMF Column Second Harmonic Threshold. This register sets the threshold for the power ratio of peak column tone to its second harmonic. A value of 0x7F0 corresponds to a 1.0 ratio.	38
11	DTMF Power Minimum Threshold. This register sets the threshold for the minimum total power in the DTMF calculation, under which the calculation is ignored.	38
12	DTMF Hot Limit Threshold. This register sets the two-step AGC in the DTMF path.	38

Oscillators

See functional description sections of tone generation, ringing, and pulse metering for guidelines on computing register values. All values are represented in twos-complement format.

Note: The values of all indirect registers are undefined following the reset state. Shaded areas denote bits that can be read and written but should be written to zeroes.

Table 37. Oscillator Indirect Registers Summary

Addr.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
13	OSC1[15:0]															
14	OSC1X[15:0]															
15	OSC1Y[15:0]															
16	OSC2[15:0]															
17	OSC2X[15:0]															
18	OSC2Y[15:0]															
19																
20	RCO[15:0]															
21	RNGX[15:0]															
22	RNGY[15:0]															
23	PLSD[15:0]															
24	PLSX[15:0]															
25	PLSCO[15:0]															

Table 38. Oscillator Indirect Registers Description

Addr.	Description	Reference Page
13	Oscillator 1 Frequency Coefficient. Sets tone generator 1 frequency.	31
14	Oscillator 1 Amplitude Register. Sets tone generator 1 signal amplitude.	31
15	Oscillator 1 Initial Phase Register. Sets initial phase of tone generator 1 signal.	31
16	Oscillator 2 Frequency Coefficient. Sets tone generator 2 frequency.	31
17	Oscillator 2 Amplitude Register. Sets tone generator 2 signal amplitude.	31
18	Oscillator 2 Initial Phase Register. Sets initial phase of tone generator 2 signal.	31
19	Ringing Oscillator DC Offset. Sets dc offset component ($V_{TIP}-V_{RING}$) to ringing waveform. The range is 0 to 94.5 V in 1.5 V increments.	33

Table 38. Oscillator Indirect Registers Description (Continued)

Addr.	Description	Reference Page
20	Ring Oscillator Frequency Coefficient. Sets ringing generator frequency.	33
21	Ring Oscillator Amplitude Register. Sets ringing generator signal amplitude.	33
22	Ring Oscillator Initial Phase Register. Sets initial phase of ringing generator signal.	33
23	Pulse Metering Oscillator Attack/Decay Ramp Rate. Sets pulse metering attack/decay ramp rate.	37
24	Pulse Metering Oscillator Amplitude Register. Sets pulse metering generator signal amplitude.	37
25	Pulse Metering Oscillator Frequency Coefficient. Sets pulse metering generator frequency.	37

Digital Programmable Gain/Attenuation

See functional description sections of digital programmable gain/attenuation for guidelines on computing register values. All values are represented in twos-complement format.

Note: The values of all indirect registers are undefined following the reset state. Shaded areas denote bits that can be read and written but should be written to zeroes.

Table 39. Digital Programmable Gain/Attenuation Indirect Registers Summary

Addr.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
26	DACG[11:0]															
27	ADCG[11:0]															

Table 40. Digital Programmable Gain/Attenuation Indirect Registers Description

Addr.	Description	Reference Page
26	Receive Path Digital to Analog Converter Gain/Attenuation. This register sets gain/attenuation for the receive path. The digitized signal is effectively multiplied by DACG to achieve gain/attenuation. A value of 0x00 corresponds to $-\infty$ dB gain (mute). A value of 0x400 corresponds to unity gain. A value of 0x7FF corresponds to a gain of 6 dB.	39
27	Transmit Path Analog to Digital Converter Gain/Attenuation. This register sets gain/attenuation for the transmit path. The digitized signal is effectively multiplied by ADCG to achieve gain/attenuation. A value of 0x00 corresponds to $-\infty$ dB gain (mute). A value of 0x400 corresponds to unity gain. A value of 0x7FF corresponds to a gain of 6 dB.	39

SLIC Control

See descriptions of linefeed interface and power monitoring for guidelines on computing register values. All values are represented in twos-complement format.

Note: The values of all indirect registers are undefined following the reset state. Shaded areas denote bits that can be read and written but should be written to zeroes.

Table 41. SLIC Control Indirect Registers Summary

Addr.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
28		LCRT[5:0]														
29		RPTP[5:0]														
30				CML[5:0]												
31				CMH[5:0]												
32		PPT12[7:0]														
33		PPT34[7:0]														
34		PPT56[7:0]														
35	NCLR[12:0]															
36	NRTP[12:0]															
37	NQ12[12:0]															
38	NQ34[12:0]															
39	NQ56[12:0]															
40				VCMR[3:0]												
41				VMIND[3:0]*												
42																
43		LCRTL[5:0]														
*Note: Si3210 only.																

Table 42. SLIC Control Indirect Registers Description

Addr.	Description	Reference Page
28	Loop Closure Threshold. Loop closure detection threshold. This register defines the upper bounds threshold if hysteresis is enabled (direct Register 108, bit 0). The range is 0–80 mA in 1.27 mA steps.	26
29	Ring Trip Threshold. Ring trip detection threshold during ringing.	36
30	Common Mode Minimum Threshold for Speed-Up. This register defines the negative common mode voltage threshold. Exceeding this threshold enables a wider bandwidth of dc linefeed control for faster settling times. The range is 0–23.625 V in 0.375 V steps.	
31	Common Mode Maximum Threshold for Speed-Up. This register defines the positive common mode voltage threshold. Exceeding this threshold enables a wider bandwidth of dc linefeed control for faster settling times. The range is 0–23.625 V in 0.375 V steps.	

Table 42. SLIC Control Indirect Registers Description (Continued)

Addr.	Description	Reference Page
32	Power Alarm Threshold for Transistors Q1 and Q2.	24
33	Power Alarm Threshold for Transistors Q3 and Q4.	24
34	Power Alarm Threshold for Transistors Q5 and Q6.	24
35	Loop Closure Filter Coefficient.	26
36	Ring Trip Filter Coefficient.	36
37	Thermal Low Pass Filter Pole for Transistors Q1 and Q2.	24
38	Thermal Low Pass Filter Pole for Transistors Q3 and Q4.	24
39	Thermal Low Pass Filter Pole for Transistors Q5 and Q6.	24
40	Common Mode Bias Adjust During Ringing. Recommended value of 6 decimal.	33
41	DC-DC Converter V_{OV} Voltage (Si3210 only). This register sets the overhead voltage, V_{OV} , to be supplied by the dc-dc converter. When the VOV bit = 0 (direct Register 66, bit 4), V_{OV} should be set between 0 and 9 V (VMIND = 0 to 6h). When the VOV bit = 1, V_{OV} should be set between 0 and 13.5 V (VMIND = 0 to 9h).	27
42	Reserved.	
43	Loop Closure Threshold—Lower Bound. This register defines the lower threshold for loop closure hysteresis, which is enabled in bit 0 of direct Register 108. The range is 0–80 mA in 1.27 mA steps.	26

FSK Control

For detailed instructions on FSK signal generation, refer to “Application Note 32: FSK Generation” (AN32). These registers support enhanced FSK generation mode, which is enabled by setting FSKEN = 1 (direct Register 108, bit 6) and REL = 1 (direct Register 32, bit 6).

Table 43. FSK Control Indirect Registers Summary

Addr.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
99	FSK0X[15:0]															
100	FSK0[15:0]															
101	FSK1X[15:0]															
102	FSK1[15:0]															
103	FSK01[15:0]															
104	FSK10[15:0]															

Table 44. FSK Control Indirect Registers Description

Addr.	Description	Reference Page
99	FSK Amplitude Coefficient for Space. When FSKEN = 1 and REL = 1, this register sets the amplitude to be used when generating a space or “0”. When the active timer (OAT1) expires, the value of this register is loaded into oscillator 1 instead of OSC1X.	33 and AN32
100	FSK Frequency Coefficient for Space. When FSKEN = 1 and REL = 1, this register sets the frequency to be used when generating a space or “0”. When the active timer (OAT1) expires, the value of this register is loaded into oscillator 1 instead of OSC1.	33 and AN32
101	FSK Amplitude Coefficient for Mark. When FSKEN = 1 and REL = 1, this register sets the amplitude to be used when generating a mark or “1”. When the active timer (OAT1) expires, the value of this register is loaded into oscillator 1 instead of OSC1X.	33 and AN32
102	FSK Frequency Coefficient for Mark. When FSKEN = 1 and REL = 1, this register sets the frequency to be used when generating a mark or “1”. When the active timer (OAT1) expires, the value of this register is loaded into oscillator 1 instead of OSC1.	33 and AN32
103	FSK Transition Parameter from 0 to 1. When FSKEN = 1 and REL = 1, this register defines a gain correction factor that is applied to signal amplitude when transitioning from a space (0) to a mark (1).	33 and AN32
104	FSK Transition Parameter from 1 to 0. When FSKEN = 1 and REL = 1, this register defines a gain correction factor that is applied to signal amplitude when transitioning from a mark (1) to a space (0).	33 and AN32

Pin Descriptions: Si3210/11/12

$\overline{\text{CS}}$	1 •	38	SCLK
$\overline{\text{INT}}$	2	37	SDI
PCLK	3	36	SDO
DRX	4	35	SDITHRU
DTX	5	34	DCDRV/DCSW
FSYNC	6	33	DCFF/DOUT
$\overline{\text{RESET}}$	7	32	TEST
SDCH/DIO1	8	31	GNDD
SDCL/DIO2	9	30	VDDD
VDDA1	10	29	ITIPN
IREF	11	28	ITIPP
CAPP	12	27	VDDA2
QGND	13	26	IRINGP
CAPM	14	25	IRINGN
STIPDC	15	24	IGMP
SRINGDC	16	23	GNDA
STIPE	17	22	IGMN
SVBAT	18	21	SRINGAC
SRINGE	19	20	STIPAC

Pin #	Pin Name	Description
1	$\overline{\text{CS}}$	Chip Select. Active low. When inactive, SCLK and SDI are ignored and SDO is high impedance. When active, the serial port is operational.
2	$\overline{\text{INT}}$	Interrupt. Maskable interrupt output. Open drain output for wire-ORed operation.
3	PCLK	PCM Bus Clock. Clock input for PCM bus timing.
4	DRX	Receive PCM Data. Input data from PCM bus.
5	DTX	Transmit PCM Data. Output data to PCM bus.
6	FSYNC	Frame Synch. 8 kHz frame synchronization signal for the PCM bus. May be short or long pulse format.
7	$\overline{\text{RESET}}$	Reset. Active low input. Hardware reset used to place all control registers in the default state.
8	SDCH/DIO1	DC Monitor/General Purpose I/O. DC-DC converter monitor input used to detect overcurrent situations in the converter (Si3210 only). General purpose I/O (Si3211/Si3212 only).
9	SDCL/DIO2	DC Monitor/General Purpose I/O. DC-DC converter monitor input used to detect overcurrent situations in the converter (Si3210 only). General purpose I/O (Si3211/Si3212 only).

Si3210/Si3211/Si3212

Pin #	Pin Name	Description
10	VDDA1	Analog Supply Voltage. Analog power supply for internal analog circuitry.
11	IREF	Current Reference. Connects to an external resistor used to provide a high accuracy reference current.
12	CAPP	SLIC Stabilization Capacitor. Capacitor used in low pass filter to stabilize SLIC feedback loops.
13	QGND	Component Reference Ground.
14	CAPM	SLIC Stabilization Capacitor. Capacitor used in low pass filter to stabilize SLIC feedback loops.
15	STIPDC	TIP Sense. Analog current input used to sense voltage on the TIP lead.
16	SRINGDC	RING Sense. Analog current input used to sense voltage on the RING lead.
17	STIPE	TIP Emitter Sense. Analog current input used to sense voltage on the Q6 emitter lead.
18	SVBAT	VBAT Sense. Analog current input used to sense voltage on dc-dc converter output voltage lead.
19	SRINGE	RING Emitter Sense. Analog current input used to sense voltage on the Q5 emitter lead.
20	STIPAC	TIP Transmit Input. Analog ac input used to detect voltage on the TIP lead.
21	SRINGAC	RING Transmit Input. Analog ac input used to detect voltage on the RING lead.
22	IGMN	Transconductance Amplifier External Resistor. Negative connection for transconductance gain setting resistor.
23	GNDA	Analog Ground. Ground connection for internal analog circuitry.
24	IGMP	Transconductance Amplifier External Resistor. Positive connection for transconductance gain setting resistor.
25	IRINGN	Negative Ring Current Control. Analog current output driving Q3.
26	IRINGP	Positive Ring Current Control. Analog current output driving Q2.
27	VDDA2	Analog Supply Voltage. Analog power supply for internal analog circuitry.
28	ITIPP	Positive TIP Current Control. Analog current output driving Q1.
29	ITIPN	Negative TIP Current Control. Analog current output driving Q4.

Pin #	Pin Name	Description
30	VDDD	Digital Supply Voltage. Digital power supply for internal digital circuitry.
31	GNDD	Digital Ground. Ground connection for internal digital circuitry.
32	TEST	Test. Enables test modes for Silicon Labs internal testing. This pin should always be tied to ground for normal operation.
33	DCFF/DOUT	DC Feed-Forward/High Current General Purpose Output. Feed-forward drive of external bipolar transistors to improve dc-dc converter efficiency (Si3210 only). High current output pin (Si3211/Si3212 only).
34	DCDRV/DCSW	DC Drive/Battery Switch. DC-DC converter control signal output which drives external bipolar transistor (Si3210 only). Battery switch control signal output which drives external bipolar transistor (Si3211/Si3212 only).
35	SDITHRU	SDI Passthrough. Cascaded SDI output signal for daisy-chain mode.
36	SDO	Serial Port Data Out. Serial port control data output.
37	SDI	Serial Port Data In. Serial port control data input.
38	SCLK	Serial Port Bit Clock Input. Serial port clock input. Controls the serial data on SDO and latches the data on SDI.

Ordering Guide

Table 45. Ordering Guide

Chip	Description	DC-DC Converter	DTMF Decoder	DCFF Pin Output	Package	Temperature
Si3210-KT	ProSLIC	✓	✓	= $\overline{\text{DCDRV}}$	TSSOP-38	0°C to 70°C
Si3210-BT	ProSLIC	✓	✓	= $\overline{\text{DCDRV}}$	TSSOP-38	–40°C to 85°C
Si3210M-KT	ProSLIC	✓	✓	= DCDRV	TSSOP-38	0°C to 70°C
Si3210M-BT	ProSLIC	✓	✓	= DCDRV	TSSOP-38	–40°C to 85°C
Si3211-KT	ProSLIC		✓	n/a	TSSOP-38	0°C to 70°C
Si3211-BT	ProSLIC		✓	n/a	TSSOP-38	–40°C to 85°C
Si3212-KT	ProSLIC			n/a	TSSOP-38	0°C to 70°C
Si3212-BT	ProSLIC			n/a	TSSOP-38	–40°C to 85°C

Package Outline: 38-Pin TSSOP

Figure 31 illustrates the package details for the Si321x. Table 46 lists the values for the dimensions shown in the illustration.

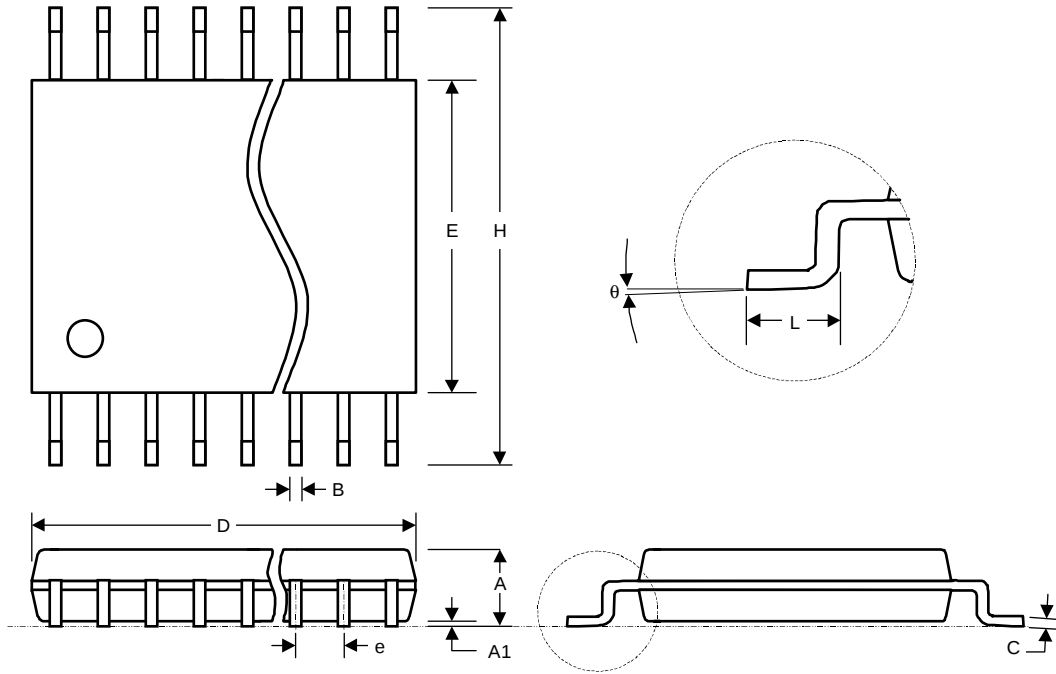


Figure 31. 38-pin Thin Shrink Small Outline Package (TSSOP)

Table 46. Package Diagram Dimensions

Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	—	0.047	—	1.1
A1	0.002	0.006	0.05	0.15
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.381 BSC		9.7 BSC	
E	0.169	0.177	4.30	4.50
e	.02 BSC		.5 BSC	
H	0.252 BSC		6.40 BSC	
L	0.018	0.030	0.45	0.75
θ	0°	8°	0°	8°

Document Changes from Revision 0.9 to Revision 1.0

General Change Summary

- Updates to describe revision E silicon
- Added Si3210M device and description
- Modified current application schematics and component lists
- Added MOSFET/transformer application schematic and component list
- Added optional equivalent Q5, Q6 bias circuit
- Updated register descriptions relating to current, voltage, and power measurement, and to revision E modifications

List of Document Changes

- Figure 9: Si3210 Typical Application Circuit Using BJT/Inductor DC-DC Converter: Updated
- Table 12: Si3210 External Component Values—BJT/Inductor: Updated
- Figure 10: Si3210M Typical Application Circuit Using MOSFET/Transformer DC-DC Converter: Added
- Table 13: Si3210M External Component Values—BMOSFET/Transformer: Added
- Figure 11: Si3211/12 Typical Application Circuit Using External Battery: Updated
- Table 14: Si3211/12 External Component Values—External Battery: Updated
- Figure 12: Si321x Optional Equivalent Q5, Q6 Bias Circuit: Added
- Table 15: Si321x Optional Bias Component Values: Added
- Section: Power Monitoring and Fault Line Detection: power calculation example updated
- Table 17: Associated Power Monitoring and Power Fault Registers: updated
- Section: Battery Voltage Generation and Switching: Updated
- Section: Linefeed Considerations During Ringing: Corrected equation for VOVR
- Table 18: Measured Realtime Linefeed Interface Characteristics: Updated
- Table 19: Associated Power Monitoring and Power Fault Registers: Updated
- Table 21: Si3210 and Si3210M Differences: Added
- Register 0: PN updated
- Register 14: PLL0F removed
- Register 66: EXTBAT removed
- Register 77: PWR0M updated
- Registers 80–89: Updated
- Register 92: DCN updated
- Register 93: DCPOL updated
- Table 33: Oscillator Indirect Registers Summary: Updated
- Indirect Register 30: CML updated
- Indirect Register 31: CMH updated
- Pin Descriptions: Updated
- Table 40: Ordering Guide: Updated

Document Changes from Revision 1.0 to Revision 1.1

- Modified current application schematics and components lists
- Indirect Register 28: Updated
- Indirect Register 43: Updated
- Section: Serial Peripheral Interface: Updated

NOTES:

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